TE0711 Test Board

Revision v.2

Exported on 2024-01-24

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0711+Test+Board

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4 Overview

This example contains a simple MicroBlaze Design with an endless loop application printing "Hello Trenz Module TE0711" and letting the onBoard LED blink in order D1 to D3.

Refer to http://trenz.org/te0711-info[1] for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2021.2
- MicroBlaze
- UART
- QSPI Flash
- LED

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2022-08-22	2021.2	TE0711-test_board-vivado_2021.2-build_15_20220822132519.zip TE0711-test_board_noprebuilt-vivado_2021.2-build_15_20220822132519.zip	Waldemar Hanemann	• 2021.2 update • document style update
2020-09-01	2019.2	TE0711-test_board-vivado_2019.2-build_14_20200901073500.zip TE0711-test_board_noprebuilt-vivado_2019.2-build_14_20200901073630.zip	John Hartfiel	• 2019.2 update
2017-12-07	2017.2	TE0711-test_board_noprebuilt-vivado_2017.2-build_05_20171207122944.zip TE0711-test_board-vivado_2017.2-build_05_20171207122644.zip	John Hartfiel	• initial release

Table 1: Design Revision History

1 https://wiki.trenz-electronic.de/display/PD/TE0711+Resources

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2021.2	needed, Vivado is included into Vitis installation

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[2]

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0711-01-35-2C	35_2c	REV01	NA	32MB	NA	NA	NA
TE0711-01-100-2C	100_2c	REV01	NA	32MB	NA	NA	NA
TE0711-01-35-2I	35_2i	REV01	NA	32MB	NA	NA	NA

2 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0711-01-100-2I	100_2i	REV01	NA	32MB	NA	NA	NA
TE0711-01-S001	100_2i	REV01	NA	32MB	NA	NA	NA

Table 4: Hardware Modules

*used as reference

Design supports following carriers:

Carrier Model	Notes
TE0701	
TE0703*	
TE0705	
TE0706	
TEBA0841	

Table 5: Hardware Carrier

*used as reference

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Table 6: Additional Hardware

*used as reference

4.5 Content

For general structure and usage of the reference design, see Project Delivery - AMD devices[3]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
---	---	---

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface

3 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices

File	File-Extension	Description
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebuilt content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0711 "Test Board" Reference Design[4]

4 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/3x4/TE0711/Reference_Design/2021.2/test_board

5 Design Flow

> Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools[5]
- Vivado Projects - TE Reference Design[6]
- Project Delivery.[7]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[8]

> **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths----------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
--------------------------------------------------------------------
-------------------------TE Reference Design---------------------------
--------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.

5 https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDevelopmentTools-XilinxSoftware-BasicUserGuides
6 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices
8 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices#ProjectDeliveryAMDdevices-Currentlylimitationsoffunctionality

- optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

  > ⚠ Note: Select correct one, see also Vivado Board Part Flow[9]

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")

```
\prebuilt\hardware\")">
TE::hw_build_design -export_prebuilt
```

> ⓘ Using Vivado GUI is the same, except file export to prebuilt folder.

5. Generate Programming Files with Vitis
   a. Run on Vivado TCL:

Script generates applications and bootable files, which are defined in "sw_lib\apps_list.csv"

```
TE::sw_run_vitis -all
```

   b. Copy "\prebuilt\software\<short name>\hello_te0717.elf" into "\firmware\microblaze_0\"
   c. Regenerate Vivado Project or Update Bitfile only, with new "hello_te0717.elf"

   > ⚠ TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis[10]

9 https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow
10 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging[11]

6.1.1 Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select create and open delivery binary folder

   > ⓘ Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

6.1.2 QSPI-Boot mode

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

   run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

   ```
   TE::pr_program_flash -swapp hello_te0711
   ```

3. Power your Board OFF and ON or press the RESET button to start the application and see the output in the console

6.1.3 JTAG

Not used on this example.

6.2 Usage

1. Prepare HW like described on section Programming (see page 13)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode

11 https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDevelopmentTools-XilinxSoftwareProgrammingandDebugging

> Note: See TRM of the Carrier, which is used.

4. Power On PCB
   boot process

   1. FPGA Loads Bitfile from Flash
   2. hello_te0711.elf application starts on MicroBlaze
   3. Hello Trenz will be printed on UART console

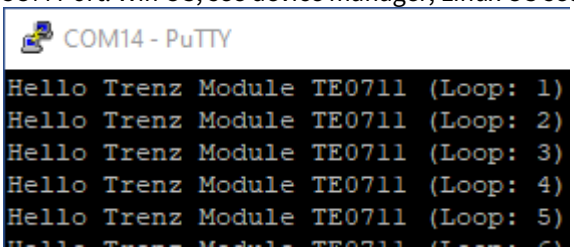
   info: Do not reboot, if Bitfile programming over JTAG is used as programming method.

a. ### 6.2.1 UART

Open Serial Console (e.g. putty)

i. Speed: 9600

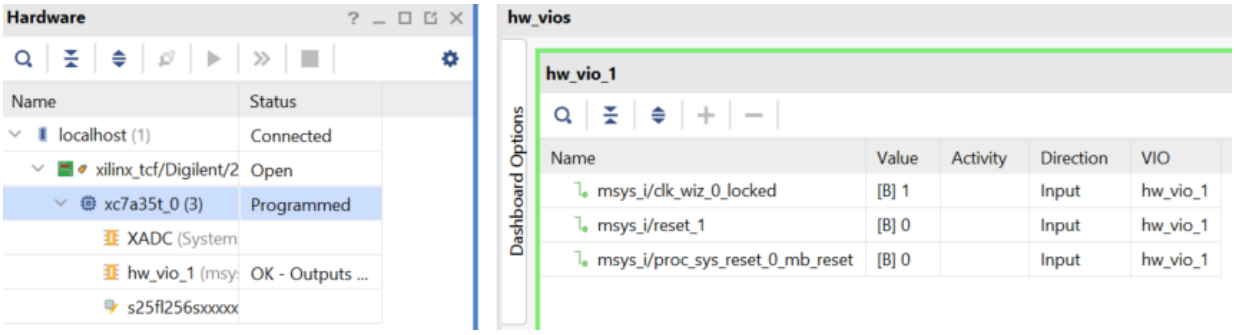
ii. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)



6.2.2 Vivado HW Manager

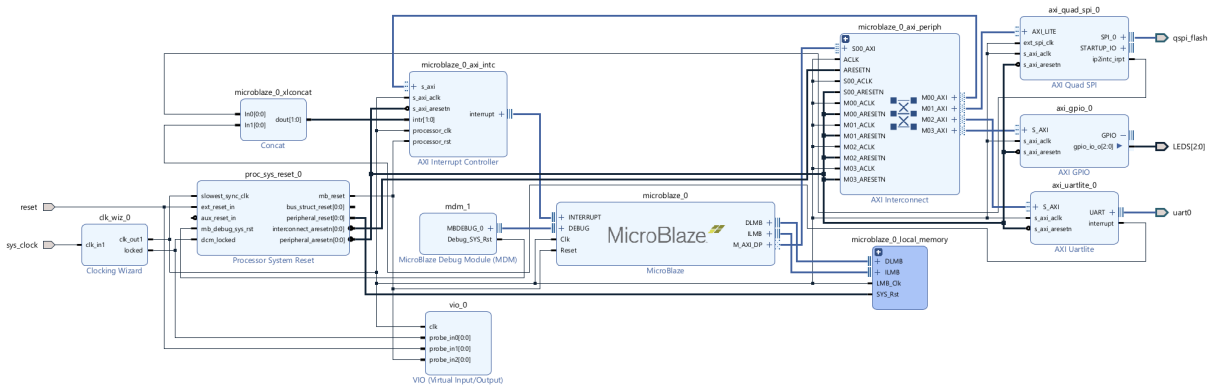
Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

- Control:
- Monitoring:
  - Active High External Reset
  - Active High Processor System Reset



7 System Design - Vivado

7.1 Block Design



7.2 Constraints

7.2.1 Basic module constraints

_i_bitgen_common.xdc

```
#
# Default common settings that do not depend assembly variant
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

_i_bitgen.xdc

```
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLDOWN [current_design]
```

7.2.2 Design specific constraints

_i_io.xdc

```
set_property PACKAGE_PIN A8 [get_ports {LEDS[0]}]
set_property PACKAGE_PIN L15 [get_ports {LEDS[1]}]
set_property PACKAGE_PIN R17 [get_ports {LEDS[2]}]
set_property IOSTANDARD LVCMOS18 [get_ports {LEDS[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LEDS[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LEDS[2]}]
set_property PULLDOWN true [get_ports reset]
```

8 Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis[12]

8.1 Application

Template location: "<project folder>\sw_lib\sw_apps\"

8.1.1 Hello TE0711

Trenz Hello World example as endless loop

Template location: \sw_lib\sw_apps\hello_te0711

The printed Text and the blinking of the red LED can be modified

12 https://wiki.trenz-electronic.de/display/PD/Vitis

9 Additional Software

No additional software is needed.

10 App. A: Change History and Legal Notices

10.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2022-08-22	V.10	Waldemar Hanemann[13]	• 2021.2 release • document style update
2020-09-02	v.9	John Hartfiel	• 2019.2 release • Docu update
2018-11-30	v.8	John Hartfiel	• correction download link
2017-12-07	v.7	John Hartfiel	• 2017.2 release
--	all	Waldemar Hanemann[14]	--

Table 10: Document change history.

10.2 Legal Notices

10.3 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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13 https://wiki.trenz-electronic.de/display/~w.hanemann
14 https://wiki.trenz-electronic.de/display/~w.hanemann

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RoHS

15 http://guidance.echa.europa.eu/
16 https://echa.europa.eu/candidate-list-table
17 http://www.echa.europa.eu/

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