



TE0820 Test Board

Revision v.62

Exported on 2021-06-01

Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0820+Test+Board>

1 Table of Contents

1	Table of Contents.....	2
2	Table of Figures.....	4
3	Table of Tables	5
4	Overview.....	6
4.1	Key Features.....	6
4.2	Revision History	6
4.3	Release Notes and Know Issues	10
4.4	Requirements.....	11
4.4.1	Software	11
4.4.2	Hardware.....	11
4.5	Content.....	16
4.5.1	Design Sources.....	16
4.5.2	Additional Sources.....	16
4.5.3	Prebuilt.....	16
4.5.4	Download	17
5	Design Flow	18
6	Launch	20
6.1	Programming	20
6.1.1	Get prebuilt boot binaries	20
6.1.2	QSPI	20
6.1.3	SD	20
6.1.4	JTAG.....	21
6.2	Usage	21
6.2.1	Linux	21
6.2.2	Vivado HW Manager	21
7	System Design - Vivado.....	23
7.1	Block Design.....	23
7.1.1	PCB REV03	23
7.1.2	PCB REV01 REV02.....	24
7.1.3	PS Interfaces.....	24
7.2	Constrains.....	25
7.2.1	Basic module constrains.....	25
7.2.2	Design specific constrain	25
8	Software Design - Vitis	26
8.1	Application	26
8.1.1	zynqmp_fsbl.....	26

8.1.2	zynqmp_fsbl_flash.....	26
8.1.3	zynqmp_pmufw	26
8.1.4	hello_te0820.....	26
8.1.5	u-boot	27
9	Software Design - PetaLinux.....	28
9.1	Config.....	28
9.2	U-Boot.....	28
9.3	Device Tree.....	29
9.4	Kernel.....	30
9.5	Rootfs.....	30
9.6	Applications.....	30
9.6.1	startup	30
9.6.2	webfwu	30
10	Additional Software	31
10.1	SI5338	31
11	Appx. A: Change History and Legal Notices	32
11.1	Document Change History.....	32
11.2	Legal Notices	34
11.3	Data Privacy.....	34
11.4	Document Warranty.....	34
11.5	Limitation of Liability.....	34
11.6	Copyright Notice	35
11.7	Technology Licenses.....	35
11.8	Environmental Protection	35
11.9	REACH, RoHS and WEEE	35

2 Table of Figures

Figure 1: Vivado Hardware Manager	22
Figure 2: Vivado Hardware Manager PCB REV01,REV02	22

3 Table of Tables

Table 1: Design Revision History	6
Table 2: Known Issues.....	10
Table 3: Software	11
Table 4: Hardware Modules.....	11
Table 5: Hardware Carrier.....	15
Table 6: Additional Hardware.....	15
Table 7: Design sources	16
Table 8: Additional design sources	16
Table 9: Prebuilt files (only on ZIP with prebuilt content)	16
Table 10: Document change history.....	32

4 Overview

ZynqMP PS Design with Linux Example and simple frequency counter to measure SI5338 Reference CLK with Vivado HW-Manager.

Wiki Resources page: <http://trenz.org/te0820-info>

4.1 Key Features

- Vitis/Vivado 2019.2
- PetaLinux
- SD
- ETH
- USB
- I2C
- RTC
- FMeter
- MAC from EEPROM
- User LED (PCB REV03 only)
- Modified FSBL for SI5338 programming
- Special FSBL for QSPI programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-04-08	2019.2	TE0820-test_board_noprebuilt-vivado_2019.2-build_10_20200408073458.zip TE0820-test_board-vivado_2019.2-build_10_20200408073444.zip	John Hartfiel	<ul style="list-style-type: none">• script update• new assembly variants
2020-03-25	2019.2	TE0820-test_board_noprebuilt-vivado_2019.2-build_8_20200325083817.zip TE0820-test_board-vivado_2019.2-build_8_20200325083750.zip	John Hartfiel	<ul style="list-style-type: none">• script update• Board Part update (minor changes)

Date	Vivado	Project Built	Authors	Description
2020-01-22	2019.2	TE0820-test_board_noprebuilt-vivado_2019.2-build_3_20200122154341.zip TE0820-test_board-vivado_2019.2-build_3_20200122154318.zip	John Hartfiel	<ul style="list-style-type: none"> script update for linux user
2020-01-14	2019.2	TE0820-test_board-vivado_2019.2-build_3_20200114081551.zip TE0820-test_board_noprebuilt-vivado_2019.2-build_3_20200114081612.zip	John Hartfiel	<ul style="list-style-type: none"> add fsbl_flash binary Vitis script updates (include linux domain and prebuilt linux files for vitis) prebuilt binary export on selection guide
2019-12-19	2019.2	TE0820-test_board-vivado_2019.2-build_1_20191219075647.zip TE0820-test_board_noprebuilt-vivado_2019.2-build_1_20191219080228.zip	John Hartfiel	<ul style="list-style-type: none"> 2019.2 update Vitis support
2019-10-29	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_09_20191029071045.zip TE0820-test_board-vivado_2018.3-build_09_20191029071028.zip	John Hartfiel	<ul style="list-style-type: none"> new assembly variants
2019-08-09	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_07_20190809084040.zip TE0820-test_board-vivado_2018.3-build_07_20190809083901.zip	John Hartfiel	<ul style="list-style-type: none"> bugfix fsbl (removed second PSU init)
2019-06-19	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_06_20190619073300.zip TE0820-test_board-vivado_2018.3-build_06_20190619073243.zip	John Hartfiel	<ul style="list-style-type: none"> new assembly variants USB2 only (change PS IP and device tree) FSBL changes

Date	Vivado	Project Built	Authors	Description
2019-04-01	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_03_20190401130135.zip TE0820-test_board-vivado_2018.3-build_03_20190401130123.zip	John Hartfiel	<ul style="list-style-type: none"> renamed ...D variants to ...A
2019-02-21	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_01_20190221103025.zip TE0820-test_board-vivado_2018.3-build_01_20190221102913.zip	John Hartfiel	<ul style="list-style-type: none"> TE Script update rework of the FSBLs SI5338 CLKBuilder Pro Project some additional Linux features MAC from EEPROM new assembly variants remove special compiler flags, which was needed in 2018.2
2018-10-31	2018.2	TE0820-test_board_noprebuilt-vivado_2018.2-build_03_20181031164506.zip TE0820-test_board-vivado_2018.2-build_03_20181031164452.zip	John Hartfiel	<ul style="list-style-type: none"> new assembly variants update optional petalinux startup init script
2018-09-12	2018.2	TE0820-test_board_noprebuilt-vivado_2018.2-build_03_20180912094615.zip TE0820-test_board-vivado_2018.2-build_03_20180912094558.zip	John Hartfiel	<ul style="list-style-type: none"> correction: <ul style="list-style-type: none"> TE0820-03-4EV-1EA has 2GB DDR, now 2GB instead of 1GB is initialised small changes on DDR setup of TE0820-02-2EG-1EE
2018-08-15	2018.2	TE0820-test_board-vivado_2018.2-build_01_20180706212937.zip TE0820-test_board_noprebuilt-vivado_2018.2-build_01_20180706212952.zip	John Hartfiel	<ul style="list-style-type: none"> different design for REV03 small petalinux changes IO renaming additional notes for FSBL generated with Win SDK changed *.bif
2018-06-19	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180619160713.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180619160728.zip	John Hartfiel	<ul style="list-style-type: none"> bugfix board part files BANK1 MIO voltages Add "dummy" PS USB3 parameter so solve problems with some USB2 devices

Date	Vivado	Project Built	Authors	Description
2018-05-24	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180524151356.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180524151342.zip	John Hartfiel	<ul style="list-style-type: none"> solved Linux Flash issue new assembly variant
2018-04-25	2017.4	TE0820-test_board-vivado_2017.4-build_07_20180425134435.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_07_20180425134459.zip	John Hartfiel	<ul style="list-style-type: none"> new assembly variants
2018-02-06	2017.4	TE0820-test_board-vivado_2017.4-build_06_20180206203359.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_06_20180206203414.zip	John Hartfiel	<ul style="list-style-type: none"> solved JTAG/Linux issue
2018-02-01	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180201084319.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180201094724.zip	John Hartfiel	<ul style="list-style-type: none"> board part csv update
2018-01-24	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180124085247.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180124085303.zip	John Hartfiel	<ul style="list-style-type: none"> rework board part files solved USB, QSPI and PHy issue
2017-11-21	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171121160552.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171121160606.zip	John Hartfiel	<ul style="list-style-type: none"> solved SD SDX Cards Problem Separate csv name for all assembly variants

Date	Vivado	Project Built	Authors	Description
2017-11-20	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171120162931.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171120162851.zip	John Hartfiel	<ul style="list-style-type: none"> solved SD WP Problem
2017-10-19	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171019104824.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171019104837.zip	John Hartfiel	<ul style="list-style-type: none"> initial release

Table 1: Design Revision History

4.3 Release Notes and Known Issues

Issues	Description	Workaround	To be fixed version
Flash access on Linux	Device tree is not correct on Linux	add compatibility to "compatible "jedec,spinosr""	Solved with 20180524 update
USB UART Terminal is blocked / SDK Debugging is blocked	This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager.	<p>Do not use HW Manager connection, or if debugging is necessary:</p> <ol style="list-style-type: none"> 1. Boot linux with usb terminal 2. From the terminal: root root mount ifconfig eth0 3. Open two new SSH terminals via ethernet: root root , run user application ... 4. Exit and close the usb terminal 	Solved with 20180206 update

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2019.2	needed Vivado is included into Vitis installation
PetaLinux	2019.2	needed
SI ClockBuilder Pro	---	optional

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).¹

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-ES1	es1	REV01	1G B -	64MB -	4G B -	NA	Not longer supported by vivado
TE0820-02-02EG-1E	2eg_1e_1gb	REV02	1G B	64MB	4G B	NA	NA
TE0820-02-02EG-1E3	2eg_1e_1gb	REV02	1G B	64MB	4G B	2.5 mm connectors	NA
TE0820-02-02CG-1E	2cg_1e_1gb	REV02	1G B	64MB	4G B	NA	NA

¹ <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-02-03EG-1E	3eg_1e_1gb	REV02	1GB	64MB	4GB	NA	NA
TE0820-02-03EG-1E3	3eg_1e_1gb	REV02	1GB	64MB	4GB	2.5 mm connectors	NA
TE0820-02-03CG-1E	3cg_1e_1gb	REV02	1GB	64MB	4GB	NA	NA
TE0820-02-02EG-1EA	2eg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-02-02EG-1EL	2eg_1e_1gb	REV02	1GB	128MB	4GB	2.5 mm connectors	NA
TE0820-02-02CG-1EA	2cg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-02-03EG-1EA	3eg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-02-03EG-1EL	3eg_1e_1gb	REV02	1GB	128MB	4GB	2.5 mm connectors	NA
TE0820-02-03CG-1EA	3cg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-02-04CG-1EA	4cg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-03-04EV-1EA	4ev_1e_2gb	REV03	2GB	128MB	4GB	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-03-02CG-1EA	2cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02EG-1EA	2eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02EG-1EL	2eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-03CG-1EA	3cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-04CG-1EA	4cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EA	3eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EL	3eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-2AI21FA	2cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FL	2eg_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-3AI210A	3cg_1i_2gb	REV03	2GB	128MB	0GB	NA	NA
TE0820-03-3BE21FA	3eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-03-3BE21FL	3eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-02CG-1ED	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2AE21FA	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FA	2eg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3AE21FA	3cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3AI21FA	3cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4AE21FA	4cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DE21FA	4ev_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DI21FA	4ev_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DE21FL	4ev_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-4AE21FI	4cg_1e_x_2gb	REV03	2GB	128MB	8GB	without ETH PHY	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-03-4DE21FC	4ev_1e_2gb	REV03	2GB	128MB	8GB	without encryption NCNR	NA
TE0820-03-4AI21FI	4cg_1i_x_2gb	REV03	2GB	128MB	8GB	without ETH PHY	NA

Table 4: Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TE0701	<ul style="list-style-type: none"> Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers²
TE0703	<ul style="list-style-type: none"> Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 cm carriers³ Used as reference carrier.
TE0705	<ul style="list-style-type: none"> Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers⁴
TE0706	<ul style="list-style-type: none"> Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers⁵
TEBA0841	<ul style="list-style-type: none"> Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers⁶ No SD Slot available, pins goes to Pin Header For TEBA0841 REV01, please contact TE support

Table 5: Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI
Cooler	It's recommended to use cooler on ZynqMP device

Table 6: Additional Hardware² <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>³ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>⁴ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>⁵ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>⁶ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>

4.5 Content

For general structure and of the reference design, see [Project Delivery - Xilinx devices](#)⁷

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/SI5338	SI5338 Project with current PLL Configuration
init.sh	<design name>/sd/	Additional Initialization Script for Linux

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)

⁷ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebuilt content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0820 "Test Board" Reference Design⁸

⁸ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/Reference_Design/2019.2/test_board

5 Design Flow

⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [Xilinx Development Tools](#)⁹
- [Vivado Projects - TE Reference Design](#)¹⁰
- [Project Delivery](#)¹¹

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery](#) [Currently limitations of functionality](#)¹²

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

```
C:\WINDOWS\system32\cmd.exe
B:\Design\cores\xilinx\2018.3\design\TE0820\test_board>setlocal
-- Set design paths --
-- Run Design with: _create_win_setup
-- Use Design Path: B:\Design\cores\xilinx\2018.3\design\TE0820\test_board\

----- TE Reference Design -----
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (x) Exit Batch (nothing is done!)
-- (0) Module selection guide, project creation...
-- (1) Create minimum setup of CMD-Files and exit Batch
-- (2) Create maximum setup of CMD-Files and exit Batch
-- 
Select (ex.: '0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
 - a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" Note: Select correct one, see also [TE Board Part Files](#)¹³
5. Create XSA and export to prebuilt folder
 - a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
 Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder

⁹ <https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides>

¹⁰ <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

¹¹ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

¹² <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality>

¹³ <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported XSA
 - a. XSA is exported to "prebuilt\hardware\<short name>"
Note: HW Export from Vivado GUI create another path as default workspace.
Create Linux images on VM, see [PetaLinux KICKstart](#)¹⁴
 - i. Use TE Template from "/os/petalinux"
7. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
 - a. "prebuilt\os\petalinux\<DDR size>" or "prebuilt\os\petalinux\<short name>"
Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise "prebuilt\os\petalinux\<DDR size>"
8. Generate Programming Files with Vitis
 - a. Run on Vivado TCL: TE::sw_run_vitis -all
Note: Depending of PC performance this can take several minutes. Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv" and open Vitis
 - b. (alternative) Start Vitis with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used. See [Vitis](#)¹⁵

¹⁴ <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

¹⁵ <https://wiki.trenz-electronic.de/display/PD/Vitis>

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging¹⁶](#)

Note: Depending on CPLD Firmware and Boot Mode settings, QSPI boot with Linux image on SD or complete SD Boot is possible.

6.1.1 Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:
2. Press 0 and enter to start "Module Selection Guide"
 - a. Select assembly version
 - b. Validate selection
 - c. Select Create and open delivery binary folder

Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

6.1.2 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash -swapp u-boot
Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
optional "TE::pr_program_flash -swapp hello_te0820" possible
4. Copy image.ub on SD-Card
 - use files from (<project foler>/_binaries_<Artikel Name>)/boot_linux from generated binary folder, see: [Get prebuilt boot binaries\(see page 20\)](#)
 - or use prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
5. Insert SD-Card

6.1.3 SD

Use this description for CPLD Firmware with SD Boot selectable.

1. Copy image.ub and Boot.bin on SD-Card.
 - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Insert SD-Card in SD-Slot.

¹⁶ <https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging>

6.1.4 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section [Programming](#)(see page 20)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card or QSPI as Boot Mode (Depends on used programming variant)
Note: See TRM of the Carrier, which is used.
4. Power On PCB
Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD/QSPI Flash into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR

6.2.1 Linux

1. Open Serial Console (e.g. putty)
 - a. Speed: 115200
 - b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
Note: Wait until Linux boot finished For Linux Login use:
 - a. User Name: root
 - b. Password: root
3. You can use Linux shell now.
 - a. I2C 0 Bus type: i2cdetect -y -r 0
 - b. RTC check: dmesg | grep rtc
 - c. ETH0 works with udhcpc
 - d. USB type "lsusb" or connect USB2.0 device
4. Option Features
 - a. Webserver to get access to Zynq
 - i. insert IP on web browser to start web interface
 - b. init.sh scripts
 - i. add init.sh script on SD, content will be load automatically on startup (template included in ./misc/SD)

6.2.2 Vivado HW Manager

SI5338_CLK0 Counter:

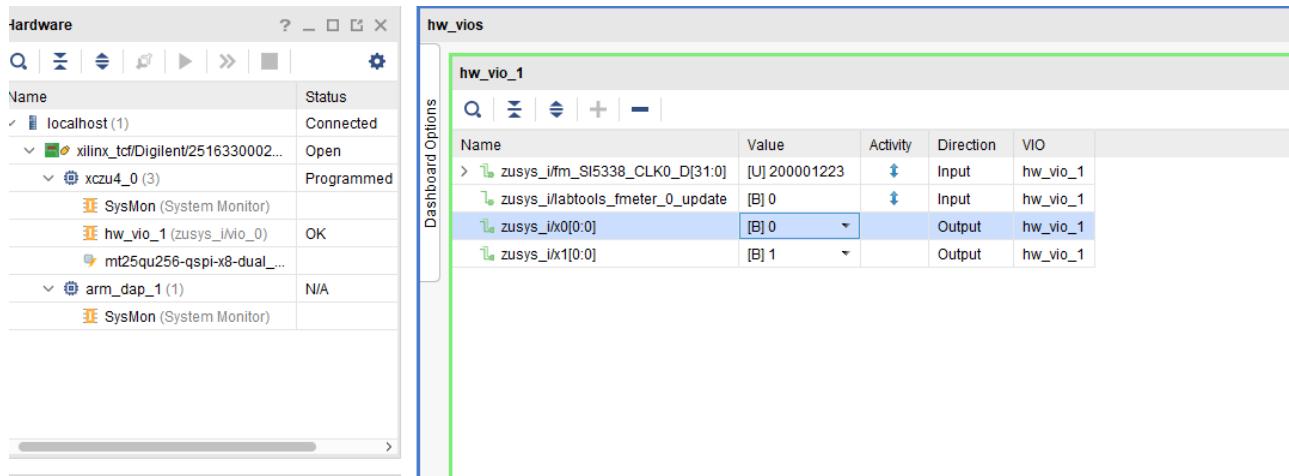
1. Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).
 - a. Set radix from VIO signals to unsigned integer.
Note: Frequency Counter is inaccurate and displayed unit is Hz

SI5338 CLK is configured to 200MHz by default.

PCB REV03 Design:

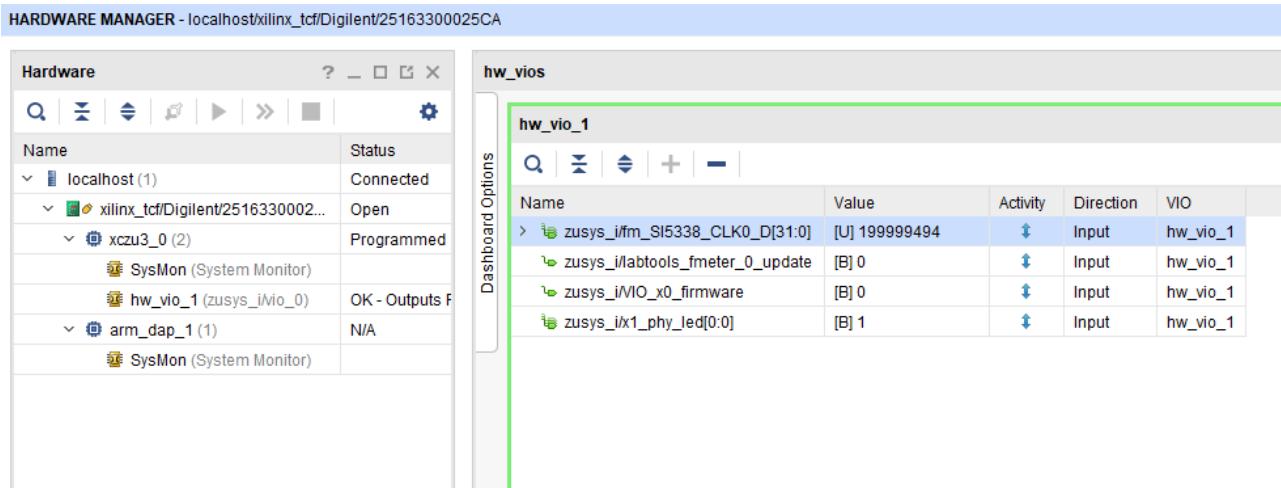
- User LED, see: [TE0820 CPLD](#)¹⁷

¹⁷ <https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD#TE0820CPLD-LED>

**Figure 1: Vivado Hardware Manager**

PCB REV01, REV02 Design:

- PHY LEDS, see: [TE0820-REV01_REV02 CPLD¹⁸](#)
- CPLD Firmware, see: [TE0820-REV01_REV02 CPLD¹⁹](#)

**Figure 2: Vivado Hardware Manager PCB REV01,REV02**

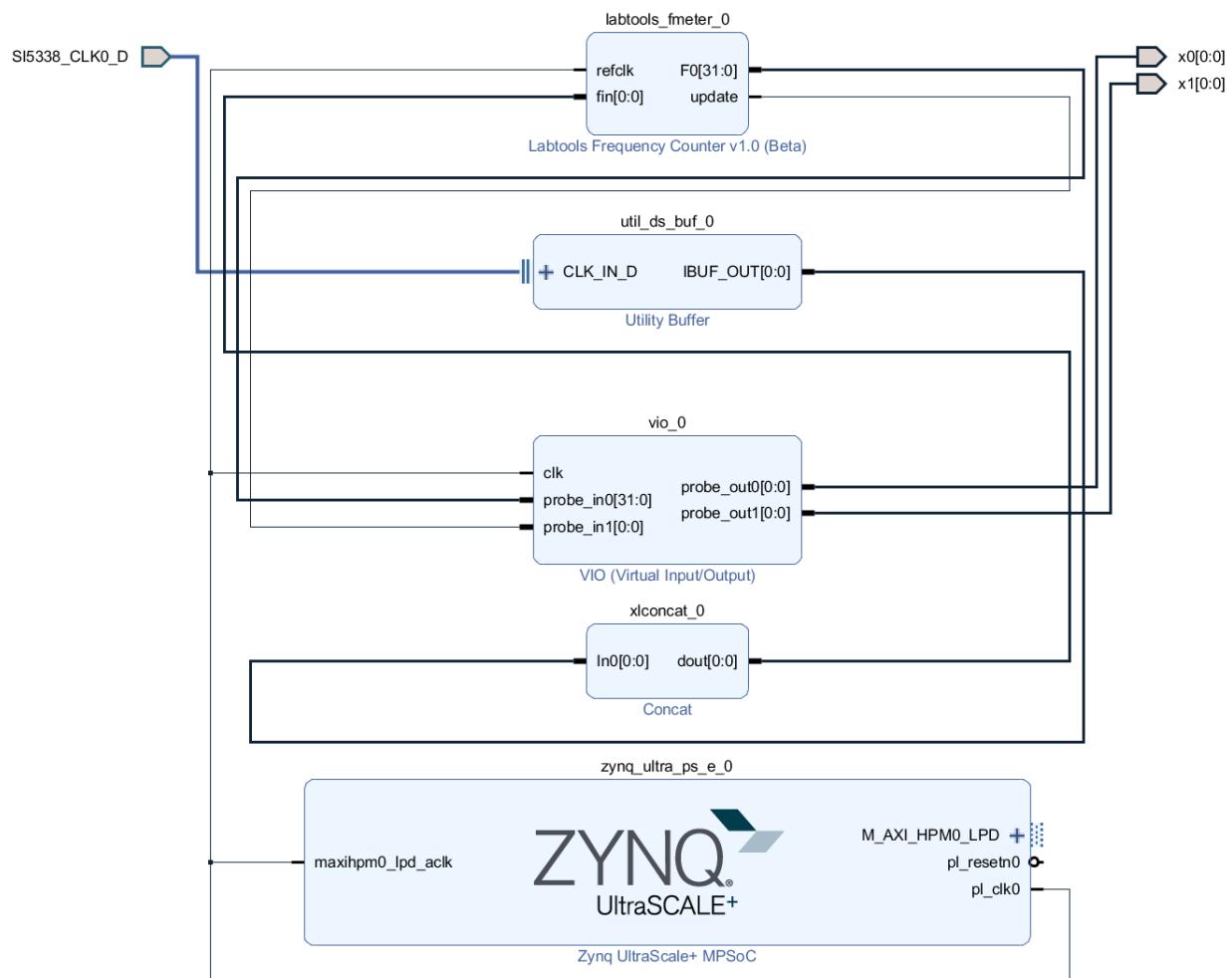
¹⁸ https://wiki.trenz-electronic.de/display/PD/TE0820-REV01_REV02+CPLD#TE0820REV01_REV02CPLD-X0/X1Pin

¹⁹ https://wiki.trenz-electronic.de/display/PD/TE0820-REV01_REV02+CPLD#TE0820REV01_REV02CPLD-X0/X1Pin

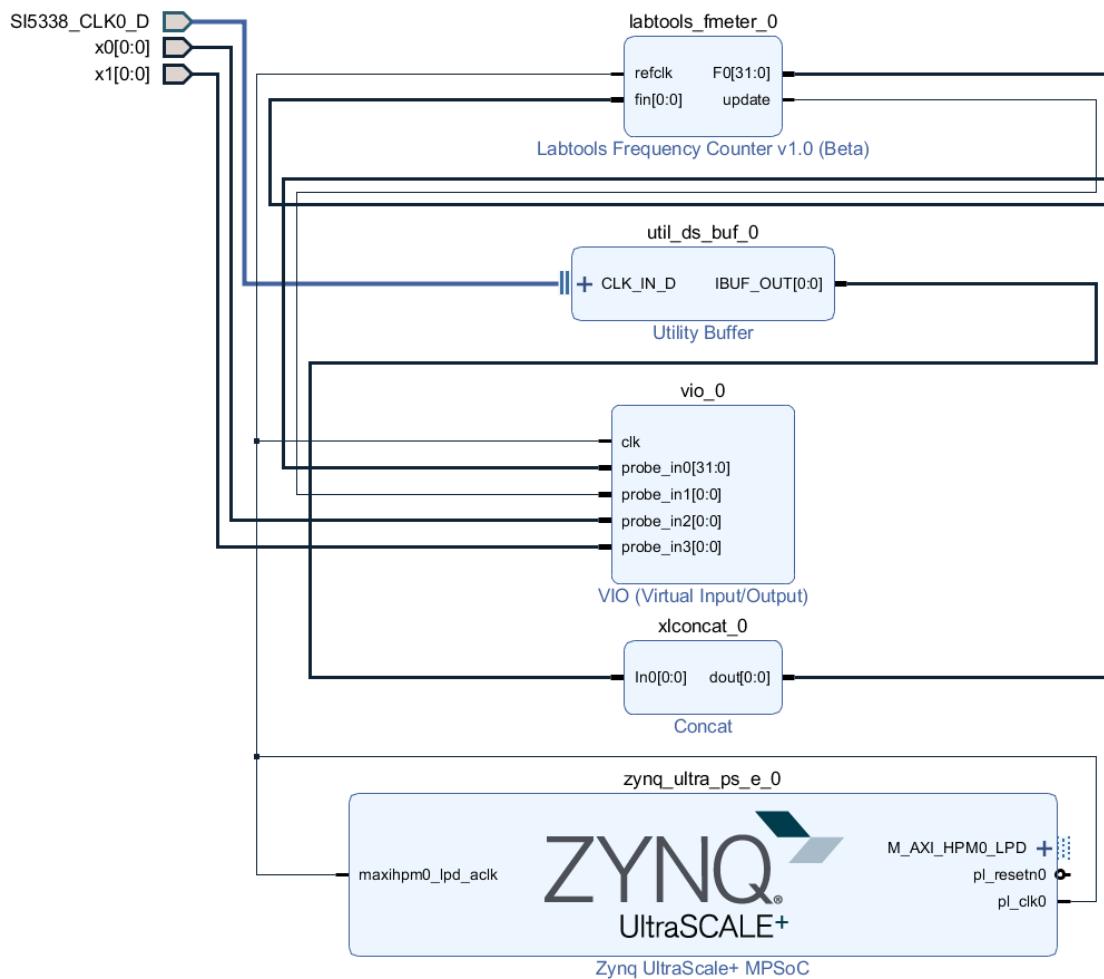
7 System Design - Vivado

7.1 Block Design

7.1.1 PCB REV03



7.1.2 PCB REV01 REV02



7.1.3 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
UART0	MIO

Type	Note
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO, USB2 only

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN_PULLNONE [current_design]
```

7.2.2 Design specific constrain

_i_io.xdc

```
set_property PACKAGE_PIN K9 [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property IOSTANDARD LVDS [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property DIFF_TERM TRUE [get_ports {SI5338_CLK0_D_clk_p[0]}]

set_property PACKAGE_PIN H1 [get_ports {x0[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x0[0]}]
set_property PACKAGE_PIN J1 [get_ports {x1[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1[0]}]
```

8 Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis²⁰

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 zynqmp_fsbl

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c(search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)\n
- General Changes:
 - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
 - Si5338 Configuration
 - ETH+OTG Reset over MIO

8.1.2 zynqmp_fsbl_flash

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl_initialisation.c, xfsbl_hw.h, xfsbl_handoff.c, xfsbl_main.c
- General Changes:
 - Display FSBL Banner
 - Set FSBL Boot Mode to JTAG
 - Disable Memory initialisation

8.1.3 zynqmp_pmufw

Xilinx default PMU firmware.

8.1.4 hello_te0820

Hello TE0820 is a Xilinx Hello World example as endless loop instead of one console output.

²⁰ <https://wiki.trenz-electronic.de/display/PD/Vitis>

8.1.5 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart²¹](#)

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- CONFIG_SUBSYSTEM_ETHERNET_PSU_ETHERNET_3_MAC=""

9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set
- CONFIG_I2C_EEPROM=y
- CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET=0xFA
- CONFIG_SYS_I2C_EEPROM_ADDR=0x50
- CONFIG_SYS_I2C_EEPROM_BUS=0
- CONFIG_SYS_EEPROM_SIZE=256
- CONFIG_SYS_EEPROM_PAGE_WRITE_BITS=0
- CONFIG_SYS_EEPROM_PAGE_WRITE_DELAY_MS=0
- CONFIG_SYS_I2C_EEPROM_ADDR_LEN=1
- CONFIG_SYS_I2C_EEPROM_ADDR_OVERFLOW=0

Change platform-top.h:



²¹ <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

9.3 Device Tree

```
/include/ "system-conf.dtsi"
{
    chosen {
        xlnx,eeprom = &eeprom;
    };
};

/* SDIO */

&sdhci1 {
    disable-wp;
    no-1-8-v;
};

/* ETH PHY */
&gem3 {

    status = "okay";
    ethernet_phy0: ethernet-phy@0 {
        compatible = "marvell,88e1510";
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/* USB 2.0 */

/* USB */
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    maximum-speed = "high-speed";
    /delete-property/phy-names;
    /delete-property/phys;
    /delete-property/snps,usb3_lpm_capable;
    snps,dis_u2_susphy_quirk;
    snps,dis_u3_susphy_quirk;
};

&usb0 {
    status = "okay";
    /delete-property/ clocks;
    /delete-property/ clock-names;
    clocks = <0x3 0x20>;
    clock-names = "bus_clk";
};

/* QSPI PHY */
```

```

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec.spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

&i2c0 {
    eeprom: eeprom@50 {
        compatible = "atmel,24c08";
        reg = <0x50>;
    };
};

```

9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_CPU_IDLE is not set (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ is not set (only needed to fix JTAG Debug issue)
- CONFIG_EDAC_CORTEX_ARM64=y

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- CONFIG_i2c-tools=y
- CONFIG_busybox-httdp=y (for web server app)
- CONFIG_packagegroup-petalinux-utils(util-linux,cpufrequtils,bridge-utils,mtd-utils,usutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

9.6.2 webfwu

Webserver application acmeble for Zynq access. Need busybox-httdp

10 Additional Software

10.1 SI5338

File location <design name>/misc/Si5338/Si5338-*.slabtimproj

General documentation how you work with these project will be available on [Si5338](#)²²

²² <https://wiki.trenz-electronic.de/display/PD/Si5338>

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
📅 2020-05-07	v.62(see page 6)	@ John Hartfiel ²³	<ul style="list-style-type: none"> update programming section
2020-04-08	v.61	John Hartfiel	<ul style="list-style-type: none"> script update new assembly variants
2020-03-25	v.60	John Hartfiel	<ul style="list-style-type: none"> script update
2020-01-21	v.59	John Hartfiel	<ul style="list-style-type: none"> Script update for linux user
2020-01-14	v.58	John Hartfiel	<ul style="list-style-type: none"> Script update, new features docu update add missing binary files
2019-12-19	v.57	John Hartfiel	<ul style="list-style-type: none"> 2019.2 release
2019-10-29	v.56	John Hartfiel	<ul style="list-style-type: none"> new assembly variants
2019-08-09	v.55	John Hartfiel	<ul style="list-style-type: none"> bugfix fsbl
2019-06-19	v.54	John Hartfiel	<ul style="list-style-type: none"> design changes new variants
2019-04-01	v.53	John Hartfiel	<ul style="list-style-type: none"> some notes renamed ..D variants to ...A
2018-09-21	v.47	John Hartfiel	<ul style="list-style-type: none"> 2018.3 release finished (include design reworks)

²³ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

Date	Document Revision	Authors	Description
2018-10-31	v.43	John Hartfiel	<ul style="list-style-type: none"> • Update Design files for 2GB variants • rebuilt petalinux for optional init script
2018-09-12	v.41	John Hartfiel	<ul style="list-style-type: none"> • Update Design files for 2GB variants
2018-07-11	v.40	John Hartfiel	<ul style="list-style-type: none"> • add notes to ES1
2018-07-06	v.38	John Hartfiel	<ul style="list-style-type: none"> • 2018.2 release finished
2018-06-19	v.34	John Hartfiel	<ul style="list-style-type: none"> • Design Files Update
2018-02-13	v.29	John Hartfiel	<ul style="list-style-type: none"> • Design Files Update
2018-02-06	v.27	John Hartfiel	<ul style="list-style-type: none"> • Design Files Update
2018-01-29	v.26	John Hartfiel	<ul style="list-style-type: none"> • Update Known Issues
2018-01-24	v.25	John Hartfiel	<ul style="list-style-type: none"> • Release 2017.4
2018-01-10	v.24	John Hartfiel	<ul style="list-style-type: none"> • Update Known Issues
2017-12-20	v.23	John Hartfiel	<ul style="list-style-type: none"> • Typo correction • Update HW Module Table Description
2017-11-21	v.19	John Hartfiel	<ul style="list-style-type: none"> • Design Update
2017-11-20	v.18	John Hartfiel	<ul style="list-style-type: none"> • Design Update • Add Variants with 128MB Flash
2017-11-13	v.16	John Hartfiel	<ul style="list-style-type: none"> • Update Carrier sections
2017-11-06	v.15	John Hartfiel	<ul style="list-style-type: none"> • Typo corrected

Date	Document Revision	Authors	Description
2017-10-23	v.13	John Hartfiel	<ul style="list-style-type: none"> • Update Key Features section • Style Update Additional Software section
2017-10-19	v.9	John Hartfiel	<ul style="list-style-type: none"> • Release 2017.2
2017-09-11	v.1	@ John Hartfiel ²⁴	Initial release
	All	@ John Hartfiel ²⁵	

Table 10: Document change history.

11.2 Legal Notices

11.3 Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

11.4 Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

11.5 Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials

²⁴ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

²⁵ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

11.6 Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

11.7 Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used / modified / copied only in accordance with the terms of such license.

11.8 Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

11.9 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH²⁶](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List²⁷](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)²⁸](#).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union.

²⁶ <http://guidance.echa.europa.eu/>

²⁷ <https://echa.europa.eu/candidate-list-table>

²⁸ <http://www.echa.europa.eu/>

Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

 2019-06-07