TE0823 Test Board

Revision v.4

Exported on 2021-08-17

Online version of this document:

https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=122855441

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4 Overview

ZynqMP PS Design with Linux Example and simple frequency counter to measure SI5338 Reference CLK with Vivado HW-Manager.
Wiki Resources page: http://trenz.org/te0820-info

4.1 Key Features

- Vitis/Vivado 2019.2
- PetaLinux
- SD
- ETH
- USB
- I2C
- RTC
- FMeter
- MAC from EEPROM
- User LED
- Modified FSBL for SI5338 programming
- Special FSBL for QSPI programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-03-16	2019.2	TE0823-test_board-vivado_2019.2-build_8_20200316163150.zip TE0823-test_board_noprebuilt-vivado_2019.2-build_8_20200316163202.zip	John Hartfiel	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2019.2	needed Vivado is included into Vitis installation
PetaLinux	2019.2	needed
SI ClockBuilder Pro	---	optional

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[1]

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0823-01-3PIU1FL	3cg_1li_1gb	REV01	1GB	128MB	8GB	NA	NA

Table 4: Hardware Modules
Design supports following carriers:

Carrier Model	Notes
TE0701	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[2]
TE0703	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 cm carriers [3] • Used as reference carrier.
TE0705	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[4]

1 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
2 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
3 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
4 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers

Carrier Model	Notes
TE0706	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[5]
TEBA0841	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[6] • No SD Slot available, pins goes to Pin Header • For TEBA0841 REV01, please contact TE support
TEF1001	• mportant: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[7]

Table 5: Hardware Carrier
Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct typ
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI
Cooler	It's recommended to use cooler on ZynqMP device

Table 6: Additional Hardware

4.5 Content

For general structure and of the reference design, see Project Delivery - Xilinx devices[8]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

5 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
6 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
7 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
8 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

Type	Location	Notes
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/Si5338	SI5338 Project with current PLL Configuration
init.sh	<design name>/sd/	Additional Initialization Script for Linux

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification forVitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)

File	File-Extension	Description
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebult content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0823 "Test Board" Reference Design[9]

9 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0823/Reference_Design/2019.2/test_board

5 Design Flow

> Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

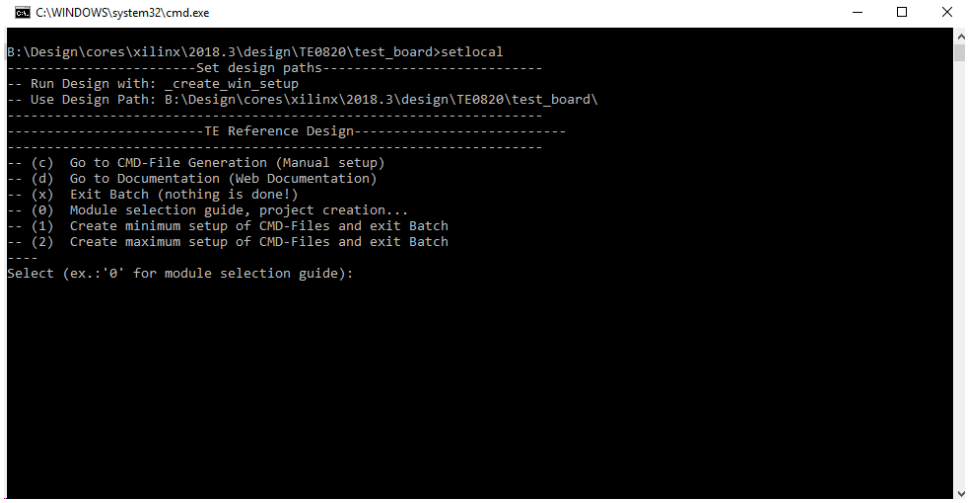
See also:

- Xilinx Development Tools[10]
- Vivado Projects - TE Reference Design[11]
- Project Delivery.[12]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[13]

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
   a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" Note: Select correct one, see also TE Board Part Files[14]
5. Create XSA and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder

10 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
11 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
12 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
13 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality
14 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported XSA
    a. XSA is exported to "prebuilt\hardware\<short name>"
       Note: HW Export from Vivado GUI create another path as default workspace.
       Create Linux images on VM, see PetaLinux KICKstart[15]
        i. Use TE Template from "/os/petalinux"
7. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
    a. "prebuilt\os\petalinux\<DDR size>" or "prebuilt\os\petalinux\<short name>"
       Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise "prebuilt\os\petalinux\<DDR size"
8. Generate Programming Files with Vitis
    a. Run on Vivado TCL: TE::sw_run_vitis -all
       Note: Depending of PC performance this can take several minutes. Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv" and open Vitis
    b. (alternative) Start Vitis with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
       Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used. See Vitis[16]

15 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
16 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging[17]

Note: Depending on CPLD Firmware and Boot Mode settings, QSPI boot with Linux image on SD or complete SD Boot is possible.

6.1.1 Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder
      Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

6.1.2 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
   optional "TE::pr_program_flash_binfile -swapp hello_te0823" possible
4. Copy image.ub on SD-Card
   - use files from (<project foler>/_binaries_<Artikel Name>)/boot_linux from generated binary folder,see: Get prebuilt boot binaries(see page 13)
   - or use prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
5. Insert SD-Card

6.1.3 SD

Use this description for CPLD Firmware with SD Boot selectable.

1. Copy image.ub and Boot.bin on SD-Card.
   - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Insert SD-Card in SD-Slot.

17 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging

6.1.4 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming(see page 13)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card or QSPI as Boot Mode (Depends on used programming variant)
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD/QSPI Flash into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root
3. You can use Linux shell now.
   a. I2C 0 Bus type: i2cdetect -y -r 0
   b. RTC check: dmesg | grep rtc
   c. ETH0 works with udhcpc
   d. USB type "lsusb" or connect USB2.0 device
4. Option Features
   a. Webserver to get access to Zynq
      i. insert IP on web browser to start web interface
   b. init.sh scripts
      i. add init.sh script on SD, content will be load automatically on startup (template included in ./misc/SD)

6.2.2 Vivado HW Manager

1. Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

Control:

- GTR Power: set X0=0 and X1=1 to disable GTR Power
- USER LED: On/OFF

Monitoring:

- SI5338_CLK0 Counter: 200MHz with example Design
  - Set radix from VIO signals to unsigned integer.
    Note: Frequency Counter is inaccurate and displayed unit is Hz
- ETH PHY LEDs

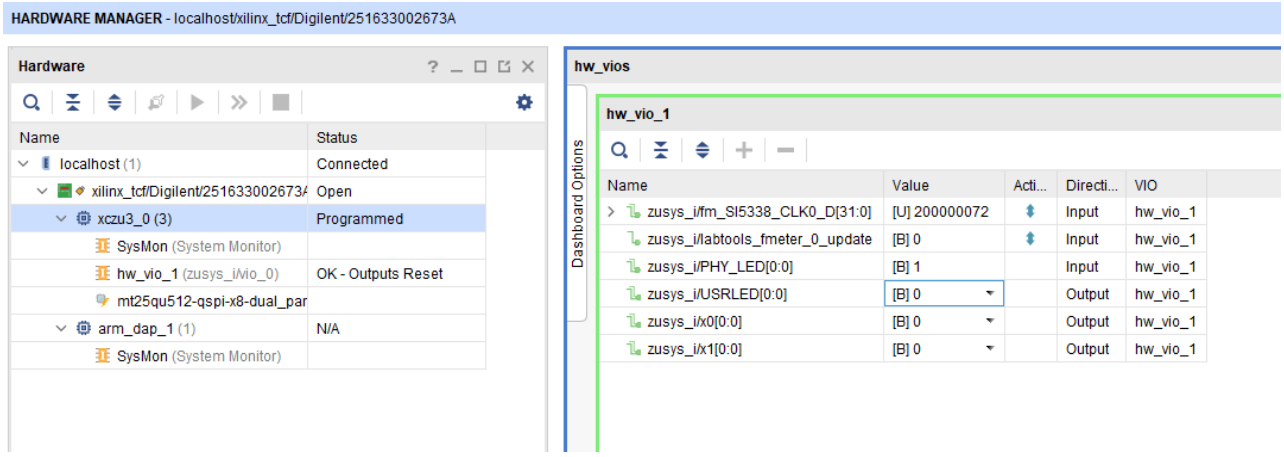
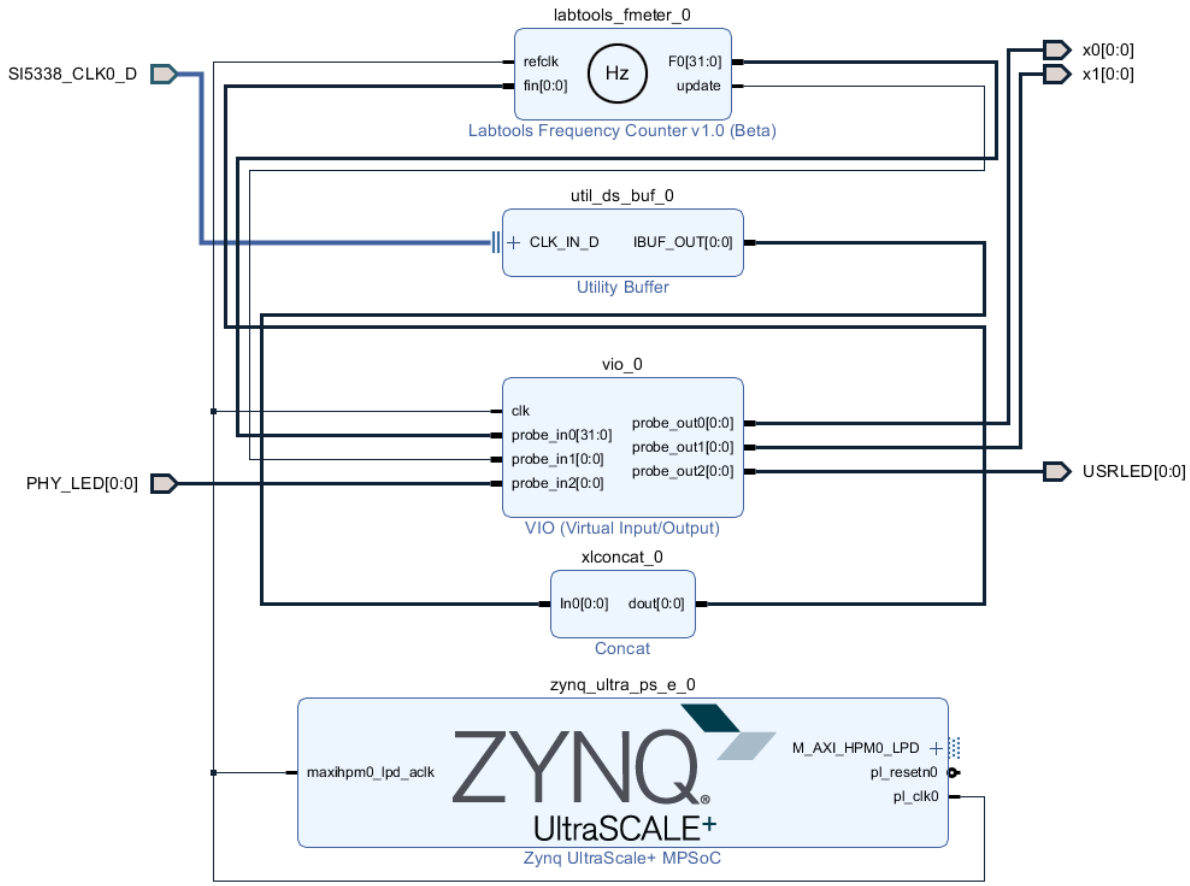


Figure 1: Vivado Hardware Manager

7 System Design - Vivado

7.1 Block Design



7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO

Type	Note
UART0	MIO
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO, USB2 only

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design
```

7.2.2 Design specific constrain

_i_io.xdc

```
set_property PACKAGE_PIN K9 [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property IOSTANDARD LVDS [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property DIFF_TERM TRUE [get_ports {SI5338_CLK0_D_clk_p[0]}]

set_property PACKAGE_PIN B13 [get_ports {x0[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x0[0]}]
set_property PACKAGE_PIN B14 [get_ports {x1[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1[0]}]

set_property PACKAGE_PIN C13 [get_ports {PHY_LED[0]}]
set_property PACKAGE_PIN C14 [get_ports {PHY_LED[1]}]
set_property IOSTANDARD LVCMOS18 [get_ports {PHY_LED*}]
set_property PACKAGE_PIN A15 [get_ports {USRLED[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USRLED*}]
set_property PACKAGE_PIN B14 [get_ports {x1[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1[0]}]
```

8 Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis[18]

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 zynqmp_fsbl

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c(search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)\n\
- General Changes:
    - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
    - Si5338 Configuration
    - ETH+OTG Reset over MIO

8.1.2 zynqmp_fsbl_flash

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl_initialisation.c, xfsbl_hw.h, xfsbl_handoff.c, xfsbl_main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

8.1.3 zynqmp_pmufw

Xilinx default PMU firmware.

8.1.4 hello_te0823

Hello TE0823 is a Xilinx Hello World example as endless loop instead of one console output.

18 https://wiki.trenz-electronic.de/display/PD/Vitis

8.1.5 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart[19]

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- CONFIG_SUBSYSTEM_ETHERNET_PSU_ETHERNET_3_MAC=""

9.2 U-Boot

Start with **petalinux-config -c u-boot**
Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set
- CONFIG_I2C_EEPROM=y
- CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET=0xFA
- CONFIG_SYS_I2C_EEPROM_ADDR=0x50
- CONFIG_SYS_I2C_EEPROM_BUS=0
- CONFIG_SYS_EEPROM_SIZE=256
- CONFIG_SYS_EEPROM_PAGE_WRITE_BITS=0
- CONFIG_SYS_EEPROM_PAGE_WRITE_DELAY_MS=0
- CONFIG_SYS_I2C_EEPROM_ADDR_LEN=1
- CONFIG_SYS_I2C_EEPROM_ADDR_OVERFLOW=0

Change platform-top.h:

19 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart

9.3 Device Tree

```
/include/ "system-conf.dtsi"
/ {
  chosen {
    xlnx,eeprom = &eeprom;
  };
};


/* SDIO */

&sdhci1 {
   disable-wp;
   no-1-8-v;
};

/* ETH PHY */
&gem3 {

    status = "okay";
  ethernet_phy0: ethernet-phy@0 {
        compatible = "marvell,88e1510";
        device_type = "ethernet-phy";
            reg = <1>;
    };
};
/* USB 2.0 */

/* USB  */
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    maximum-speed = "high-speed";
    /delete-property/phy-names;
    /delete-property/phys;
    /delete-property/snps,usb3_lpm_capable;
     snps,dis_u2_susphy_quirk;
    snps,dis_u3_susphy_quirk;
};

&usb0 {
    status = "okay";
    /delete-property/ clocks;
    /delete-property/ clock-names;
    clocks = <0x3 0x20>;
    clock-names = "bus_clk";
};




/* QSPI PHY */
```

```
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

&i2c0 {
  eeprom: eeprom@50 {
     compatible = "atmel,24c08";
     reg = <0x50>;
  };
};
```

9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_CPU_IDLE is not set (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ is not set (only needed to fix JTAG Debug issue)
- CONFIG_EDAC_CORTEX_ARM64=y

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- CONFIG_i2c-tools=y
- CONFIG_busybox-httpd=y (for web server app)
- CONFIG_packagegroup-petalinux-utils(util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

9.6.2 webfwu

Webserver application accemble for Zynq access. Need busybox-httpd

10 Additional Software

10.1 SI5338

File location <design name>/misc/Si5338/Si5338-*.slabtimeproj

General documentation how you work with these project will be available on Si5338[20]

20 https://wiki.trenz-electronic.de/display/PD/Si5338

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2020-03-17	v.4[21]	@ John Hartfiel[22]	• 2019.2 release
	All	@ Mohsen Chamanbaz[23], John Hartfiel[24]	

Table 10: Document change history.

11.2 Legal Notices

11.3 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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21 https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=122855441
22 https://wiki.trenz-electronic.de/display/~j.hartfiel
23 https://wiki.trenz-electronic.de/display/~M.Chamanbaz
24 https://wiki.trenz-electronic.de/display/~j.hartfiel

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25 http://guidance.echa.europa.eu/
26 https://echa.europa.eu/candidate-list-table
27 http://www.echa.europa.eu/

necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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2019-06-07