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U_J1
J1.SchDoc

U_J2
J2.SchDoc

U_J3
J3.SchDoc

U_J4
J4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_B64
B64.SchDoc

U_B65
B65.SchDoc

U_B66
B66.SchDoc

U_B_GT
B_GT.SchDoc

U_B_PS_GT
B_PS_GT.SchDoc

U_PS_DDR
PS_DDR.SchDoc

U_B_MIO
B_MIO.SchDoc

U_B_HD
B_HD.SchDoc

U_Clock
Clock.SchDoc

U_CONFIG
CONFIG.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_DDR4-RAM_3
DDR4-RAM_3.SchDoc

U_DDR4-RAM_4
DDR4-RAM_4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

U_POWER
POWER.SchDoc

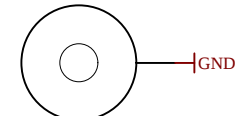
U_POWER_2
POWER_2.SchDoc

U_POWER_4
POWER_4.SchDoc

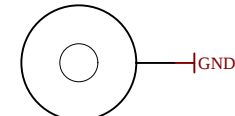
U_REV_CH
Revision_Changes.SchDoc

Special notes:

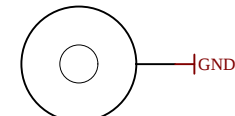
*Low power FPGA
VCCINT = 0.72V*



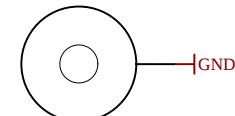
Mount.Hole 3.2mm für Unterlegscheibe



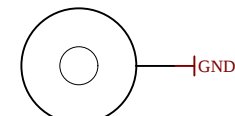
Mount.Hole 3.2mm für Unterlegscheibe



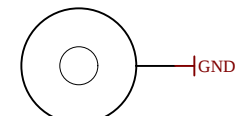
Mount.Hole 3.2mm für Unterlegscheibe



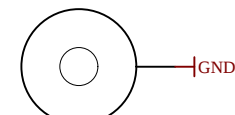
Mount.Hole 3.2mm für Unterlegscheibe



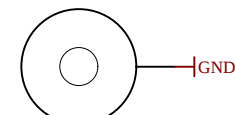
Mount.Hole 3.2mm für Unterlegscheibe



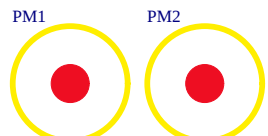
Mount.Hole 3.2mm für Unterlegscheibe



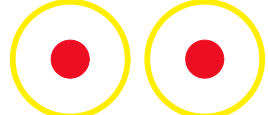
Mount.Hole 3.2mm für Unterlegscheibe



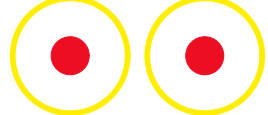
Mount.Hole 3.2mm für Unterlegscheibe



FIDU-DOT - mini PM3 FIDU-DOT - mini PM4



FIDU-DOT - mini PM5 FIDU-DOT - mini PM6



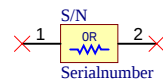
FIDU-DOT - mini FIDU-DOT - mini

LOGO1

TE Logo PRINT Layer

LOGO PRINT

Serial
Serialnumber 6,3 x 6.3mm



Title: TE0803		
A4	Number: TE0803 3RI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page1 of 26
Filename: TE0803.SchDoc		

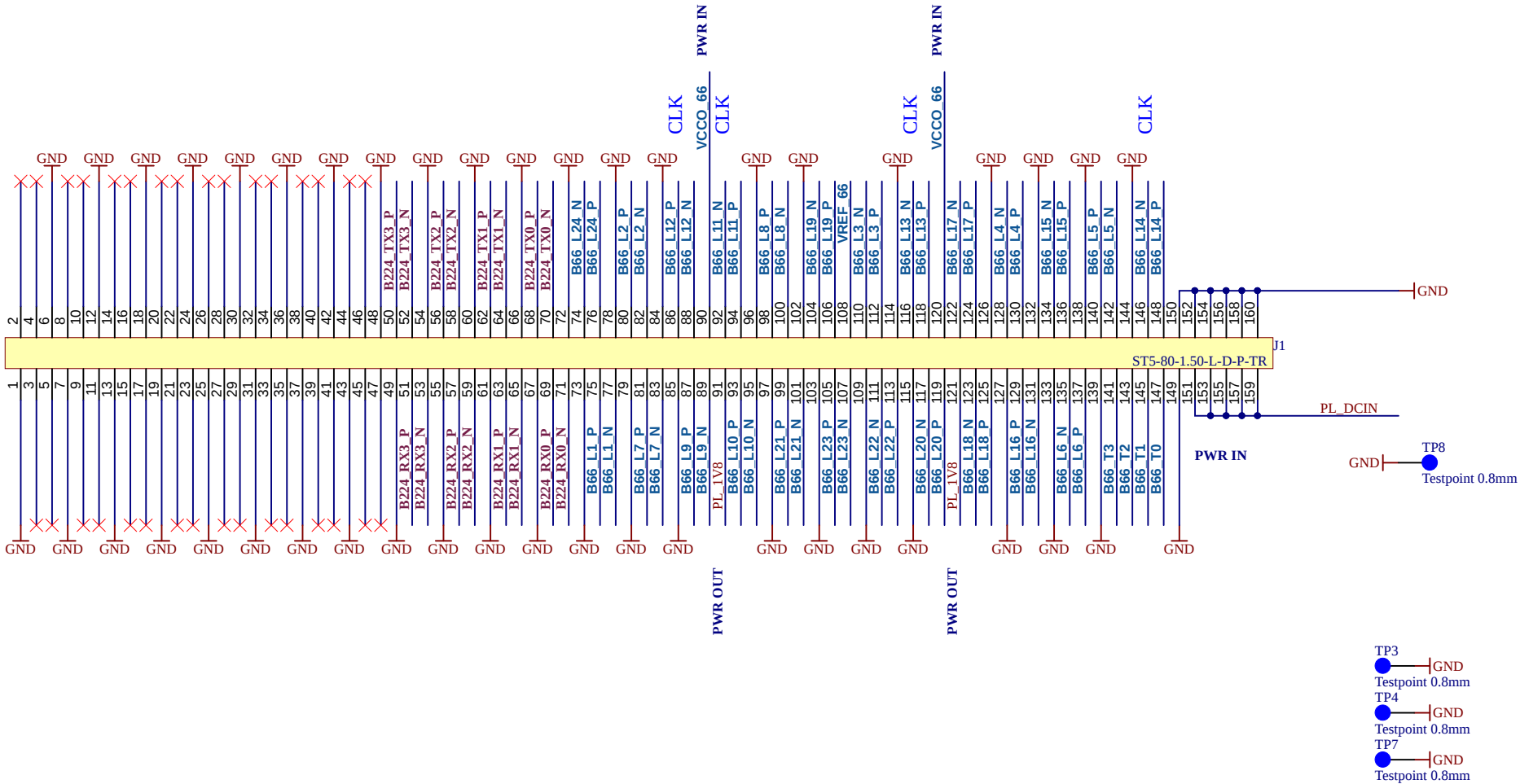
Assembly variant	3RI21-A
Created by	VY
Modified by	VY
Modified at	2020-02-12
SVN Revision	9100 [Locally Modified]

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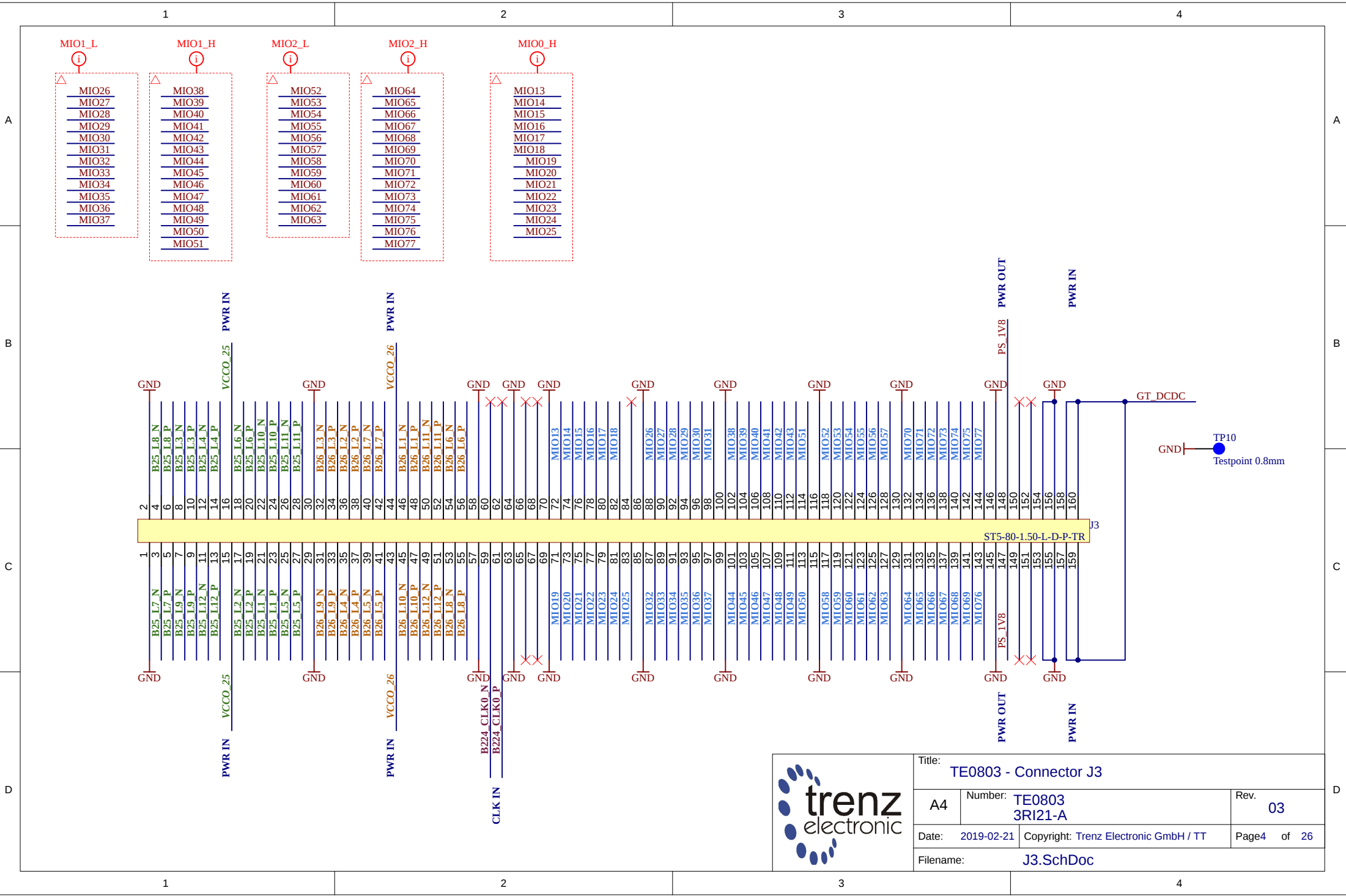
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Title:		TE0803 - Connector J1	
A4	Number:	TE0803 3RI21-A	Rev. 03
Date:	2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename:		J1.SchDoc	



Title: TE0803 - Connector J3		
A4	Number: TE0803 3RI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page4 of 26
Filename: J3.SchDoc		

A

B

C

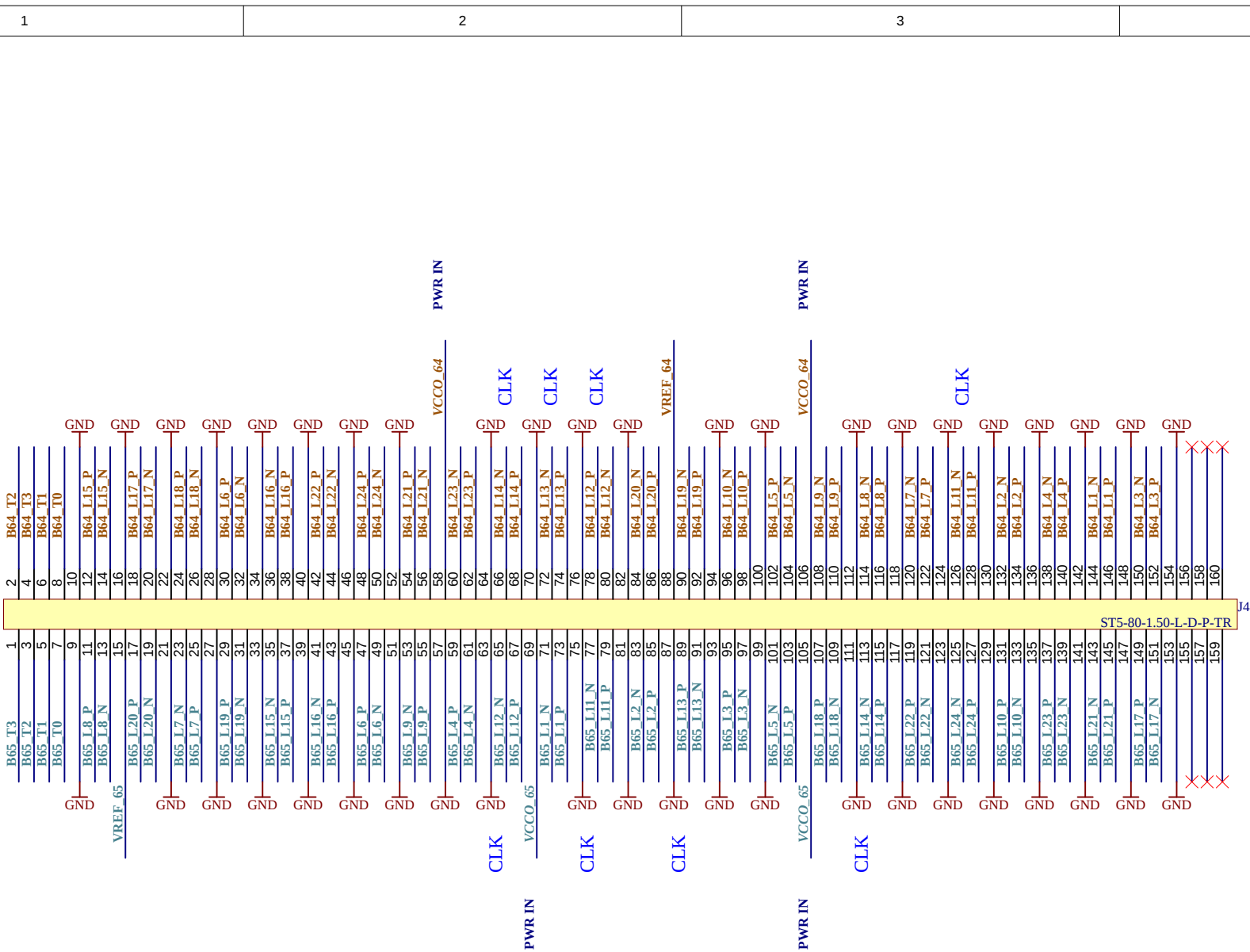
D

A

B

C

D



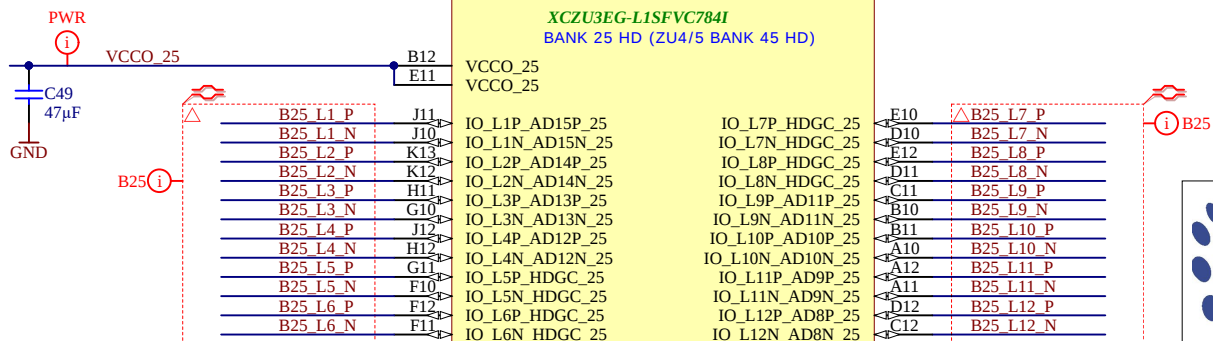
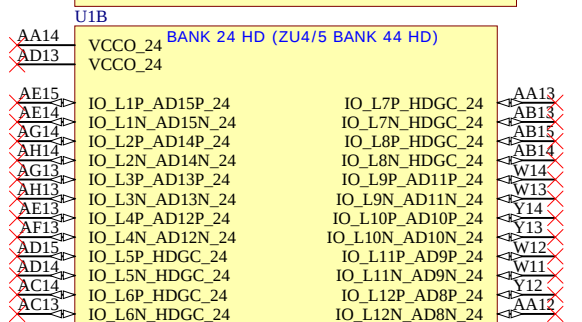
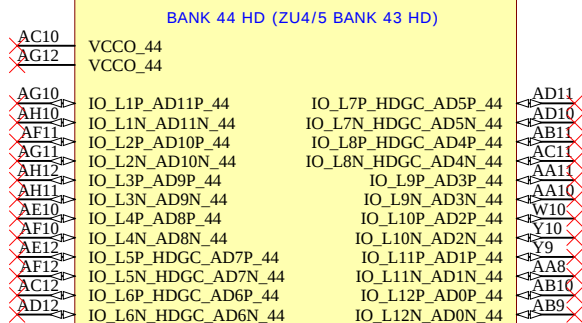
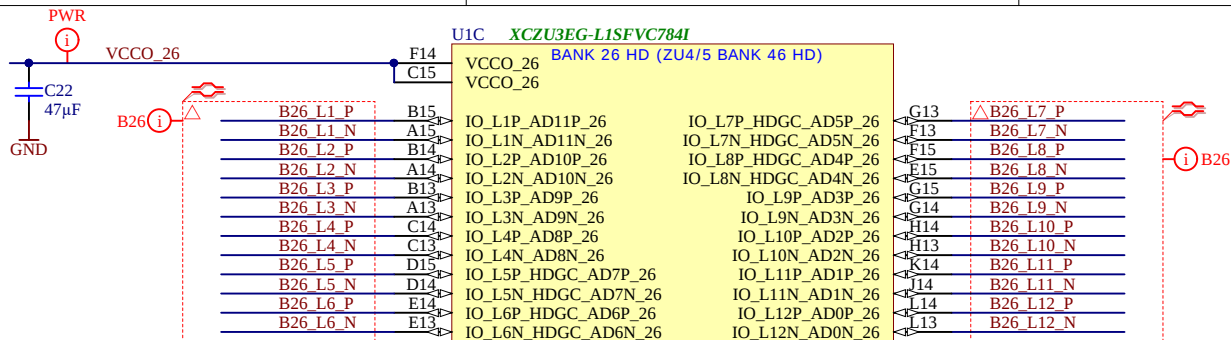
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A4	Number: TE0803 3RI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		

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Title: TE0803 - HD Banks			
A4	Number: TE0803 3RI21-A	Rev. 03	
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page6 of 26
Filename: B HD.SchDoc			

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A

A

B

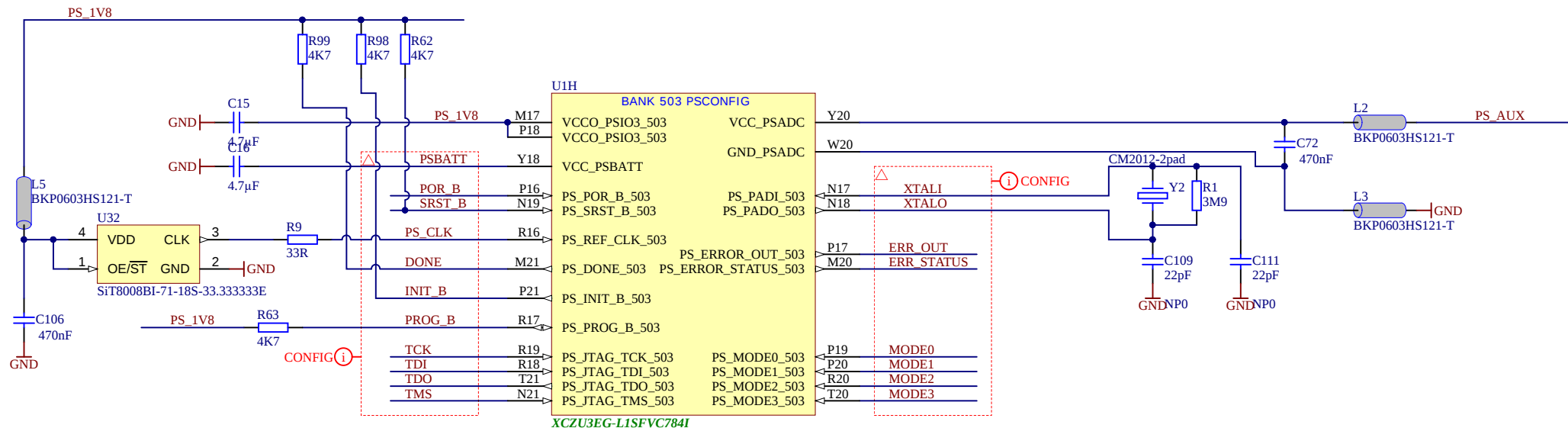
B

C

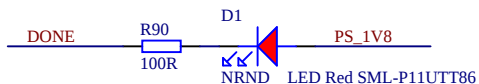
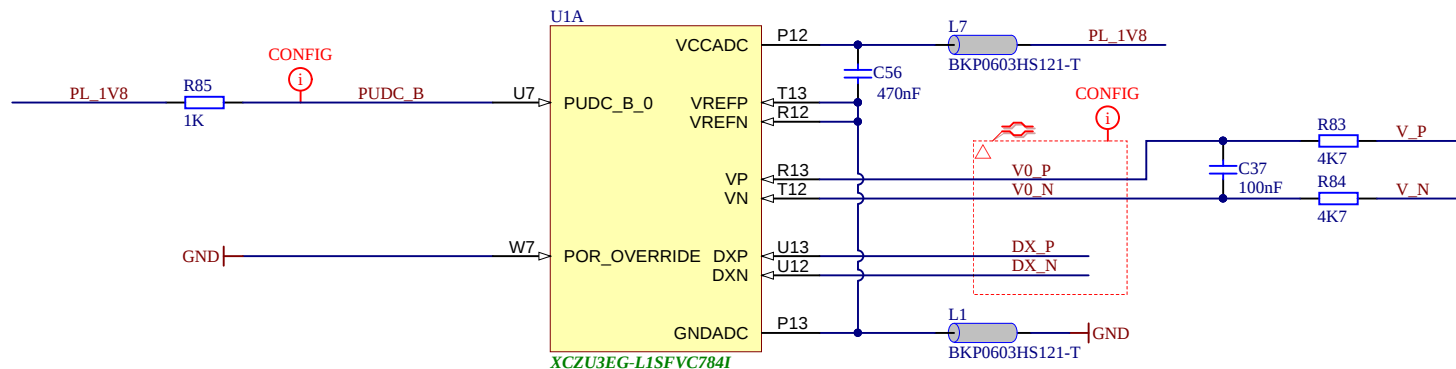
C

D

D



PS_CLK
TP32



		Title: TE0803 - Config	
		A4	Rev. 03
Date: 2019-02-21		Number: TE0803 3R121-A	Page 7 of 26
Filename: CONFIG.SchDoc		Copyright: Trenz Electronic GmbH / TT	

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A

A

B

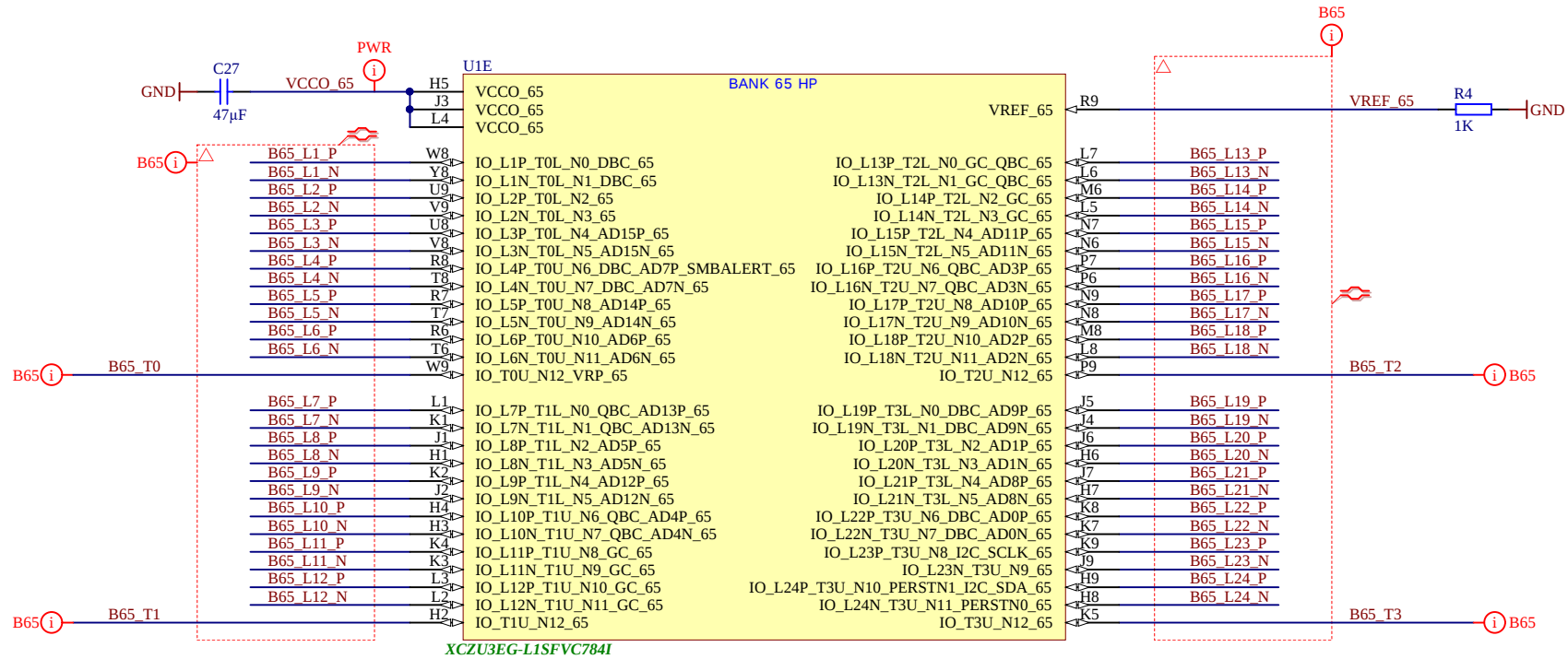
B

C

C

D

D



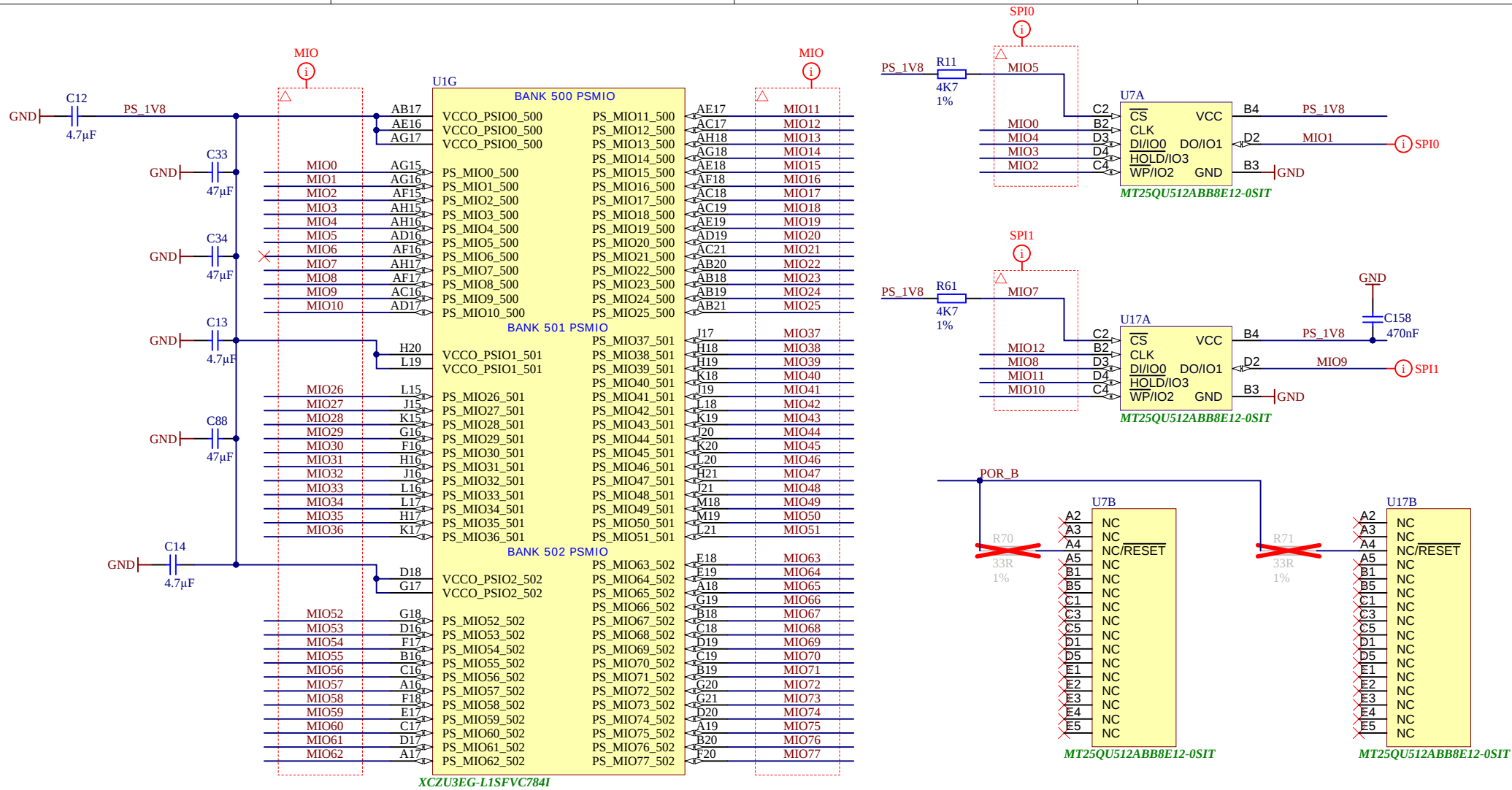
Title: TE0803 - B65			
A4	Number: TE0803 3RI21-A	Rev. 03	
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page9 of 26
Filename: B65.SchDoc			

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Title: TE0803 - MIO Banks			
A4	Number:	TE0803 3RI21-A	Rev. 03
	Date:	2019-02-21	Page11 of 26
	Filename:	B_MIO.SchDoc	

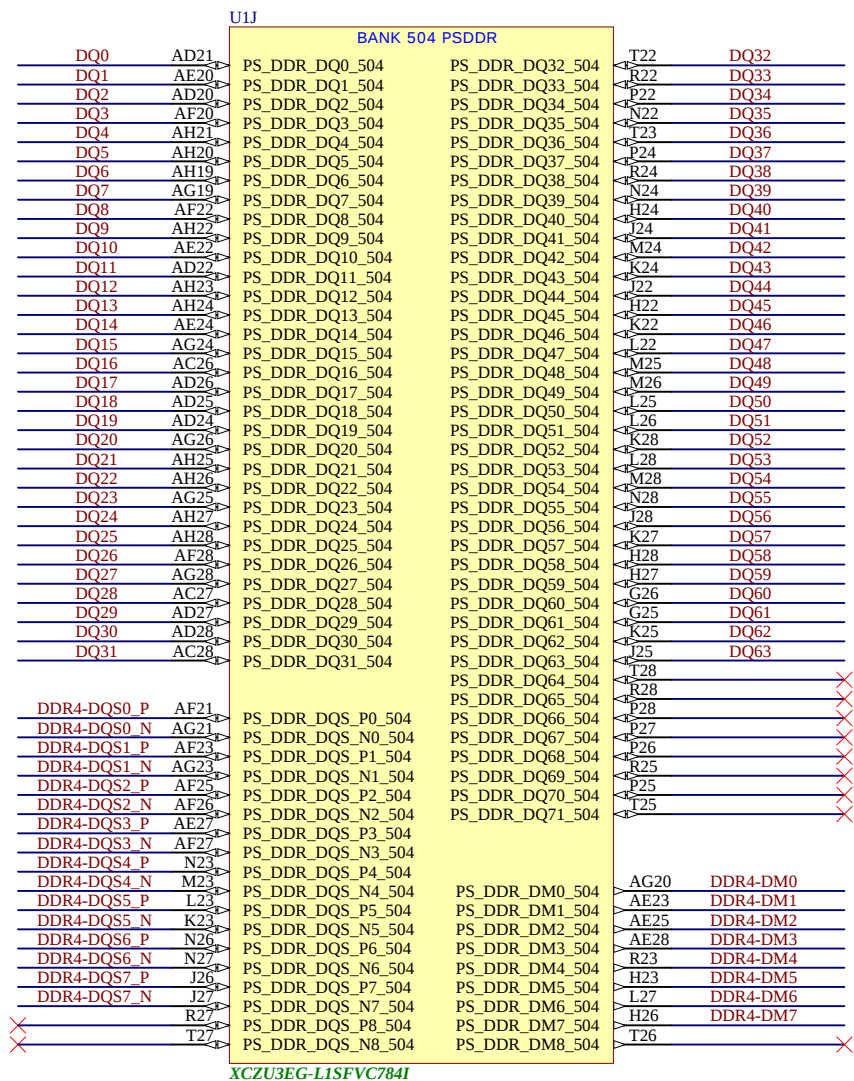
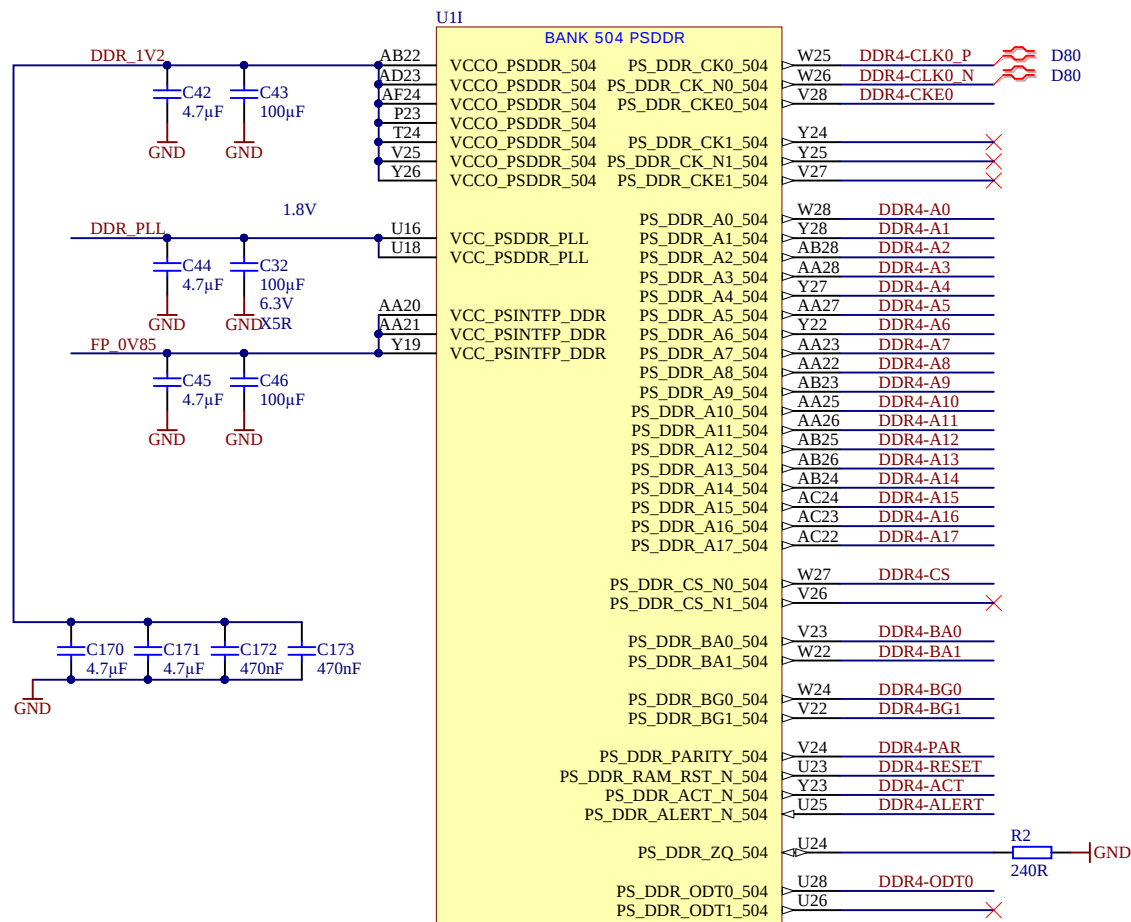


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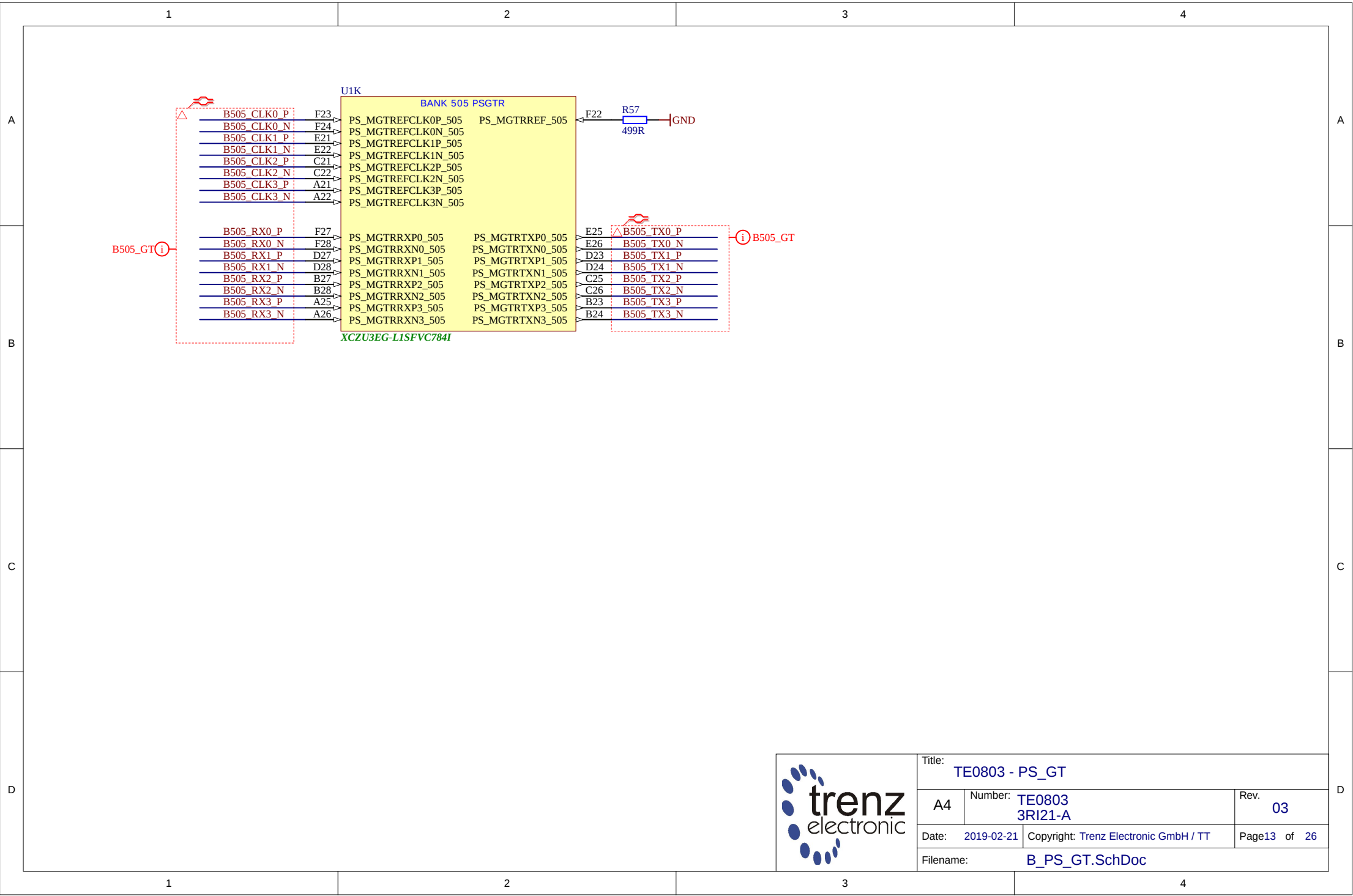
Title: TE0803 - PS_DDR			
A4	Number: TE0803 3RI21-A		Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page12 of 26
Filename:		PS_DDR.SchDoc	

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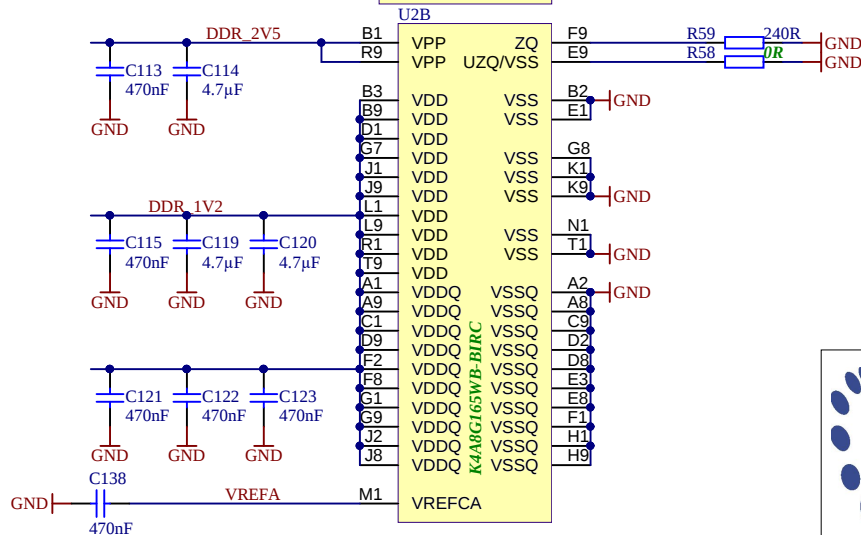
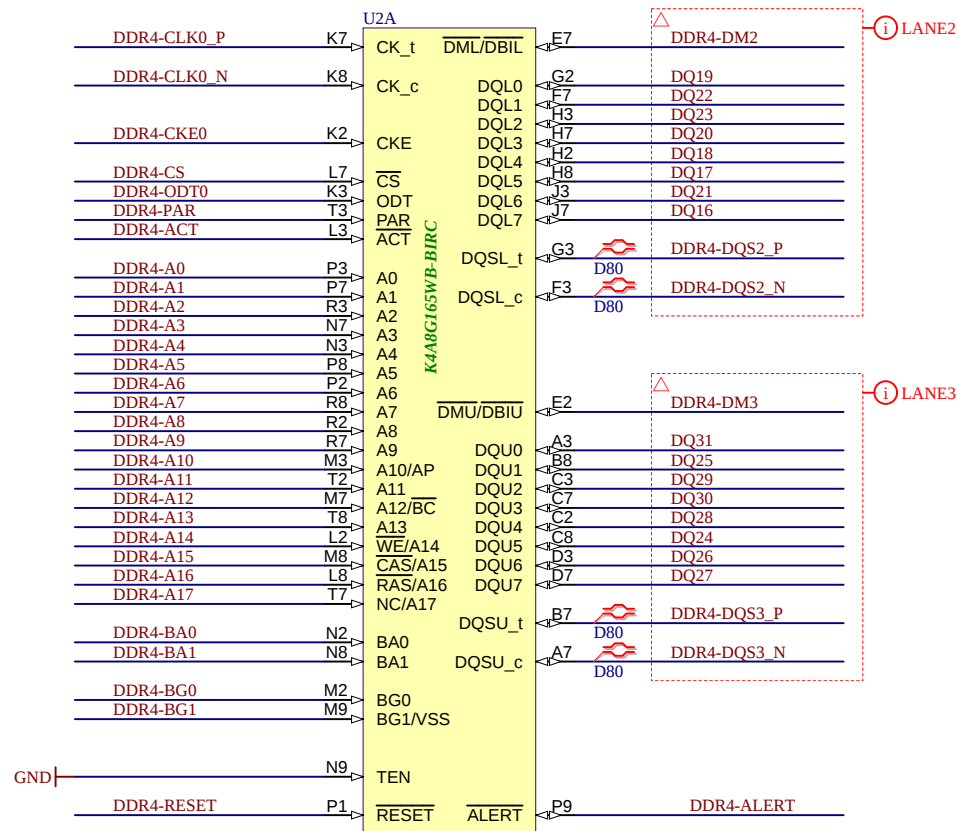


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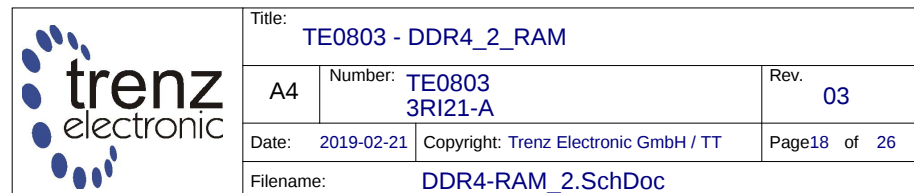
Title: TE0803 - DDR4_1_RAM		
A4	Number: TE0803 3RI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page17 of 26
Filename: DDR4-RAM.SchDoc		

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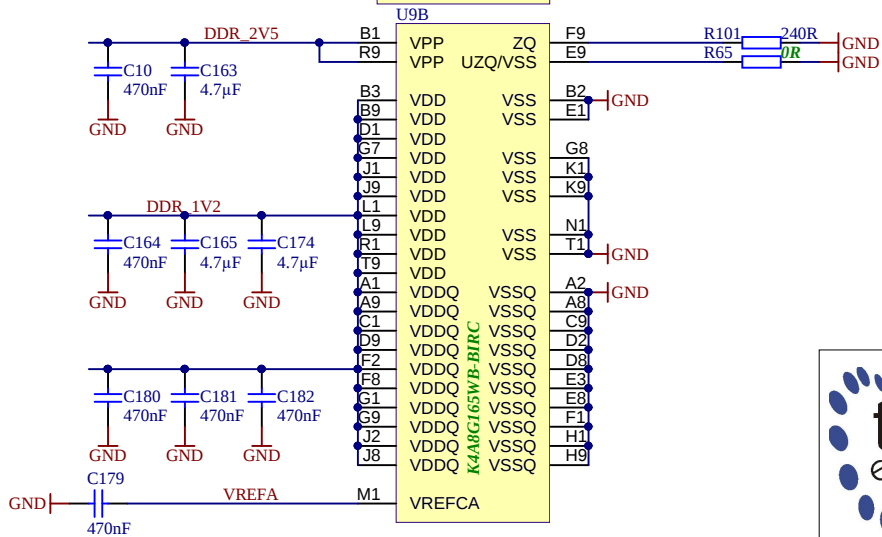
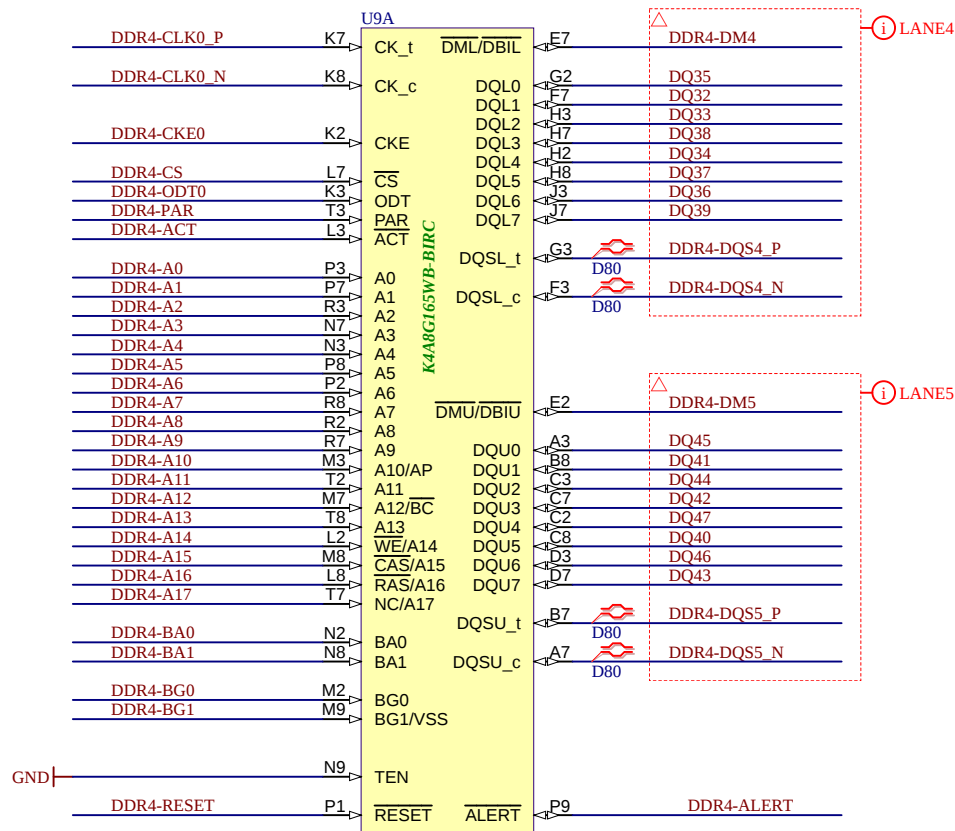


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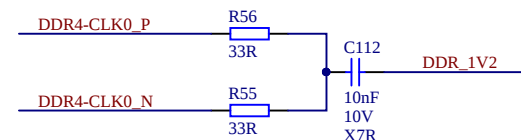
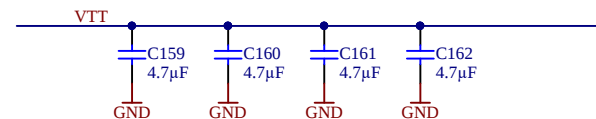
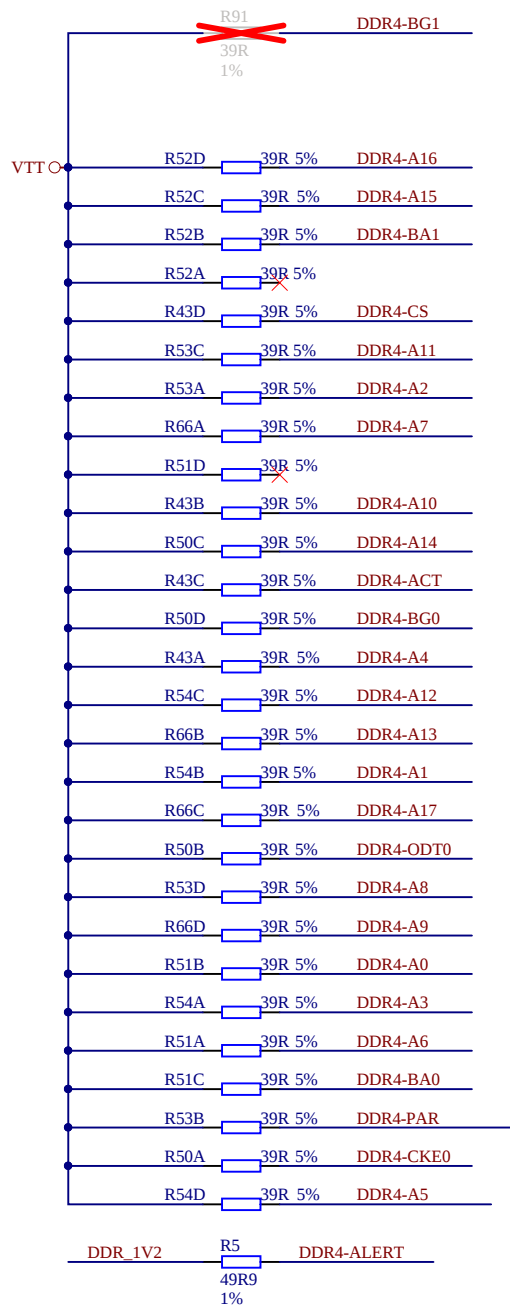
Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 3RI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page19 of 26
Filename: DDR4-RAM_3.SchDoc		

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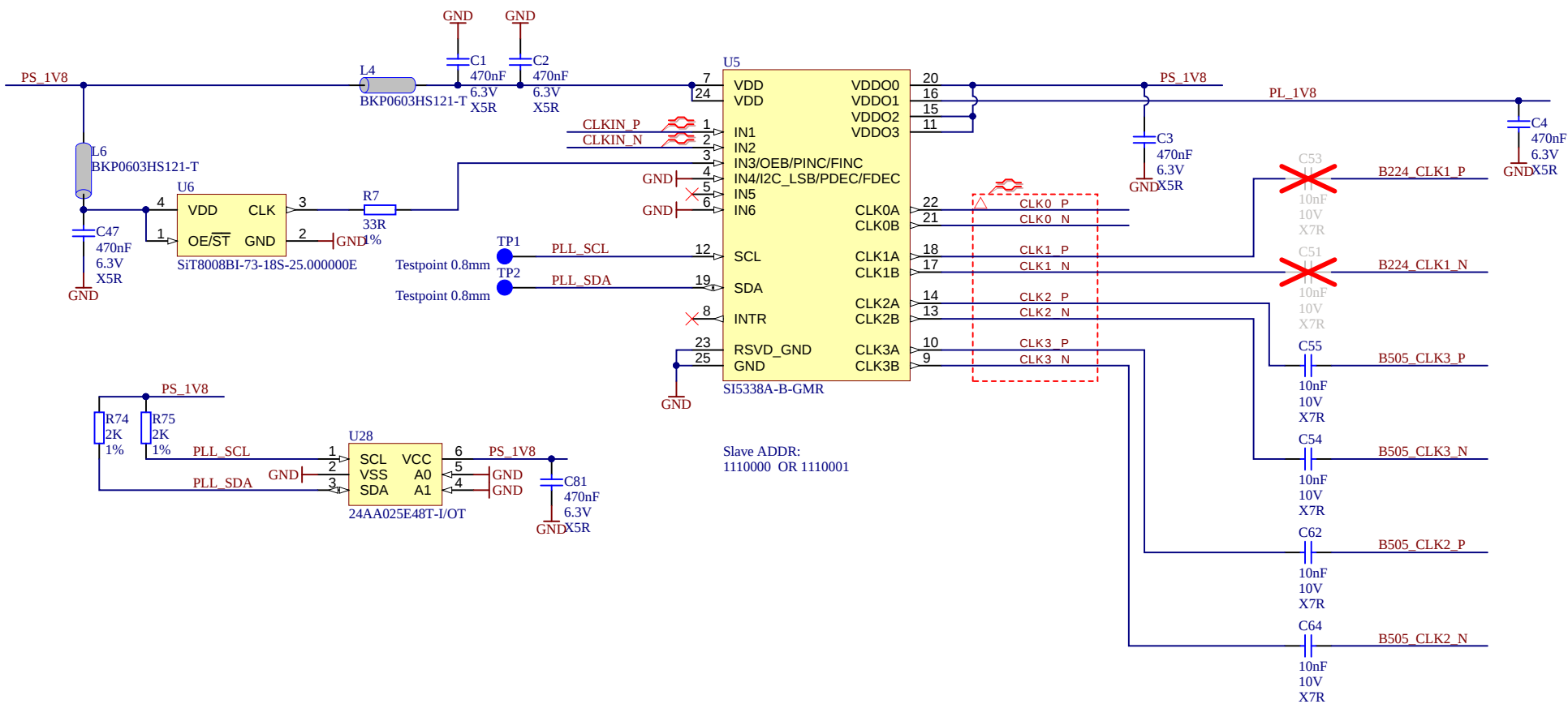
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		A4 Number: TE0803 3R121-A	Rev. 03
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: DDR4-TERM.SchDoc		Page21 of 26	



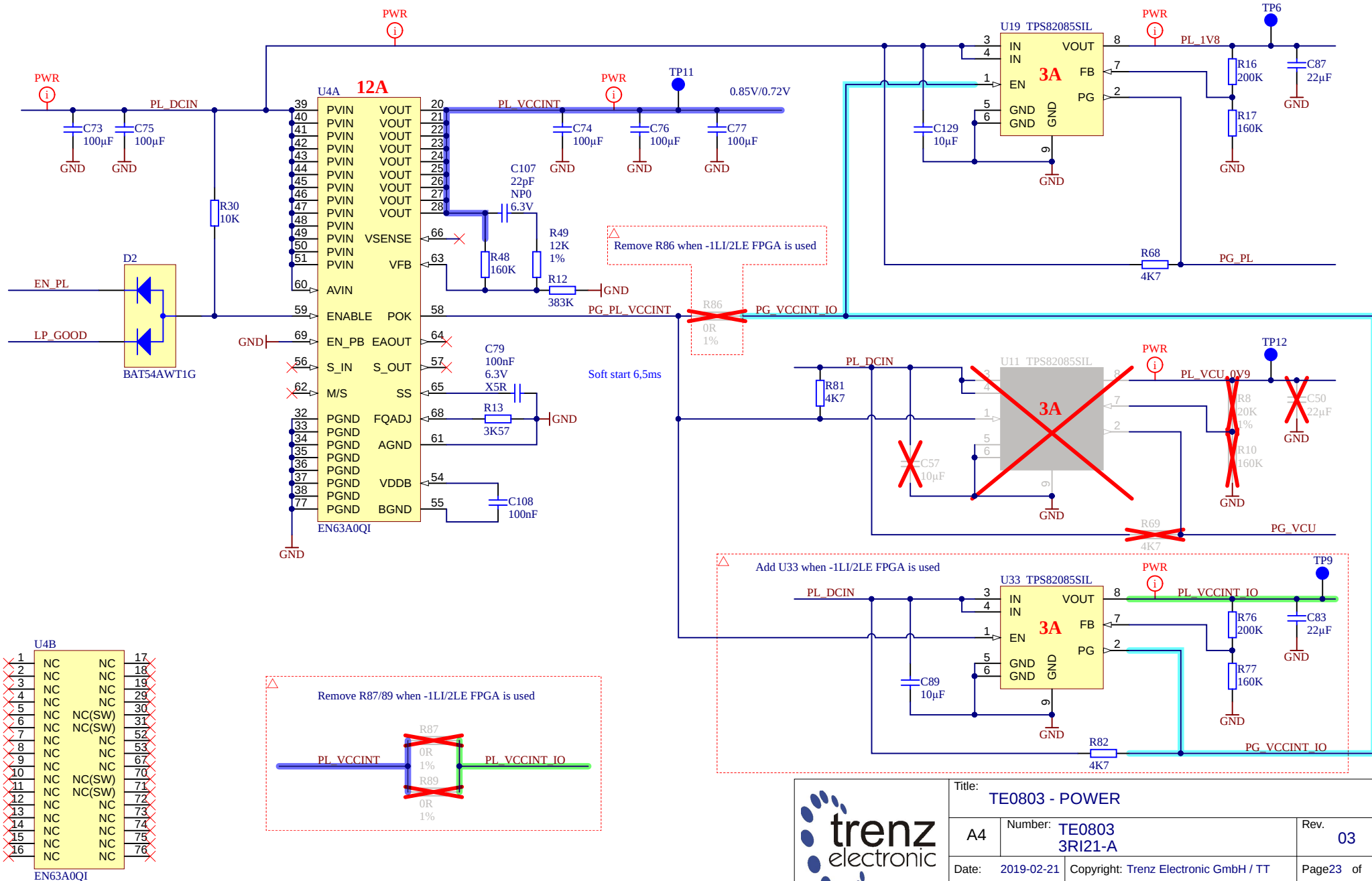
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	A4	Number: TE0803 3R121-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page22 of 26
	Filename: Clock.SchDoc		

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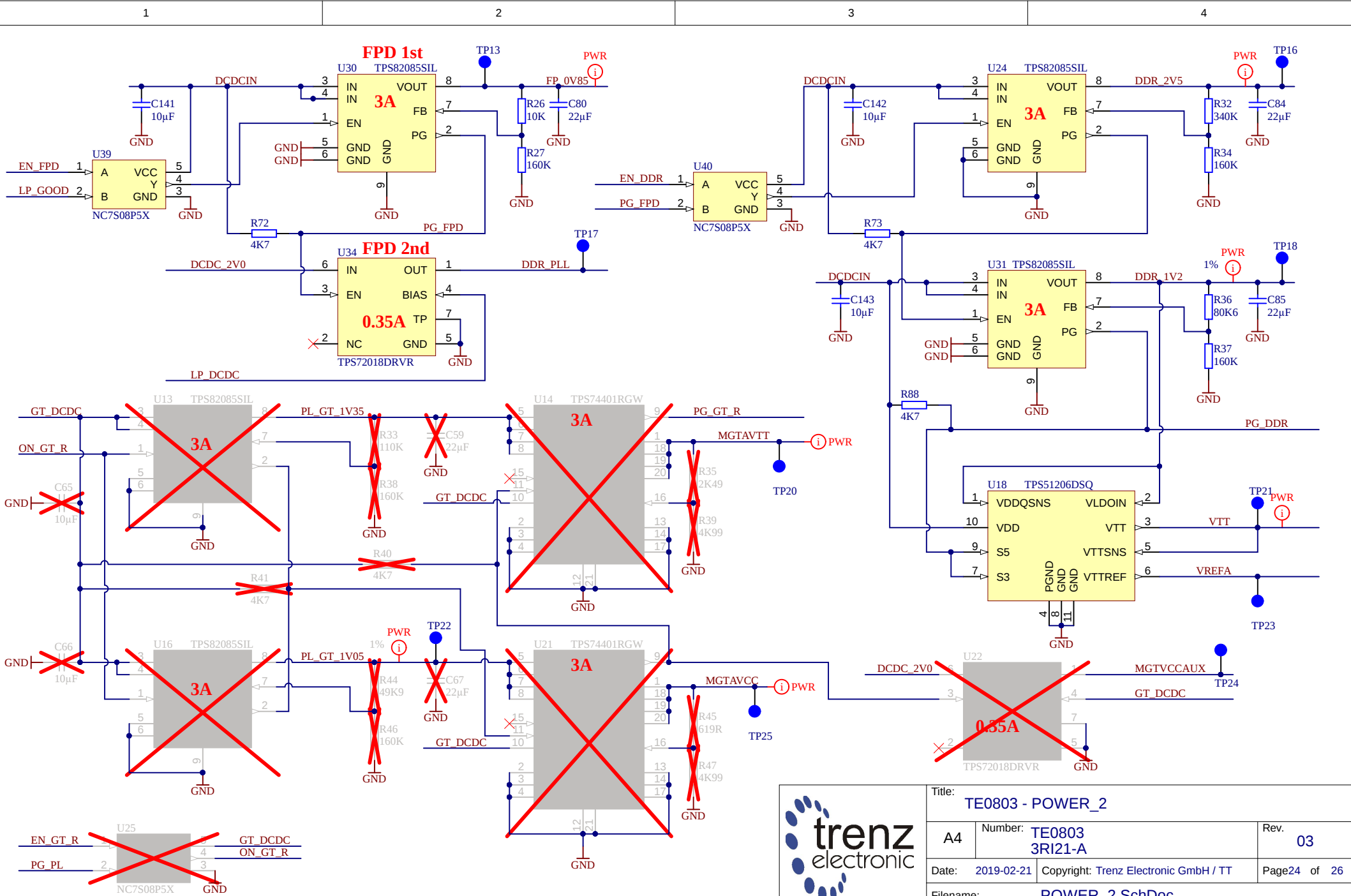


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Title: TE0803 - POWER_2		
A4	Number: TE0803 3RI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	
Filename: POWER_2.SchDoc	Page24 of 26	

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CHANGES REV01a (20.11.2017):

1) VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR_PLL
- 2) All differential pairs with length matched with tolerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):

- 1) Added support of DDP DDR4
- 2) Added support of Low power FPGA (-L1/L2).
- 3) Revised testpoints
- 4) Revised J1-J4 connectors net label style



Title: TE0803 - Changes list			
A4	Number: TE0803 3RI21-A	Rev. 03	
Date: 2019-02-21	Copyright: Trenz Electronic GmbH		Page26 of 26
Filename:		Revision_Changes.SchDoc	

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