TE0807 Test Board

Revision v.15

Exported on 2022-05-18

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0807+Test+Board

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4 Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via SDK.

Refer to http://trenz.org/te0807-info for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2020.2
- QSPI
- Custom Carrier (minimum PS Design with available module components only)
- Modified FSBL (some additional outputs only)
- Special FSBL for QSPI Programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2021-02-08	2020.2	TE0807-test_board_noprebuilt-vivado_2020.2-build_1_20210208093457.zip TE0807-test_board-vivado_2020.2-build_1_20210208093443.zip	John Hartfiel	• 2020.2 update
2020-10-06	2019.2	TE0807-test_board_noprebuilt-vivado_2019.2-build_15_20201006121447.zip TE0807-test_board-vivado_2019.2-build_15_20201006121342.zip	John Hartfiel	• new assembly variants
2020-03-25	2019.2	TE0807-test_board_noprebuilt-vivado_2019.2-build_8_20200325082749.zip TE0807-test_board-vivado_2019.2-build_8_20200325082730.zip	John Hartfiel	• script update
2020-01-27	2019.2	TE0807-test_board_noprebuilt-vivado_2019.2-build_4_20200127075704.zip	John Hartfiel	• 2019.2 update • Vitis support

Date	Vivado	Project Built	Authors	Description
		TE0807-test_board-vivado_2019.2-build_4_20200127075454.zip		
2019-05-22	2018.3	TE0807-test_board_noprebuilt-vivado_2018.3-build_05_20190522132408.zip TE0807-test_board-vivado_2018.3-build_05_20190522132356.zip	John Hartfiel	• custom FSBL • Note: Prebuilt for ES2 version not included
2019-02-08	2018.2	TE0807-test_board_noprebuilt-vivado_2018.2-build_04_20190207111539.zip TE0807-test_board-vivado_2018.2-build_04_20190207111524.zip	John Hartfiel	• new assembly variant
2018-09-04	2018.2	TE0807-test_board_noprebuilt-vivado_2018.2-build_03_20180904121458.zip TE0807-test_board-vivado_2018.2-build_03_20180904121522.zip	John Hartfiel	• additional notes for FSBL generated with Win SDK • changed *.bif
2018-01-18	2017.4	TE0807-test_board_noprebuilt-vivado_2017.4-build_05_20180118152119.zip TE0807-test_board-vivado_2017.4-build_05_20180118152104.zip	John Hartfiel	• rework Board Part Files
2017-11-14	2017.2	TE0807-test_board_noprebuilt-vivado_2017.2-build_05_20171114115524.zip TE0807-test_board-vivado_2017.2-build_05_20171114115511.zip	John Hartfiel	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2020.2	needed, Vivado is included into Vitis installation

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[1]

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
~~TE0807-01-07EV-ES~~	~~es2_2gb~~	~~REV01~~	~~2GB~~	~~64GB~~	~~NA~~	~~NA~~	~~Not longer supported by vivado~~
TE0807-02-07EV-1E	7ev_1e_4gb	REV02	4GB	64GB	NA	NA	NA
TE0807-02-07EV-1EK	7ev_1e_4gb	REV02	4GB	64GB	NA	NA	with heat sink
TE0807-02-4BE21-A	4eg_1e_4gb	REV02	4GB	128MB	NA	NA	NA

1 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0807-02-7DE21-A	7ev_1e_4gb	REV02	4GB	128MB	NA	NA	NA
TE0807-02-7DI21-C	7ev_1i_4gb	REV02	4GB	128MB	NA	NA	without encryption
TE0807-02-7DI21-A	7ev_1i_4gb	REV02	4GB	128MB	NA	NA	NA
TE0807-02-4AI21-A	4cg_1i_4gb	REV02	4GB	128MB	NA	NA	NA
TE0807-02-5AI21-A	5cg_1i_4gb	REV02	4GB	128MB	NA	NA	NA
TE0807-02-7AI21-A	7cg_1i_4gb	REV02	4GB	128MB	NA	NA	NA
TE0807-02-7DI24-A	7ev_1i_4gb	REV02	4GB	512MB	NA	NA	NA
TE0807-02-7DE21-AK	7ev_1e_4gb	REV02	4GB	128MB	NA	NA	with heat sink
TE0807-02-4AI21-X	4cg_1i_4gb	REV02	4GB	128MB	NA	NA	U41 replaced with diode
TE0807-02-4BE21-AK	4eg_1e_4gb	REV02	4GB	128MB	NA	NA	with heat sink
TE0807-02-7DI21-AK	7ev_1i_4gb	REV02	4GB	128MB	NA	NA	with heat sink
TE0807-02-5DI21-A	5ev_1i_4gb	REV02	4GB	128MB	NA	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0807-02-7NE21-A	7ev_3e_4gb	REV02	4GB	128MB	NA	NA	NA
TE0807-03-5DI21-A	5ev_1i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0807-03-7NE21-A	7ev_3e_4gb	REV03	4GB	128MB	NA	NA	NA
TE0807-03-4AI21-X	4cg_1i_4gb	REV03	4GB	128MB	NA	NA	U41 replaced with diode
TE0807-03-4AI21-A	4cg_1i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0807-03-4AI21-C	4cg_1i_4gb	REV03	4GB	128MB	NA	NA	without encryption
TE0807-03-4BE21-A	4eg_1e_4gb	REV03	4GB	128MB	NA	NA	NA
TE0807-03-5AI21-A	5cg_1i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0807-03-7AI21-A	7cg_1i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0807-03-7DE21-A	7ev_1e_4gb	REV03	4GB	128MB	NA	NA	NA
TE0807-03-7DE21-AK	7ev_1e_4gb	REV03	4GB	128MB	NA	NA	with heat sink
TE0807-03-7DI21-A	7ev_1i_4gb	REV03	4GB	128MB	NA	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0807-03-7DI21-C	7ev_1i_4gb	REV03	4GB	128MB	NA	NA	without encryption
TE0807-03-7DI24-A	7ev_1i_4gb	REV03	4GB	512MB	NA	NA	NA

Table 4: Hardware Modules
Note: Design contains also Board Part Files for TE0807+TEBF0808 configuration, this boart part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
Custom PCB	use simple Board Part files, if MIO connected is different to TEBF0808
TEBF0808	Used as reference carrier.
TEBT0808-01	Change UART0 to UART1 (MIO68...69) and regenerate design

Table 5: Hardware Carrier
Additional HW Requirements:

Additional Hardware	Notes
---	---

Table 6: Additional Hardware

4.5 Content

For general structure and of the reference design, see Project Delivery - Xilinx devices[2]

4.5.1 Design Sources

2 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
---	---	---

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File

File	File-Extension	Description
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebult content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0807 "Test Board" Reference Design[3]

3 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0807/Reference_Design/2020.2/test_board

5 Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

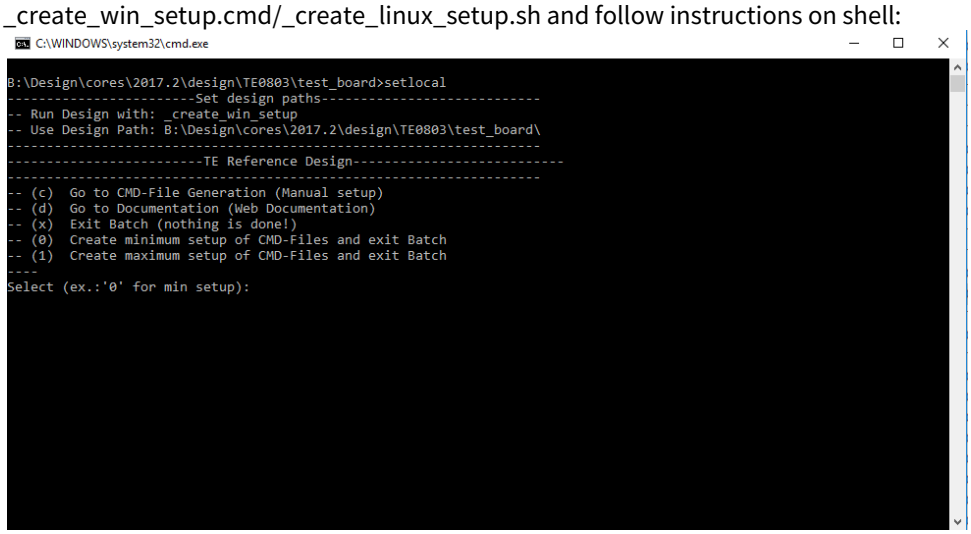
See also:

- Xilinx Development Tools[4]
- Vivado Projects - TE Reference Design[5]
- Project Delivery.[6]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[7]

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
   a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
      Note: Select correct one, see TE Board Part Files
      [8] Important: Use Board Part Files, which **did not** ends with *_tebf0808
5. Create XAS and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder

4 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
5 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
6 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality
8 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

6. Generate Programming Files with Vitis
    a. Run on Vivado TCL: TE::sw_run_vitis -all
       Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
    b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
       Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used.
       See Vitis[9]

9 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging[10]

6.1.1 Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder
   Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

6.1.2 QSPI

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp hello_te0807
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup

6.1.3 SD

This does not work, because SD controller is not selected on PS.

6.1.4 JTAG

Load configuration and Application with Vitis Debugger into device.

6.2 Usage

QSPI Boot:

1. Prepare HW like described on section Programming(see page 17)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI Card as Boot Mode
   Note: See TRM of the Carrier, which is used.

10 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging

4. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from QSPI into OCM, 2. FSBL loads Application into DDR

7 System Design - Vivado

7.1 Block Design

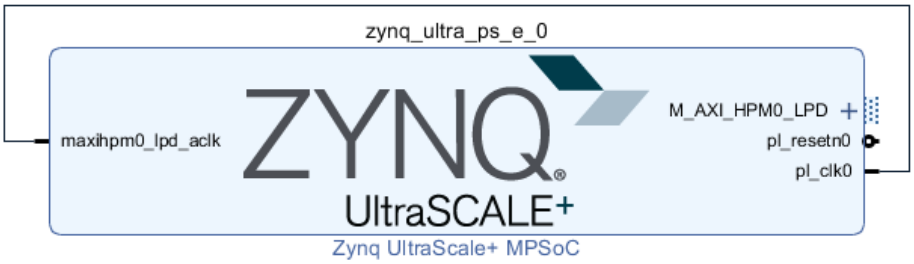


Figure 1: Block Design

7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
UART0	MIO, please select other one, if you have connected uart to second controller or other MIO
SWDT0..1	
TTC0..3	

Table 10: PS Interfaces

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

7.2.2 Design specific constrain

Not needed.

8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:

Vitis[11]

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 zynqmp_fsbl

TE modified 2020.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c(search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)\n\
- General Changes:
    - Display FSBL Banner and Device Name

8.1.2 zynqmp_fsbl_flash

TE modified 2020.2 FSBL

General:

- Modified Files: xfsbl_initialisation.c, xfsbl_hw.h, xfsbl_handoff.c, xfsbl_main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

8.1.3 hello_te0807

Hello TE0807 is a Xilinx Hello World example as endless loop instead of one console output.

11 https://wiki.trenz-electronic.de/display/PD/Vitis

9 Additional Software

No additional software is needed.

10 Appx. A: Change History and Legal Notices

10.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2021-02-08	v.15(see page 6)	@ John Hartfiel[12]	• new assembly variants • document style update
2020-10-06	v.14	John Hartfiel	• new assembly variants
2020-03-25	v.13	John Hartfiel	• script update
2020-01-27	v.12	John Hartfiel	• Release 2019.2 • new assembly variants
2019-05-22	v.10	John Hartfiel	• Release 2018.3
2019-02-07	v.9	John Hartfiel	• new assembly variant
2018-09-04	v.7	John Hartfiel	• Release 2018.2
2018-02-08	v.5	John Hartfiel	• Release 2017.4
2017-11-14	v.3	John Hartfiel	• Release 2017.2
--	all	@ John Hartfiel[13]	--

10.2 Legal Notices

10.3 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

12 https://wiki.trenz-electronic.de/display/~j.hartfiel
13 https://wiki.trenz-electronic.de/display/~j.hartfiel

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14 http://guidance.echa.europa.eu/

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2019-06-07

15 https://echa.europa.eu/candidate-list-table
16 http://www.echa.europa.eu/