TE0817 StarterKit

Revision v.5

Exported on 2023-06-29

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0817+StarterKit

1 Table of Contents

2 Table of Figures

3 Table of Tables

4 Overview

Refer to http://trenz.org/te0817-info for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2021.2.1
- TEBF0818
- Linux
- USB
- ETH
- MAC from EEPROM
- PCIe
- SATA
- SD
- I2C
- RGPIO
- Display Port (DP)
- user LED access
- Modified FSBL for Si5345 programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2022-09-12	2021.2.1	TE0817-StarterKit-vivado_2021.2-build_15_20220912093833.zip TE0817-StarterKit_noprebuilt-vivado_2021.2-build_15_20220912093833.zip	Manuela Strücker	• update board part file compatible to Vivado 2021.2.1

Date	Vivado	Project Built	Authors	Description
2022-06-27	2021.2	TE0817-StarterKit-vivado_2021.2-build_14_20220627122156.zip TE0817-StarterKit_noprebuilt-vivado_2021.2-build_14_20220627122156.zip	Manuela Strücker	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see Xilinx Forum Request[1]	use corresponding board files for the Vivado versions	--

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2021.2.1	needed, Vivado is included into Vitis installation
PetaLinux	2021.2	needed

1 https://support.xilinx.com/s/feed/0D54U00005Wbon6SAB?language=en_US

Software	Version	Note
SI ClockBuilder Pro	---	optional

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[2]

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0817-01-7DE21-A*	7ev_1e_4gb	REV01	4GB	128MB	NA	NA	NA

Table 4: Hardware Modules
*used as reference

Design supports following carriers:

Carrier Model	Notes
TEBF0818	

Table 5: Hardware Carrier
*used as reference

Additional HW Requirements:

Additional Hardware	Notes
Display Port Monitor	Optional HW Not all monitors are supported, also Adapter to other Standard can make trouble. Design was tested with **DELL U2412M**

2 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Additional Hardware	Notes
USB Keyboard	Optional HW Can be used to get access to console which is show on Display Port
USB Stick	Optional HW USB was tested with USB memory stick
SATA Disk	Optional HW
PCIe Card	Optional HW
ETH cable	Optional HW Ethernet works with DHCP, but can be setup also manually
SD card	with fat32 partition

Table 6: Additional Hardware
*used as reference

4.5 Content

For general structure and usage of the reference design, see Project Delivery - Xilinx devices[3]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts

3 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

Type	Location	Notes
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
SI5345	<project folder>\misc\PLL\Si5345_D	SI5345 Project with current PLL Configuration
init.sh	<project folder>\misc\sd\	Additional Initialization Script for Linux

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface

File	File-Extension	Description
Diverse Reports	---	Report files in different formats
Device Tree	*.dts	Device tree (2 possible, one for u-boot and one for linux)
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebuilt content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0817 "Starterkit" Reference Design[4]

4 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0817/Reference_Design/2021.2/StarterKit

5 Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools[5]
- Vivado Projects - TE Reference Design[6]
- Project Delivery.[7]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[8]

> ⚠ **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths----------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
------------------------------------------------------------------
-------------------------TE Reference Design--------------------------
------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.

5 https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDevelopmentTools-XilinxSoftware-BasicUserGuides
6 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
8 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality

- optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

  Note: Select correct one, see also Vivado Board Part Flow[9]

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")

```
\prebuilt\hardware\")">
TE::hw_build_design -export_prebuilt
```

Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart[10]
   - use TE Template from "<project folder>\os\petalinux"
   - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
   - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr[11]
7. Copy PetaLinux build image files to prebuilt folder
   - copy **u-boot.elf**, **u-boot.dtb, system.dtb**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

     "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

8. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE
Scripts on Vivado TCL)
```

TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis[12]

9 https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow
10 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
11 https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr
12 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.
Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging[13]

6.1.1 Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select create and open delivery binary folder

   ⓘ Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

6.1.2 QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

   run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

   ```
   TE::pr_program_flash -swapp hello_te0817
   ```

3. Set Boot Mode to **QSPI-Boot.**
   - Depends on Carrier, see carrier TRM.

6.1.3 SD-Boot mode

1. Copy **image.ub, boot.src** and **Boot.bin** on **SD**
   - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder, see: Get prebuilt boot binaries(see page 15)
   - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
2. Set Boot Mode to SD-Boot.
   - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

13 https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDevelopmentTools-XilinxSoftwareProgrammingandDebugging

6.1.4 JTAG

Not used on this example.

6.2 Usage

1. Prepare HW like described on section Programming(see page 15)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

   Note: See TRM of the Carrier, which is used.

   Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
   The boot options described above describe the common boot processes for this hardware; other boot options are possible.
   For more information see Distro Boot with Boot.scr[14]

4. (Optional with TEBF0818) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional with TEBF0818) Connect SATA Disc
6. (Optional with TEBF0818) Connect Display Port Monitor (List of usable Monitors: https://www.xilinx.com/support/answers/68671.html)
7. (Optional with TEBF0818) Connect Network Cable
8. Power On PCB
   boot process

   1. ZynqMP Boot ROM loads FSBL from SD/QSPI into OCM,

   2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from SD/QSPI into DDR,

   3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   - Speed: 115200
   - select COM Port

     Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:

```
# password default disabled with 2021.2 petalinux release
petalinux login: root
```

14 https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr

```
Password: root
```

> Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
i2cdetect -y -r 0   (check I2C 0 Bus, replace 0 with other bus number is
also possible)
dmesg | grep rtc    (RTC check)
udhcpc              (ETH0 check)
lsusb               (USB check)
lspci               (PCIe check)
```

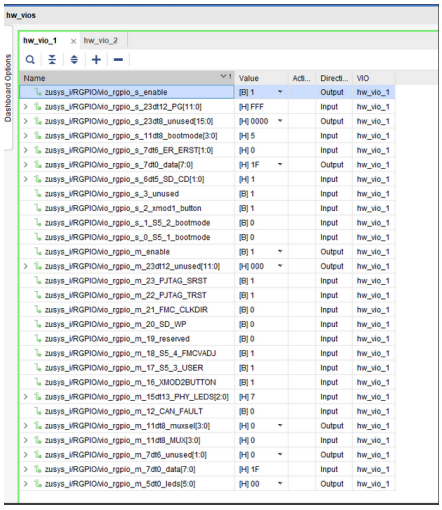
4. Option Features
   - Webserver to get access to ZynqMP
     - insert IP on web browser to start web interface
   - init.sh scripts
     - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

6.2.2 Vivado HW Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

- RGPIO Interface (**Important**: CPLD Firmware REV07 or newer is needed) for Control and Monitoring:
  - Set Enable to send Write date over RGPIO interface.
    - **CPLD** Description: TEBF0818 CPLD[15]
      - Buttons, LEDs, Status...

- Control:
  - LEDs: XMOD 2 (without green dot) and HD LED are accessible.
  - CAN_S



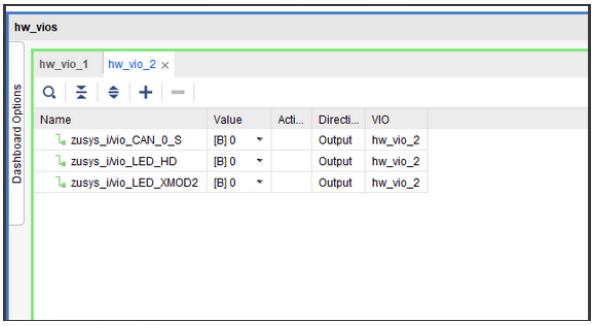


Table 10: Vivado Hardware Manager

15 https://wiki.trenz-electronic.de/display/PD/TEBF0818+CPLD

7 System Design - Vivado

7.1 Block Design

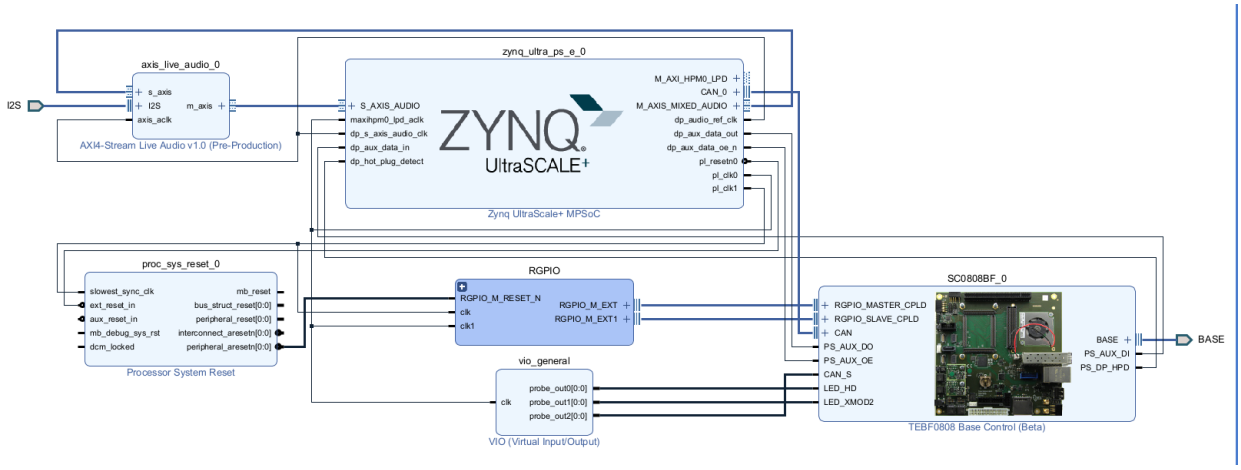


Figure 1: Block Design

7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
CAN0	EMIO
I2C0	MIO
PJTAG0	MIO
UART0	MIO
GPIO0	MIO

Type	Note
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO/GTP
PCIe	MIO/GTP
SATA	GTP
Display Port	EMIO/GTP

Table 11: PS Interfaces

7.2 Constraints

7.2.1 Basic module constraints

_i_bitgen.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

7.2.2 Design specific constraints

_i_io.xdc

```
#System Controller IP
#HDIO_SC0  J3:C13  LED_HD
#HDIO_SC1  J3:C14
#HDIO_SC2  J3:D14
#HDIO_SC3  J3:D15
#HDIO_SC4  J3:D18
#HDIO_SC5  J3:D19
#HDIO_SC6  J3:C17
#HDIO_SC7  J3:C18
#HDIO_SC10  J3:A13
#HDIO_SC11  J3:A14
```

```
#HDIO_SC12  J3:B14
#HDIO_SC13  J3:B15
#HDIO_SC14  J3:A17
#HDIO_SC15  J3:A18
#HDIO_SC16  J3:B18  CAN S
#HDIO_SC17  J3:B19  LED_XMOD
#HDIO_SC18  J3:B22  CAN TX
#HDIO_SC19  J3:B23  CAN RX


set_property PACKAGE_PIN A13 [get_ports BASE_sc0]
set_property PACKAGE_PIN D14 [get_ports BASE_sc5]
set_property PACKAGE_PIN B14 [get_ports BASE_sc6]
set_property PACKAGE_PIN C14 [get_ports BASE_sc7]

set_property PACKAGE_PIN K11 [get_ports BASE_sc10_io]
set_property PACKAGE_PIN K12 [get_ports BASE_sc11]
set_property PACKAGE_PIN G14 [get_ports BASE_sc12]
set_property PACKAGE_PIN H14 [get_ports BASE_sc13]
set_property PACKAGE_PIN E12 [get_ports BASE_sc14]
set_property PACKAGE_PIN F12 [get_ports BASE_sc15]
set_property PACKAGE_PIN H12 [get_ports BASE_sc16]
set_property PACKAGE_PIN H13 [get_ports BASE_sc17]
set_property PACKAGE_PIN J12 [get_ports BASE_sc18]
set_property PACKAGE_PIN K13 [get_ports BASE_sc19]

set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc0]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc16]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc17]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc18]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc19]

# PLL
#J4:A28 B64_L14_P
#set_property PACKAGE_PIN AF17 [get_ports {si570_clk_p[0]}]
#set_property IOSTANDARD LVDS [get_ports {si570_clk_p[0]}]
#set_property IOSTANDARD LVDS [get_ports {si570_clk_n[0]}]



# Audio Codec
#LRCLK      J3:D22 B47_L9_N
#BCLK       J3:D23 B47_L9_P
#DAC_SDATA  J3:C21 B47_L7_N
#ADC_SDATA  J3:C22 B47_L7_P

set_property PACKAGE_PIN C12 [get_ports I2S_lrclk ]
```

```
set_property PACKAGE_PIN D12 [get_ports I2S_bclk ]
set_property PACKAGE_PIN E13 [get_ports I2S_sdin ]
set_property PACKAGE_PIN E14 [get_ports I2S_sdout ]

set_property IOSTANDARD LVCMOS18 [get_ports I2S_lrclk ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_bclk ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdin ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdout ]
```

8 Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis[16]

8.1 Application

Template location: "<project folder>\sw_lib\sw_apps\"

8.1.1 zynqmp_fsbl

TE modified 2021.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)
- General Changes:
    - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
    - Si5345 Configuration
    - OTG+PCIe Reset over MIO
    - I2C MUX for EEPROM MAC

8.1.2 zynqmp_fsbl_flash

TE modified 2021.2 FSBL

General:

- Modified Files: xfsbl_initialisation.c, xfsbl_hw.h, xfsbl_handoff.c, xfsbl_main.c
- General Changes:
    - Display FSBL Banner
    - Set Boot Mode to JTAG

8.1.3 zynqmp_pmufw

Xilinx default PMU firmware.

8.1.4 hello_te0817

Hello TE0817 is a Xilinx Hello World example as endless loop instead of one console output.

16 https://wiki.trenz-electronic.de/display/PD/Vitis

8.1.5 u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart[17]

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- select SD default instead of eMMC:
  - CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- generate u-boot.dtb:
  - CONFIG_SUBSYSTEM_UBOOT_EXT_DTB=y
- add new flash partition for bootscr and sizing
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART0_SIZE=0xA00000
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART2_SIZE=0x2000000
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_NAME="bootscr"
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_SIZE=0x80000

9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- MAC from eeprom together with uboot and device tree settings:
  - CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET=0xFA
  - CONFIG_ENV_OVERWRITE=y
  - CONFIG_SYS_I2C_EEPROM_ADDR=0x50
  - CONFIG_SYS_I2C_EEPROM_BUS=7
- Boot Modes:
  - CONFIG_QSPI_BOOT=y
  - CONFIG_SD_BOOT=y
  - # CONFIG_ENV_IS_IN_NAND is not set
  - CONFIG_BOOT_SCRIPT_OFFSET=0x2A40000

Change platform-top.h:

```
#include <configs/xilinx_zynqmp.h>
#no changes
```

17 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart

9.3 Device Tree

project-spec\meta-user\recipes-bsp\device-tree\files\system-user.dtsi

```
/include/ "system-conf.dtsi"


/*------------------ gtr --------------------*/

//https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18841716/
Zynq+Ultrascale+MPSOC+Linux+SIOU+driver

/ {
  refclk3:psgtr_dp_clock {
          compatible = "fixed-clock";
          #clock-cells = <0x00>;
          clock-frequency = <27000000>;
  };

   refclk2:psgtr_pcie_usb_clock {
           compatible = "fixed-clock";
           #clock-cells = <0x00>;
           clock-frequency = <100000000>;
   };

  refclk1:psgtr_sata_clock {
          compatible = "fixed-clock";
          #clock-cells = <0x00>;
          clock-frequency = <150000000>;
  };

  //refclk0:psgtr_unused_clock {
  //        compatible = "fixed-clock";
  //        #clock-cells = <0x00>;
  //        clock-frequency = <100000000>;
  //};
};

&psgtr {
  clocks = <&refclk1 &refclk2 &refclk3>;
  /* ref clk instances used per lane */
  clock-names = "ref1\0ref2\0ref3";
};



/*------------------ SD --------------------*/
&sdhci0 {
    // disable-wp;
    no-1-8-v;

};
```

```
&sdhci1 {
    // disable-wp;
    no-1-8-v;

};


/*------------------ USB --------------------*/
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    snps,usb3_lpm_capable;
    snps,dis_u3_susphy_quirk;
    snps,dis_u2_susphy_quirk;
    phy-names = "usb2-phy","usb3-phy";
    maximum-speed = "super-speed";
};


/*------------------ ETH PHY --------------------*/
&gem3 {
    phy-handle = <&phy0>;

    nvmem-cells = <&eth0_addr>;
    nvmem-cell-names = "mac-address";

    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};


/*------------------ QSPI --------------------*/
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};


/*------------------ I2C --------------------*/
&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;
        i2c@0 { // MCLK TEBF0808 SI5338A, 570FBB000290DG_unassembled
            reg = <0>;
```

```
        };
        i2c@1 { // SFP TEBF0808 PCF8574DWR
            reg = <1>;
        };
        i2c@2 { // PCIe
            reg = <2>;
        };
        i2c@3 { // SFP1 TEBF0808
            reg = <3>;
        };
        i2c@4 {// SFP2 TEBF0808
            reg = <4>;
        };
        i2c@5 { // TEBF0808 EEPROM
            reg = <5>;
            eeprom: eeprom@50 {
                compatible = "microchip,24aa025", "atmel,24c02";
                reg = <0x50>;

                #address-cells = <1>;
                #size-cells = <1>;
                eth0_addr: eth-mac-addr@FA {
                  reg = <0xFA 0x06>;
                };
           };
        };
        i2c@6 { // TEBF0808 FMC
            reg = <6>;
        };
        i2c@7 { // TEBF0808 USB HUB
            reg = <7>;
        };
    };
    i2cswitch@77 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x77>;
        i2c-mux-idle-disconnect;
        i2c@0 { // TEBF0808 PMOD P1
            reg = <0>;
        };
        i2c@1 { // i2c Audio Codec
            reg = <1>;
            /*
            adau1761: adau1761@38 {
                compatible = "adi,adau1761";
                reg = <0x38>;
            };
            */
        };
        i2c@2 { // TEBF0808 Firefly A
            reg = <2>;
        };
        i2c@3 { // TEBF0808 Firefly B
            reg = <3>;
        };
```

```
        i2c@4 { //Module PLL Si5338 or SI5345
            reg = <4>;
        };
        i2c@5 { //TEBF0808 CPLD
            reg = <5>;
        };
        i2c@6 { //TEBF0808 Firefly PCF8574DWR
            reg = <6>;
        };
        i2c@7 { // TEBF0808 PMOD P3
            reg = <7>;
        };
    };
};
```

project-spec\meta-user\recipes-bsp\uboot-device-tree\files\system-user.dtsi

```
/include/ "system-conf.dtsi"


/*------------------ gtr --------------------*/

//https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18841716/
Zynq+Ultrascale+MPSOC+Linux+SIOU+driver

/ {
  refclk3:psgtr_dp_clock {
          compatible = "fixed-clock";
          #clock-cells = <0x00>;
          clock-frequency = <27000000>;
  };

   refclk2:psgtr_pcie_usb_clock {
           compatible = "fixed-clock";
           #clock-cells = <0x00>;
           clock-frequency = <100000000>;
   };

  refclk1:psgtr_sata_clock {
          compatible = "fixed-clock";
          #clock-cells = <0x00>;
          clock-frequency = <150000000>;
  };

  //refclk0:psgtr_unused_clock {
  //        compatible = "fixed-clock";
  //        #clock-cells = <0x00>;
  //        clock-frequency = <100000000>;
  //};
};

&psgtr {
  clocks = <&refclk1 &refclk2 &refclk3>;
  /* ref clk instances used per lane */
```

```
  clock-names = "ref1\0ref2\0ref3";
};



/*------------------ SD --------------------*/
&sdhci0 {
    // disable-wp;
    no-1-8-v;

};

&sdhci1 {
    // disable-wp;
    no-1-8-v;

};


/*------------------ USB --------------------*/
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    snps,usb3_lpm_capable;
    snps,dis_u3_susphy_quirk;
    snps,dis_u2_susphy_quirk;
    phy-names = "usb2-phy","usb3-phy";
    maximum-speed = "super-speed";
};


/*------------------ ETH PHY --------------------*/
&gem3 {
    phy-handle = <&phy0>;

    nvmem-cells = <&eth0_addr>;
    nvmem-cell-names = "mac-address";

    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};


/*------------------ QSPI --------------------*/
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};
```

```
/*------------------ I2C --------------------*/
&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;
        i2c@0 { // MCLK TEBF0808 SI5338A, 570FBB000290DG_unassembled
            reg = <0>;
        };
        i2c@1 { // SFP TEBF0808 PCF8574DWR
            reg = <1>;
        };
        i2c@2 { // PCIe
            reg = <2>;
        };
        i2c@3 { // SFP1 TEBF0808
            reg = <3>;
        };
        i2c@4 {// SFP2 TEBF0808
            reg = <4>;
        };
        i2c@5 { // TEBF0808 EEPROM
            reg = <5>;
            eeprom: eeprom@50 {
                compatible = "microchip,24aa025", "atmel,24c02";
                reg = <0x50>;

                #address-cells = <1>;
                #size-cells = <1>;
                eth0_addr: eth-mac-addr@FA {
                  reg = <0xFA 0x06>;
                };
           };
        };
        i2c@6 { // TEBF0808 FMC
            reg = <6>;
        };
        i2c@7 { // TEBF0808 USB HUB
            reg = <7>;
        };
    };
    i2cswitch@77 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x77>;
        i2c-mux-idle-disconnect;
        i2c@0 { // TEBF0808 PMOD P1
            reg = <0>;
        };
        i2c@1 { // i2c Audio Codec
            reg = <1>;
            /*
```

```
            adau1761: adau1761@38 {
                compatible = "adi,adau1761";
                reg = <0x38>;
            };
            */
        };
        i2c@2 { // TEBF0808 Firefly A
            reg = <2>;
        };
        i2c@3 { // TEBF0808 Firefly B
            reg = <3>;
        };
        i2c@4 { //Module PLL Si5338 or SI5345
            reg = <4>;
        };
        i2c@5 { //TEBF0808 CPLD
            reg = <5>;
        };
        i2c@6 { //TEBF0808 Firefly PCF8574DWR
            reg = <6>;
        };
        i2c@7 { // TEBF0808 PMOD P3
            reg = <7>;
        };
    };
};
```

9.4 FSBL patch

currently not included

9.5 Kernel

Start with **petalinux-config -c kernel**

Changes:

- Only needed to fix JTAG Debug issue:
  - # CONFIG_CPU_IDLE is not set
  - # CONFIG_CPU_FREQ is not set
  - CONFIG_EDAC_CORTEX_ARM64=y
- Support PCIe memory card
  - CONFIG_NVME_CORE=y
  - CONFIG_BLK_DEV_NVME=y
  - # CONFIG_NVME_MULTIPATH is not set
  - # CONFIG_NVME_HWMON is not set
  - # CONFIG_NVME_TCP is not set
  - CONFIG_NVME_TARGET=y
  - # CONFIG_NVME_TARGET_PASSTHRU is not set
  - # CONFIG_NVME_TARGET_LOOP is not set
  - # CONFIG_NVME_TARGET_FC is not set
  - # CONFIG_NVME_TARGET_TCP is not set
  - CONFIG_SATA_AHCI=y
  - CONFIG_SATA_MOBILE_LPM_POLICY=0

- CONFIG_NVM=y
- CONFIG_NVM_PBLK=y
- CONFIG_NVM_PBLK_DEBUG=y

9.6 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- For web server app:
  - CONFIG_busybox-httpd=y
- For additional test tools only:
  - CONFIG_i2c-tools=y
  - CONFIG_packagegroup-petalinux-utils=y (util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)

9.7 Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

9.7.1 startup

Script App to load init.sh from SD Card if available.

9.7.2 webfwu

Webserver application suitable for ZynqMP access. Need busybox-httpd

10 Additional Software

10.1 SI5345

File location "<project folder>\misc\PLL\Si5345_D\Si5345-*.slabtimeproj"

General documentation how you work with this project will be available on Si5345[18]

18 https://wiki.trenz-electronic.de/display/PD/Si5345

11 App. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2022-09-12	v.5(see page 6)	Manuela Strücker[19]	• update board part file compatible to Vivado 2021.2.1
2022-09-06	v.4	Manuela Strücker	• initial release
--	all	Manuela Strücker[20]	--

Table 12: Document change history.

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities.

21 http://guidance.echa.europa.eu/
22 https://echa.europa.eu/candidate-list-table
23 http://www.echa.europa.eu/

Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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