



TE0726 Test Board

Revision v.17

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Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0726+Test+Board>

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4 Overview

Zynq PS Design with Linux Example.

Refer to <http://trenz.org/te0726-info> for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2019.2
- PetaLinux
- SD
- ETH
- USB
- I2C
- Special FSBL for QSPI programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-04-08	2019.2	TE0726-test_board_noprebuilt-vivado_2019.2-build_10_20200408185842.zip TE0726-test_board-vivado_2019.2-build_10_20200408185804.zip	Mohsen Chamanbaz/ John Hartfiel	<ul style="list-style-type: none"> • changes FSBL flash
2020-03-25	2019.2	TE0726-test_board_noprebuilt-vivado_2019.2-build_8_20200325080535.zip TE0726-test_board-vivado_2019.2-build_8_20200325080528.zip	Mohsen Chamanbaz/ John Hartfiel	<ul style="list-style-type: none"> • script update
2020-02-14	2019.2	TE0726-test_board_noprebuilt-vivado_2019.2-build_5_20200214091531.zip TE0726-test_board-vivado_2019.2-build_5_20200214091442.zip	Mohsen Chamanbaz	<ul style="list-style-type: none"> • Update to 19.2 • Vitis support • prebuilt binary export on selection guide
2019-12-12	2018.3	te0726-test_board_noprebuilt-vivado_2018.3-build_10_20191211160322.zip te0726-test_board-vivado_2018.3-build_10_20191211160314.zip	Mohsen Chamanbaz	<ul style="list-style-type: none"> • FSBL update to 18.3 • additional linux apps

Date	Vivado	Project Built	Authors	Description
2018-07-13	2018.2	te0726-test_board_noprebuilt-vivado_2018.2-build_02_20180713155548.zip te0726-test_board-vivado_2018.2-build_02_20180713155535.zip	John Hartfiel	<ul style="list-style-type: none"> Changed SDK Notes on FSBL template for Flash programming
2018-07-11	2018.2	te0726-test_board_noprebuilt-vivado_2018.2-build_02_20180711113737.zip te0726-test_board-vivado_2018.2-build_02_20180711113722.zip	John Hartfiel	<ul style="list-style-type: none"> change note for REV01 no design changes
2018-02-17	2017.4	te0726-test_board-vivado_2017.4-build_08_20180517084735.zip te0726-test_board_noprebuilt-vivado_2017.4-build_08_20180517084604.zip	John Hartfiel	<ul style="list-style-type: none"> correction netboot offset for 128MB variant
2018-02-16	2017.4	te0726-test_board-vivado_2017.4-build_06_20180216205357.zip te0726-test_board_noprebuilt-vivado_2017.4-build_06_20180216205410.zip	John Hartfiel	<ul style="list-style-type: none"> correction PS REFCLK for 01 variant
2018-01-31	2017.4	te0726-test_board-vivado_2017.4-build_05_20180131115412.zip te0726-test_board_noprebuilt-vivado_2017.4-build_05_20180131115451.zip	John Hartfiel	<ul style="list-style-type: none"> initial release 2017.4

Table 1: Design Revision History

4.3 Release Notes and Known Issues

Issues	Description	Workaround	To be fixed version
Flash Programming failed with 19.2	Depending on Flash content Flash programming failed with provided fsbl_flash (Xilinx AR# 70548 ¹) 2019.2 version	<ul style="list-style-type: none"> Option1: <ul style="list-style-type: none"> In case Flash is empty, use fsbl_flash on programming GUI In case Flash is programmed use normal fsbl on programming GUI Option2: use in both case fsbl_flash on programming GUI and Vivado LabTools 2018.3 	---

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation
PetaLinux	2019.2	needed

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).²

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMM C	Others	Notes
te0726-01	01	REV01	64MB	16MB	NA	NA	

¹ <https://www.xilinx.com/support/answers/70548.html>

² <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMM C	Others	Notes
te0726-03r	r	REV03,REV02	128 MB	16MB	NA	NA	
te0726-03m	m	REV03,REV02	512 MB	16MB	NA	NA	
te0726-03-07s-1c	7s	REV03,REV02	512 MB	16MB	NA	NA	

Table 4: Hardware Modules

Design supports following carriers:

Carrier Model	Notes

Table 5: Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable	Connect to USB2 or better USB3 Hub for proper power over USB

Table 6: Additional Hardware

4.5 Content

For general structure and of the reference design, see [Project Delivery - Xilinx devices](#)³

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

³ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

Type	Location	Notes
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
init.sh	<design name>/misc/sd/	Additional Initialization Script for Linux

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebuilt content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0726 "Test Board" Reference Design⁴

⁴ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/special/TE0726/Reference_Design/2019.2/test_board

5 Design Flow

⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [Xilinx Development Tools⁵](#)
- [Vivado Projects - TE Reference Design⁶](#)
- [Project Delivery.⁷](#)

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery](#) [Currently limitations of functionality⁸](#)

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

```

C:\WINDOWS\system32\cmd.exe
B:\Design\cores\xilinx\2018.3\design\TE0723\test_board>setlocal
-- Set design paths --
-- Run Design with: _create_win_setup
-- Use Design Path: B:\Design\cores\xilinx\2018.3\design\TE0723\test_board\
----- TE Reference Design -----
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (x) Exit Batch (nothing is done)
-- (0) Module selection guide, project creation...
-- (1) Create minimum setup of CMD-Files and exit Batch
-- (2) Create maximum setup of CMD-Files and exit Batch
-----
Select (ex.: '0' for module selection guide):

```

2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
 - a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" Note: Select correct one, see [TE Board Part Files⁹](#)
5. Create HDF and export to prebuilt folder
 - a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
 Note: Script generate design and export files into '\prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (uboot.elf and image.ub) with exported XSA

⁵ <https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides>

⁶ <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

⁷ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

⁸ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality>

⁹ <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

- a. XSA is exported to "prebuilt\hardware\<short name>"
Note: HW Export from Vivado GUI create another path as default workspace.
Create Linux images on VM, see [PetaLinux KICKstart](#)¹⁰
 - i. Use TE Template from /os/petalinux
7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
 - a. "prebuilt\os\petalinux\<ddr size>" or "prebuilt\os\petalinux\<short name>"
8. Generate Programming Files with Vitis
 - a. Run on Vivado TCL: TE::sw_run_vitis -all
Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
 - b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
Note: TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)¹¹

¹⁰ <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

¹¹ <https://wiki.trenz-electronic.de/display/PD/Vitis>

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging¹²](#)

6.1.1 Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
 - a. Select assembly version
 - b. Validate selection
 - c. Select Create and open delivery binary folder

Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

6.1.2 QSPI

1. Connect JTAG and power module (TE0726 can be powered via JTAG USB or external)
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash -swapp u-boot
Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
optional "TE::pr_program_flash -swapp hello_te0726" possible
4. Copy image.ub on SD-Card
 - use files from (<project foler>/_binaries_<Articel Name>)/boot_linux from generated binary folder, see: [Get prebuilt boot binaries\(see page 14\)](#)
 - or use prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
 - Important: Do not copy Boot.bin on SD(is not used see SD note), only other files.
5. Insert SD-Card

6.1.3 SD

Xilinx Zynq devices in CLG225 package do not support SD Card boot directly from ROM bootloader. Use QSPI for primary boot and SD for secondary boot (uboot)

6.1.4 JTAG

Not used on this Example.

¹² <https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging>

6.2 Usage

1. Prepare HW like described on section [Programming](#)(see page 14)
2. Connect UART USB (most cases same as JTAG)
3. Insert SD Card with image.ub
4. Power On PCB
Note: 1. Zynq Boot ROM loads FSBL from QSPI into OCM, 2. FSBL loads U-boot from QSPI into DDR, 3. U-boot load Linux from SD into DDR

6.2.1 Linux

1. Open Serial Console (e.g. putty)
 - a. Speed: 115200
 - b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
Note: Wait until Linux boot finished For Linux Login use:
 - a. User Name: root
 - b. Password: root
3. You can use Linux shell now.
 - a. I2C 1 Bus type: i2cdetect -y -r 1
 - b. ETH0 works with udhcpc
 - c. USB: insert USB device
4. Option Features
 - a. Webserver to get access to Zynq
 - i. insert IP on web browser to start web interface
 - b. init.sh scripts
 - i. add init.sh script on SD, content will be load automatically on startup (template included in ./misc/SD)

7 System Design - Vivado

7.1 Block Design

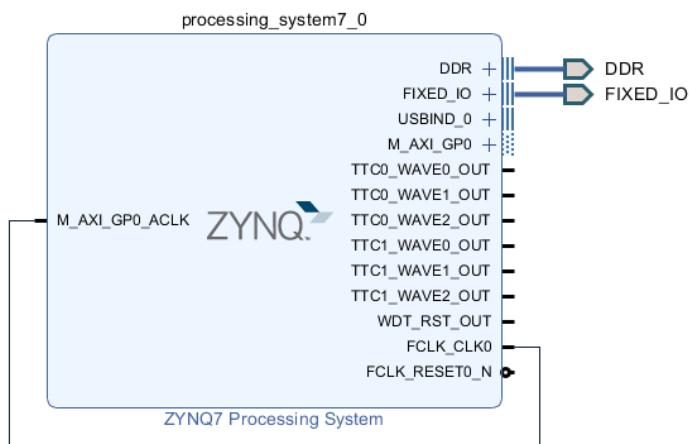


Figure 1: Block Design

7.1.1 PS Interfaces

Type	Note
DDR	---
QSPI	MIO
SD1	MIO
I2C1	MIO
UART1	MIO
GPIO	MIO
TTC0..1	EMIO
WDT	EMIO

Type	Note
USB0	MIO, ETH over USB
USB RST	MIO

Table 10: PS Interfaces

7.2 Constraints

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
#  
# Common BITGEN related settings for TE0726  
#  
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]  
set_property CONFIG_VOLTAGE 3.3 [current_design]  
set_property CFGBVS VCCO [current_design]  
  
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]
```

7.2.2 Design specific constrain

8 Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis¹³

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 zynq_fsbl

TE modified 2019.2 FSBL

General:

- Modified Files: main.c, fsbl_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te_fsbl_hooks.h/.c(for hooks and board)\n\
- General Changes:
 - Display FSBL Banner and Device ID

Module Specific:

- ---

8.1.2 zynq_fsbl_flash

TE modified 2019.2 FSBL

General:

- Modified Files: main.c
- General Changes:
 - Display FSBL Banner
 - Set FSBL Boot Mode to JTAG
 - Disable Memory initialisation

8.1.3 hello_te0726

Hello TE0726 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.4 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

¹³ <https://wiki.trenz-electronic.de/display/PD/Vitis>

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart¹⁴](#)

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

For 64MB variant only:

- CONFIG_SUBSYSTEM_NETBOOT_OFFSET = 0x2000000

For 128MB variant only:

- CONFIG_SUBSYSTEM_NETBOOT_OFFSET = 0x4000000

9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG_ENV_IS_NOWHERE=y
CONFIG_ENV_IS_IN_SPI_FLASH is not set

Change platform-top.h:

¹⁴ <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

9.3 Device Tree

```
/include/ "system-conf.dtsi"
{
};

/* USB PHY */
{
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    };
};

&usb0 {
    dr_mode = "host";
    //dr_mode = "peripheral";
    usb-phy = <&usb_phy0>;
};

/* I2C1 */

&i2c1 {
    #address-cells = <1>;
    #size-cells = <0>;

    i2cmux0: i2cmux@70 {
        compatible = "nxp,pca9544";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x70>;

        i2c1@0 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0>;

            id_eeprom@50 {
                compatible = "atmel,24c32";
                reg = <0x50>;
            };
        };
    i2c1@1 {    // Display Interface Connector
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <1>;
    };
};
```

```
};

i2c1@2 {      // HDMI Interface Connector
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <2>;
};

i2c1@3 {      // Camera Interface Connector
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <3>;
};

};

};
```

9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_XILINX_GMII2RGMII
- CONFIG_USB_USBNET
- CONFIG_USB_NET_SMSC95XX
- CONFIG_USBIP_CORE

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- CONFIG_i2c-tools=y
- CONFIG_busybox-httpd=y (for web server app)
- CONFIG_packagegroup-petalinux-utils

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

9.6.2 webfwu

Webserver application assemble for Zynq access. Need busybox-httpd

10 Additional Software

No additional software is needed

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2020-06-23	v.17 (see page 6)	John Hartfiel ¹⁵	<ul style="list-style-type: none"> • typo
2020-04-08	v.16	John Hartfiel	<ul style="list-style-type: none"> • Design update • Programming issue note
2020-03-25	v.14	John Hartfiel	<ul style="list-style-type: none"> • script update
2020-02-19	v.13	Mohsen Chamanbaz	<ul style="list-style-type: none"> • 2019.2 release • docu update
2019-12-13	v.12	John Hartfiel	<ul style="list-style-type: none"> • 2018.3 release
2018-07-13	v.11	John Hartfiel	<ul style="list-style-type: none"> • 2018.2 release
2018-05-17	v.9	John Hartfiel	<ul style="list-style-type: none"> • bugfix design for 128MB variant
2018-03-20	v.8	John Hartfiel	<ul style="list-style-type: none"> • Link update • remove typo
2018-02-16	v.6	John Hartfiel	<ul style="list-style-type: none"> • Design update
2018-02-09	v.5	John Hartfiel	<ul style="list-style-type: none"> • 2017.4 release

¹⁵ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

Date	Document Revision	Authors	Description
--	all	Mohsen Chamanbaz ¹⁶ , John Hartfiel ¹⁷	--

Table 11: Document change history.

11.2 Legal Notices

11.3 Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

11.4 Document Warranty

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¹⁶ <https://wiki.trenz-electronic.de/display/~M.Chamanbaz>

¹⁷ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

11.7 Technology Licenses

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To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

11.9 REACH, RoHS and WEEE

REACH

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RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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¹⁸ <http://guidance.echa.europa.eu/>

¹⁹ <https://echa.europa.eu/candidate-list-table>

²⁰ <http://www.echa.europa.eu/>