GOP_XC3S200
USER'S MANUAL
V 0.9

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2. Introduction

The GOP_XC3S200 is a mini module composed of an FPGA device and a configuration memory with a PAL / GAL compatible 24 pin DIL footprint. Many additional features makes it useful and flexible:

2.1. GOP_XC3S200 Features:

- XC3S200-4VQ100C FPGA, a member of the XILINX Spartan-3 family, with a 24 or 20 pin PAL / GAL compatible DIL footprint
- Xilinx XCF01S Platform Flash configuration device
- Xilinx Parallel Cable IV or Platform USB compatible download connector 14pin / 2mm, an OHO-Elektronik low cost programmer is also availllable
- 4 Mbit SRAM 512k x 8, tAC = 55ns
- 8 Mbit user SPI FLASH
- Operating voltage from 3,5V to 5.5V, switching regulator for core voltage 1,2V
- Voltage translators for 5V I/O compatibility, selectable pullups to 5V
- Onboard Clock oscillator with 49.152 MHz for audio or RS232 applications
- 2 status leds, 8 low current user leds, 2 user tact switches, 7 configuration jumper
- A 9-pin test connector for probing internal signals, or interconnecting several GOP's
- Reverse plug in protection, solder jumpers for additional ground connections
- Easy to reuse
- Professional design, manufactured on a 6 layer PCB, Made in Germany

2.2. GOP_XC3S200 Applications:

- Upgrade from PAL / GAL devices, Redesigns
- Fast evaluation of Xilinx Spartan-3 FPGA's
- Hardware platform for VHDL / VERILOG / logic design courses
- Robotics
- High logic density applications at tight space constraints

2.3. Xilinx XC3S200 Features:

Document [1] lists lots of goodies, here are the best facts:

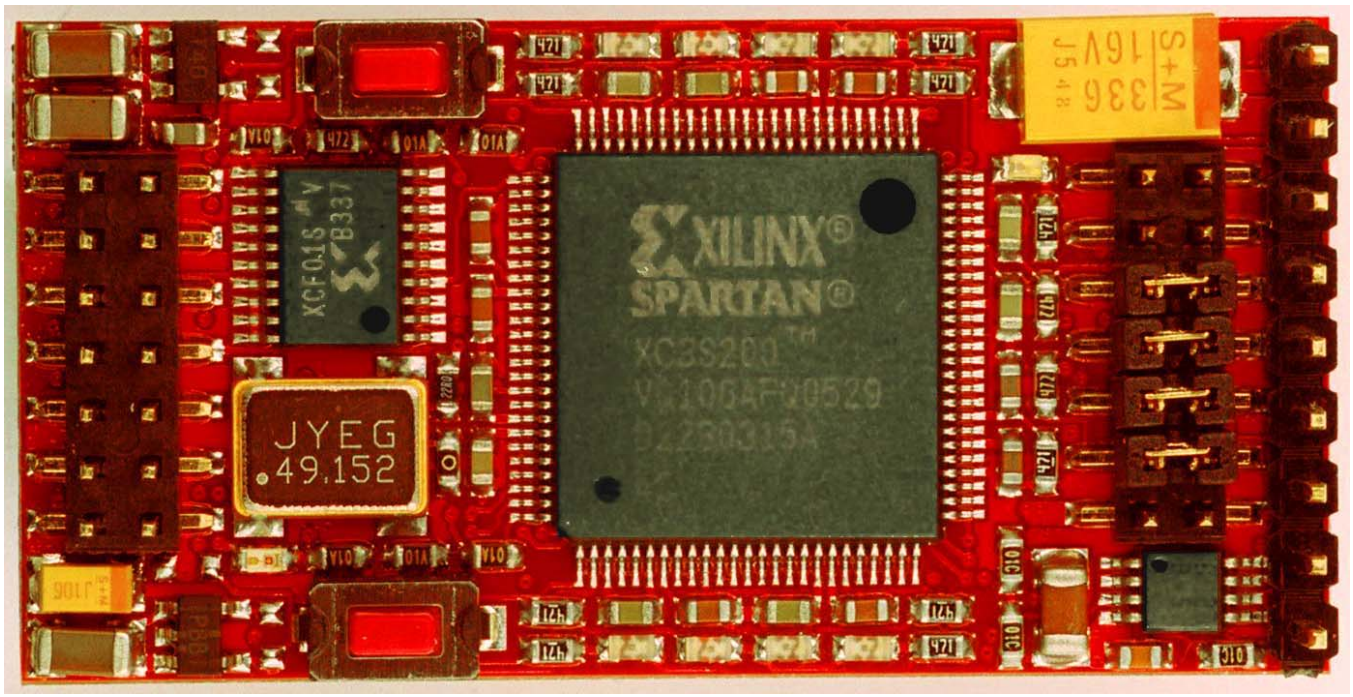
- Modern SRAM based 90nm 200000 Gate low cost FPGA
- 3840 4-input function generators, 1920 can be RAM or dual ported RAM, or shiftregisters
- SelectRAM hierarical memory, 12 x 18kbit Blockram, 30kbit distributed RAM
- 12 dedicated multipliers 18x18
- 4 Digital Clock Managers, DCM's
- Lots of I/O standards, GOP_XC3S200 supports LVCMOS33 only
- Wide multiplexers, Fast look-ahead carry logic, 8 global clock nets, JTAG interface with user access
- Free powerful VHDL / VERILOG / schematics / simulation design software availlable (Webpack)
- Unlimited reprogrammability

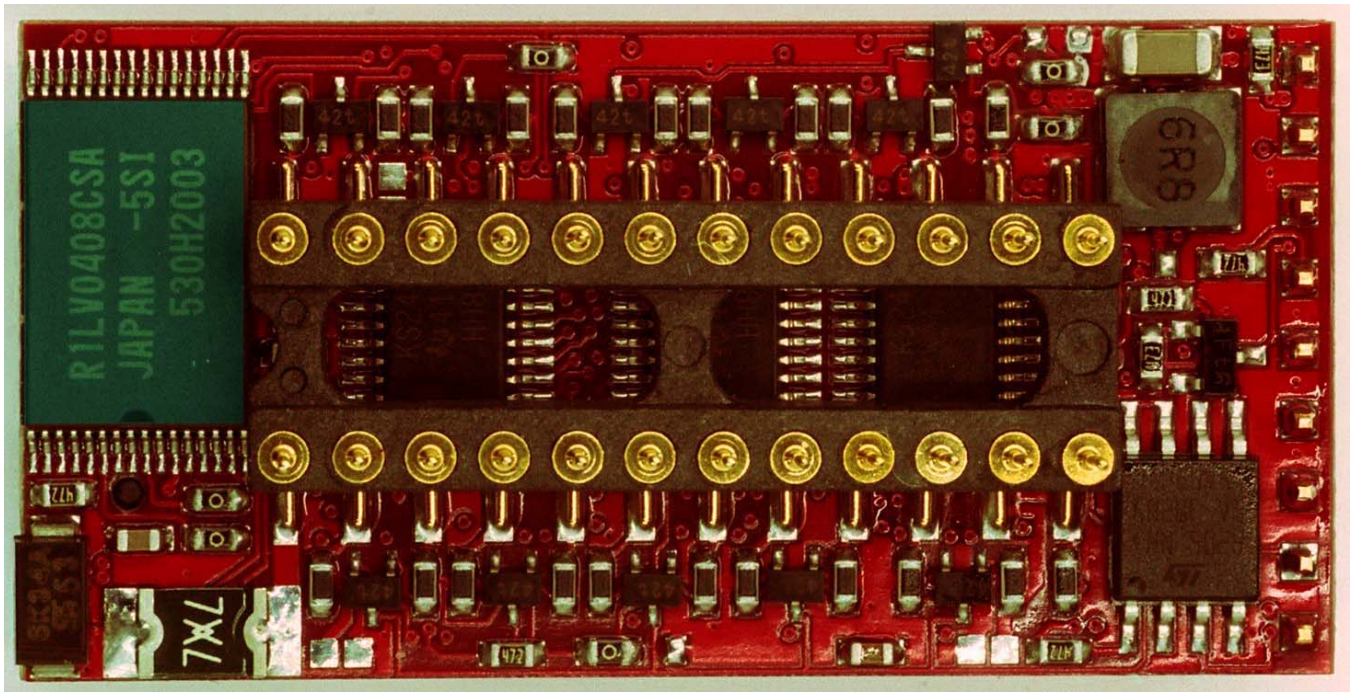
2.4. Xilinx XC3S200 Disadvantages:

The following items are not relevant in most cases.
However they should be used as a checklist, wheather an application is affected.

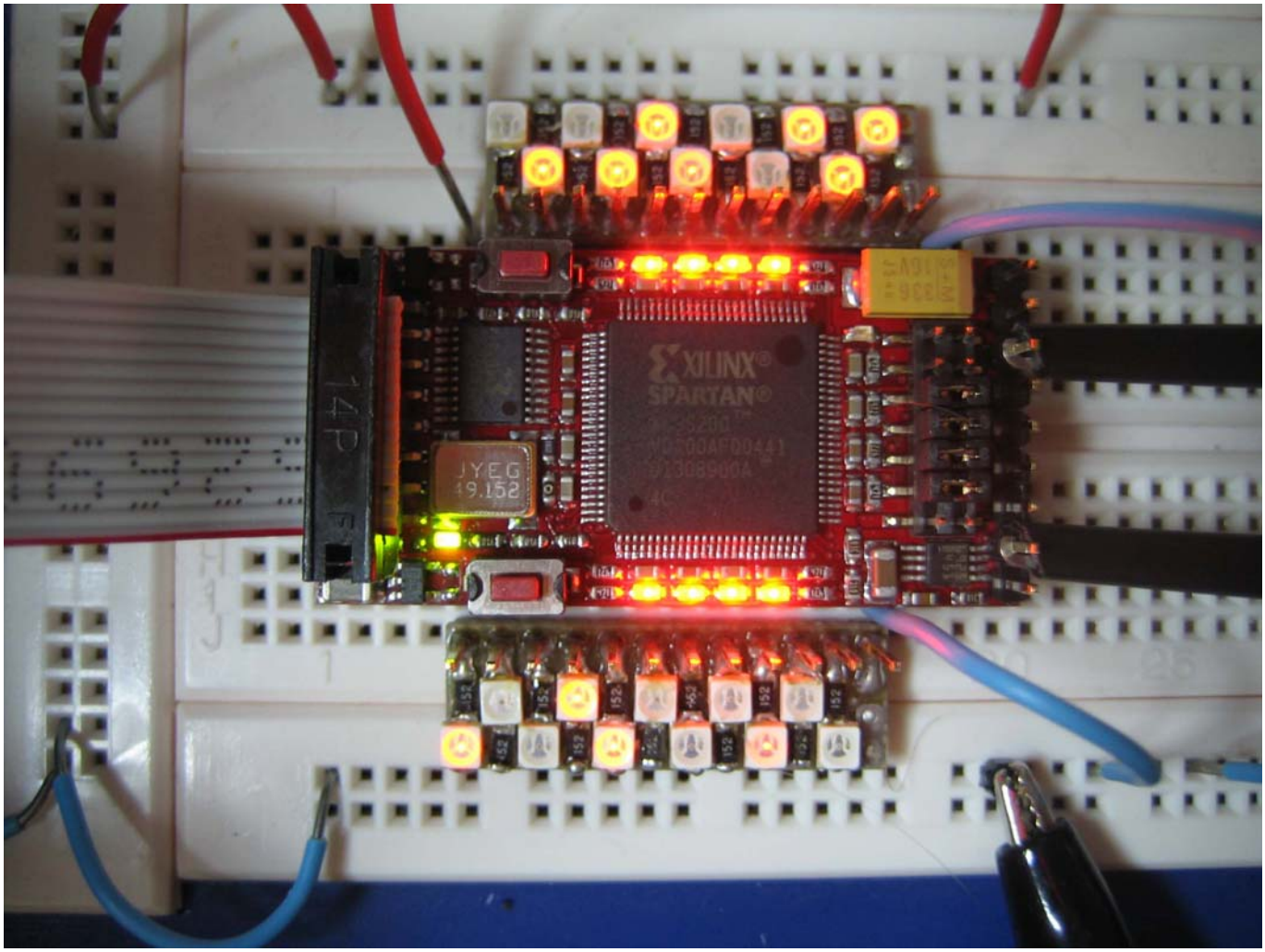
- No single chip solution, needs a configuration source like a configuration platform FLASH
- 3 different supply voltages required: core voltage 1,2V, VCCAUX 2,5V, I/O voltage
- I/O's are not 5V tolerant
- High quiescent current, in the range of tens of mAmps for each of the supply voltages for XC3S200
- Design is not protected against copyright theft, configuration bitstream can be recorded
- Lower performance FPGA compared to the luxury Virtex2 pro or Virtex4 FPGA's, especially not all luts have RAM / shiftregister capabilities
- DLL's in the DCM's have higher jitter than PLL's

2.5. GOP_XC3S200 Board Picures,Top And Bottom View.

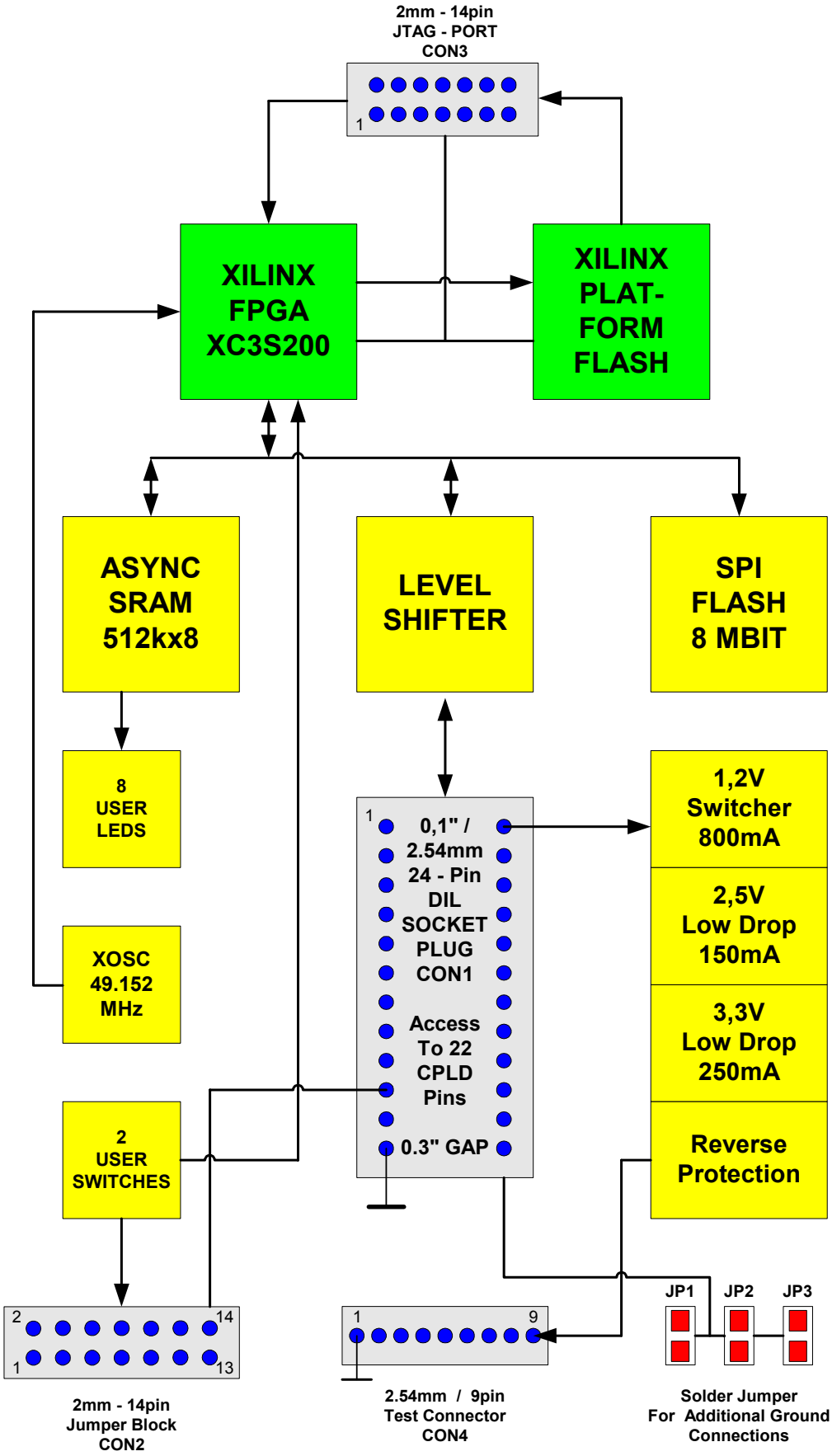




2.6. GOP_XC3S200 Board In A Lab Environment.



3. GOP_XC3S200 Board Overview



3.1. I/O Distribution

22 Xilinx XC3S200-4VQ100C FPGA I/O's are wired to a 24 pin DIL socket plug on the bottom of the module through level shifter devices 74CB3T3245, which makes the FPGA I/O's tolerant to input voltages up to 7V.
Pin 1, 2, 13, 21 and 23 of the DIL plug accesses global clock nets GCLK6, GCLK7, GCLK1, GCLK4, and GCLK5 inside the FPGA.
These clock nets can be also general purpose I/O's.

Please note, that the level shifter devices reduces the ability of the FPGA I/O's to source current, sinking current is not affected.
As an option, pullups to 5V can be enabled on pin 1 to pin 13, and pin 14 to pin 23 separately by setting jumpers on CON2 11-12 and 13-14 respectively.

Another notice is, that as long the FPGA is not configured, the DIL pins are disconnected from the FPGA, they are floating. This could be altered by RJ3.

7 I/O's are availlable to the front side test connector CON4, 2 I/O's via level shifters and 5 I/O's are directly connected to the FPGA.
Pin 6 of CON4, one of the not 5V tolerant contacts, accesses global clock net GCLK2.
Pin 7 of CON4, one of the 5V tolerant contacts, accesses global clock net GCLK3.

A crystal oscillator with an output frequency of 49,152MHz is connected to GCLK0 of the FPGA. This oscillator can be disabled completely through its power supply by removing a jumper at jumper block CON4 position 3-4.

2 I/O's are connected to user tactile switches SW1 and SW2.
SW2 can reprogram the FPGA if jumper CON2 7-8 is set. In this case reprogramming the FPGA is also possible by I/O28. Simple output a '0' on this pin, tristate otherwise.
Please do not output a '1' on this pin, because this drives a 3,3V level to the 2,5V supply by the I/O diode at signal PROG_B.

30 FPGA I/O's are connected to an asynchronious SRAM device, organized as 512kByte x 8, with an access time of 55ns.
Due to the limited amount of I/O's of an VQ100 package, some of the SRAM I/O's are shared with other resources of the GOP_XC3S200 module.

8 address lines of the SRAM are connected to 8 user leds. These leds can be enabled by jumper CON2 9-10.

3 address lines of the SRAM share the SPI FLASH signals SCK, SI, SO.

It is up to the FPGA user, to care about proper multiplexing and tristating of these signals, when all affected ressources are used.

3.2. JTAG Port

Configuration of the FPGA is done by the Platform FLASH device XCF01S if jumper CON2 5-6 is set.
Additionally, the FPGA can be programmed by the JTAG port.

The platform FLASH device can be also programmed by the JTAG interface.

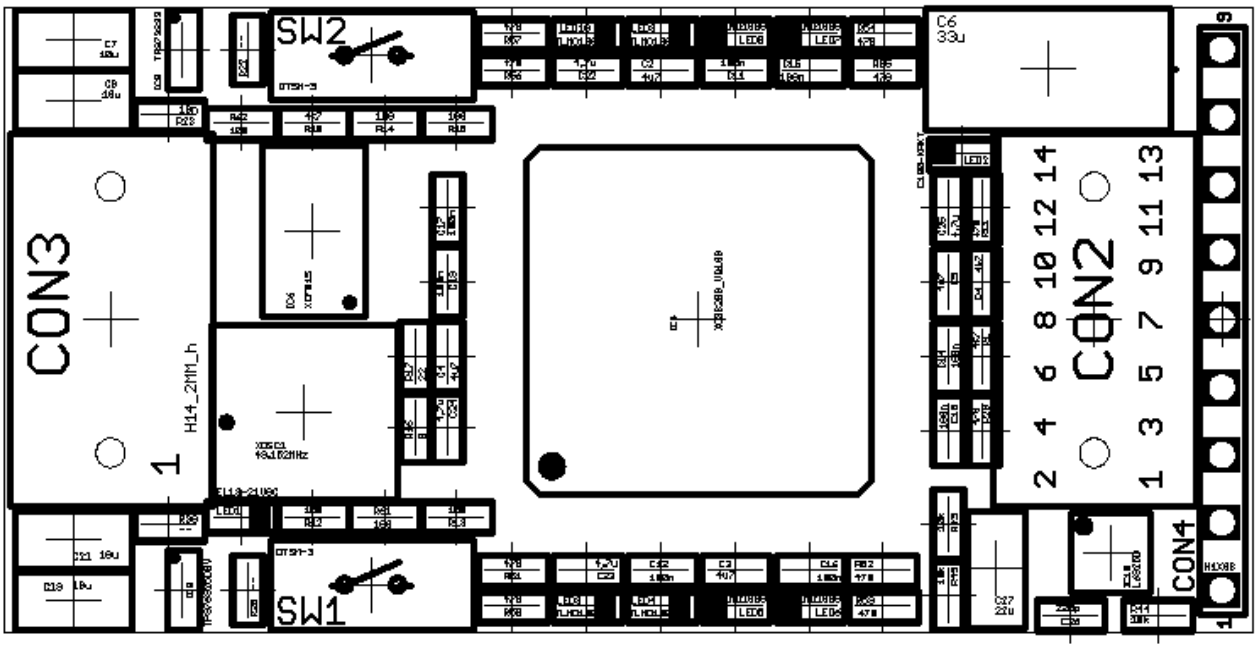
The 2 devices FPGA and Plattform FLASH are connected in a JTAG chain.
The FPGA is the first device in the chain, The Platform FLASH the second.

The configuration status of the FPGA is shown by the red status led2 and the green status led1.
If the FPGA is not configured, red led2 lights, and the green led1 is dark.
If the FPGA is configured, green led1 lights, and the red led2 is dark.

The FPGA JTAG chain is routed to the Xilinx standard 2mm 14pin JTAG port connector CON3 by serial resistors, enabling JTAG programming with 3,3V voltage levels.

The 2mm connector is also supported by the Parallel cable IV, and Platform USB cable, see [2] and [3].
Pin 1 of the port is connected to GND, which allows high speed programming with the above cables.
Pins 12, 13 and 14 of the JTAG port are not used on this module.

Please notice the pin orientation of JTAG port CON3:



3.3. Power Suppy

The module can be powered at DIL pin 24 from 3,5 to 5,5 Volts.
Module GND pin is pin 12 in 24 pin mode, and pin 10 in 20 pin mode.
An onboard switching voltage regulator produces the FPGA core voltage of 1,2V.
The regulator [4] can source up to 800mA.
Another low drop regulator generates the VCCAUX voltage of 2,5V, sourcing up to 150mA [5].
And finally a 250mA low drop regulator is responsible for the I/O voltage of 3,3V, [6].

The module has a protection against reverse insertion, or reverse power connection.
In that case, the protection shorts the power supply by a polyfuse device.
The polyfuse recovers after deactivation of the power supply.
Burn through cycles of the polyfuse are limited.
For more information, please consult the data sheet.

Even so care should be taken when plugging the module.
Consider that a short pulse of several amps can damage the environment in which the module is inserted.

ATTENTION !!!
Please note, that a voltage above 6V on the module pins 12 and 24 will destroy the voltage regulators on the module !!!
Especially the switching regulator is sensitive to overvoltage.
Therefore a maximum of 5,5V module supply voltage should be applied.

3.4. PAL / GAL Emulation Of 24 Pin And 20 Pin Devices

As a general hint, the DIL plug should be protected mechanically with the supplied DIL sockets as an adaptor.

In 24 pin mode of the module, a 24 pin socket should be used.

In 20 pin mode of the module, a 20 pin socket should be used.

Please insure, that pin 1 of the module is always pin 1 of a socket.

In the 20 pin mode, an additional GND connection must be done via a 2mm jumper on jumper block CON3 at position 1-2, see Layout Top View. This adds GND to pin 10.

In rare cases additional GND connections are desired.
Pins 3, 14 and 23 can be shorted to GND with solder jumpers JP1, JP3, JP2 respectively, on the bottom side of the module. These shorts should be soldered via a stereo microscope, to insure, that there are no other invalid connections.

4. FPGA Design Support

VHDL and UCF design templates for 20 and 24 pin configurations are availlable.

5. About GOP_XC3S200 I/O Voltage Levels

The Spartan3 FPGA series offer a broad variety of I/O voltage standards.
However on the GOP_XC3S200, only the LVCMOS33 standard is supported.
This standard is required for the level shifters [7] for conversion of 5V TTL levels as well as 5V CMOS levels.
These level shifters work bidirectional without the need of controlling it's direction.

Please note, that the level shifter devices reduces the ability of the FPGA I/O's to source current, sinking current is not affected.
The shifters incorporate a delay of 0,25ns maximum.

Further on the shifters do not clamp the outputs to it's VCC 3,3V.
They can be lifted up by pullups to a maximum of 7V.

So as an option, the GOP_XC3S200 module supports pullups to 5V or rather the voltage at pin 24. They can be enabled on pin 1 to pin 13, and pin 14 to pin 23 separately by setting jumpers on CON2 11-12 and 13-14 respectively.

With these jumpers enabled, the I/O's are nearly compatible to the IEE1284 standard.
So connection to a PC parallel printer port could be done directly.

6. Detailed XC3S200-4VQ100C FPGA Pinout Table

Pin	FPGA pin function *	(Schema net name) routed to	UCF port name **	Comment
1	I/O_L01P_7	(IO1) SRAM pin20	sa<12>	Sram address input A0 Led4
2	I/O_L01N_7	(IO2) SRAM pin21	sd<0>	Sram data I/O bit0
3	GND	GND	--	Connection to the GND Layer of the PCB
4	I/O_L21P_7	(IO4) SRAM pin22	sd<1>	Sram data I/O bit1
5	I/O_L21N_7	(IO5) SRAM pin23	sd<2>	Sram data I/O bit2
6	VCCO_7	(VCC3V3)	--	LVCMOS33 I/O Voltage 3,3V
7	VCCAUX	(VCC2V5)	--	VCCAUX must be 2,5V
8	I/O_L23P_7	(IO8) SRAM pin25	sd<3>	Sram data I/O bit3
9	I/O_L23N_7	(IO9) SRAM pin26	sd<4>	Sram data I/O bit4
10	GND	GND	--	Connection to the GND Layer of the PCB
11	I/O_L40P_7	(IO11) SRAM pin27	sd<5>	Sram data I/O bit5
12	I/O_L40N_7	(IO12) SRAM pin28	sd<6>	Sram data I/O bit6
13	I/O_L40P_6	(IO13) SRAM pin29	sd<7>	Sram data I/O bit7
14	I/O_L40N_6	(LS6) CON1 pin6	pin6 (pin6)	Connection to the 20/24pin DIL plug to pin6 via level shifter
15	I/O_L24P_6	(LS8) CON1 pin8	pin8 (pin8)	Connection to the 20/24pin DIL plug to pin8 via level shifter
16	I/O_L24N_6	(LS5) CON1 pin5	pin5 (pin5)	Connection to the 20/24pin DIL plug to pin5 via level shifter
17	I/O-P17	(LS7) CON1 pin7	pin7 (pin7)	Connection to the 20/24pin DIL plug to pin7 via level shifter
18	VCCINT	(VCC1V2)	--	Internal core Voltage 1,2V
19	VCCO_6	(VCC3V3)	--	LVCMOS33 I/O Voltage 3,3V
20	GND	GND	--	Connection to the GND Layer of the PCB
21	I/O-P21	(LS9) CON1 pin9	pin9 (pin9)	Connection to the 20/24pin DIL plug to pin9 via level shifter
22	I/O_L01P_6	(LS10) CON1 pin10	pin10 (pin10)	Connection to the 24pin DIL plug to pin10 via level shifter Short to GND by CON2 1-2 for 20pin DIL plug
23	I/O_L01N_6	(LS11) CON1 pin11	pin11 (--)	Connection to the 24pin DIL plug to pin11 via level shifter Not used for the 20pin DIL plug
24	M1	(M1) GND	--	FPGA configuration mode bits M1 is connected to GND via R2
25	M0	(M0) M2 CON2 pin6	--	FPGA configuration mode bits 1 = JTAG, 0 = conf. FLASH M0 is connected to M2 via R7 Can be set to GND by CON2 jumper 5-6
26	M2	(M2) M0 CON2 pin6	--	FPGA configuration mode bits 1 = JTAG, 0 = conf. FLASH M2 is connected to M0 via R7 Can be set to GND by CON2 jumper 5-6
27	I/O_L01P_5	(IO27)	sw1	User tact switch1, shorts IO27 to GND via 100Ω serial

		SW1		resistor, needs pullup inside the FPGA
28	I/O_L01N_5	(IO28) SW2	sw2	User tact switch2, shorts IO28 to GND via 100Ω serial resistor, needs pullup inside the FPGA Jumper CON2 7-8 enables reconfiguration by SW2
29	GND	GND	--	Connection to the GND Layer of the PCB
30	I/O_L28P_5	(tp2)	tp2	Testconnector CON4 pin 2, not 5V tolerant !!!
31	VCCO_5	(VCC3V3)	--	LVCMOS33 I/O Voltage 3,3V Alternatively 2,5V, selectable by solder jumper RJ1
32	I/O_L28N_5	(tp3)	tp3	Testconnector CON4 pin 3, not 5V tolerant !!!
33	VCCAUX	(VCC2V5)	--	VCCAUX must be 2,5V
34	I/O_L31P_5	(tp4)	tp4	Testconnector CON4 pin 4, not 5V tolerant !!!
35	I/O_L31N_5	(tp5)	tp5	Testconnector CON4 pin 5, not 5V tolerant !!!
36	GCLK2	(tp6)	tp6	Testconnector CON4 pin 7, not 5V tolerant !!! This is also an input to the global clock net GCLK2
37	GCLK3	(GIO37) LS pin14	tp7	Testconnector CON4 pin 7 via level shifter This is also an input to the global clock net GCLK3
38	GCLK0	(OSC) XOSC1 out	"osc"	Global clock net input GCLK0, 49,152MHz clock input from XOSC1
39	GCLK1	(LS13) LS pin 16 CON1 pin13	pin13 (--)	Connection to the 24pin DIL plug to pin13 via level shifter Not used for the 20pin DIL plug This is also an input to the global clock net GCLK1
40	DOUT	(DOUT) SRAM pin1 FLASH pin5	sa<0>	Multiple function pin Address sa0 input for SRAM Serial data input for FLASH
41	GND	GND	--	Connection to the GND Layer of the PCB
42	INIT	(INIT) XCF01 pin8 SRAM pin9	sa<4>	Multiple function pin FPGA configuration FLASH reset Address sa4 input for SRAM
43	I/O_L30P_4	(IO43) SRAM pin30	scs	SRAM chip select, has an external pullup, R4
44	I/O_L30N_4	(IO44) SRAM pin32	soe	SRAM output enable, has an external pullup, R1
45	VCCINT	(VCC1V2)	--	Internal core Voltage 1,2V
46	VCCO_4	(VCC3V3)	--	LVCMOS33 I/O Voltage 3,3V
47	I/O_L27P_4	(IO47) IC3 pin15	tp8	Testconnector CON4 pin 8 via level shifter
48	DIN	(DIN) SRAM pin6 FLASH pin2	sa<2>	Multiple function pin Address sa2 input for SRAM Serial data output from FLASH
49	I/O_L01P_4	(IO49)	fcs	FLASH chip select, has an external pullup, R18
50	I/O_L01N_4	(IO50) SRAM pin2	sa<9>	Sram address input A9 Led8
51	DONE	(DONE)	--	FPGA configuration ready strobe, 1 = fpga configured
52	CCLK	(CCLK)	--	FPGA configuration clock
53	I/O_L01P_3	(IO53) SRAM pin3	sa<15>	Sram address input A15 Led7
54	I/O_L01N_3	(LS14) CON1 pin14	pin14 (--)	Connection to the 24pin DIL plug to pin14 via level shifter Not used for the 20pin DIL plug
55	I/O-P17	(LS15) CON1 pin15	pin15 (pin11)	Connection to the 24pin DIL plug to pin15 via level shifter Connection to the 20pin DIL plug to pin11 via level shifter
56	GND	GND	--	Connection to the GND Layer of the PCB

57	VCCO_3	(VCC3V3)	--	LVCMOS33 I/O Voltage 3,3V
58	VCCAUX	(VCC2V5)	--	VCCAUX must be 2,5V
59	I/O-P59	(LS19) CON1 pin19	pin19 (pin15)	Connection to the 24pin DIL plug to pin19 via level shifter Connection to the 20pin DIL plug to pin15 via level shifter
60	I/O_L24P_3	(LS17) CON1 pin17	pin17 (pin13)	Connection to the 24pin DIL plug to pin17 via level shifter Connection to the 20pin DIL plug to pin13 via level shifter
61	I/O_L24N_3	(LS18) CON1 pin18	pin18 (pin14)	Connection to the 24pin DIL plug to pin18 via level shifter Connection to the 20pin DIL plug to pin14 via level shifter
62	I/O_L40P_3	(LS16) CON1 pin16	pin16 (pin12)	Connection to the 24pin DIL plug to pin16 via level shifter Connection to the 20pin DIL plug to pin12 via level shifter
63	I/O_L40N_3	(IO63) SRAM pin4	sa<1>	Sram address input A1
64	I/O_L40P_2	(IO64) SRAM pin5	swr	Sram write enable
65	I/O_L40N_2	(IO65) SRAM pin7	sa<3>	Sram address input A3
66	GND	GND	--	Connection to the GND Layer of the PCB
67	I/O_L24P_2	(IO67) SRAM pin31	sa<10>	Sram address input A10
68	I/O_L24N_2	(IO68) SRAM pin10	sa<5>	Sram address input A5
69	VCCINT	(VCC1V2)	--	Internal core Voltage 1,2V
70	VCCO_2	(VCC3V3)	--	LVCMOS33 I/O Voltage 3,3V
71	I/O_L21P_2	(IO71) SRAM pin11	sa<6>	Sram address input A6
72	I/O_L21N_2	(IO72) SRAM pin12	sa<8>	Sram address input A8
73	GND	GND	--	Connection to the GND Layer of the PCB
74	I/O_L01P_2	(IO74) SRAM pin16	sa<17>	Sram address input A17 Led10
75	I/O_L01N_2	(IO75) SRAM pin15	sa<18>	Sram address input A18 Led9
76	TDO	(FTDO) XCF01 pin4	--	FPGA JTAG chain FPGA TDO is connected to XCF01 TDI
77	TCK	(FTCK) XCF01 pin6 CON3 pin6	--	FPGA JTAG chain JTAG TCK via serial resistor to support 3,3V download adapter
78	TMS	(FTMS) XCF01 pin5 CON3 pin4	--	FPGA JTAG chain JTAG TMS via serial resistor to support 3,3V download adapter
79	I/O_L01P_1	(IO79) SRAM pin13	sa<7>	Sram address input A7
80	I/O_L01N_1	(IO80) SRAM pin14	sa<9>	Sram address input A9
81	I/O-P81	(IO81) SRAM pin17	sa<11>	Sram address input A11 Led3
82	GND	GND	--	Connection to the GND Layer of the PCB
83	VCCO_1	(VCC3V3)	--	LVCMOS33 I/O Voltage 3,3V
84	VCCAUX	(VCC2V5)	--	VCCAUX must be 2,5V
85	I/O_L31P_1	(LS20) CON1 pin20	pin20 (pin16)	Connection to the 24pin DIL plug to pin20 via level shifter Connection to the 20pin DIL plug to pin16 via level shifter
86	I/O_L31N_1	(LS22) CON1 pin22	pin22 (pin18)	Connection to the 24pin DIL plug to pin22 via level shifter Connection to the 20pin DIL plug to pin18 via level shifter
87	GCLK4	(LS21) CON1 pin21	pin21 (pin17)	Connection to the 24pin DIL plug to pin21 via level shifter Connection to the 20pin DIL plug to pin17 via level shifter

88	GCLK5	(LS23) CON1 pin23	pin23 (pin19)	Connection to the 24pin DIL plug to pin23 via level shifter Connection to the 20pin DIL plug to pin19 via level shifter
89	GCLK6	(LS1) CON1 pin1	pin1 (pin1)	Connection to the 20/24pin DIL plug to pin1 via level shifter
90	GCLK7	(LS2) CON1 pin2	pin2 (pin2)	Connection to the 20/24pin DIL plug to pin2 via level shifter
91	I/O_L31P_0	(LS4) CON1 pin4	pin4 (pin4)	Connection to the 20/24pin DIL plug to pin4 via level shifter
92	I/O_L31N_0	(LS3) CON1 pin3	pin3 (pin3)	Connection to the 20/24pin DIL plug to pin3 via level shifter
93	VCCINT	(VCC1V2)	--	Internal core Voltage 1,2V
94	VCCO_0	(VCC3V3)	--	LVCMOS33 I/O Voltage 3,3V
95	GND	GND	--	Connection to the GND Layer of the PCB
96	I/O_L01P_0	(IO96) SRAM pin18	sa<13>	Sram address input A13 Led5
97	I/O_L01N_0	(IO97) SRAM pin19	sa<14>	Sram address input A14 Led6
98	HSWAP_EN	(HSWAP) R19	--	FPGA configuration signal, put to GND by R19 0 = I/O pullups on power up, 1 = no I/O pullups
99	PROG_B	(PROG) XCF01 pin7 CON2 pin8	--	FPGA configuration reset signal, active low,, can be driven by I/O pin28 or SW2, if jumper on CON2 7-8 is set, or always by XCF01
100	TDI	(FTDI) CON3 pin10	--	FPGA JTAG chain JTAG TDI via serial resistor to support 3,3V download adapter

* FB1MC11 denotes function block1, macrocell 11
** There is an UCF file definition for 24pin, and another one for 20pin device usage

7. CON4 Test Connector Pinout Table

Pin	FPGA pin function *	(Schema net name) routed to	UCF port name **	Comment
1	GND	GND	--	Power ground plane connection
2	I/O_L28P_5	(tp2) FPGA pin30	tp2	Testconnector CON4 pin 2 to FPGA pin30 not 5V tolerant !!!
3	I/O_L28N_5	(tp3) FPGA pin32	tp3	Testconnector CON4 pin 3 to FPGA pin32 not 5V tolerant !!!
4	I/O_L31P_5	(tp4) FPGA pin34	tp4	Testconnector CON4 pin 4 to FPGA pin34 not 5V tolerant !!!
5	I/O_L31N_5	(tp5) FPGA pin36	tp5	Testconnector CON4 pin 5 to FPGA pin36 not 5V tolerant !!!
6	GCLK2	(tp6) FPGA pin36	tp6	Testconnector CON4 pin 7 to FPGA pin36 not 5V tolerant !!! This is also an input to the global clock net GCLK2
7	GCLK3	(GIO37) FPGA pin37	tp7	Testconnector CON4 pin 7 via level shifter to FPGA pin37 This is also an input to the global clock net GCLK3
8	I/O_L27P_4	(IO47) FPGA pin47	tp8	Testconnector CON4 pin 8 via level shifter to FPGA pin47
9	--	(VCC_IN) voltage reg	--	5V input voltage protected by a polyfuse

8. CON2 Configuration Jumper Options

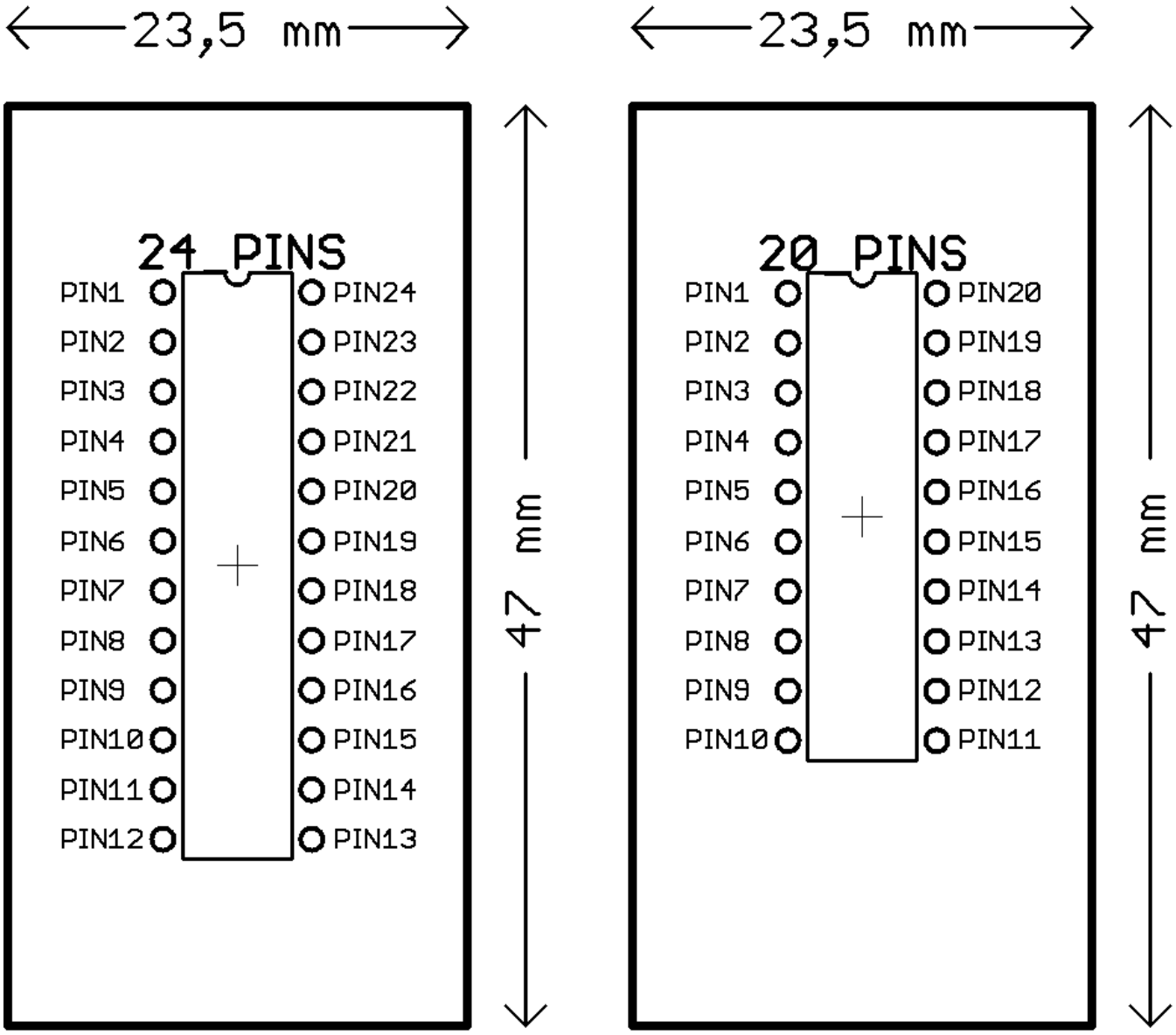
1-2	Enable 20pin PAL / GAL Emulation, put GND to pin 10 of CON1
3-4	Enable XOSC1 crystal oscillator 49,152 MHz
5-6	Enable FPGA configuration from Platform FLASH, otherwise JTAG only
7-8	Enable reprogram of the FPGA by SW2 or IO28
9-10	Enable User Leds
11-12	Enable pullups on Pin1, Pin2, Pin3, Pin4, Pin5, Pin6, Pin7, Pin8, Pin9, Pin10, Pin11, Pin13 to 5V or rather the voltage at Pin 24 of the module
13-14	Enable pullups on Pin14, Pin15, Pin16, Pin17, Pin18, Pin19, Pin20, Pin21, Pin22, Pin23 to 5V or rather the voltage at Pin 24 of the module

9. CON1 DIL Connector Pinout Table

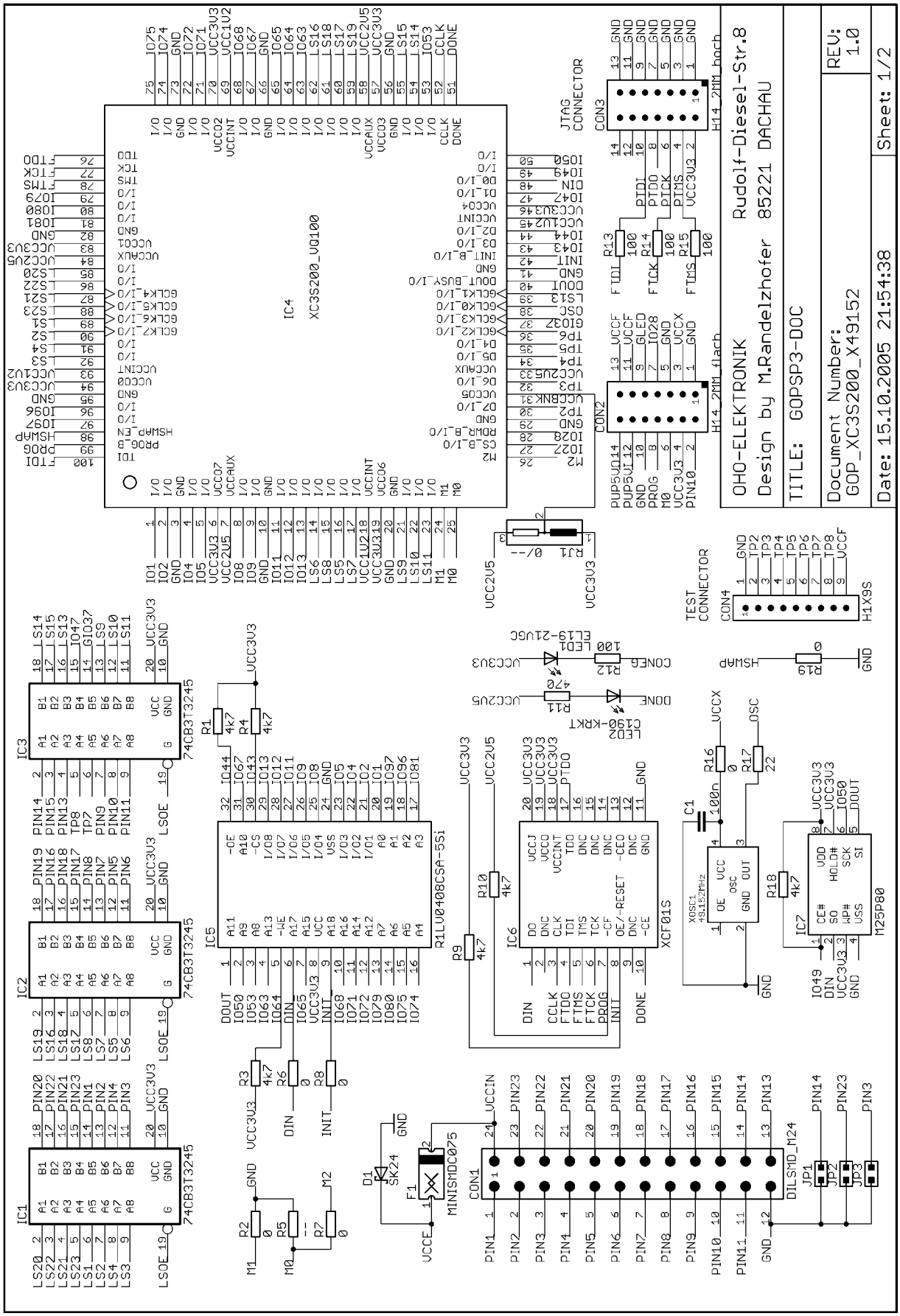
Pin	FPGA pin function *	(Schema net name) routed to	UCF port name **	Comment
1	GCLK6	(LS1) CON1 pin1	pin1 (pin1)	Connection to FPGA pin 89 via level shifter
2	GCLK7	(LS2) CON1 pin2	pin2 (pin2)	Connection to FPGA pin 90 via level shifter
3	I/O_L31N_0	(LS3) CON1 pin3	pin3 (pin3)	Connection to FPGA pin 92 via level shifter
4	I/O_L31P_0	(LS4) CON1 pin4	pin4 (pin4)	Connection to FPGA pin 91 via level shifter
5	I/O_L24N_6	(LS5) CON1 pin5	pin5 (pin5)	Connection to FPGA pin 16 via level shifter
6	I/O_L40N_6	(LS6) CON1 pin6	pin6 (pin6)	Connection to FPGA pin 14 via level shifter
7	I/O-P17	(LS7) CON1 pin7	pin7 (pin7)	Connection to FPGA pin 17 via level shifter
8	I/O_L24P_6	(LS8) CON1 pin8	pin8 (pin8)	Connection to FPGA pin 15 via level shifter
9	I/O-P21	(LS9) CON1 pin9	pin9 (pin9)	Connection to FPGA pin 21 via level shifter
10	I/O_L01P_6	(LS10) CON1 pin10	pin10 (pin10)	Connection to FPGA pin 22 via level shifter
11	I/O_L01N_6	(LS11) CON1 pin11	pin11 (--)	Connection to FPGA pin 23 via level shifter
12	GND	GND	--	Power ground plane connection
13	GCLK1	(LS13) CON1 pin13	pin13 (--)	Connection to FPGA pin 39 via level shifter
14	I/O_L01N_3	(LS14) CON1 pin14	pin14 (--)	Connection to FPGA pin 54 via level shifter
15	I/O-P17	(LS15) CON1 pin15	pin15 (pin11)	Connection to FPGA pin 55 via level shifter
16	I/O_L40P_3	(LS16) CON1 pin16	pin16 (pin12)	Connection to FPGA pin 62 via level shifter
17	I/O_L24P_3	(LS17) CON1 pin17	pin17 (pin13)	Connection to FPGA pin 60 via level shifter
18	I/O_L24N_3	(LS18) CON1 pin18	pin18 (pin14)	Connection to FPGA pin 61 via level shifter
19	I/O-P59	(LS19) CON1 pin19	pin19 (pin15)	Connection to FPGA pin 59 via level shifter
20	I/O_L31P_1	(LS20) CON1 pin20	pin20 (pin16)	Connection to FPGA pin 85 via level shifter
21	I/O_L31N_1	(LS22) CON1 pin22	pin22 (pin18)	Connection to FPGA pin 86 via level shifter
22	GCLK4	(LS21) CON1 pin21	pin21 (pin17)	Connection to FPGA pin 87 via level shifter
23	GCLK5	(LS23) CON1 pin23	pin23 (pin19)	Connection to FPGA pin 88 via level shifter
24	--	PIN_24	--	5V input voltage to the module

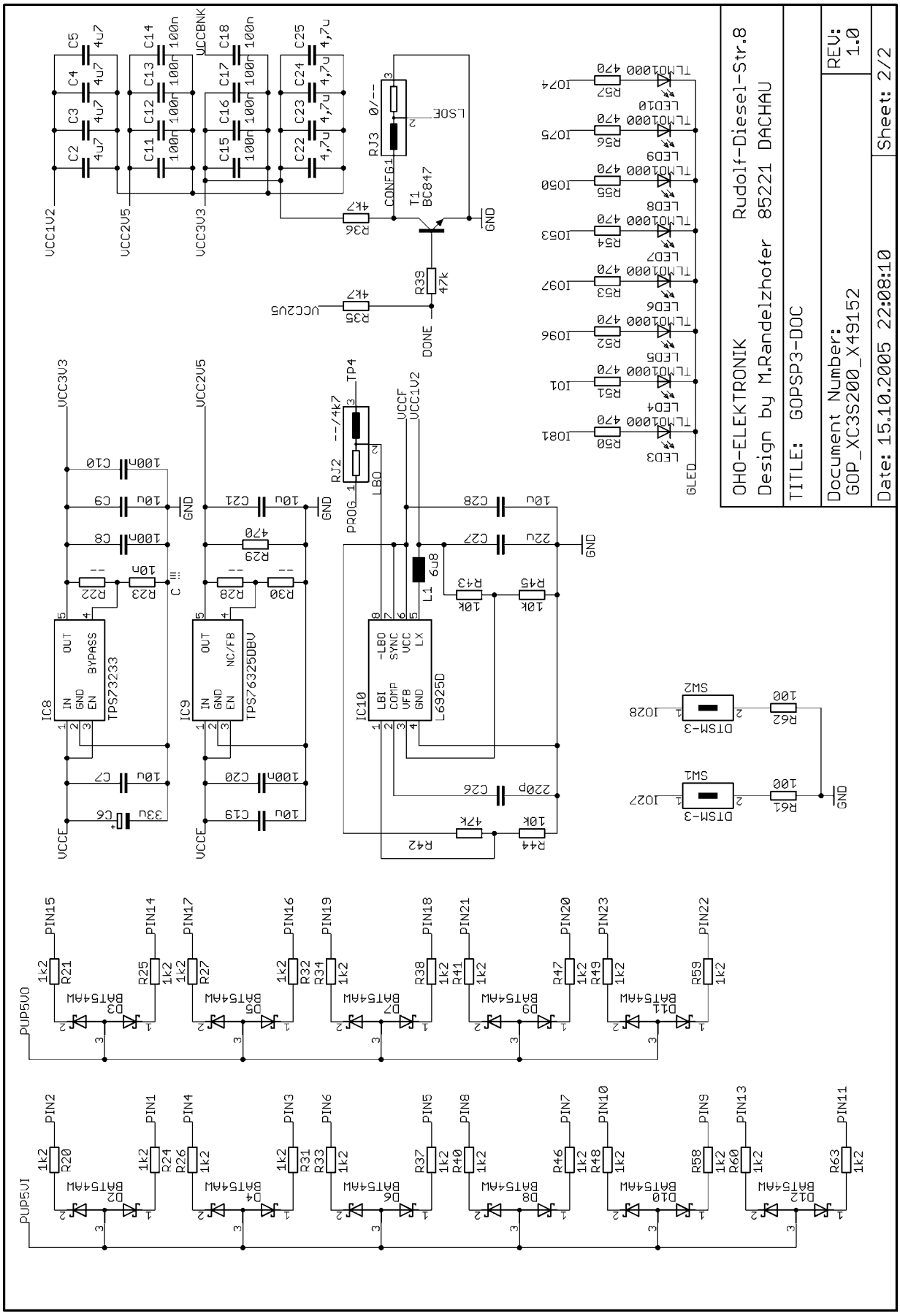
10. CON1 DIL Connector Layout

GOP_XC3S200 module top view for 24 pin and 20 pin emulation mode:

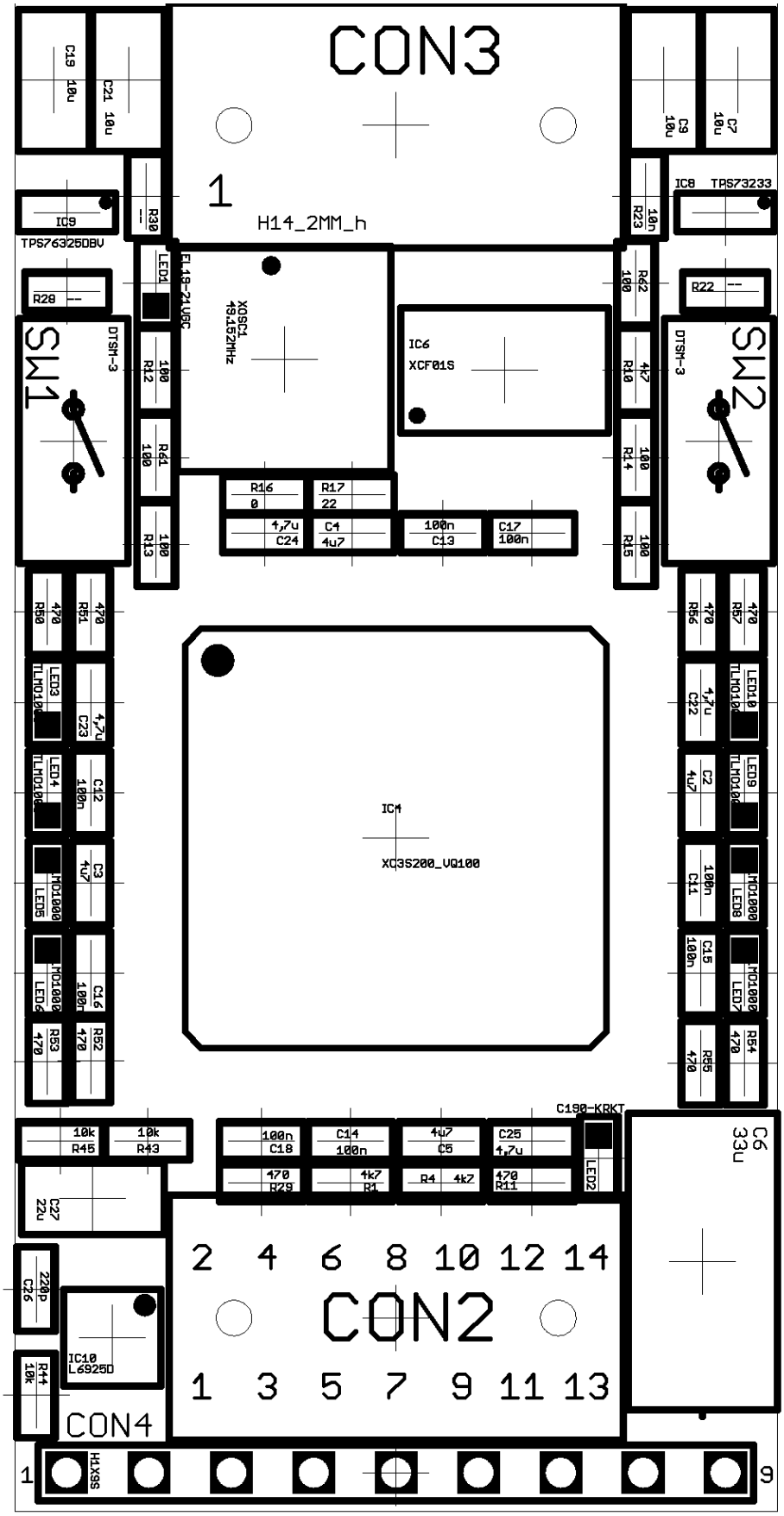


11. Schematics

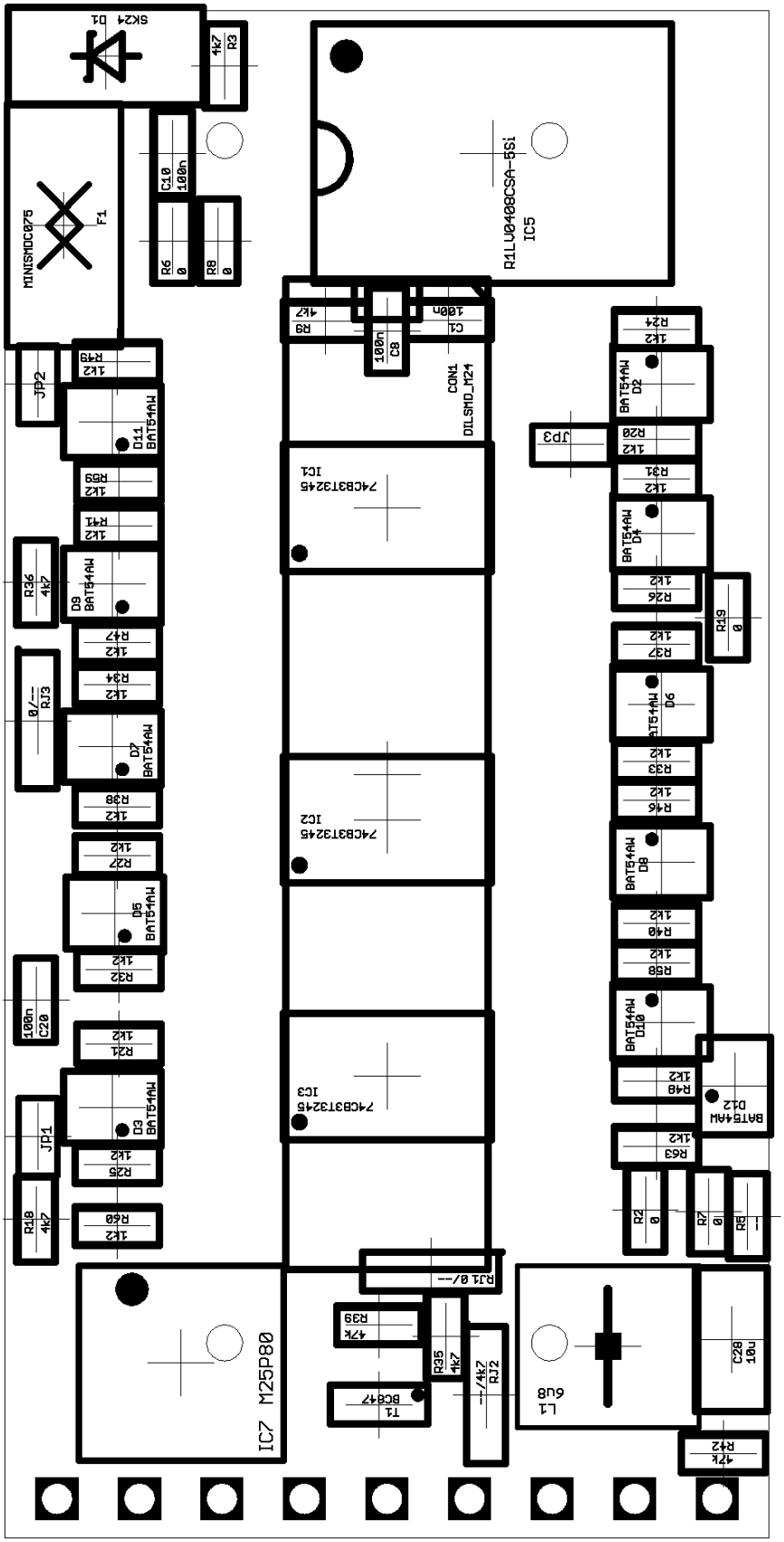



OHO-ELEKTRONIK
Rudolf-Diesel-Str.8
Design by M.Randelzhofer 85221 DACHAU
TITLE: GOPSP3-DOC
Document Number:
GOP_XC3S200_X49152
REV:
1.0
Date: 15.10.2005 22:08:10
Sheet: 2/2

12. Module Layout Top View



13. Module Layout Bottom View



14. Technical Specifications

CPLD:	Xilinx XC3S200-4VQ100 Spartan-3 FPGA
Supply Voltage on PIN24:	3,5 - 5,5V
Size:	47x 23,5mm, 1,85" x 0,925"
Height PCB to Top:	max. 8mm, 0,315"
Height PCB to Bottom:	max. 12mm, 0,472"
Weight:	12g

15. Literature

- [1] DS099 Spartan-3 Complete Data Sheet
  http://direct.xilinx.com/bvdocs/publications/ds099.pdf
- [2] DS097 Xilinx Parallel Cable IV
  http://direct.xilinx.com/bvdocs/publications/ds097.pdf
- [3] DS300 Platform Cable USB
  http://direct.xilinx.com/bvdocs/publications/ds300.pdf
- [4] L6925 High Efficiency Monolithic Synchronious Step Down Regulator
  http://www.st.com/stonline/products/literature/ds/9301/l6925d.pdf
- [5] TPS76325 Low Power 150mA Low Dropout Linear Regulators
  http://focus.ti.com/lit/ds/symlink/tps76325.pdf
- [6] TPS73233 Cap-Free NMOS 250mA Low Dropout Regulator With Reverse Current Protection
  http://focus.ti.com/lit/ds/symlink/tps73233.pdf
- [7] SN74CB3T3245 8-Bit Fet Bus Switch
  http://focus.ti.com/lit/ds/symlink/sn74cb3t3245.pdf

16. USER'S MANUAL Revisions

Version	Date	Comments
V0.9	23/10/2005	Prerelease