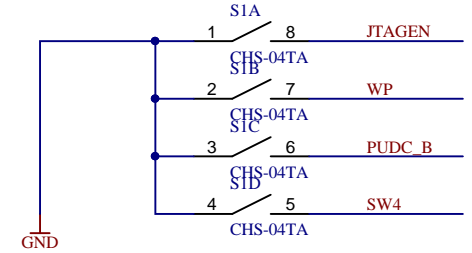
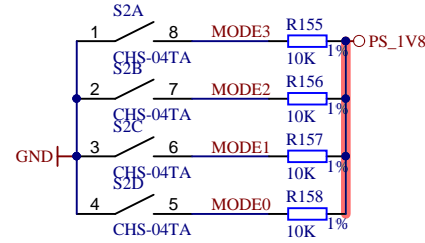
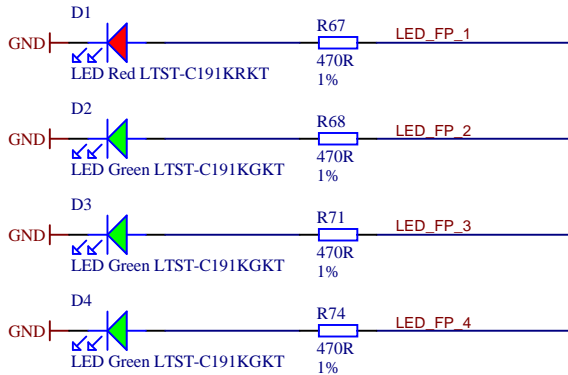
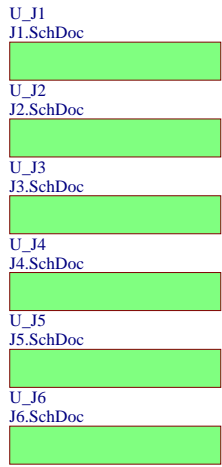
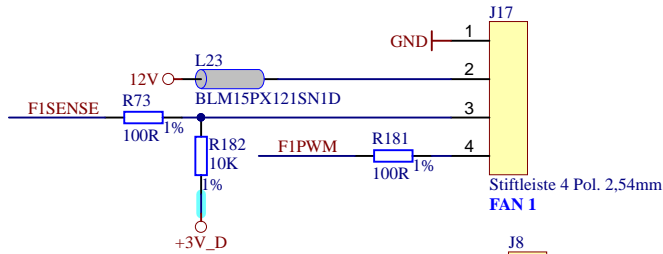
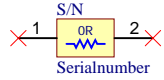


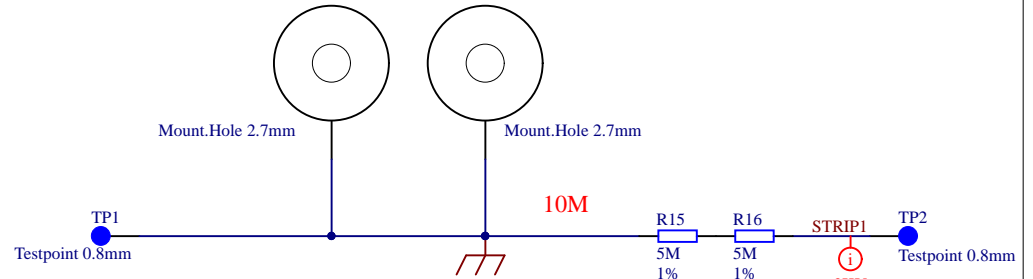
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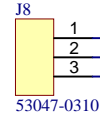
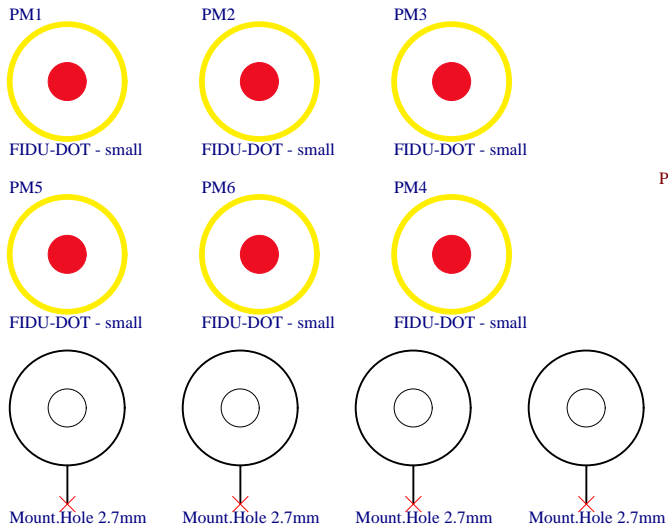
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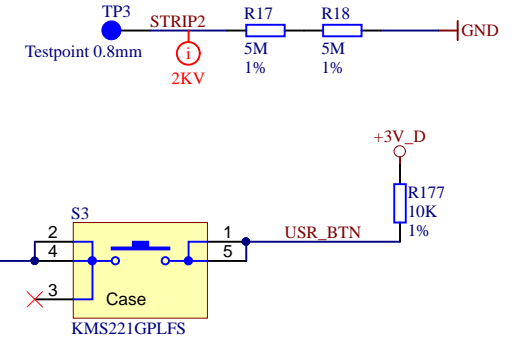
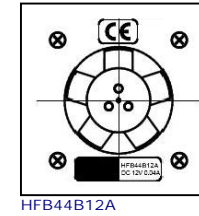
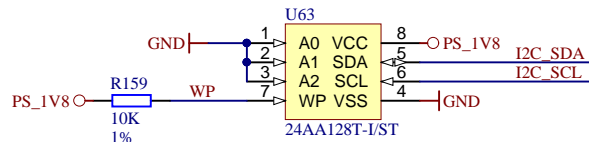
PE = STRIP, no connection to GND on the board only when inserted into RACK



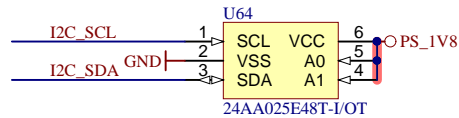
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Slave ADDR: 1010011



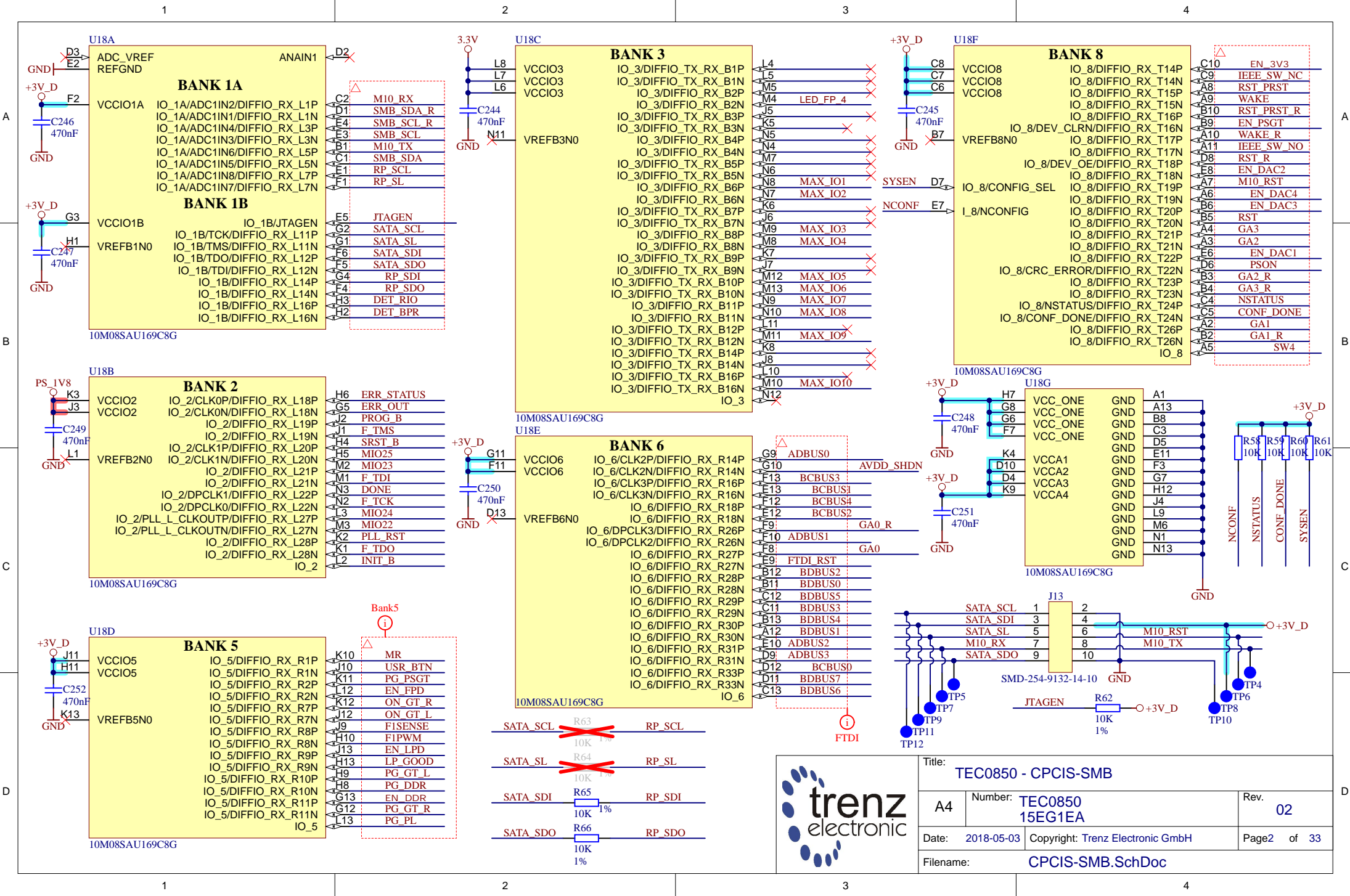
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D

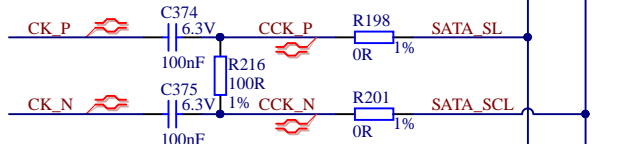
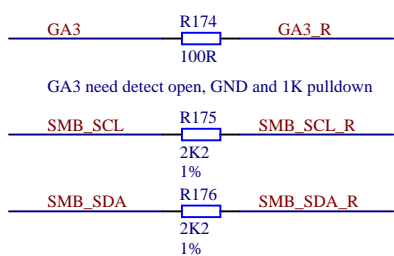
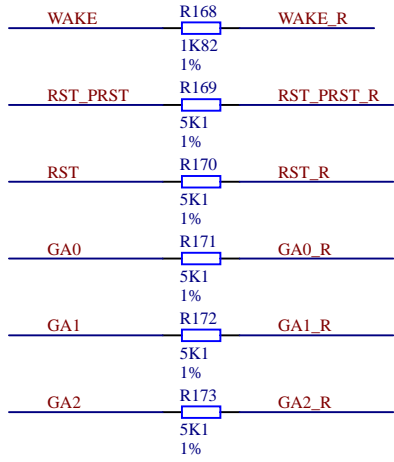


Title: TEC0850 - CPCIS-MAIN		
A4	Number: TEC0850 15EG1EA	Rev. 02
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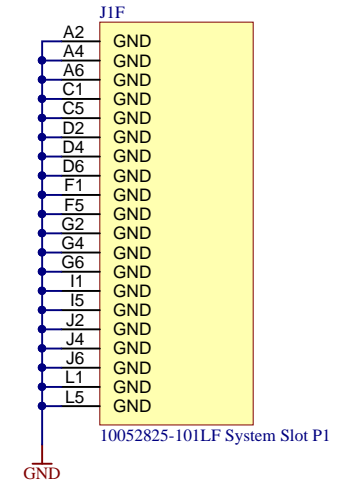
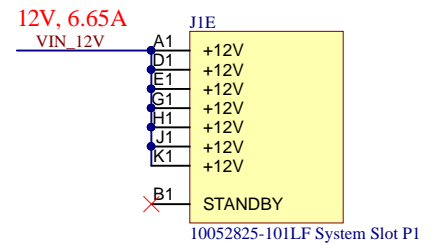
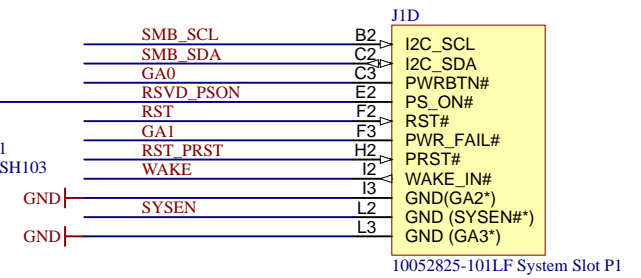
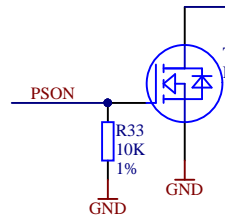
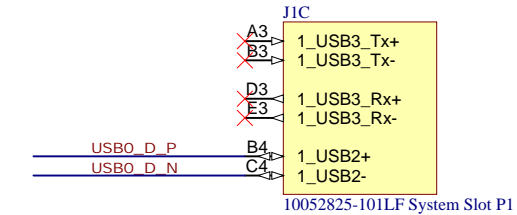
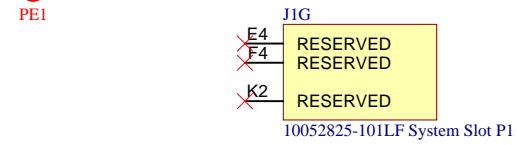
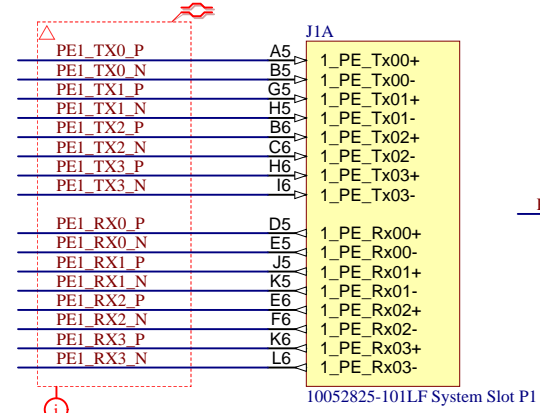


Title: TEC0850 - CPCIS-SMB			
A4	Number: TEC0850 15EG1EA	Rev. 02	
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Filename: CPCIS-SMB.SchDoc			

1.8, 2.2 and 5.1K are REQUIRED BY CPCI-S do not optimize to other values



PCB Patch:
only for 15EG1EA variant
to U18 (MAX10)



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A4 Number: TEC0850 15EG1EA Rev. 02
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1

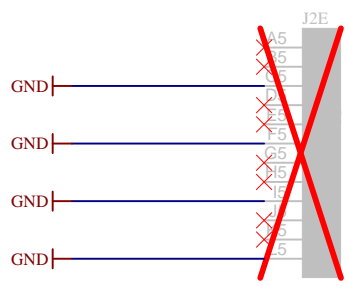
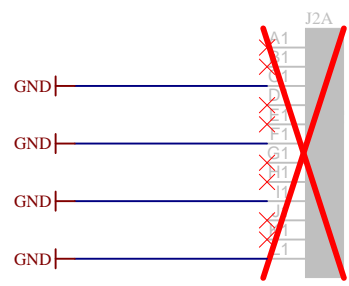
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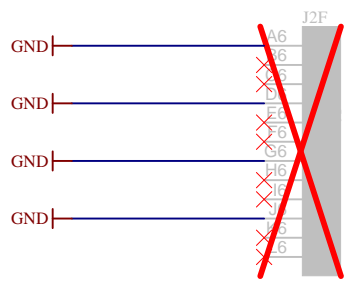
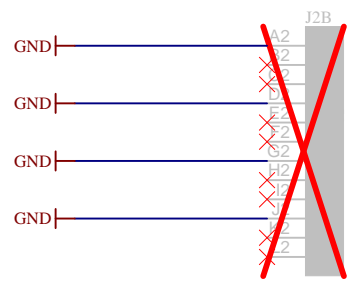
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A



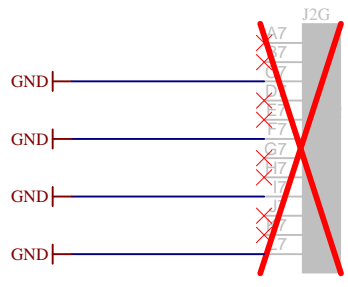
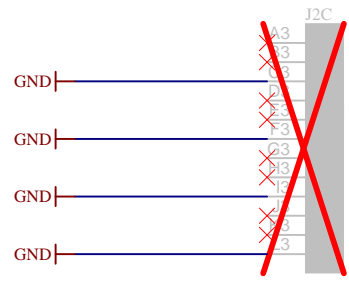
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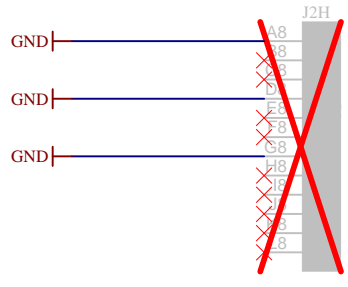
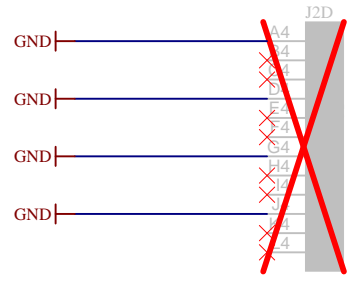
C

C



D

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Title: TEC0850 - J2		
A4	Number: TEC0850 15EG1EA	Rev. 02
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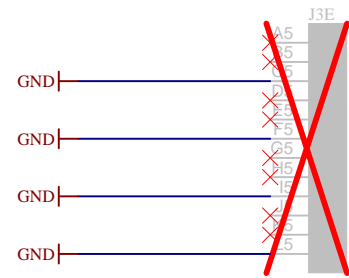
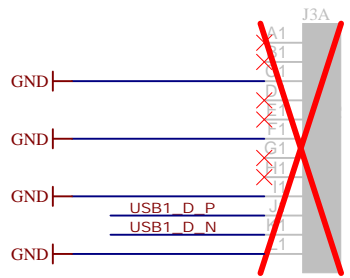
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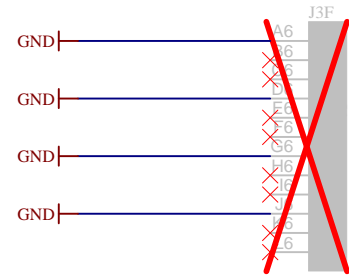
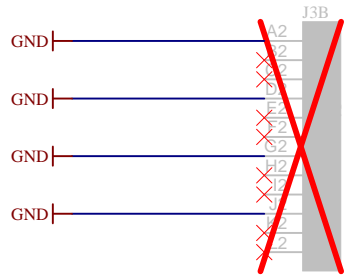
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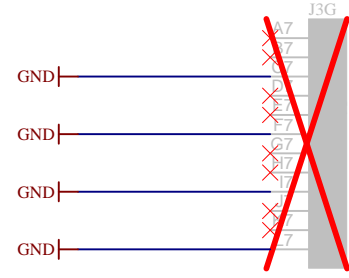
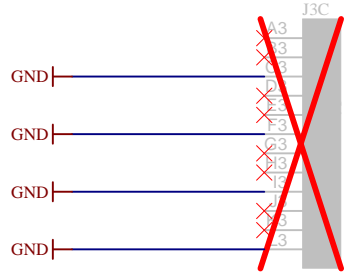
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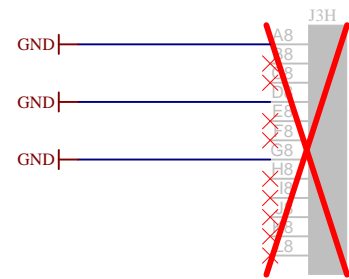
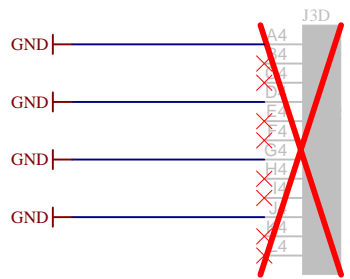
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A4	Number: TEC0850 15EG1EA	Rev. 02
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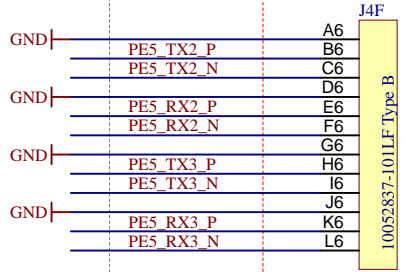
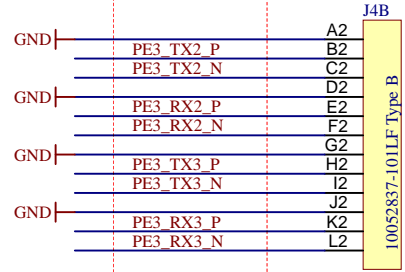
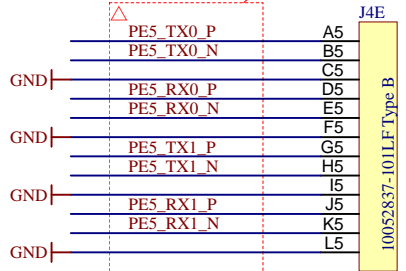
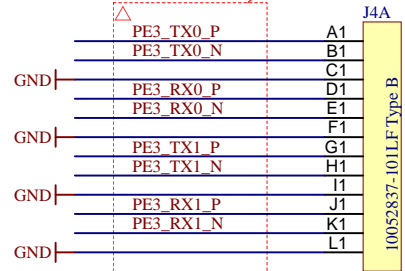
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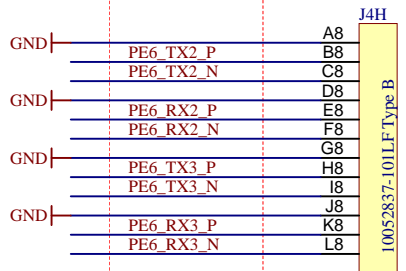
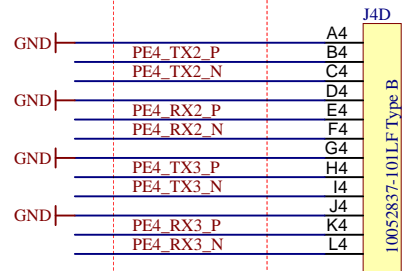
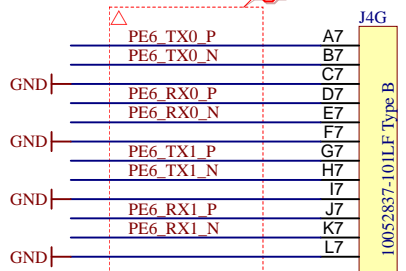
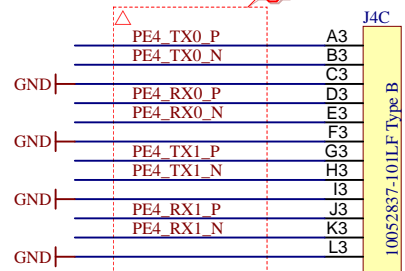
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PE3

PE5



PE4

PE6



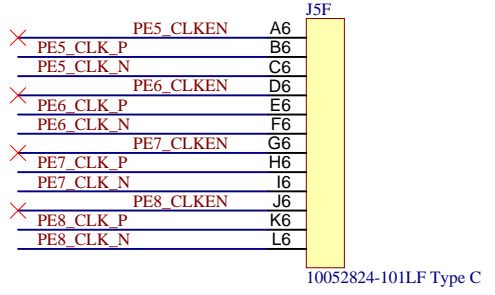
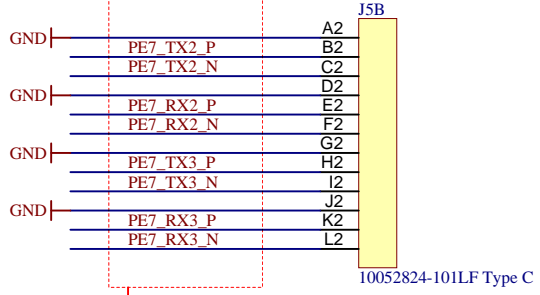
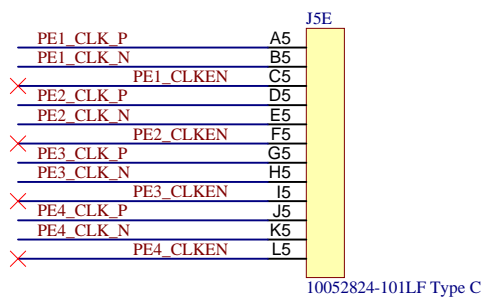
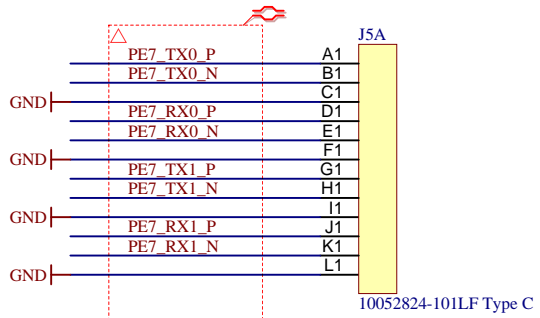
Title: TEC0850 - J4		
A4	Number: TEC0850 15EG1EA	Rev. 02
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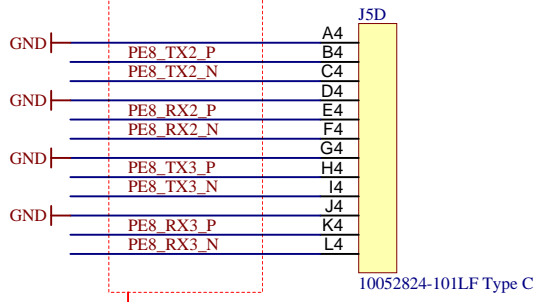
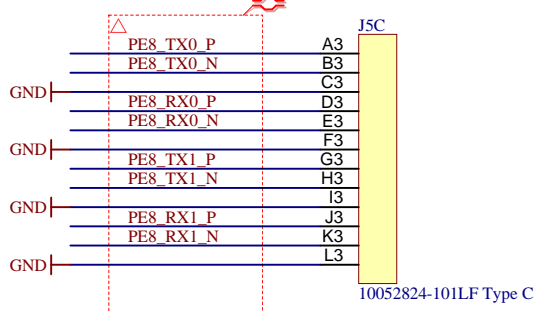
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PE7



PE8



Title: TEC0850 - J5		
A4	Number: TEC0850 15EG1EA	Rev. 02
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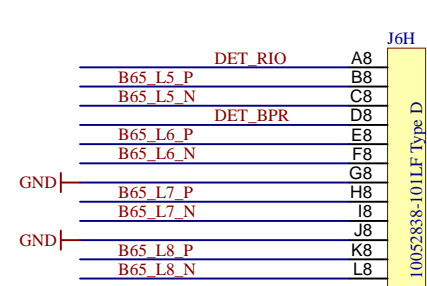
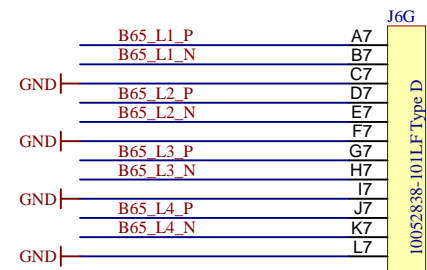
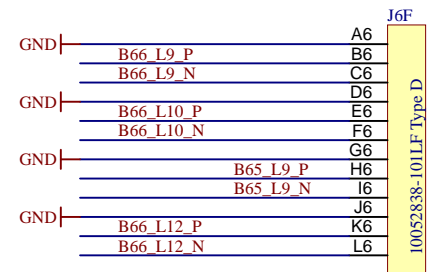
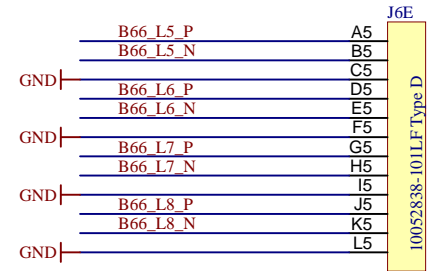
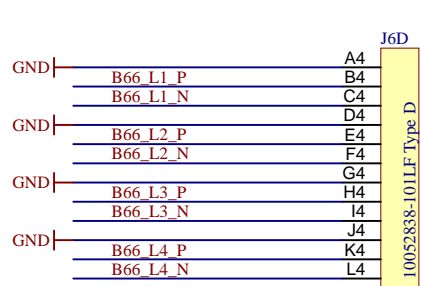
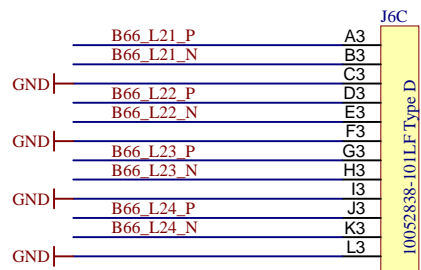
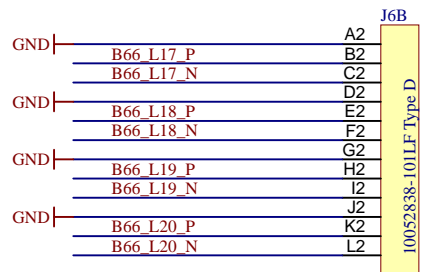
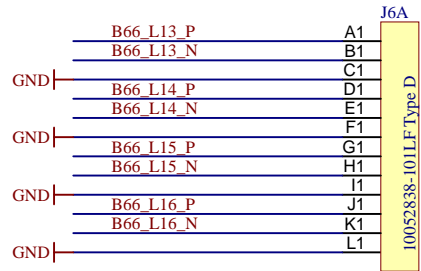
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C

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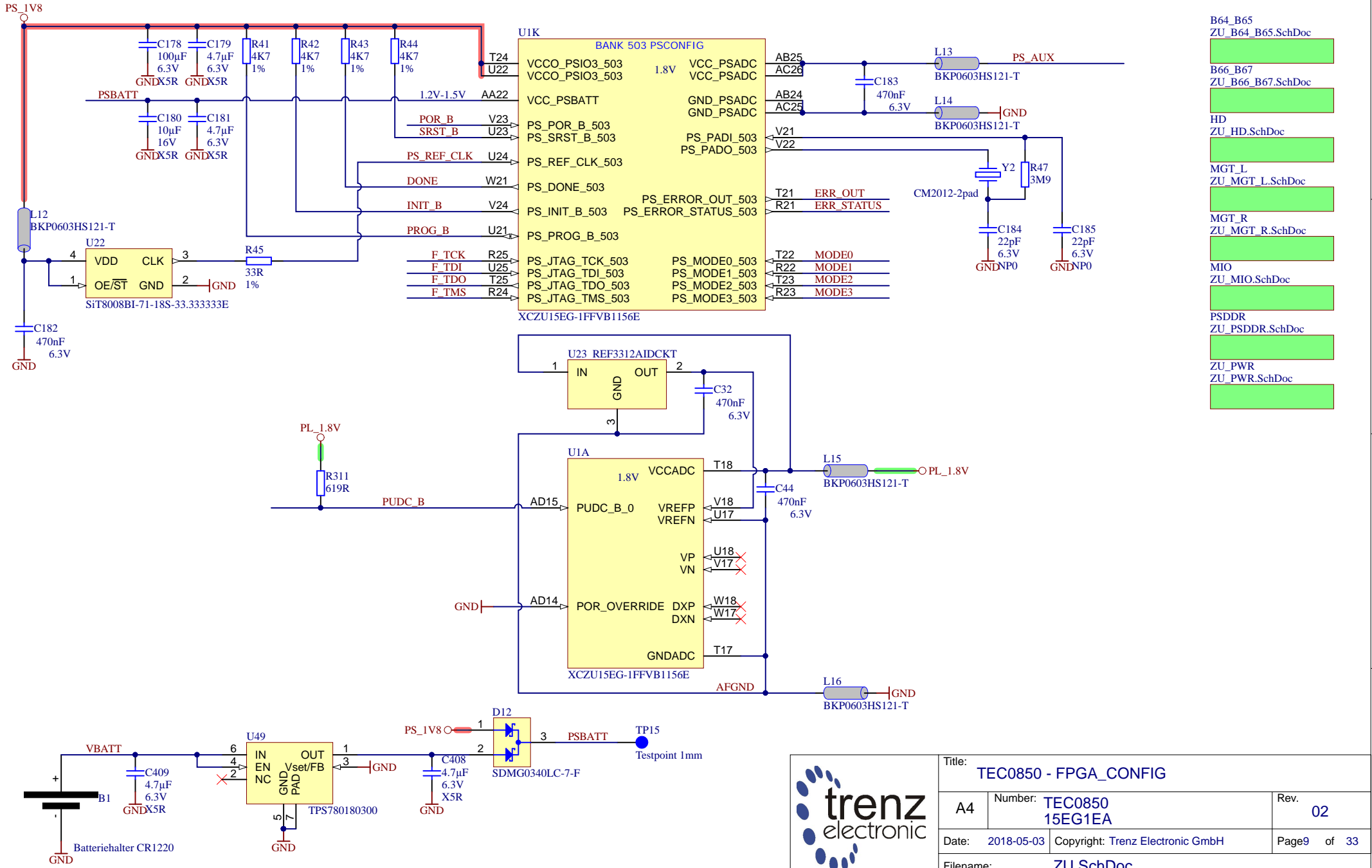
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A4	Number: TEC0850 15EG1EA	Rev. 02
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Filename: J6.SchDoc		

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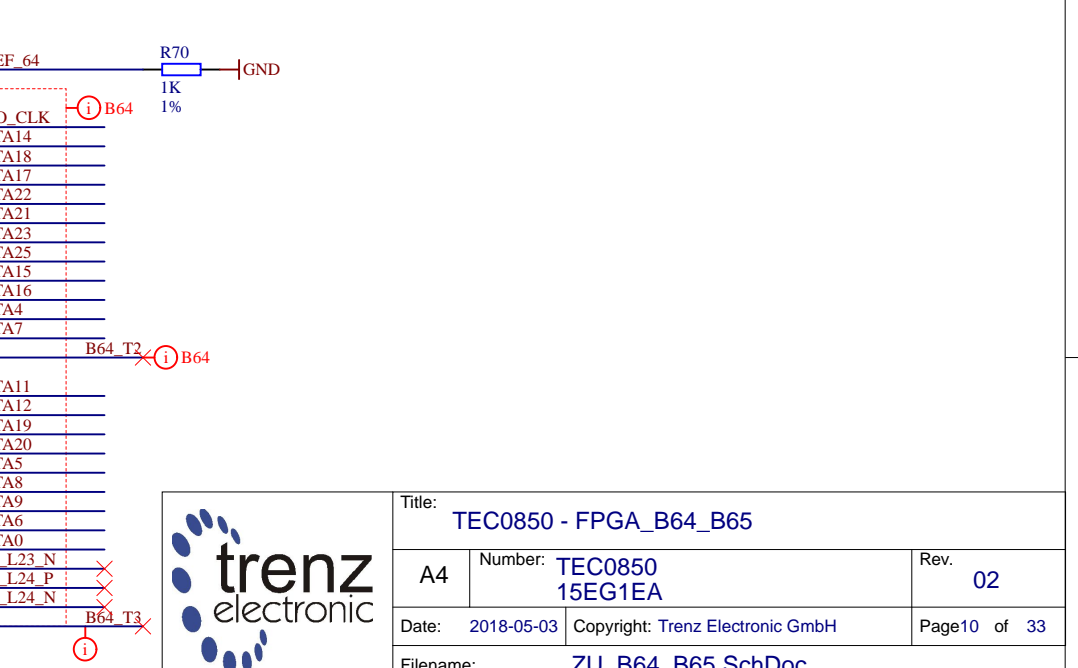
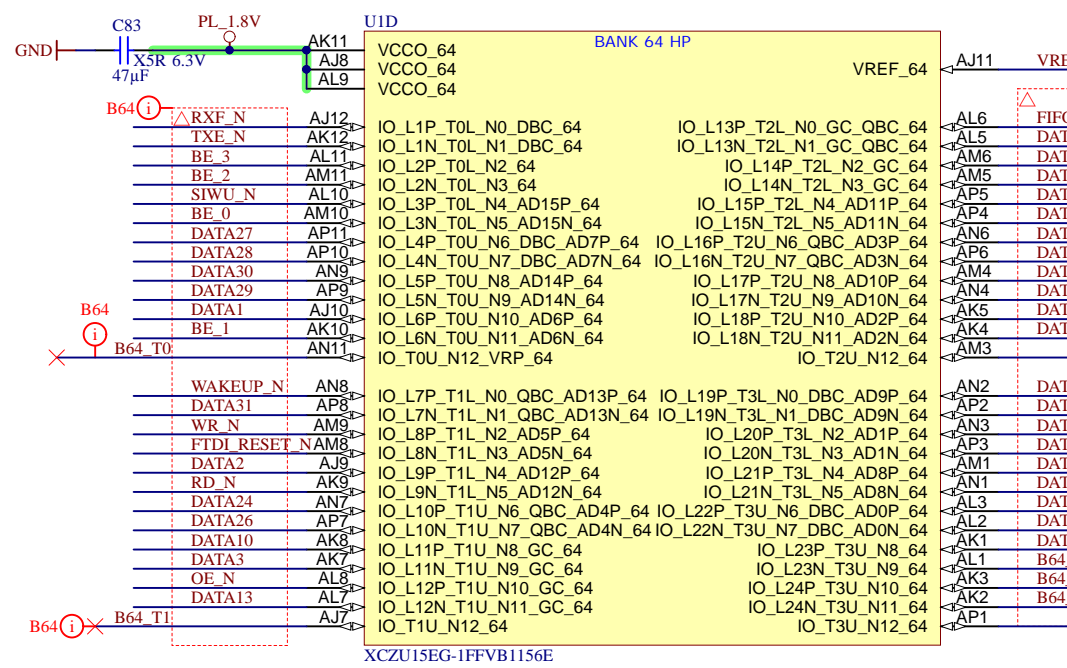
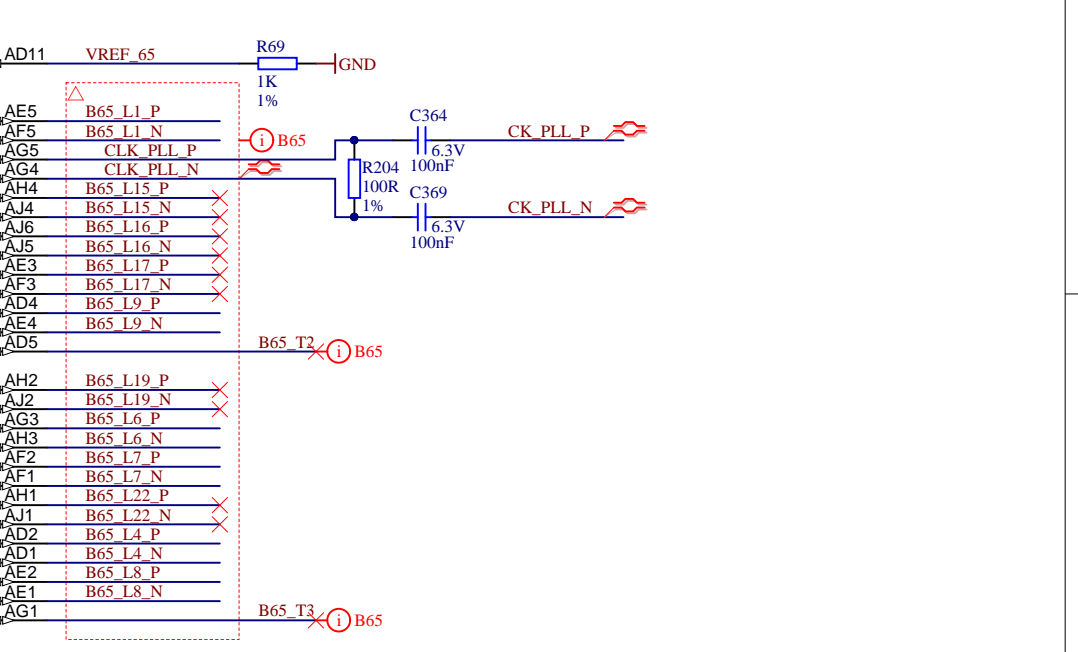
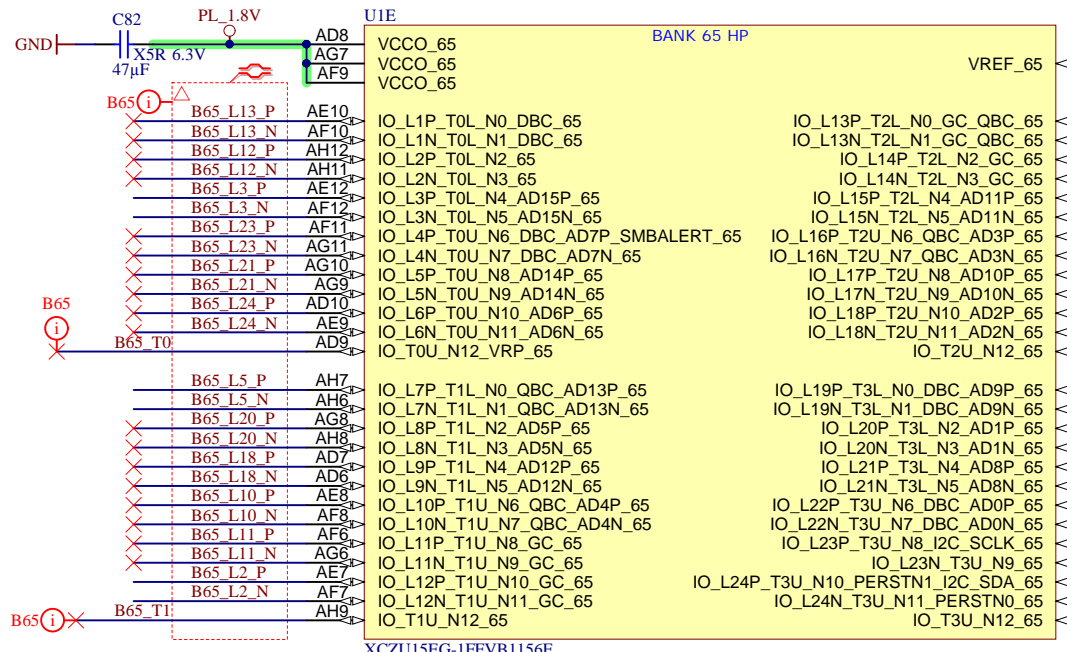
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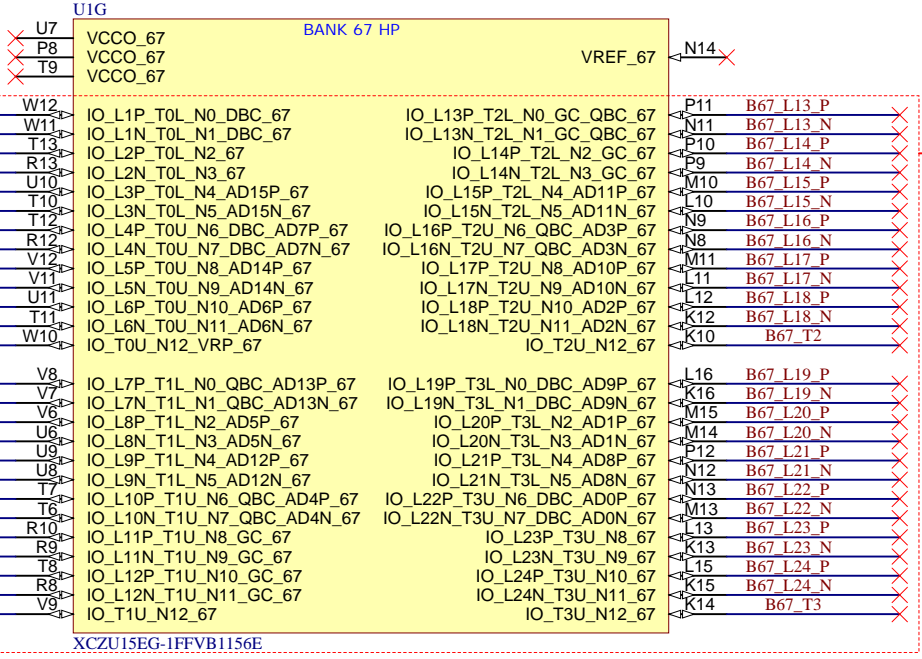
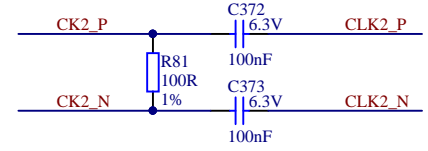
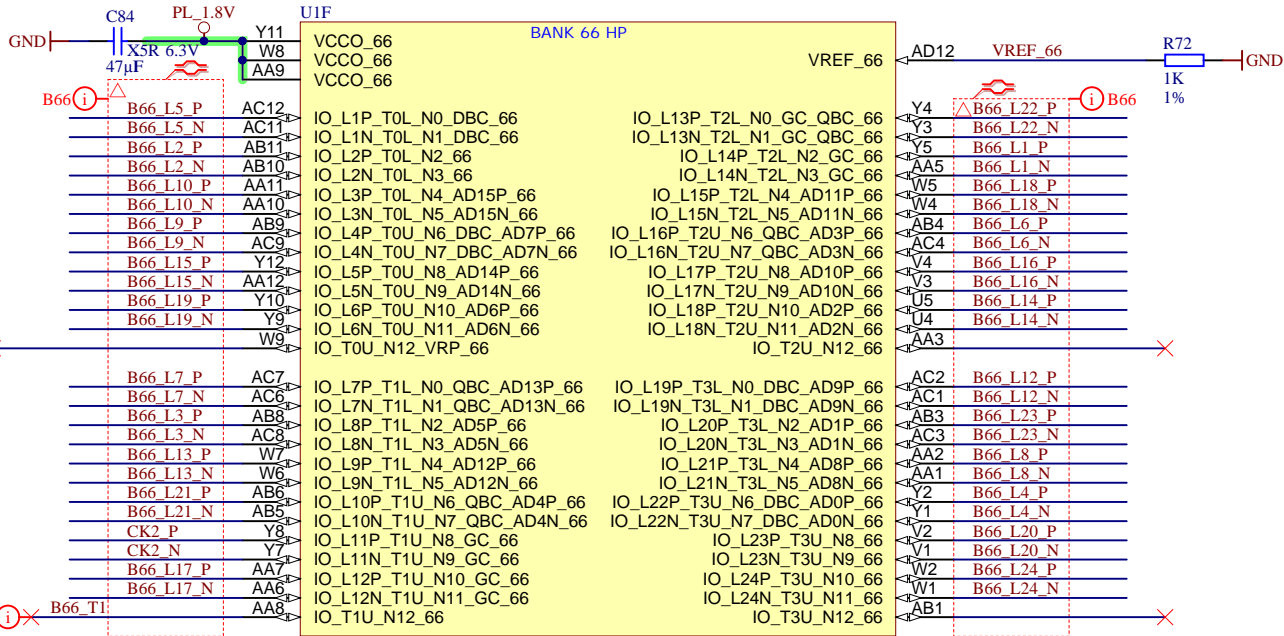
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ZU_B64_B65.SchDoc
- B66_B67
ZU_B66_B67.SchDoc
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- MGT_L
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- ZU_PWR
ZU_PWR.SchDoc



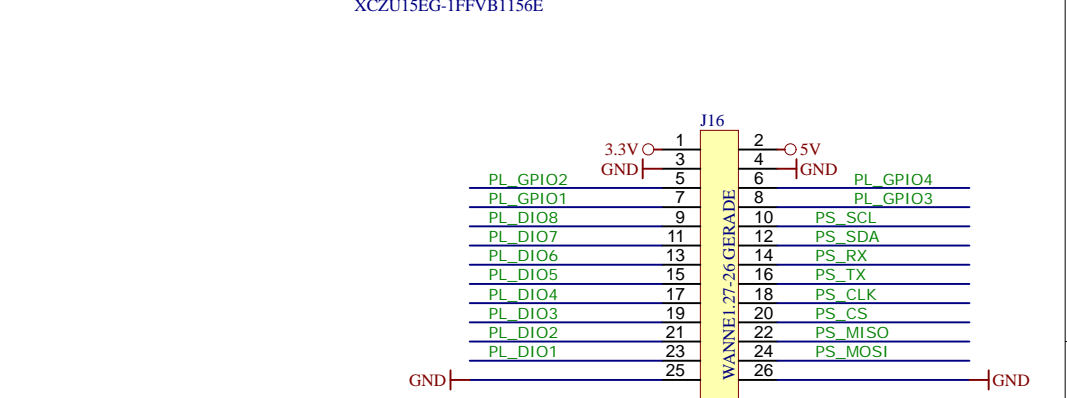
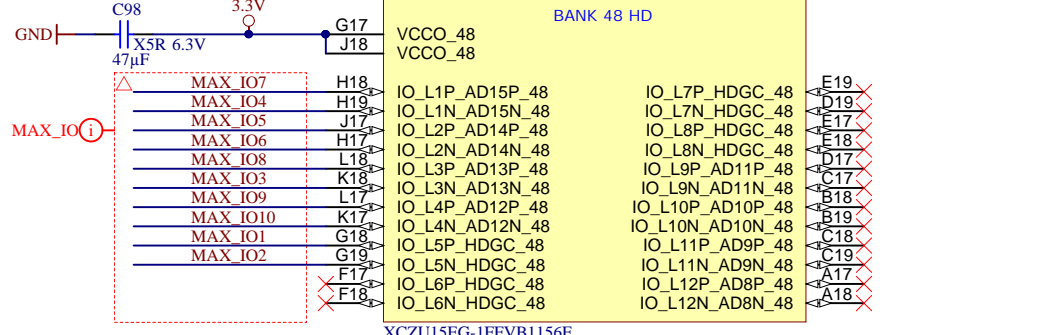
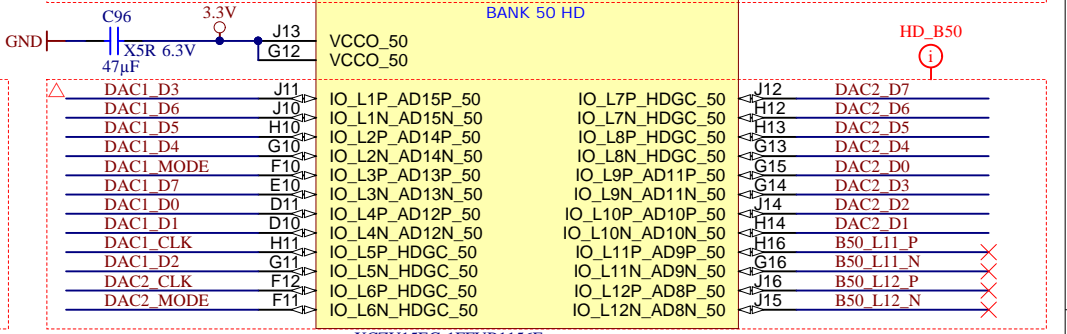
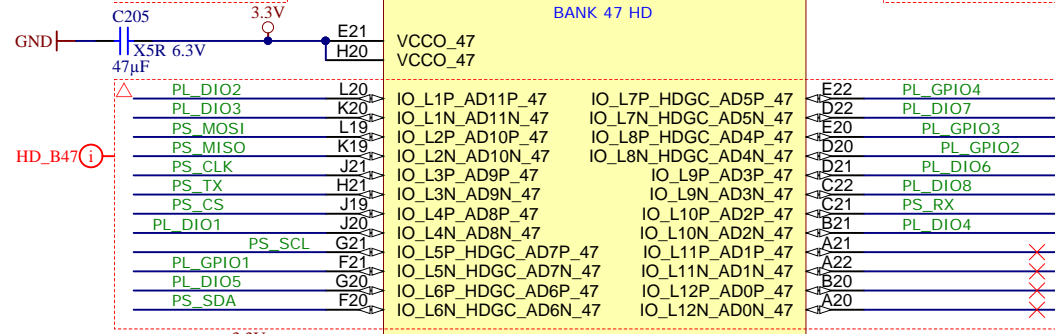
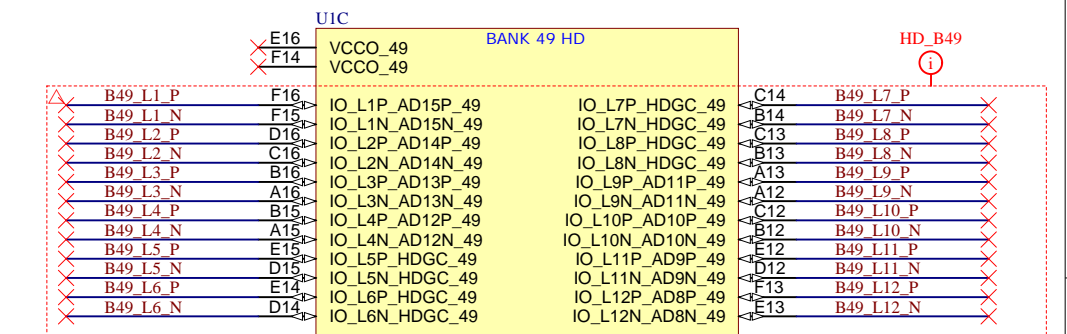
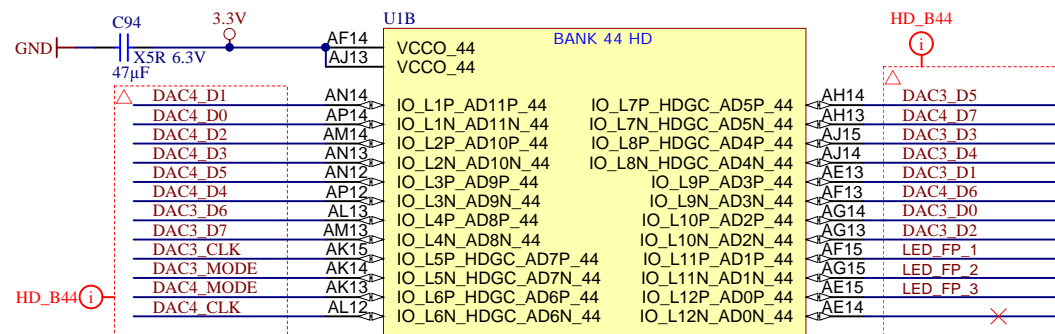
Title: TEC0850 - FPGA_CONFIG		
A4	Number: TEC0850 15EG1EA	Rev. 02
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Filename: ZU.SchDoc		



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A4	Number: TEC0850 15EG1EA	Rev. 02
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Filename: ZU_B64_B65.SchDoc		



Title: TEC0850 - FPGA_B66_B67		
A4	Number: TEC0850 15EG1EA	Rev. 02
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Title: TEC0850 - FPGA_HD		
A4	Number: TEC0850 15EG1EA	Rev. 02
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Filename: ZU_HD.SchDoc		

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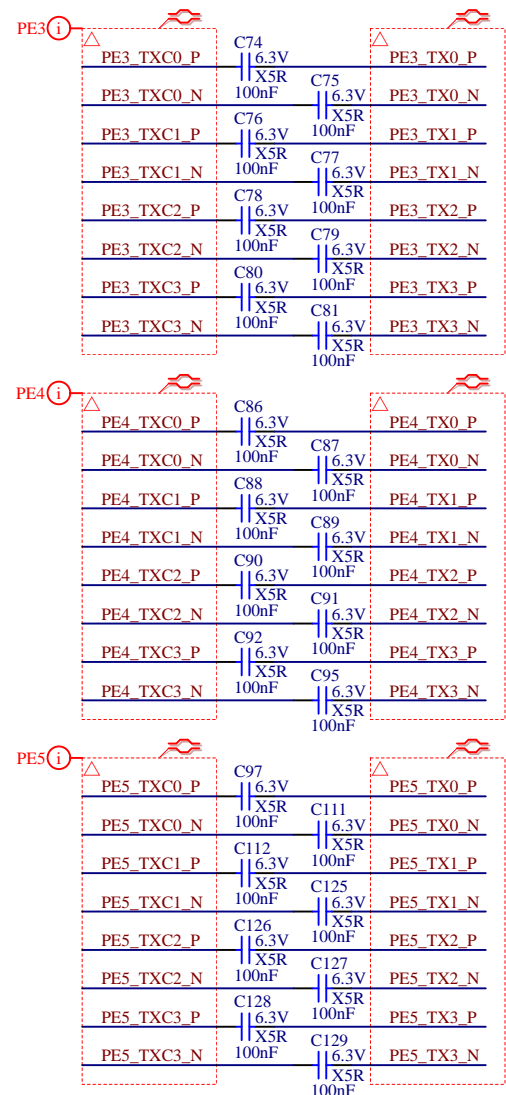
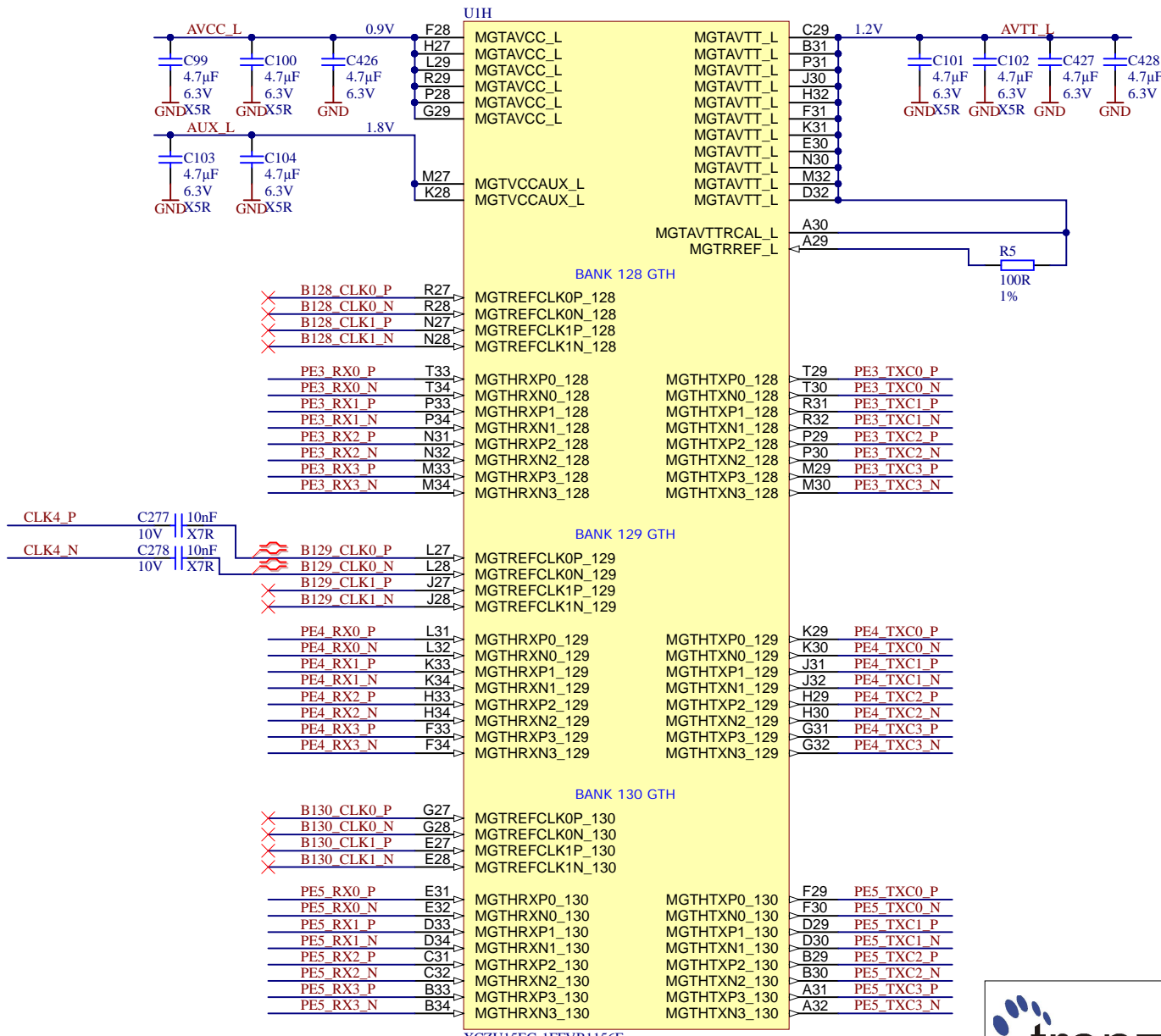
D

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D



XCZU15EG-1FFVB1156E



Title: TEC0850 - FPGA_MGT_L		
A4	Number: TEC0850 15EG1EA	Rev. 02
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Filename: ZU_MGT_L.SchDoc		

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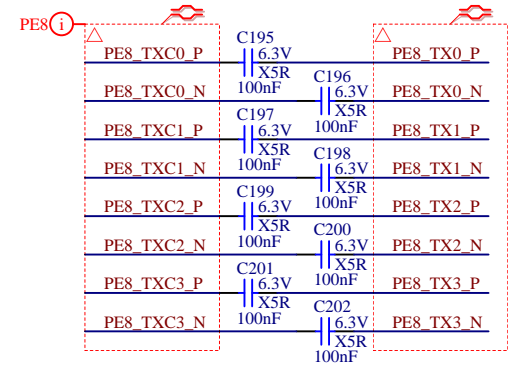
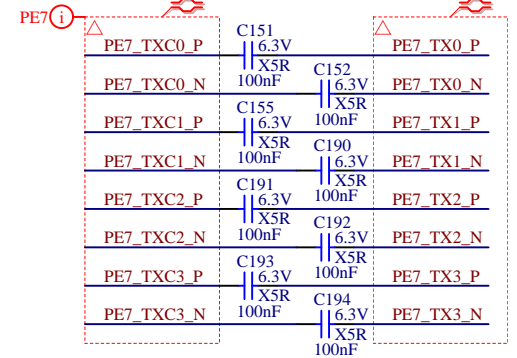
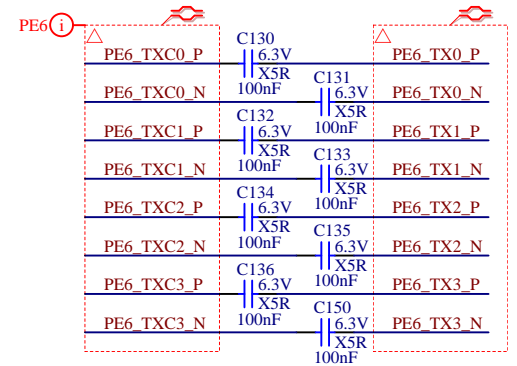
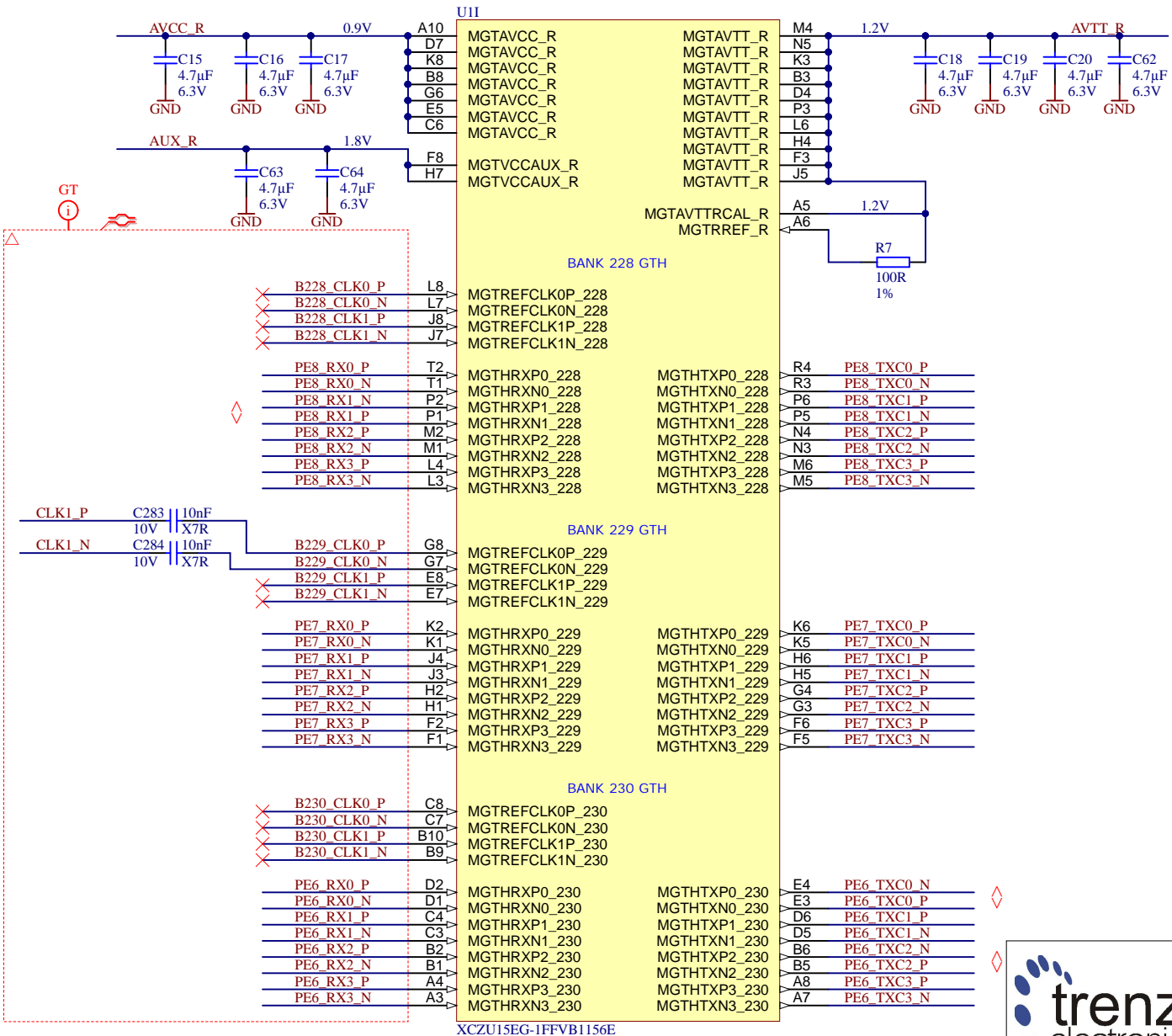
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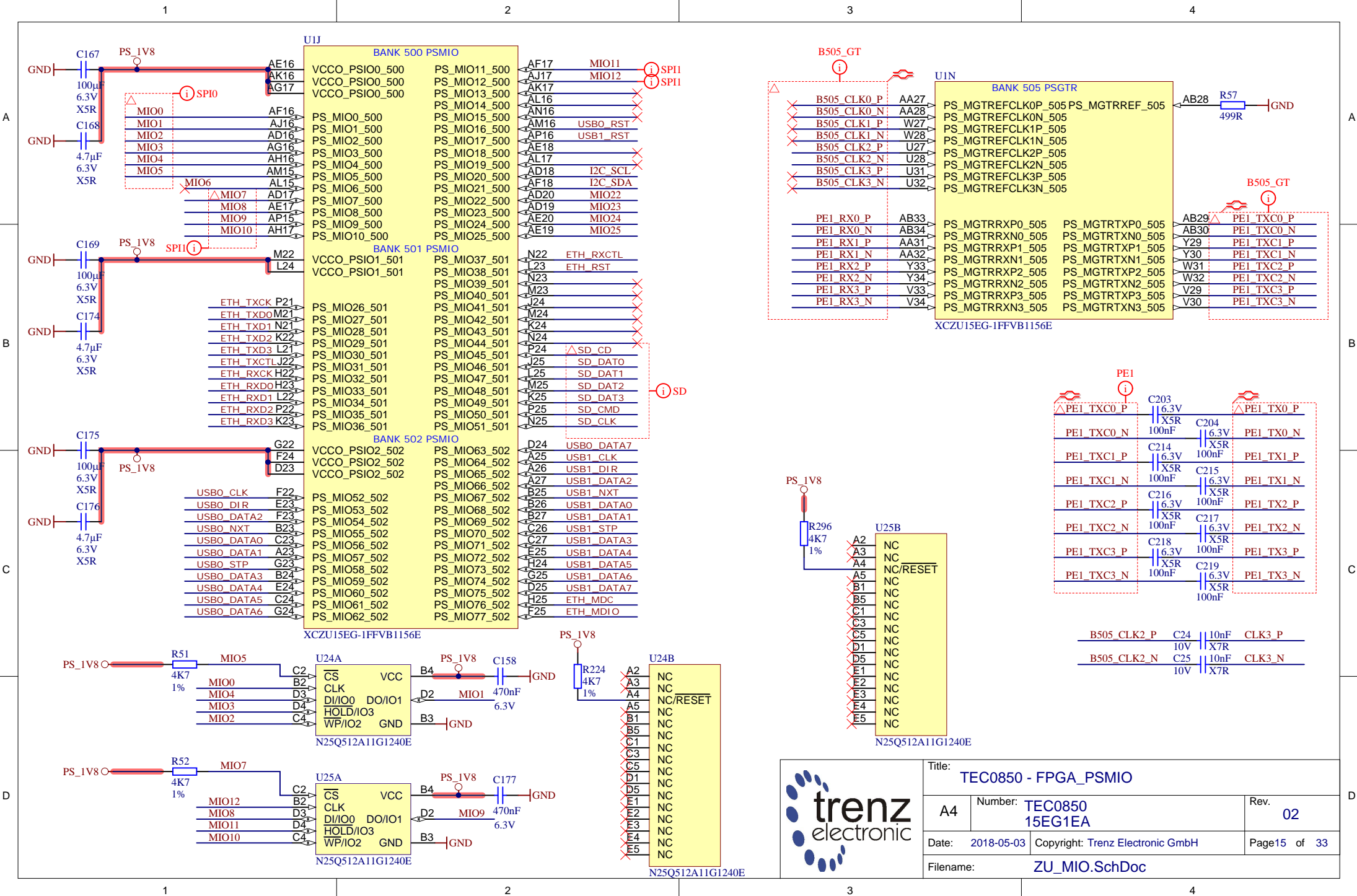
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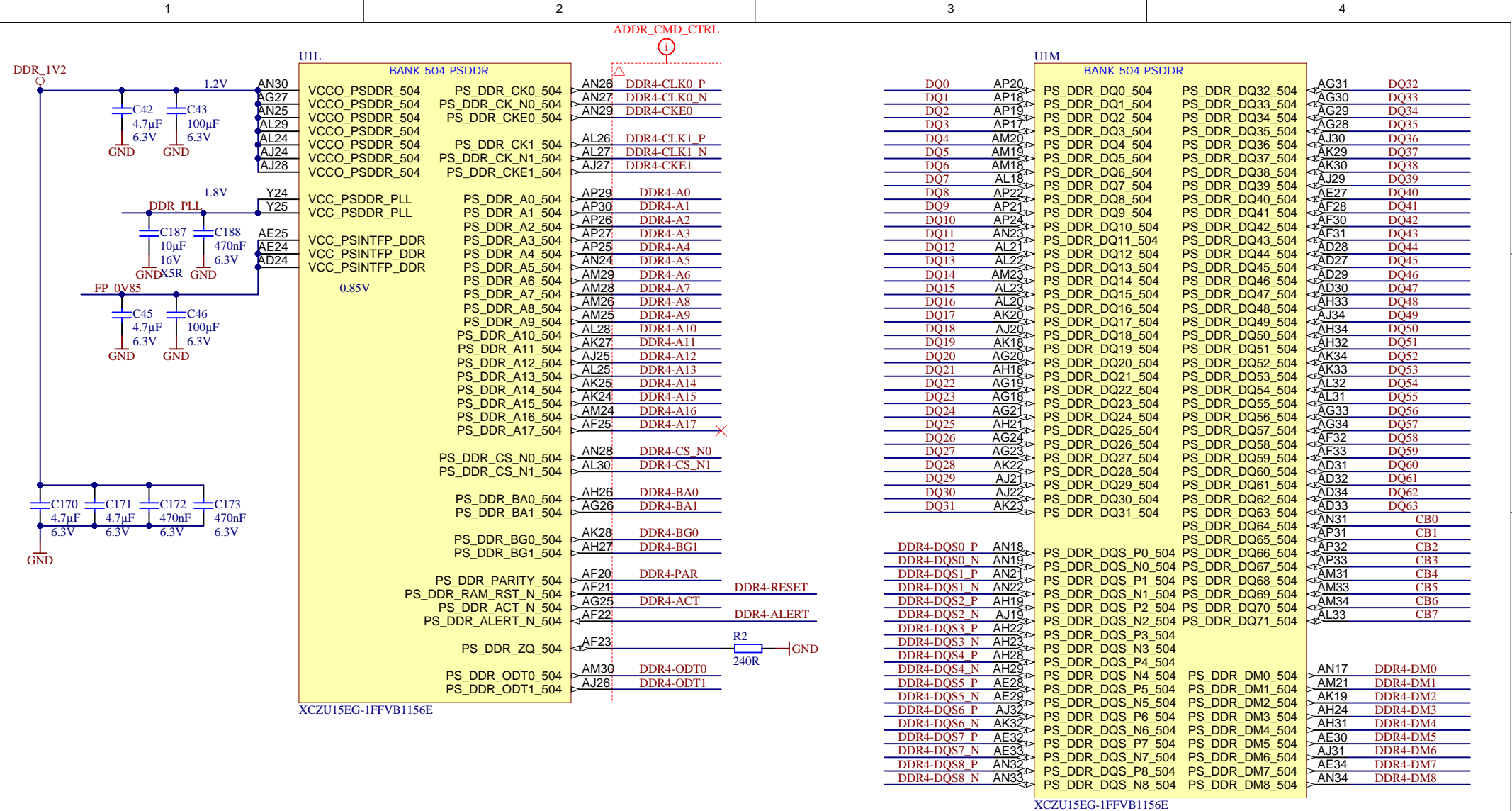
Title: TEC0850 - FPGA_MGT_R		
A4	Number: TEC0850 15EG1EA	Rev. 02
Date: 2018-05-03	Copyright: Trenz Electronic GmbH	Page 14 of 33
Filename: ZU_MGT_R.SchDoc		



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Title: **TEC0850 - FPGA_PSMIO**

A4	Number: TEC0850 15EG1EA	Rev. 02
Date: 2018-05-03	Copyright: Trenz Electronic GmbH	Page 15 of 33
Filename: ZU_MIO.SchDoc		



Title: TEC0850 - FPGA_PSDDR			
A4	Number: TEC0850 15EG1EA	Rev. 02	
Date: 2018-05-03	Copyright: Trenz Electronic GmbH		Page 16 of 33
Filename: ZU_PSDDR.SchDoc			

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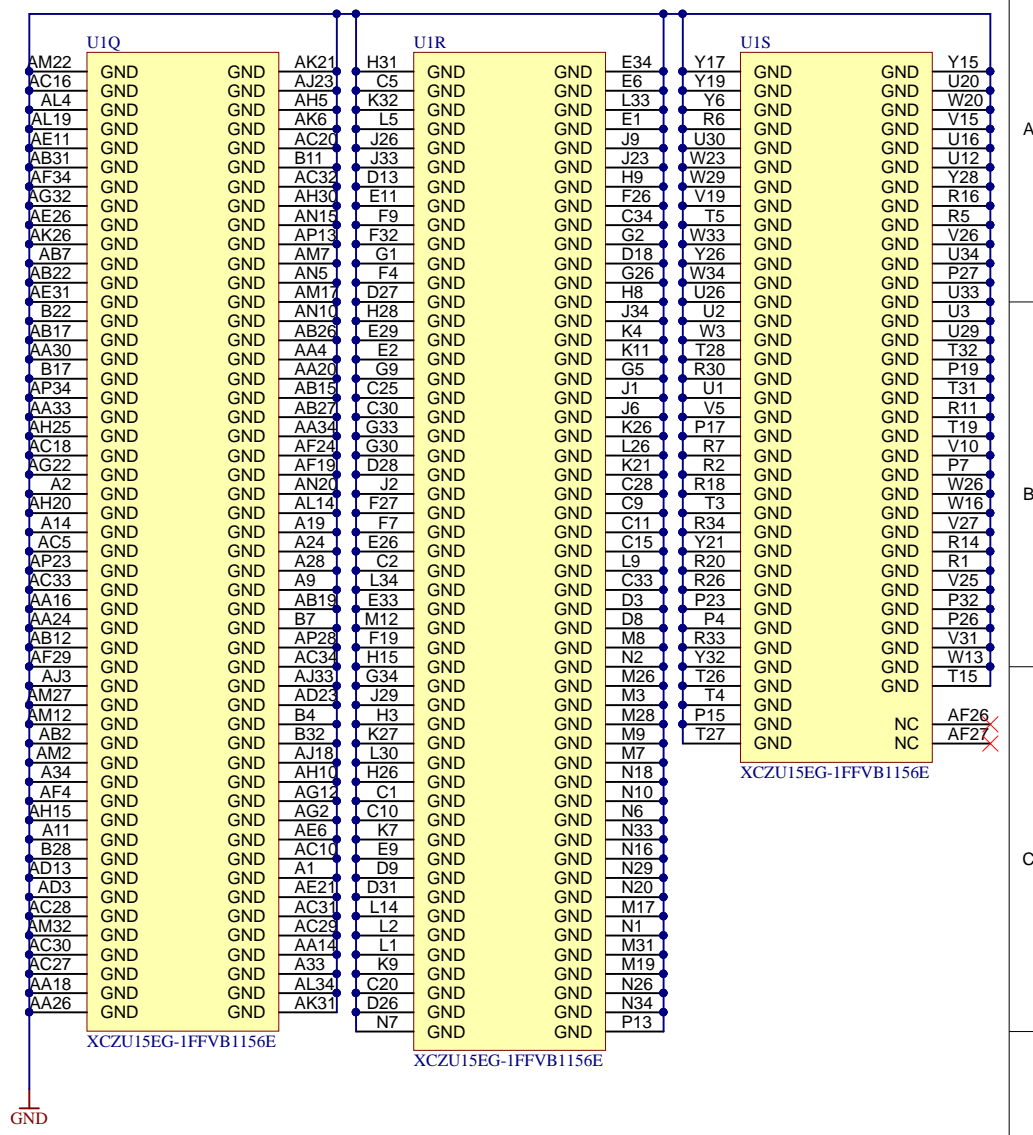
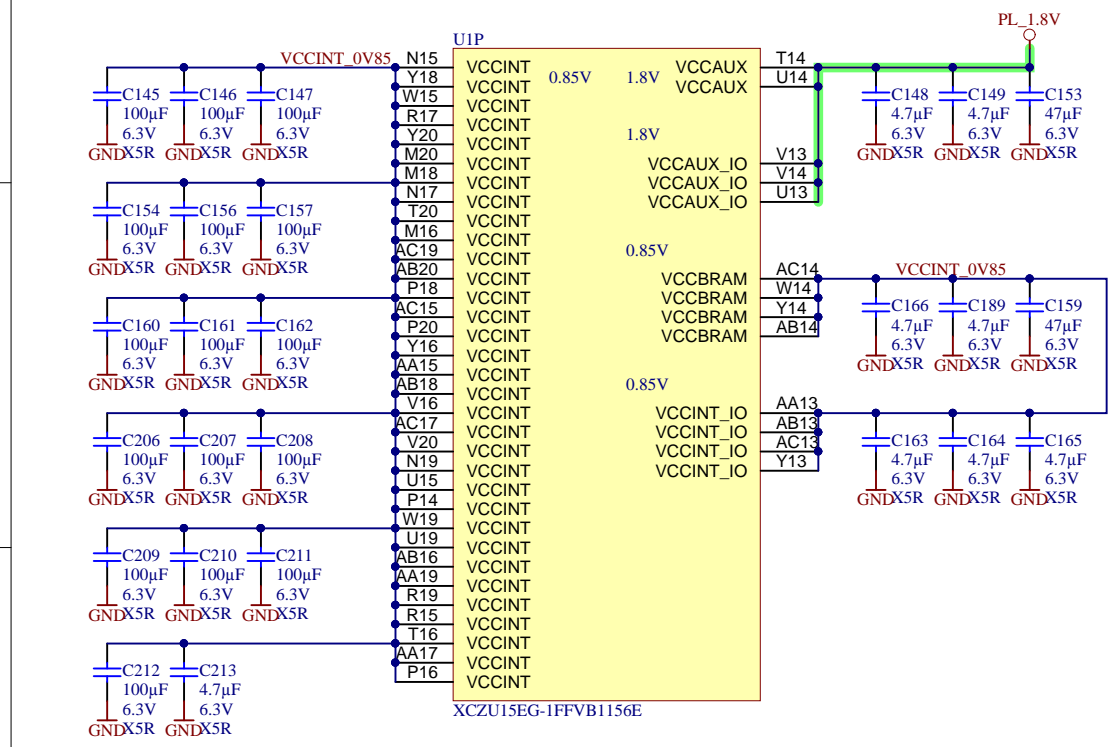
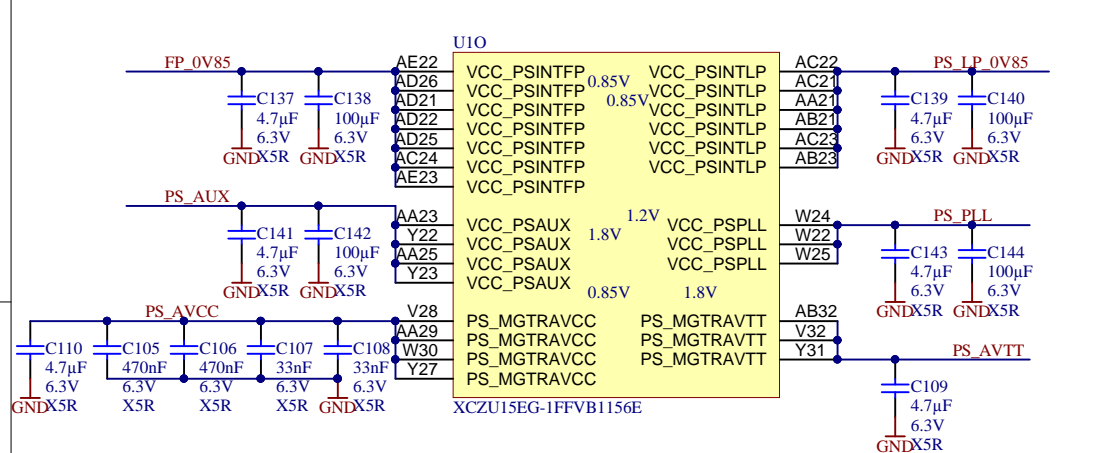
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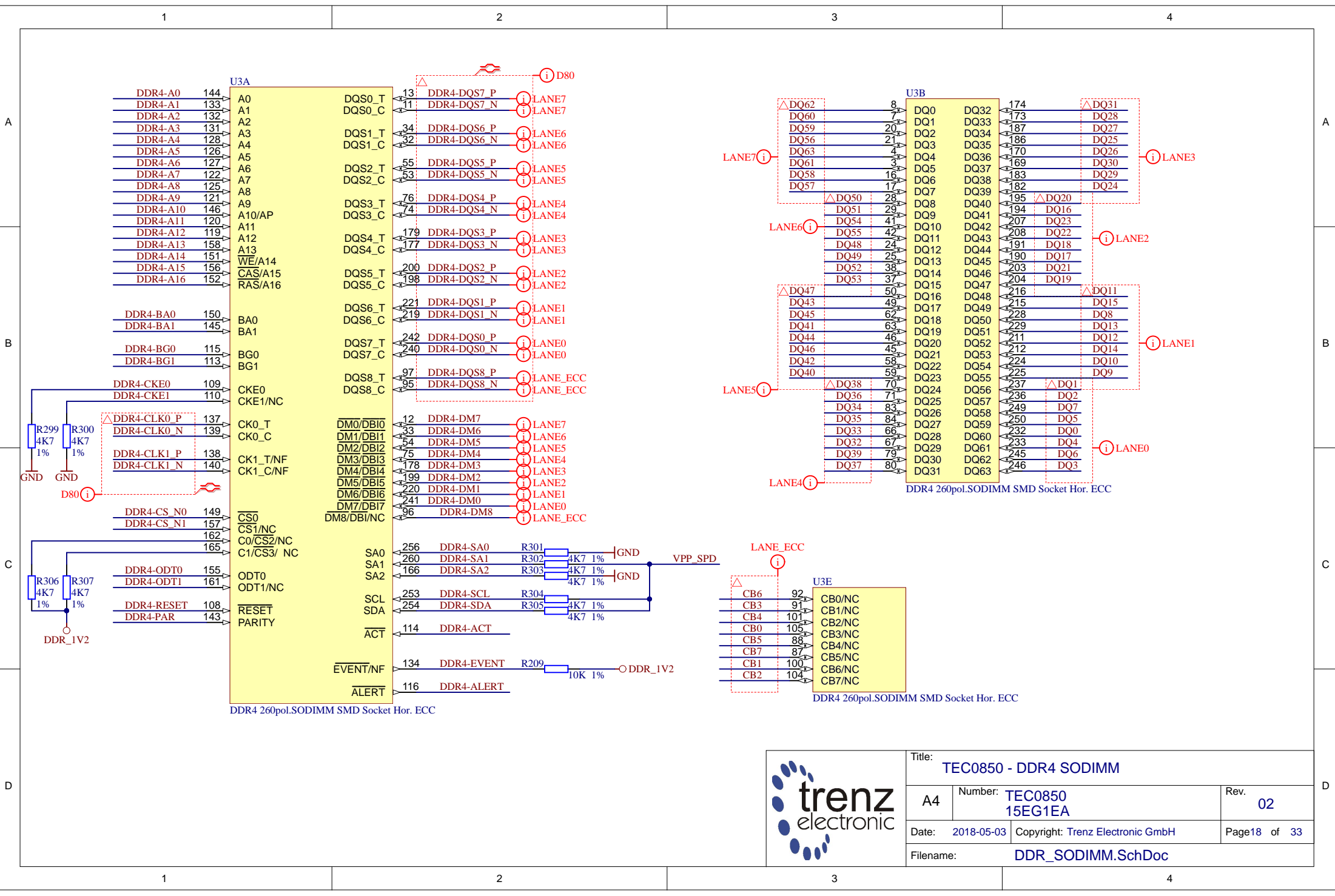
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A4	Number: TEC0850 15EG1EA	Rev. 02
Date: 2018-05-03	Copyright: Trenz Electronic GmbH	Page 17 of 33
Filename: ZU_PWR.SchDoc		


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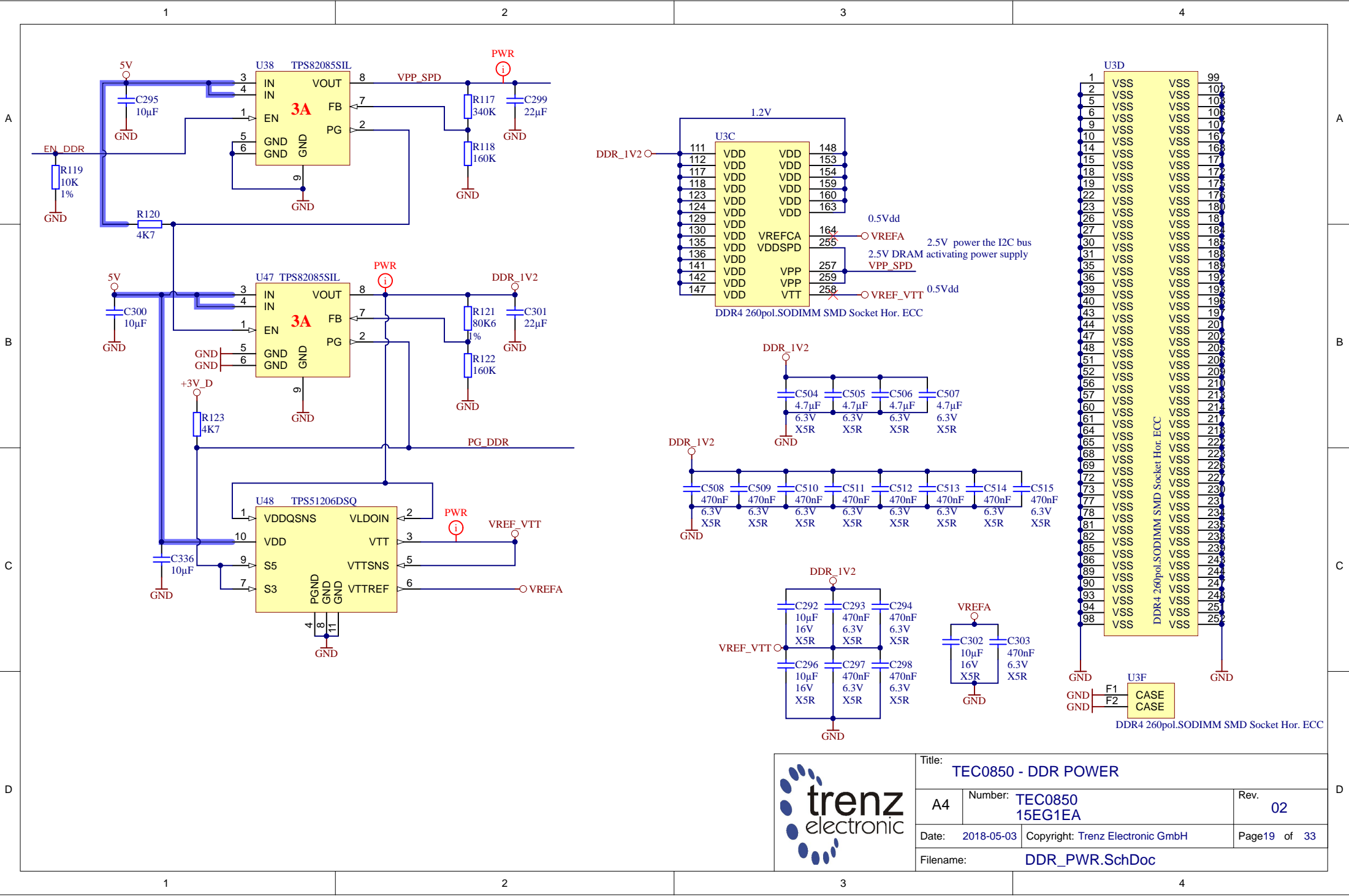
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			Title: TEC0850 - DDR4 SODIMM	
			A4	Number: TEC0850 15EG1EA
Date: 2018-05-03		Copyright: Trenz Electronic GmbH		Page 18 of 33
Filename: DDR_SODIMM.SchDoc				



Title: TEC0850 - DDR POWER		
A4	Number: TEC0850 15EG1EA	Rev. 02
Date: 2018-05-03	Copyright: Trenz Electronic GmbH	Page 19 of 33
Filename: DDR_PWR.SchDoc		

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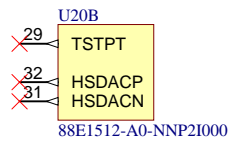
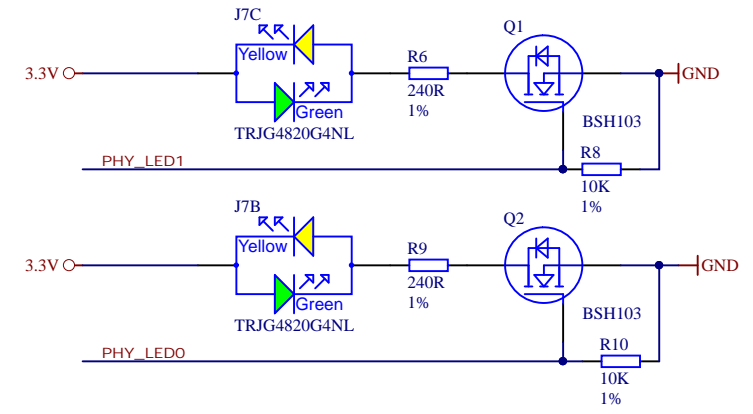
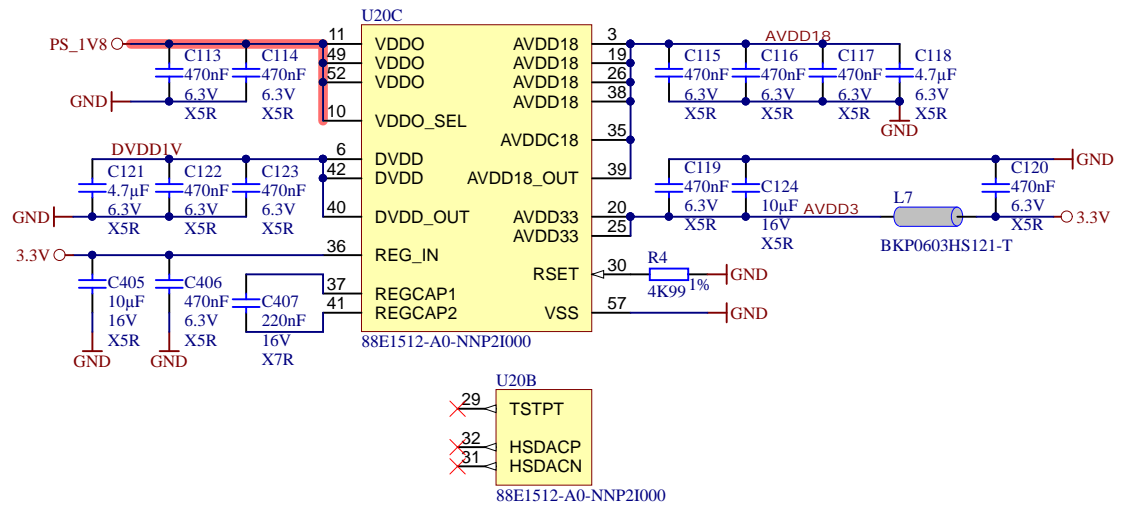
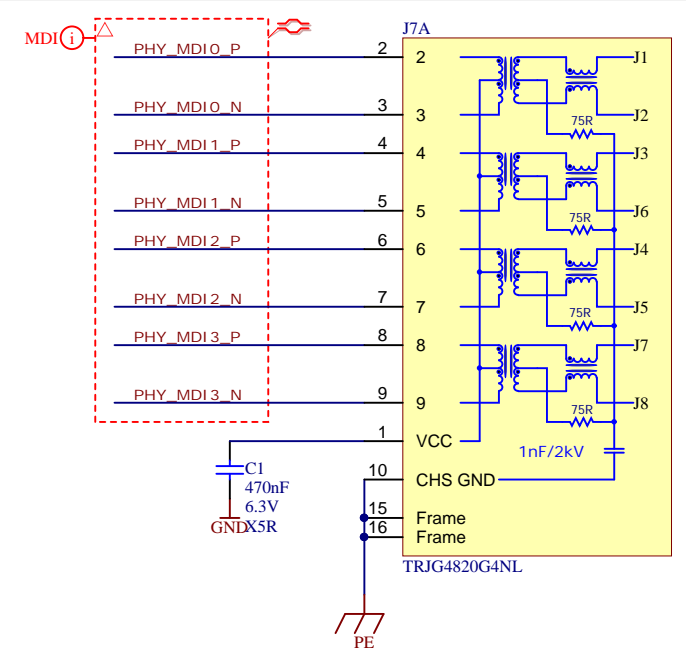
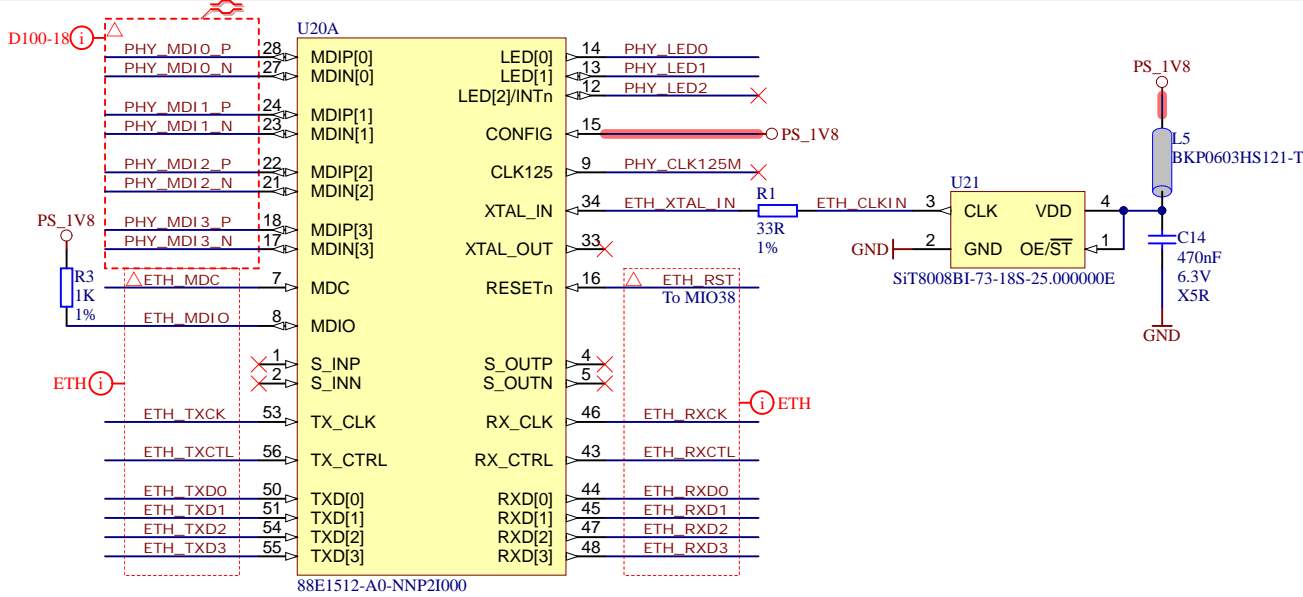
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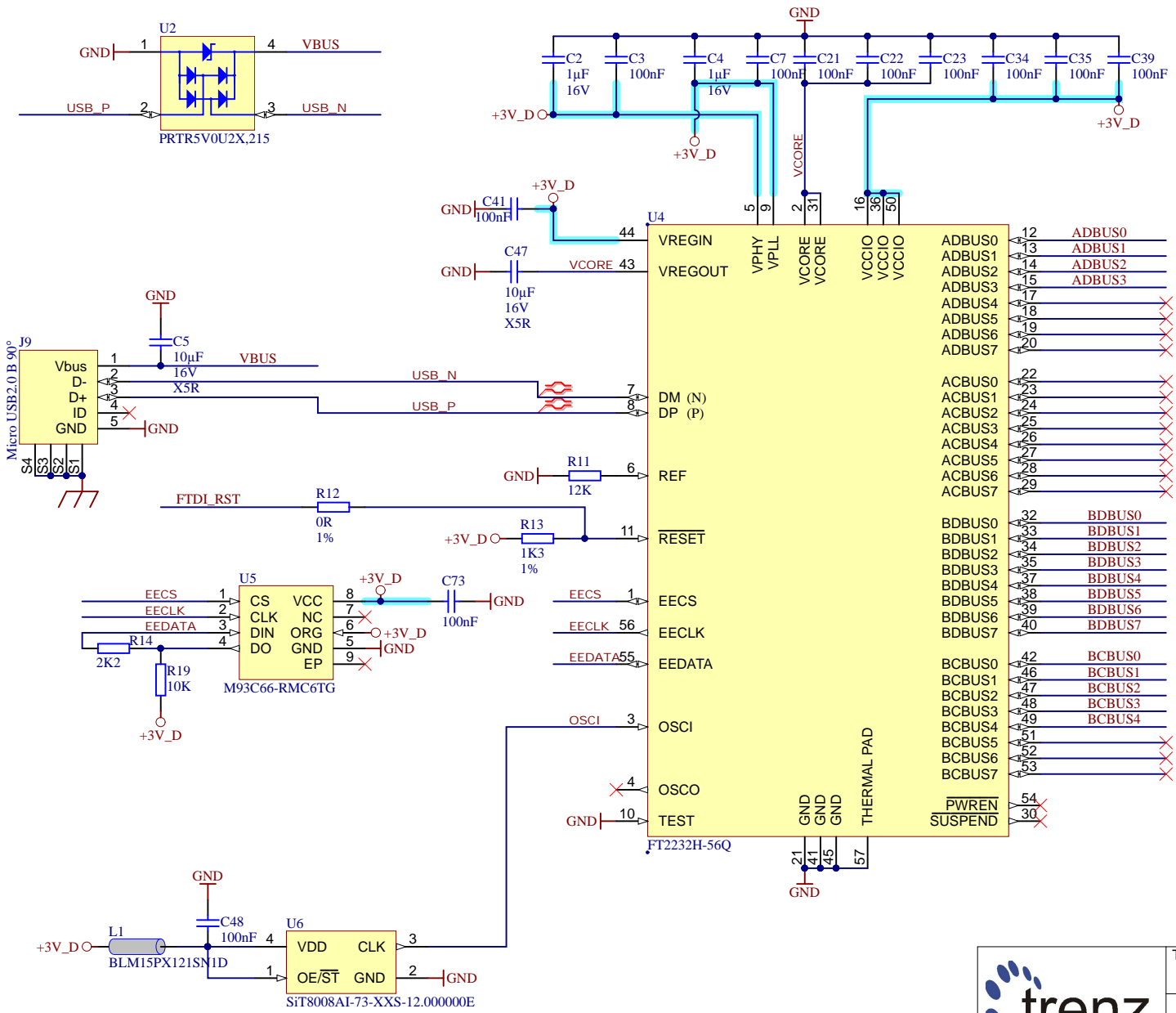
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Title: TEC0850 - ETH		
A4	Number: TEC0850 15EG1EA	Rev. 02
Date: 2018-05-03	Copyright: Trenz Electronic GmbH	Page 20 of 33
Filename: Ethernet.SchDoc		



			Title: TEC0850 - FTDI	
			A4	Number: TEC0850 15EG1EA
Date: 2018-05-03		Copyright: Trenz Electronic GmbH		Page 21 of 33
Filename: FTDI.SchDoc				

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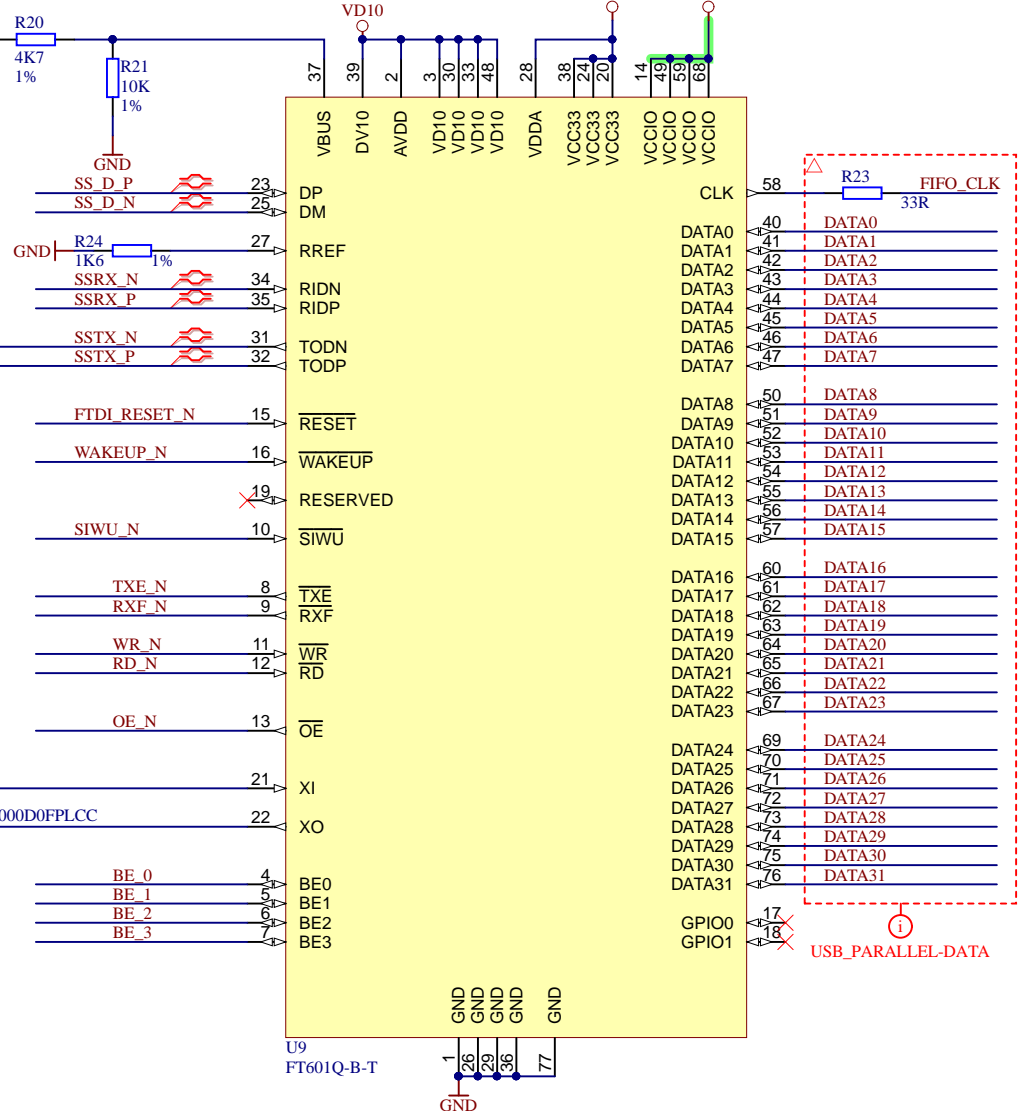
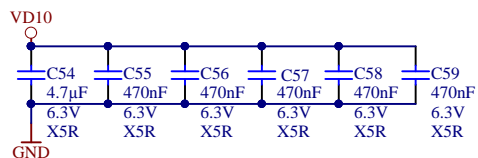
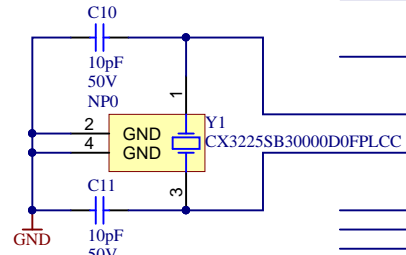
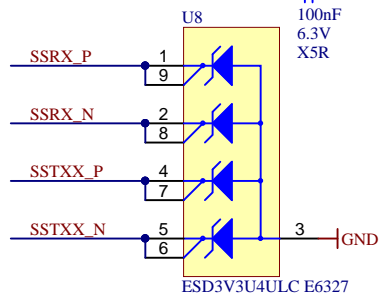
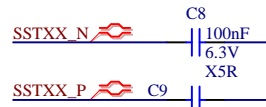
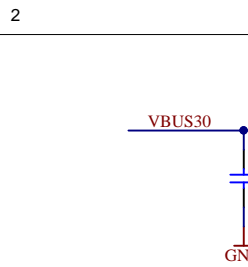
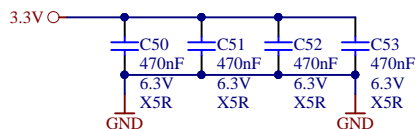
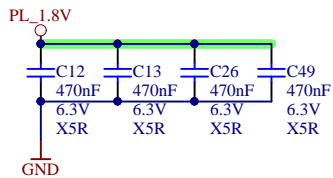
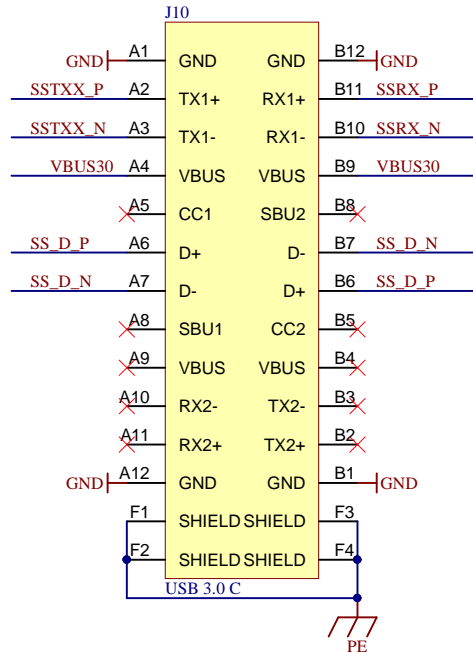
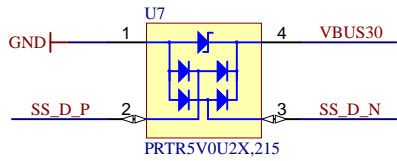
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Title: TEC0850 - USB3.0		
A4	Number: TEC0850 15EG1EA	Rev. 02
Date: 2018-05-03	Copyright: Trenz Electronic GmbH	Page 22 of 33
Filename: USB30.SchDoc		

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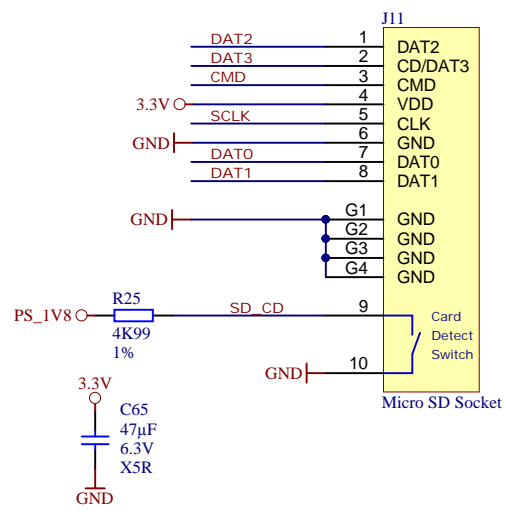
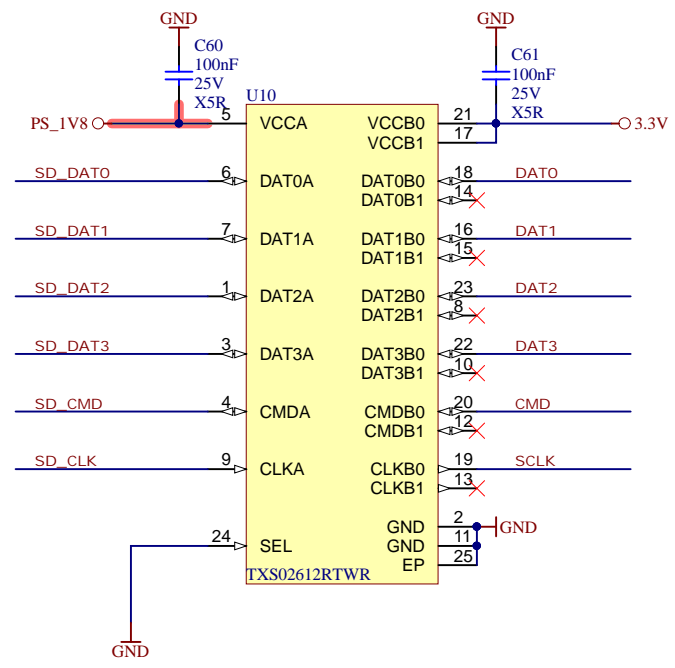
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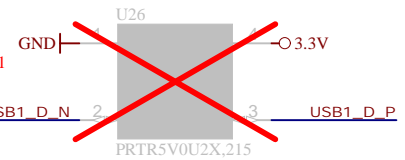
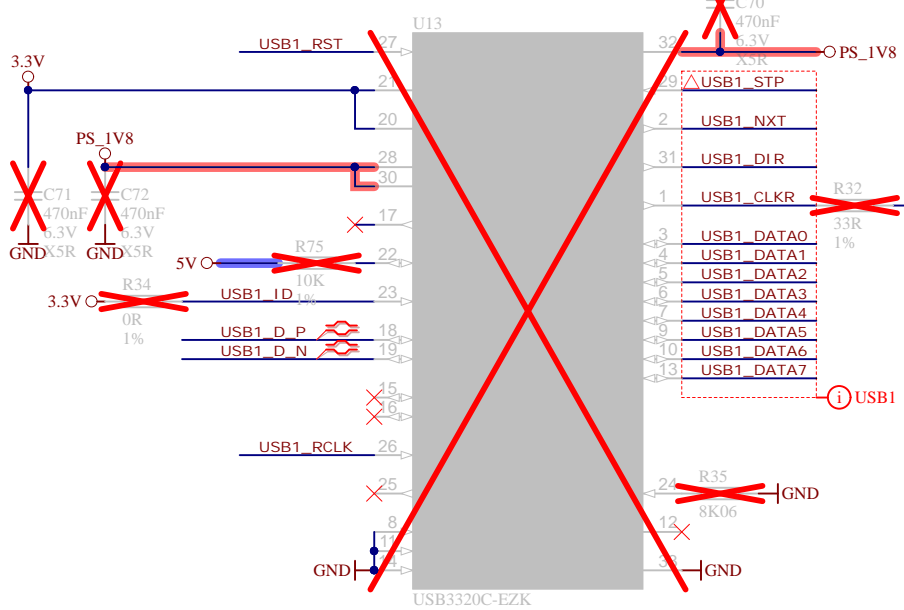
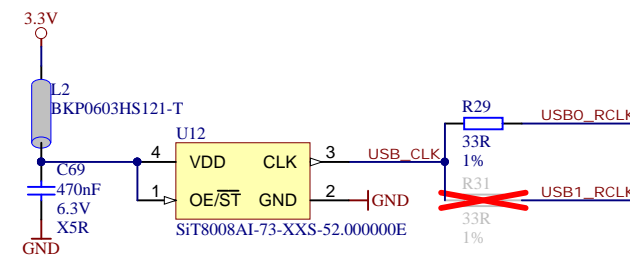
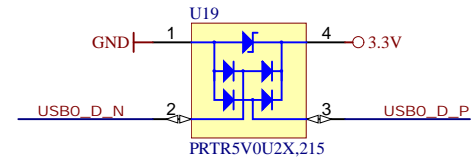
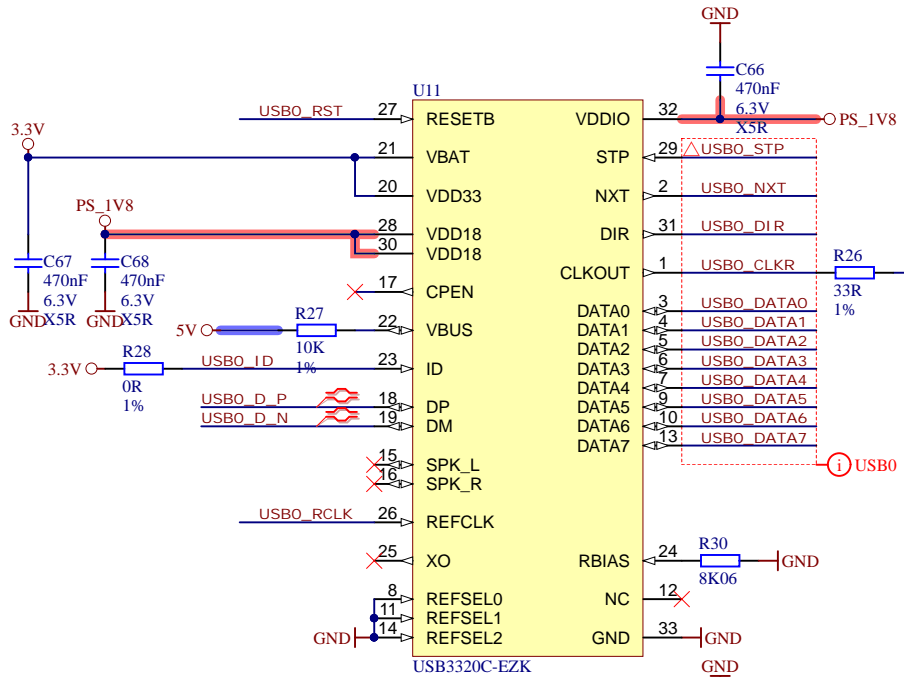
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Date: 2018-05-03		Copyright: Trenz Electronic GmbH		Page 23 of 33
Filename: SDCard.SchDoc				

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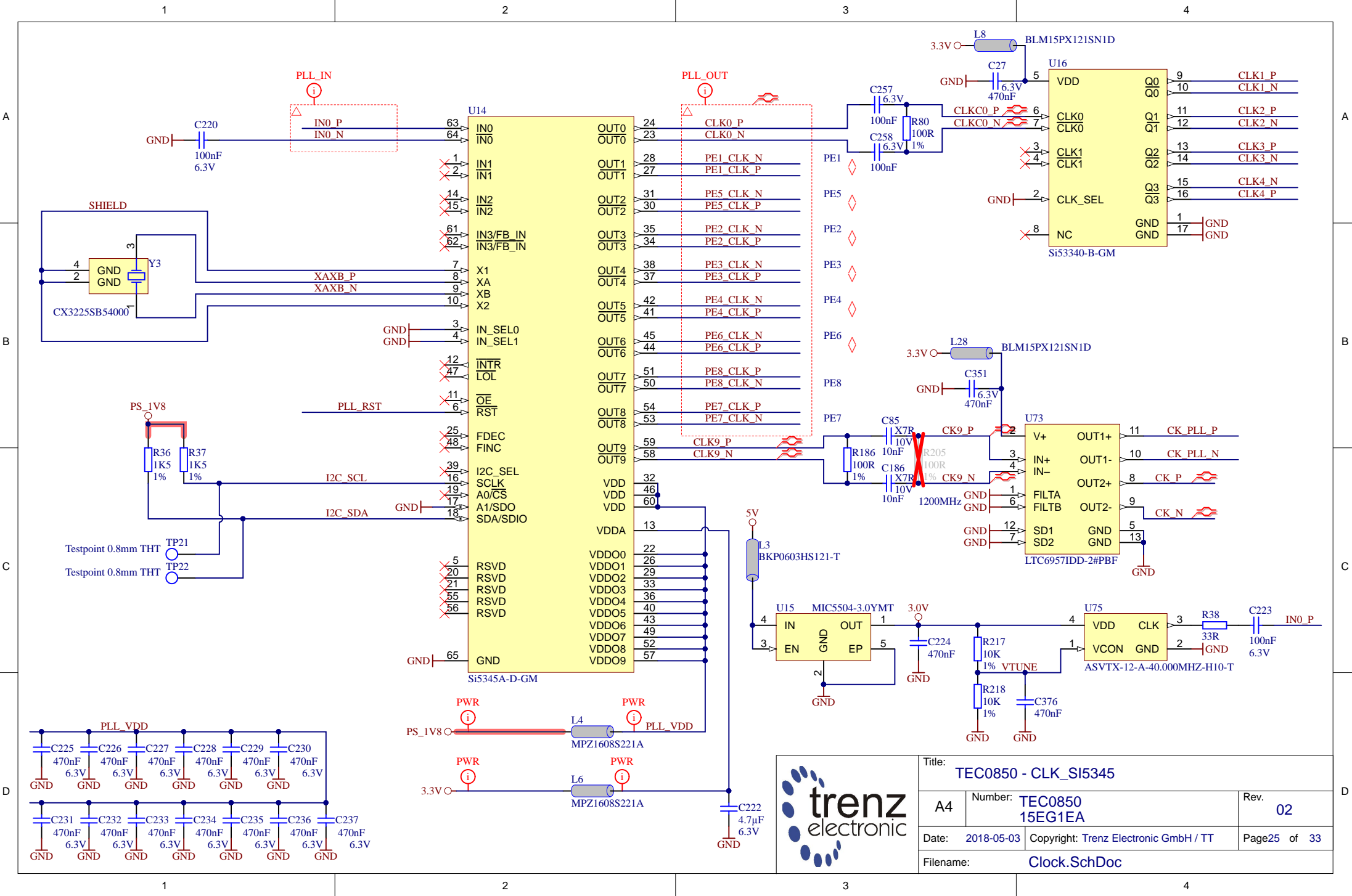
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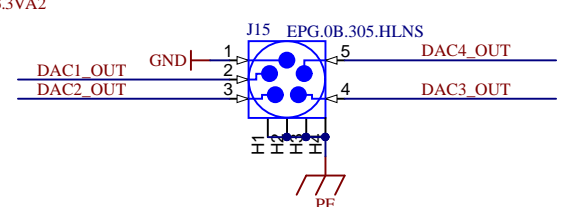
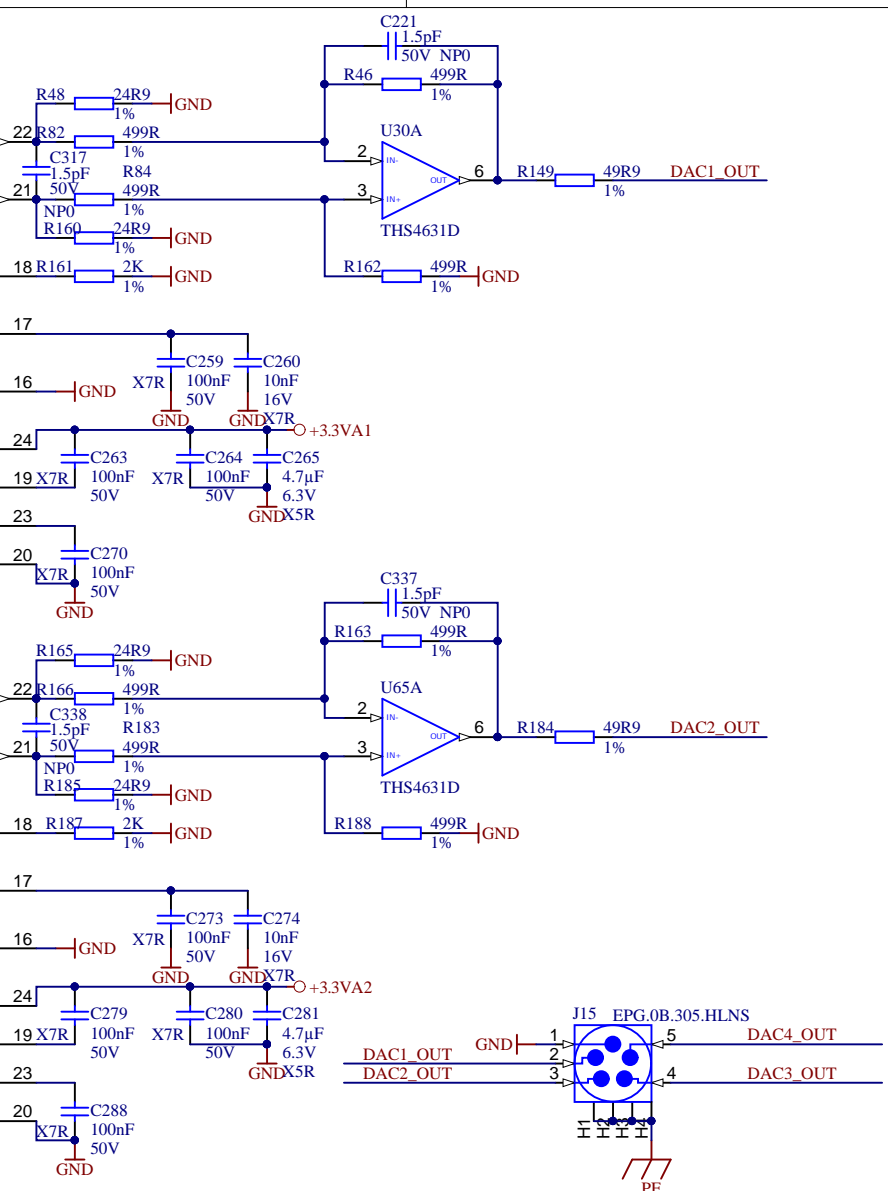
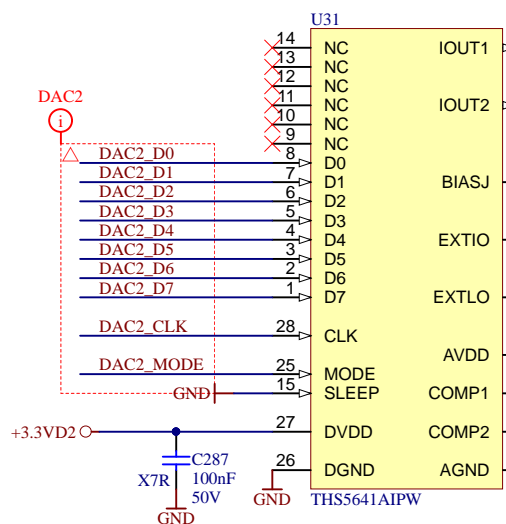
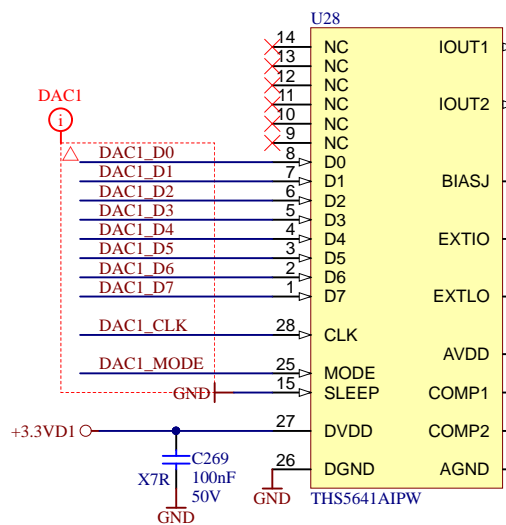
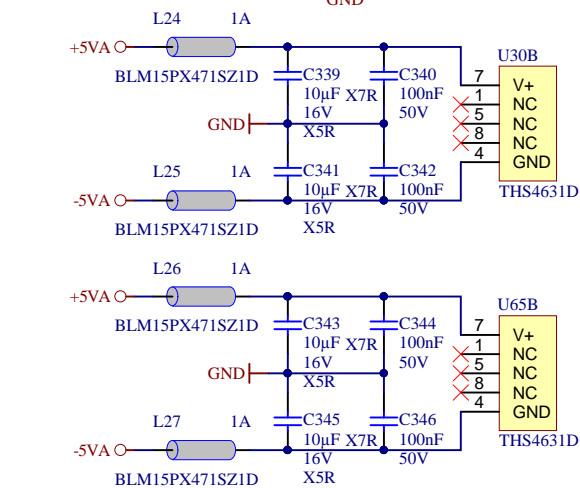
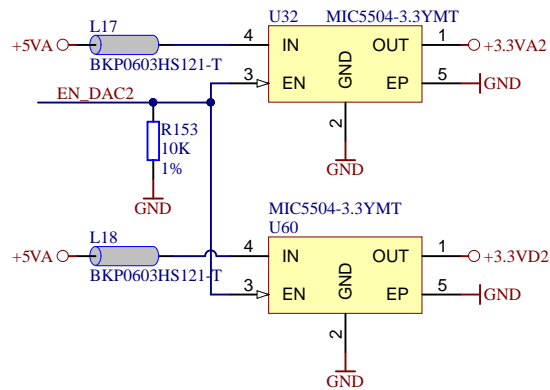
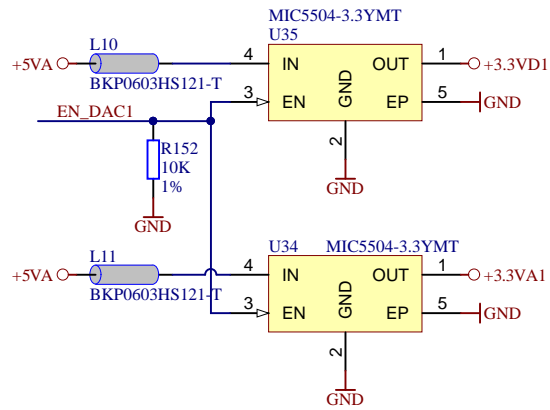
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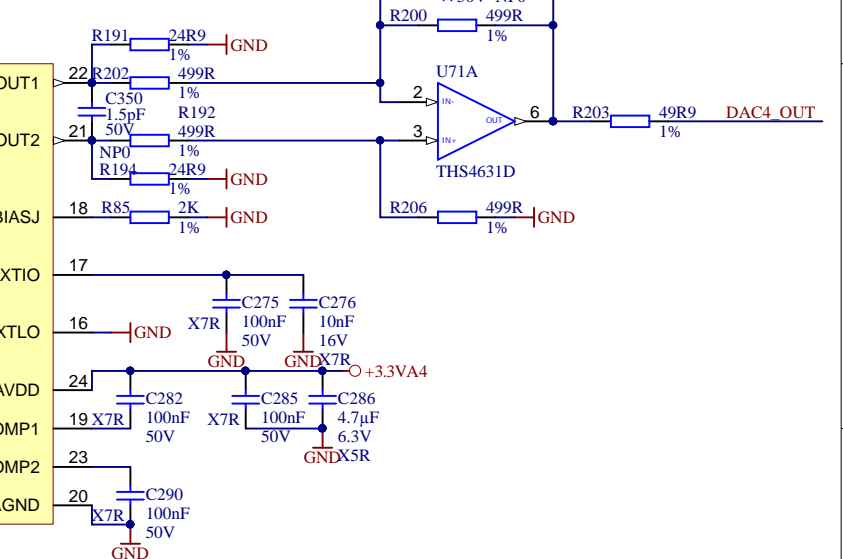
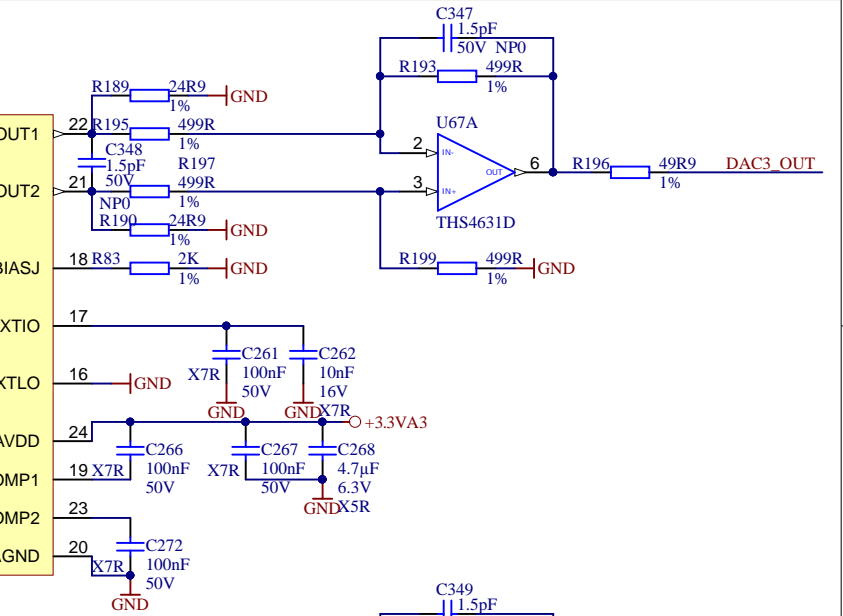
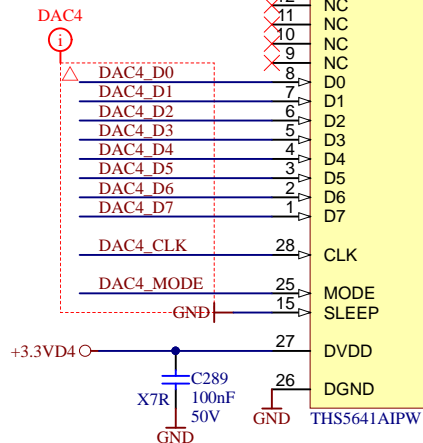
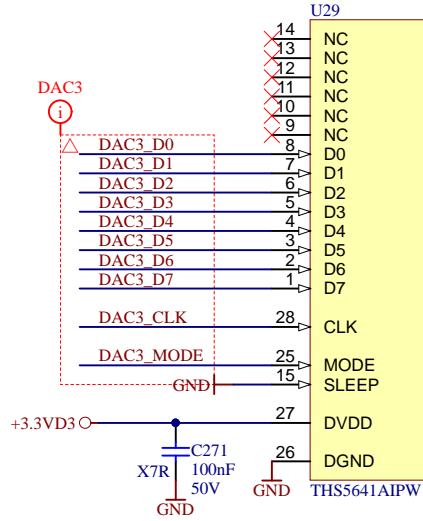
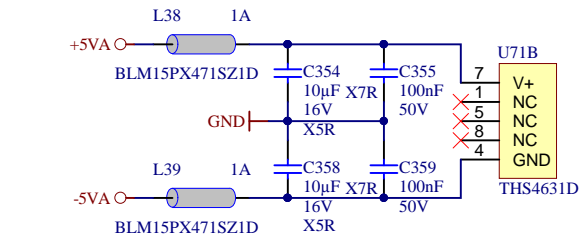
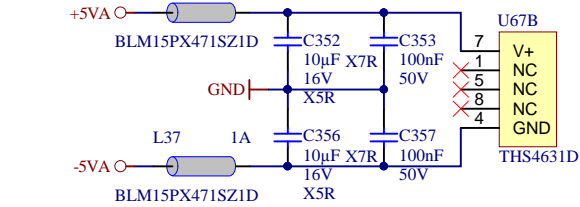
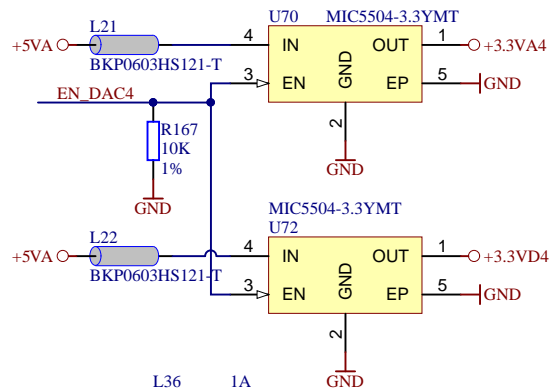
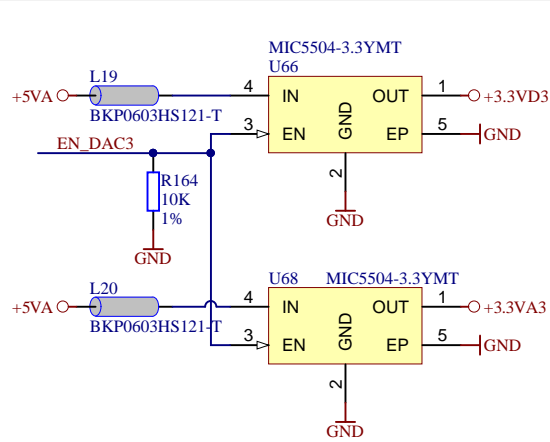
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Date: 2018-05-03	Copyright: Trenz Electronic GmbH	Page 24 of 33
Filename: USB-PHY.SchDoc		



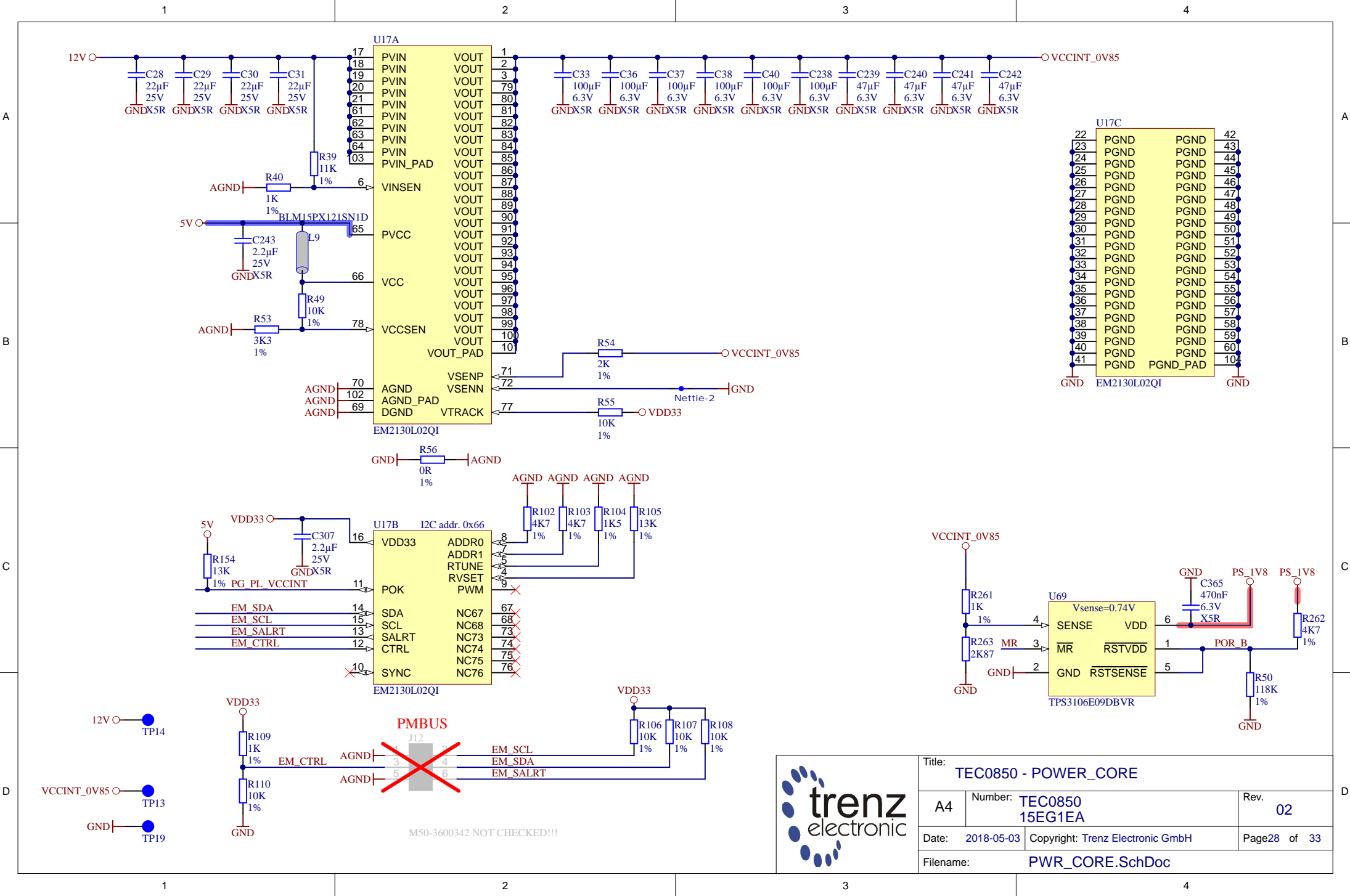
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A4	Number: TEC0850 15EG1EA	Rev. 02		
Date: 2018-05-03		Copyright: Trenz Electronic GmbH / TT		Page 25 of 33
Filename:		Clock.SchDoc		



			Title: TEC0850 - DAC1_DAC2	
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Date: 2018-05-03		Copyright: Trenz Electronic GmbH		Page 26 of 33
Filename: DAC12_8bit.SchDoc				

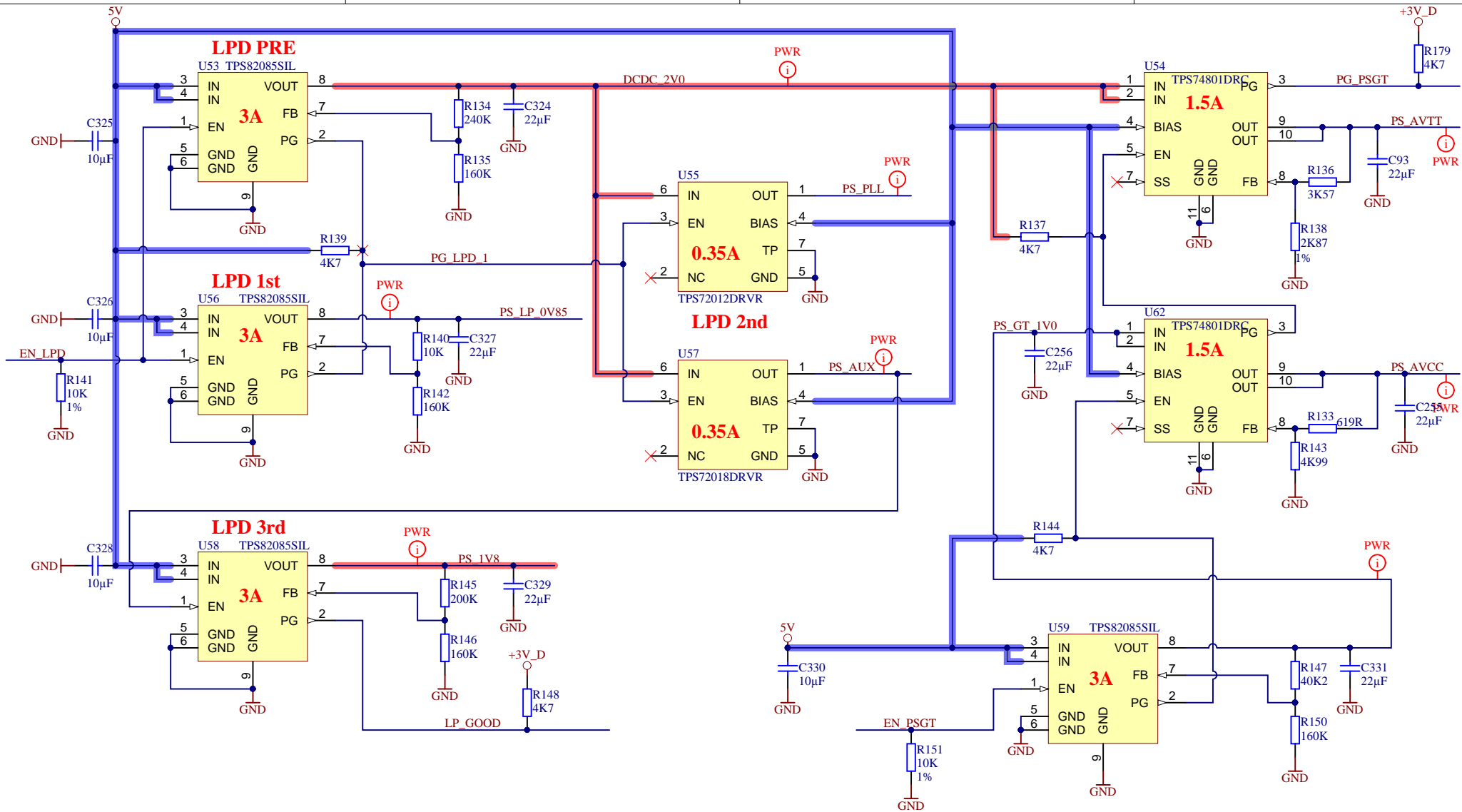



Title: TEC0850 - DAC3_DAC4		
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Date: 2018-05-03	Copyright: Trenz Electronic GmbH	Page 27 of 33
Filename: DAC34_8bit.SchDoc		

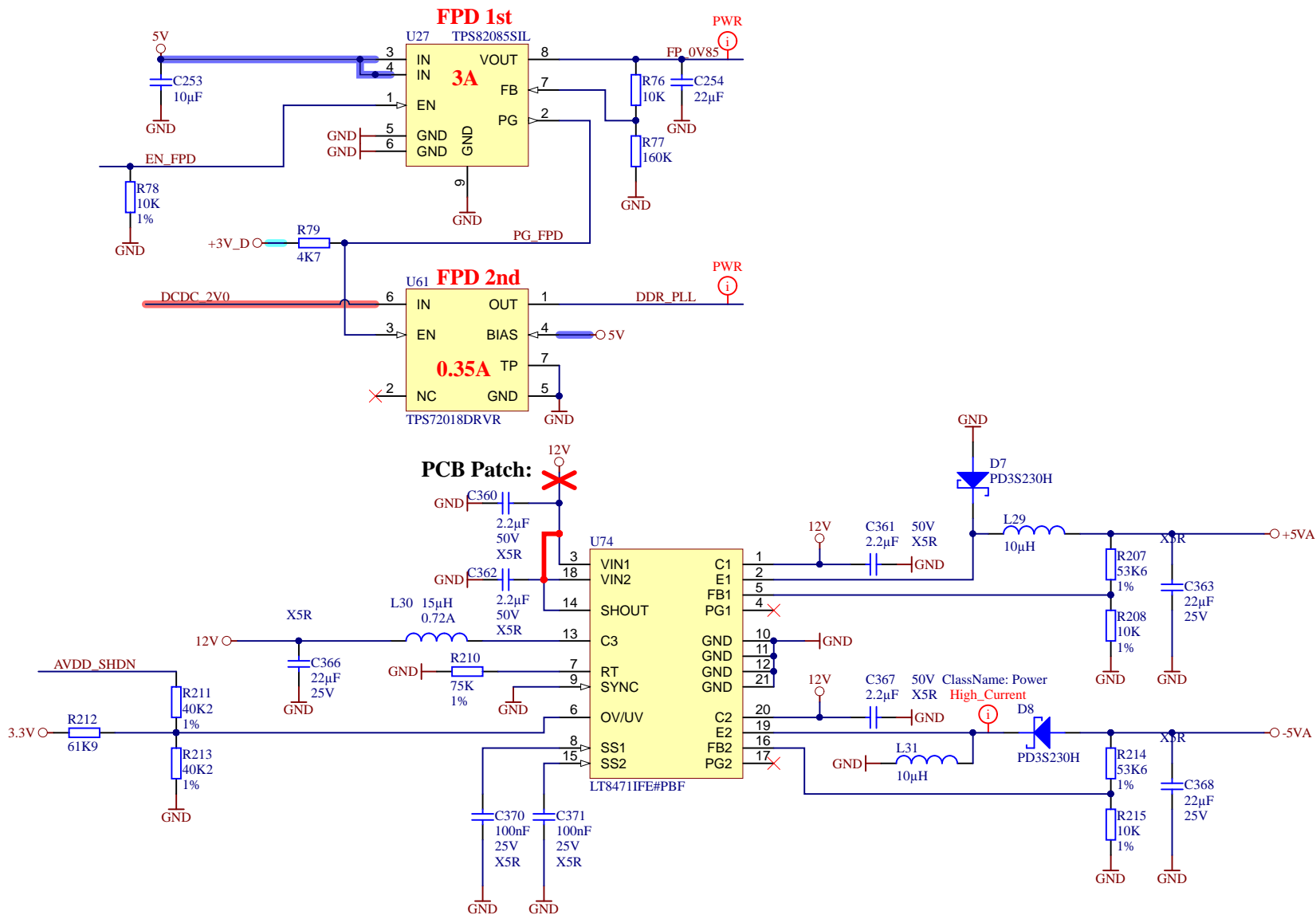


Title: TEC0850 - POWER_CORE		
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Date: 2018-05-03	Copyright: Trenz Electronic GmbH	Page 28 of 33
Filename: PWR_CORE.SchDoc		

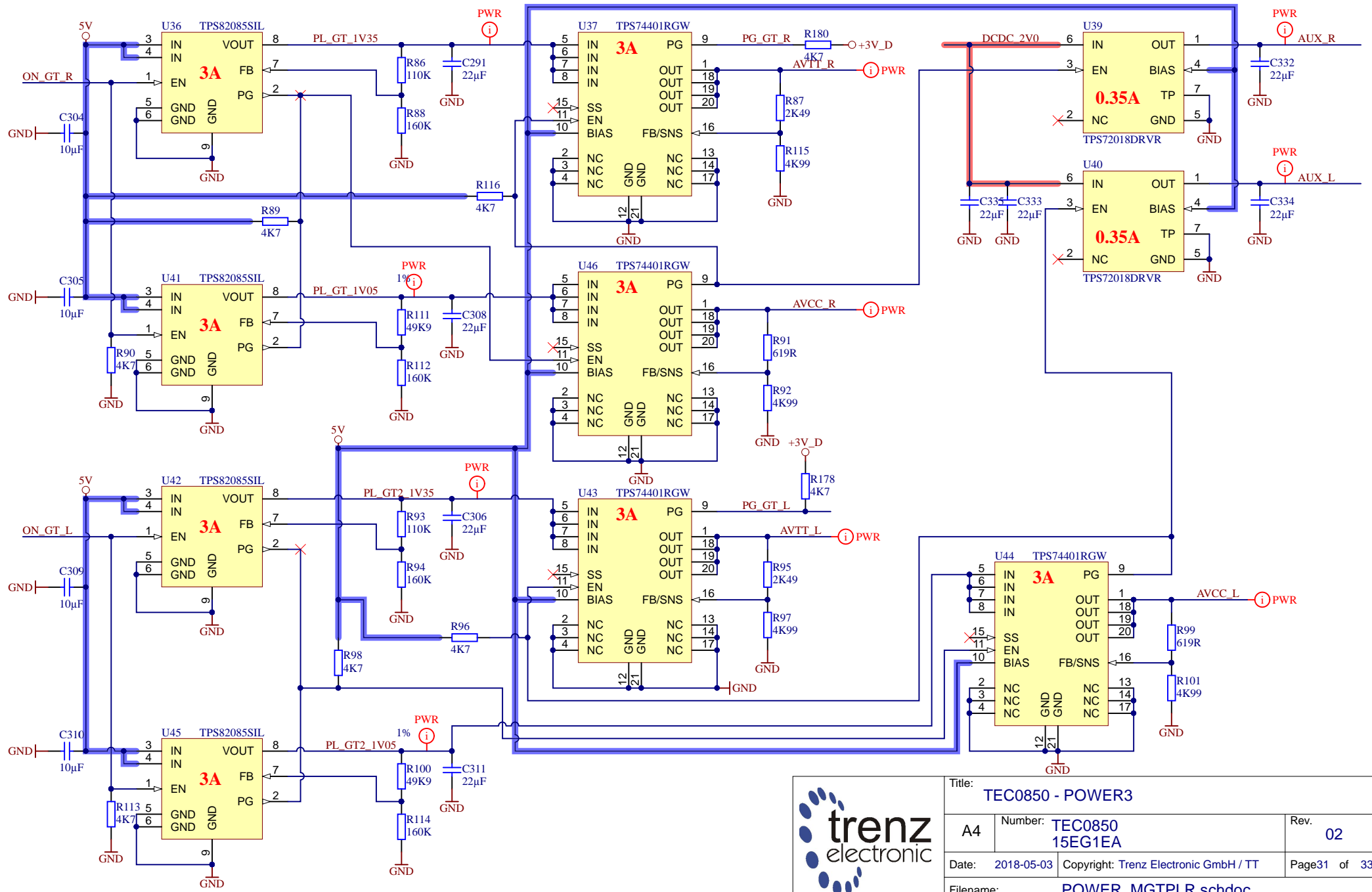
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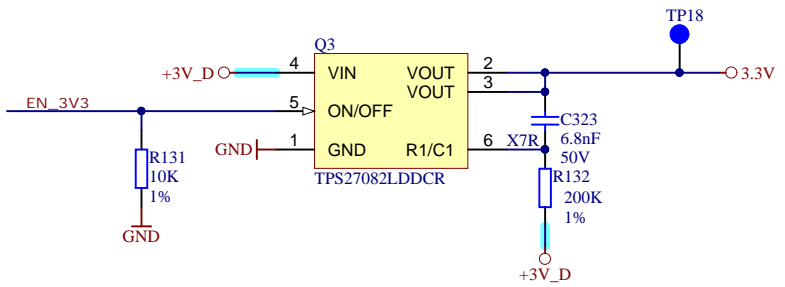
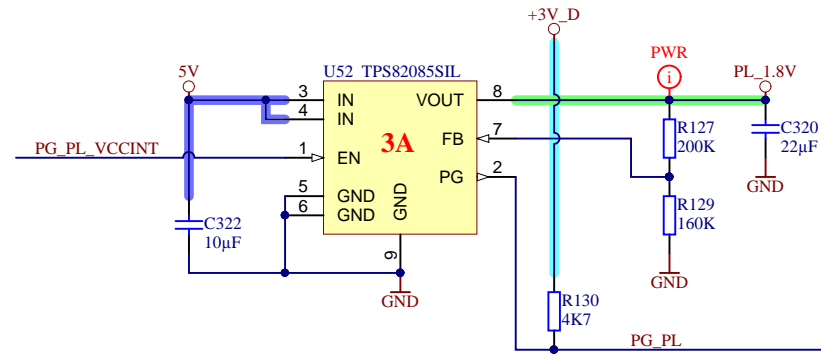
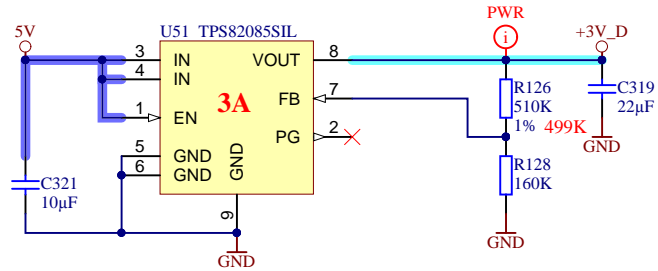
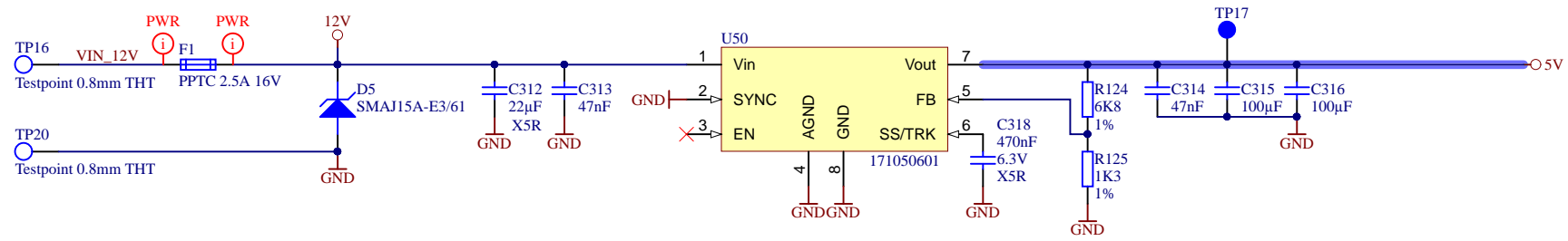
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Date: 2018-05-03		Copyright: Trenz Electronic GmbH / TT		Page 29 of 33
Filename: POWER_PSLP.schdoc				




Title: TEC0850 - POWER2		
A4	Number: TEC0850 15EG1EA	Rev. 02
Date: 2018-05-03	Copyright: Trenz Electronic GmbH / TT	Page 30 of 33
Filename: POWER_PSFP.schdoc		



Title: TEC0850 - POWER3		
A4	Number: TEC0850 15EG1EA	Rev. 02
Date: 2018-05-03	Copyright: Trenz Electronic GmbH / TT	Page 31 of 33
Filename: POWER_MGTPLR.schdoc		



	Title: TEC0850 - POWER4		
	A4	Number: TEC0850 15EG1EA	Rev. 02
	Date: 2018-05-03	Copyright: Trenz Electronic GmbH / TT	Page 32 of 33
	Filename: POWER_MGTPLL.schdoc		

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CHANGES REV01 to REV02

- 1) Fixed connection for U16 (Si53340-B-GM)
- 2) Added THT-testpoints for I2C-bus
- 3) Changed MEMS osc to TCXO osc , added LDO for TCXO osc
- 4) Use out9 from PLL, added dual output buffer ("1" -> MPSOC, B65; "2" -> J1, cPCI-serial)
- 5) Changed connector J12 (do not populated)
- 6) Added capacitors C372, C373 on the clock line (AC-coupling)
- 7) Changed OPs for DACs (LT6200IS6 -> THS4631D)
- 8) Added additional DCDC (+/-5V) for THS4631D
- 9) Added THT-testpoints for VIN/GND
- 10) full update lib

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		Title: TEC0850 - Changes list		
		A4	Number: TEC0850 15EG1EA	Rev. 02
		Date: 2018-05-03	Copyright: Trenz Electronic GmbH	Page 33 of 33
		Filename: Revision_Changes.SchDoc		

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