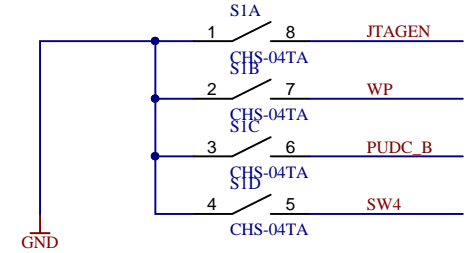
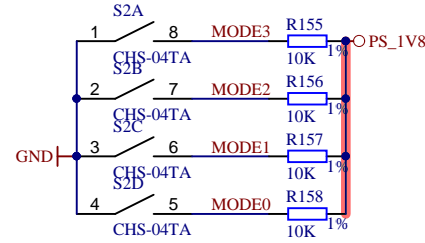
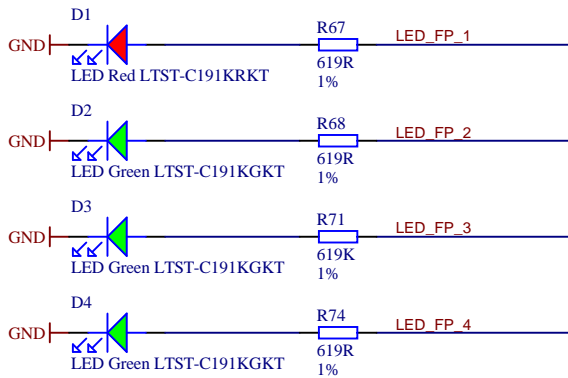
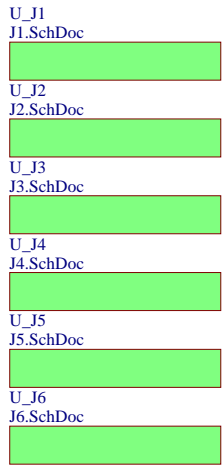
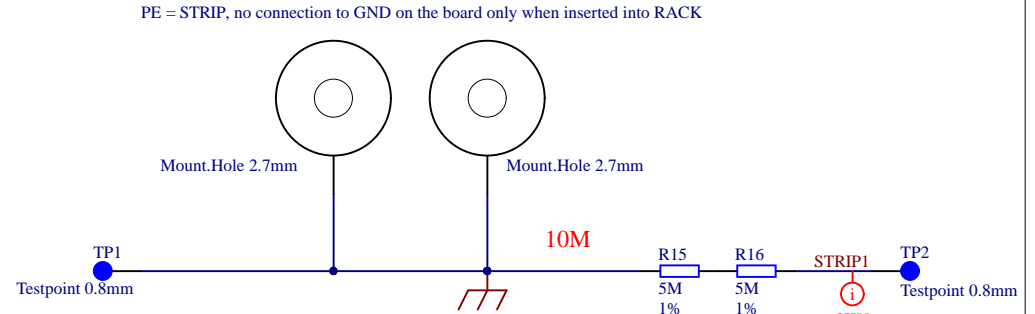
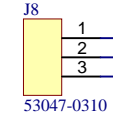
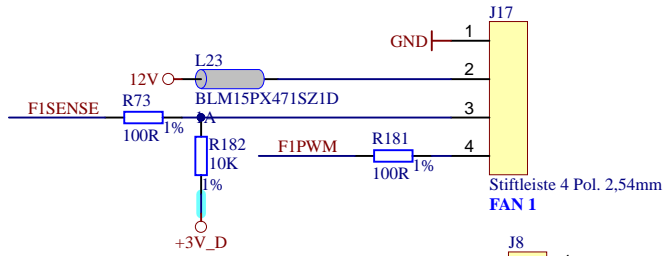
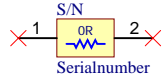


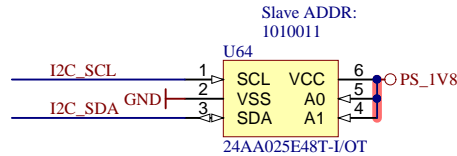
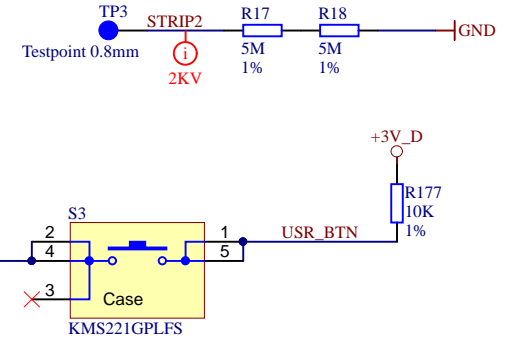
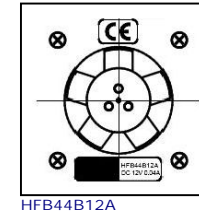
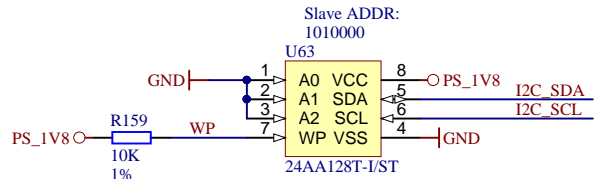
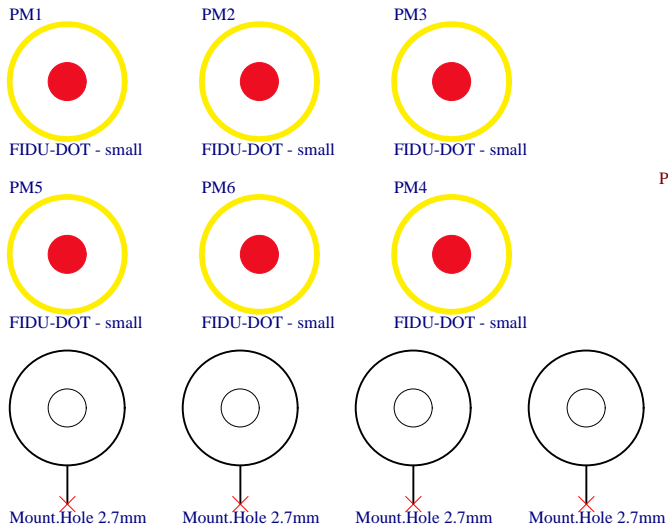
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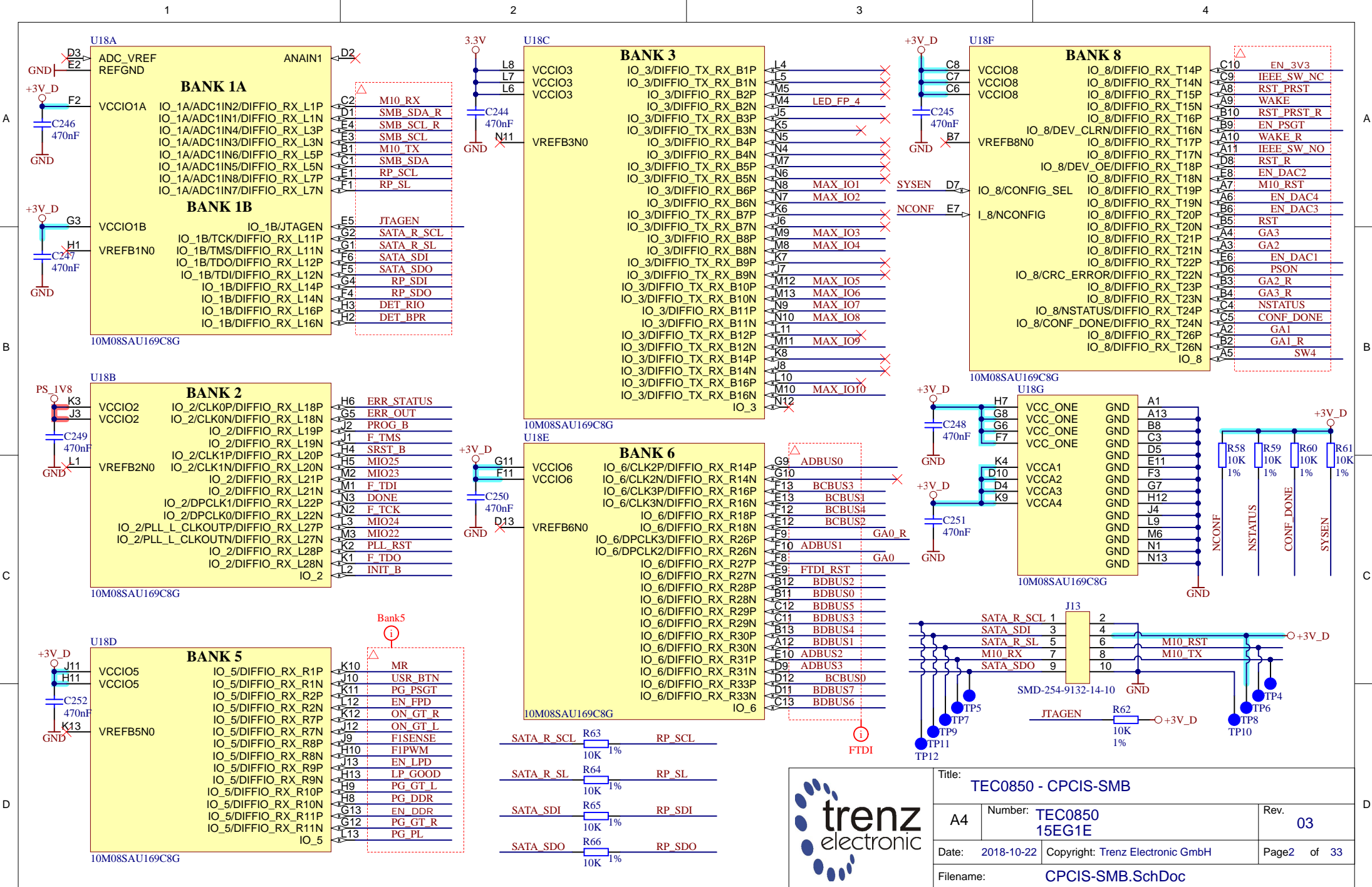
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| Title: TEC0850 - CPCIS-MAIN | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
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| Filename: CPCIS-MAIN.SchDoc | | |

A

B

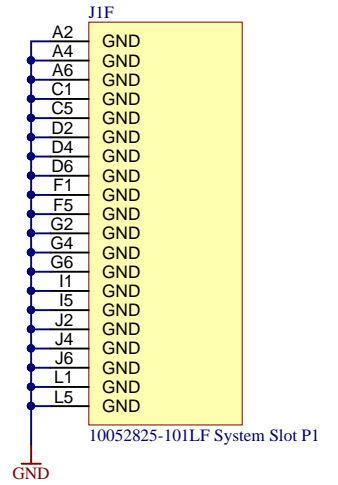
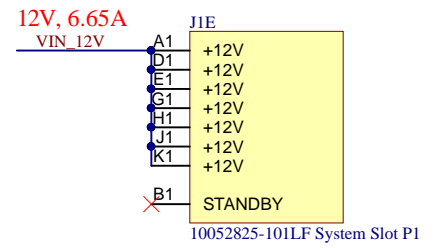
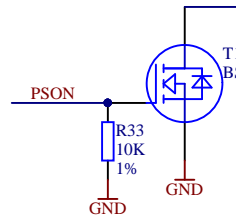
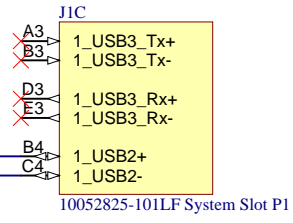
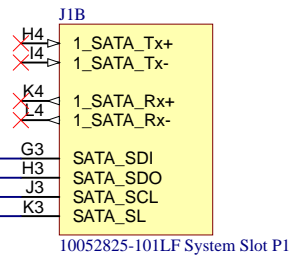
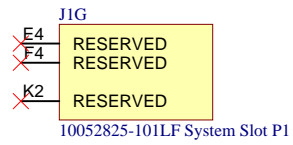
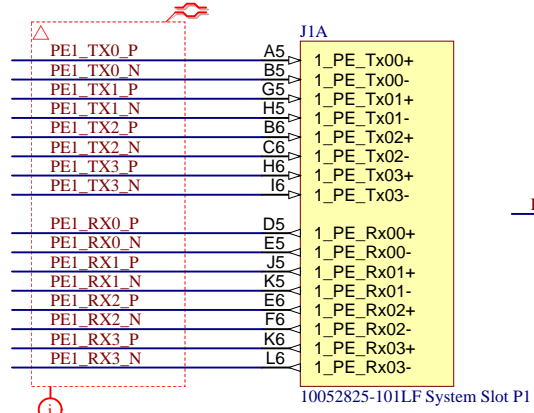
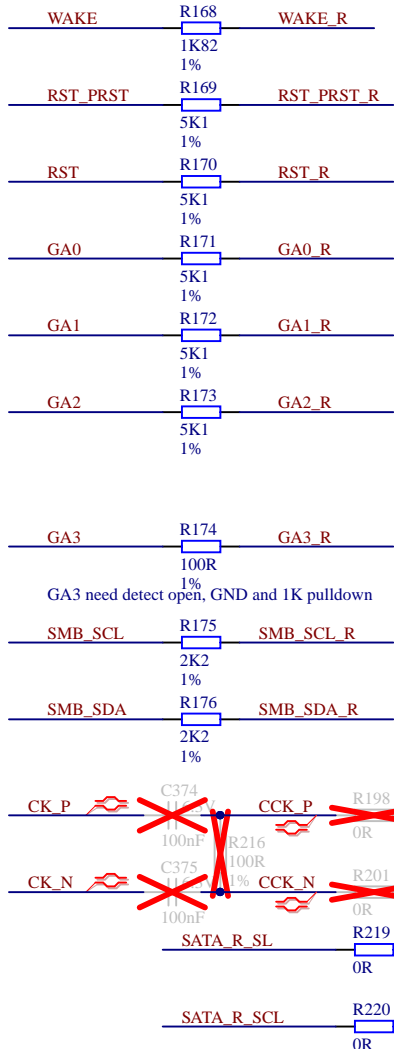
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| Title: TEC0850 - CPCIS-SMB | | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 | |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page2 of 33 | |
| Filename: CPCIS-SMB.SchDoc | | | |

1.8, 2.2 and 5.1K are REQUIRED BY CPCI-S do not optimize to other values



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|---------------------|----------------------------------|-------------|
| Title: TEC0850 - J1 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
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| Filename: J1.SchDoc | | |

1

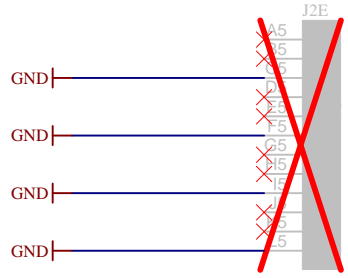
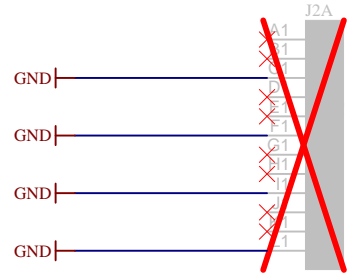
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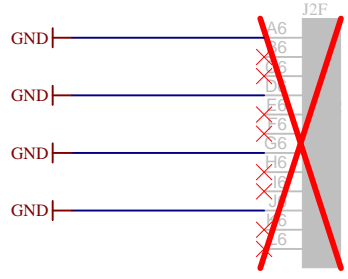
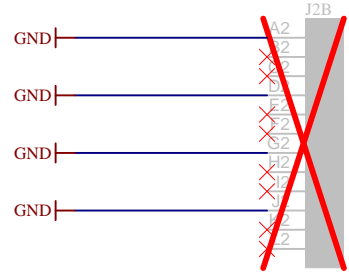
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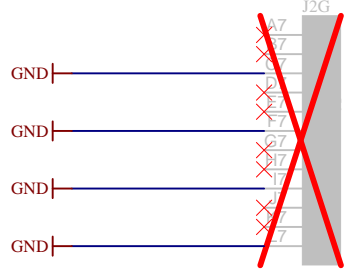
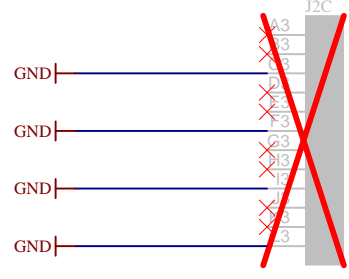
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B



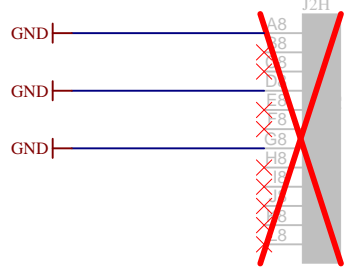
C

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| Title: TEC0850 - J2 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
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| Filename: J2.SchDoc | | |

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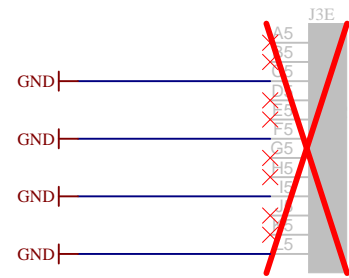
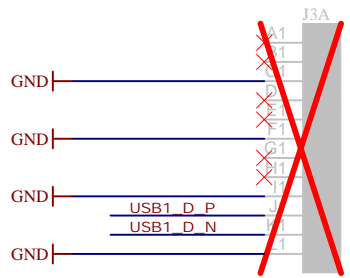
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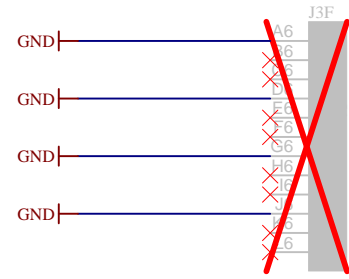
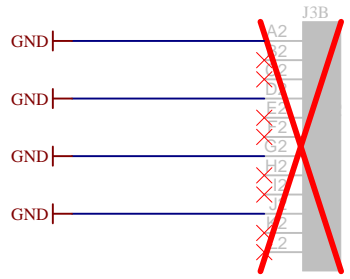
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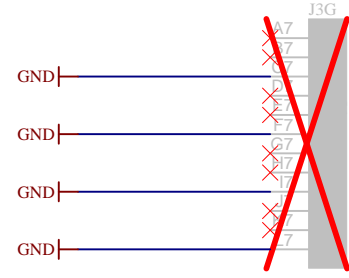
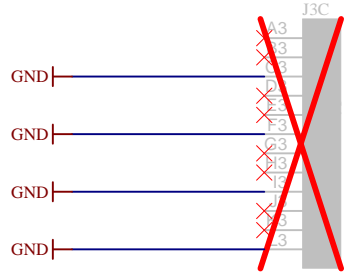
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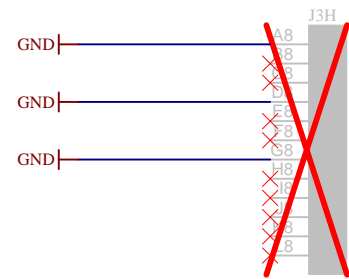
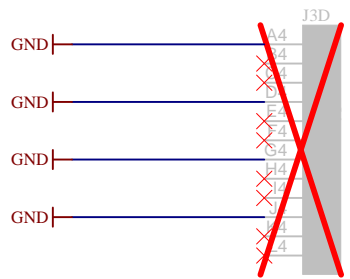
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| Title: TEC0850 - J3 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
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| Filename: J3.SchDoc | | |

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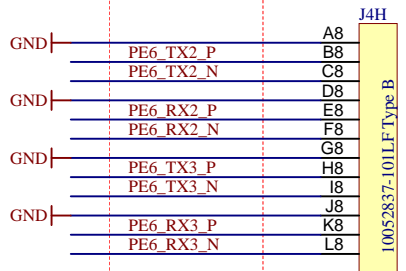
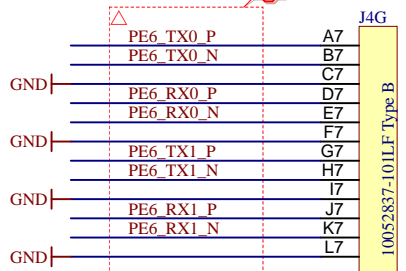
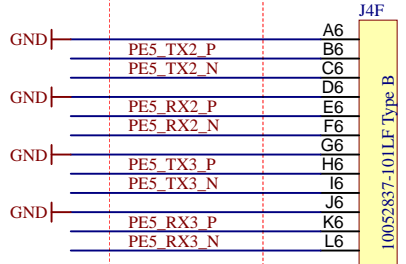
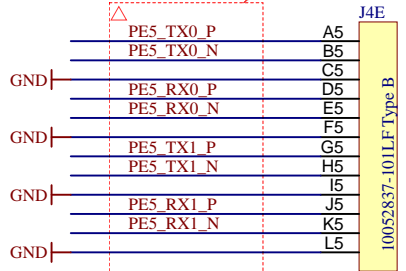
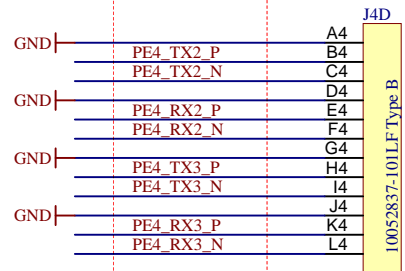
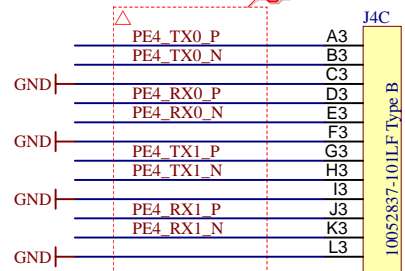
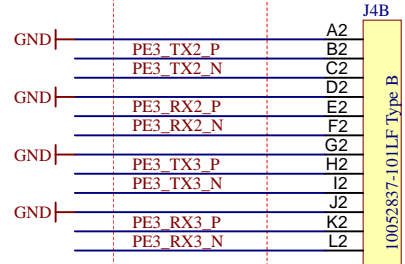
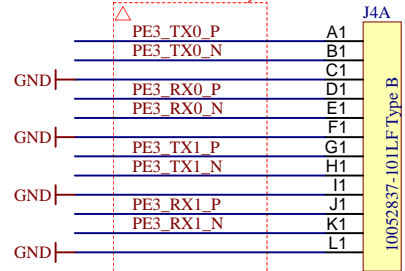
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| Title: TEC0850 - J4 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 6 of 33 |
| Filename: J4.SchDoc | | |

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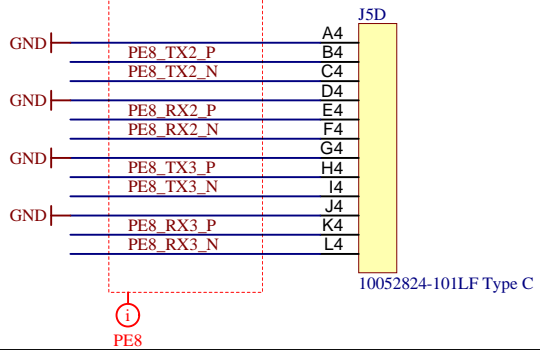
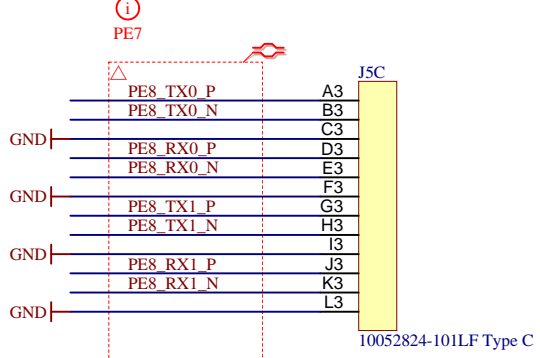
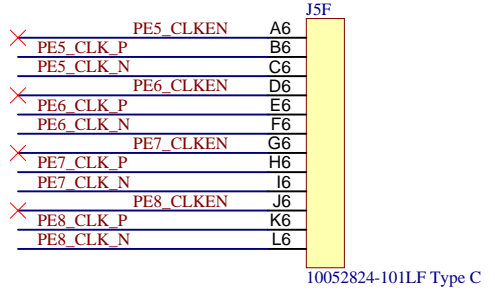
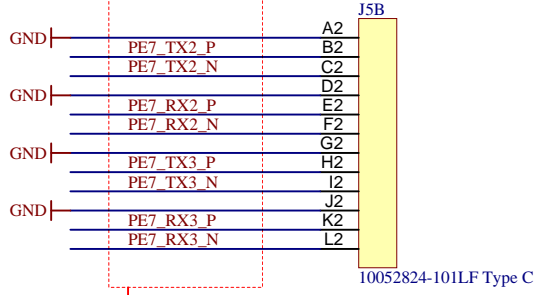
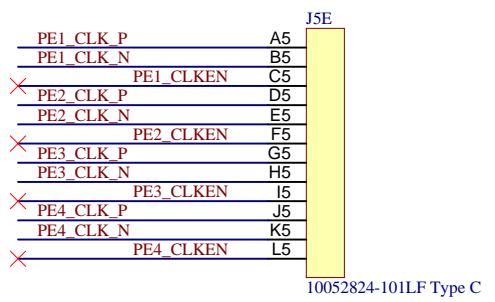
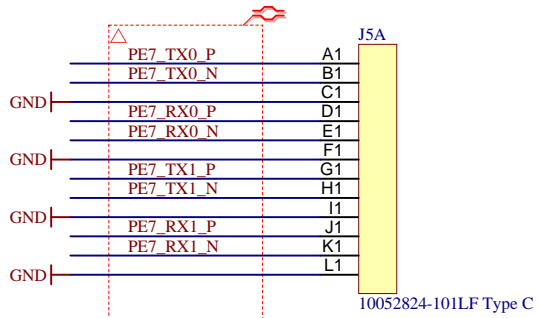
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| Title: TEC0850 - J5 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
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| Filename: J5.SchDoc | | |

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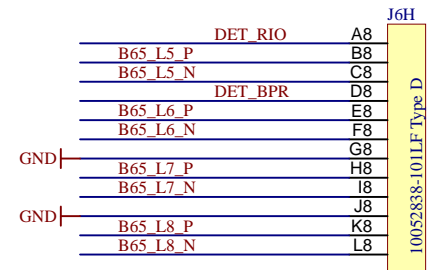
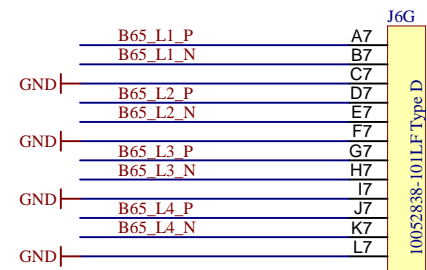
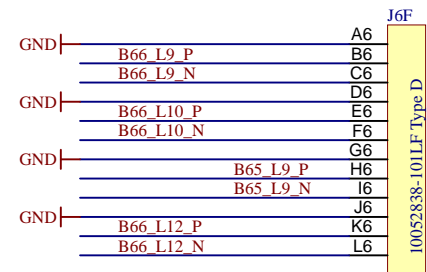
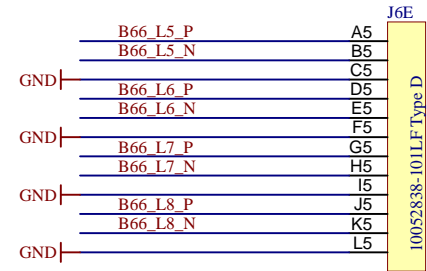
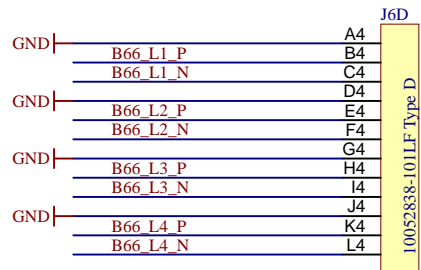
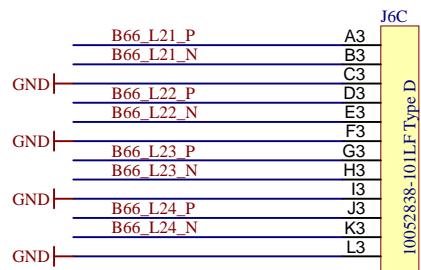
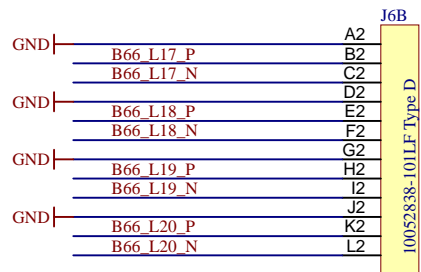
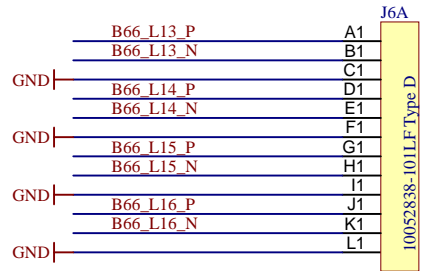
B

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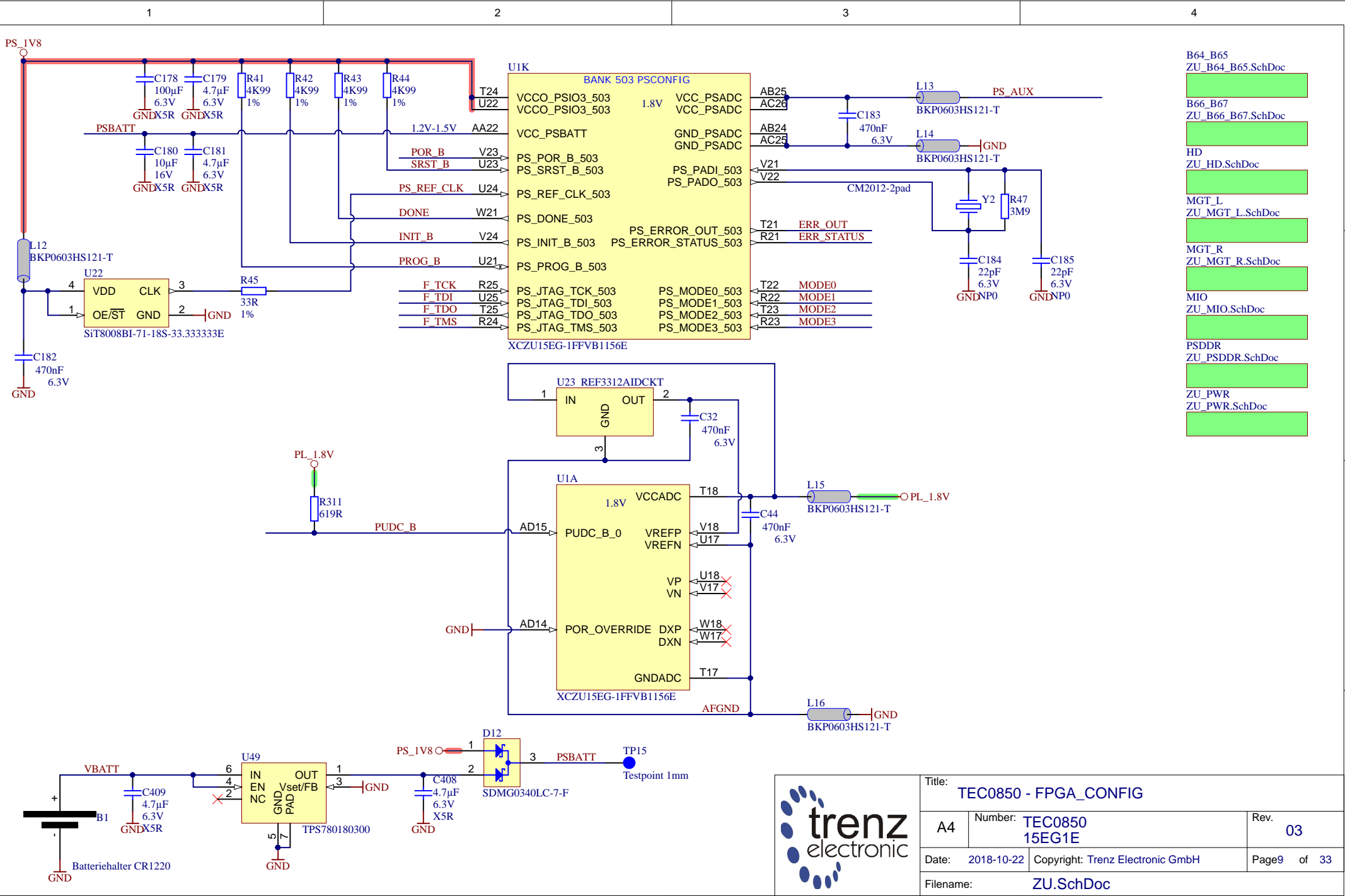
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| Title: TEC0850 - J6 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 8 of 33 |
| Filename: J6.SchDoc | | |

1

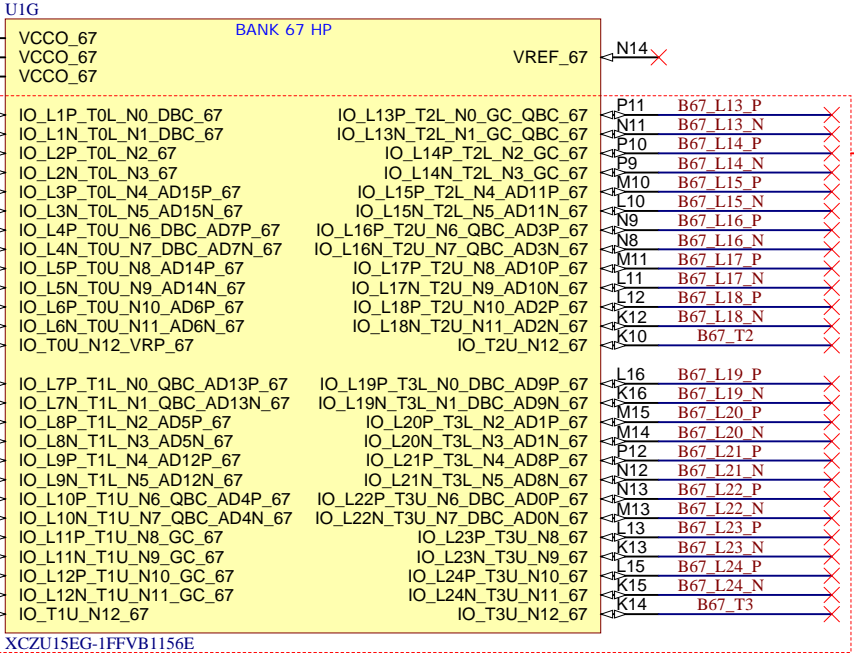
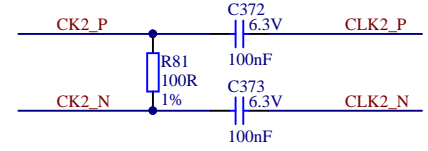
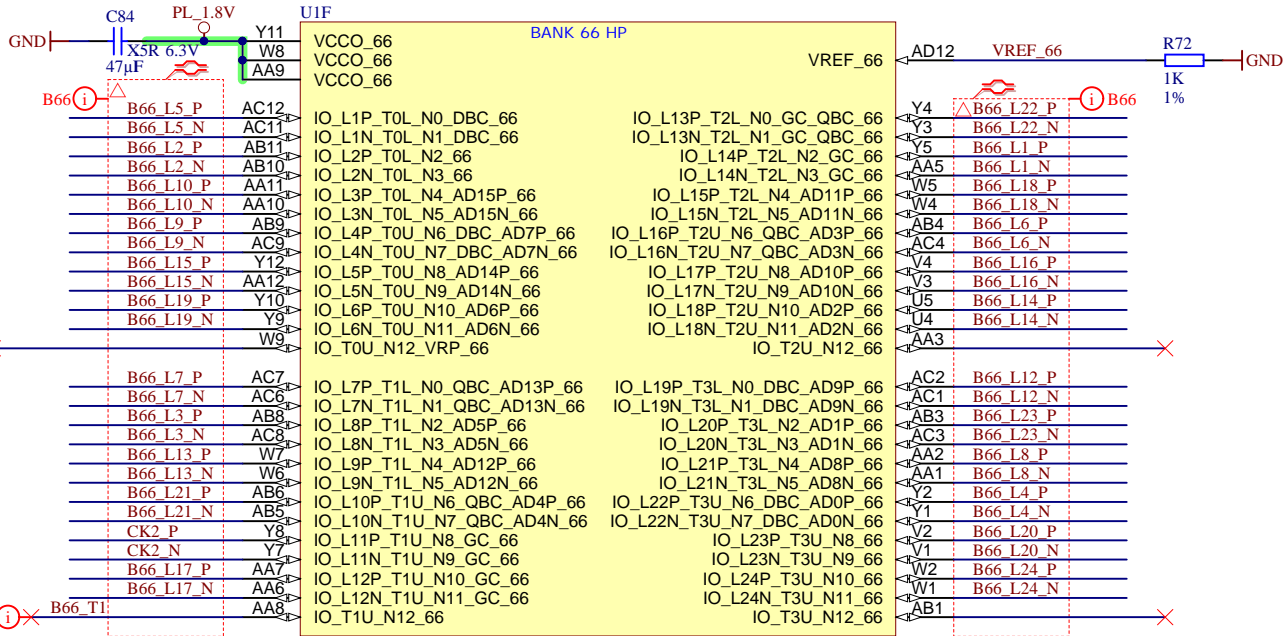
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| Title: TEC0850 - FPGA_CONFIG | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page9 of 33 |
| Filename: ZU.SchDoc | | |



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| Title: TEC0850 - FPGA_B66_B67 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 11 of 33 |
| Filename: ZU_B66_B67.SchDoc | | |

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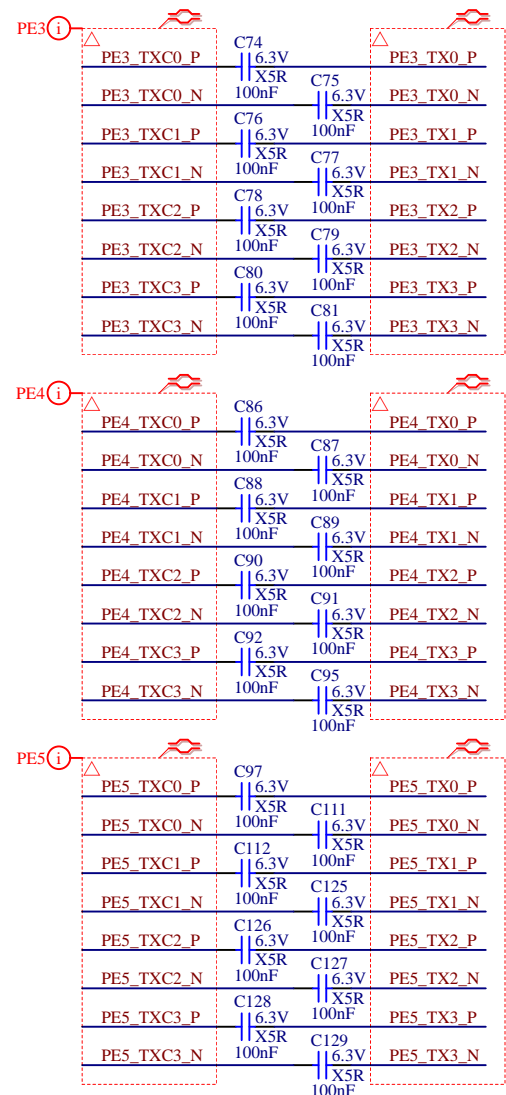
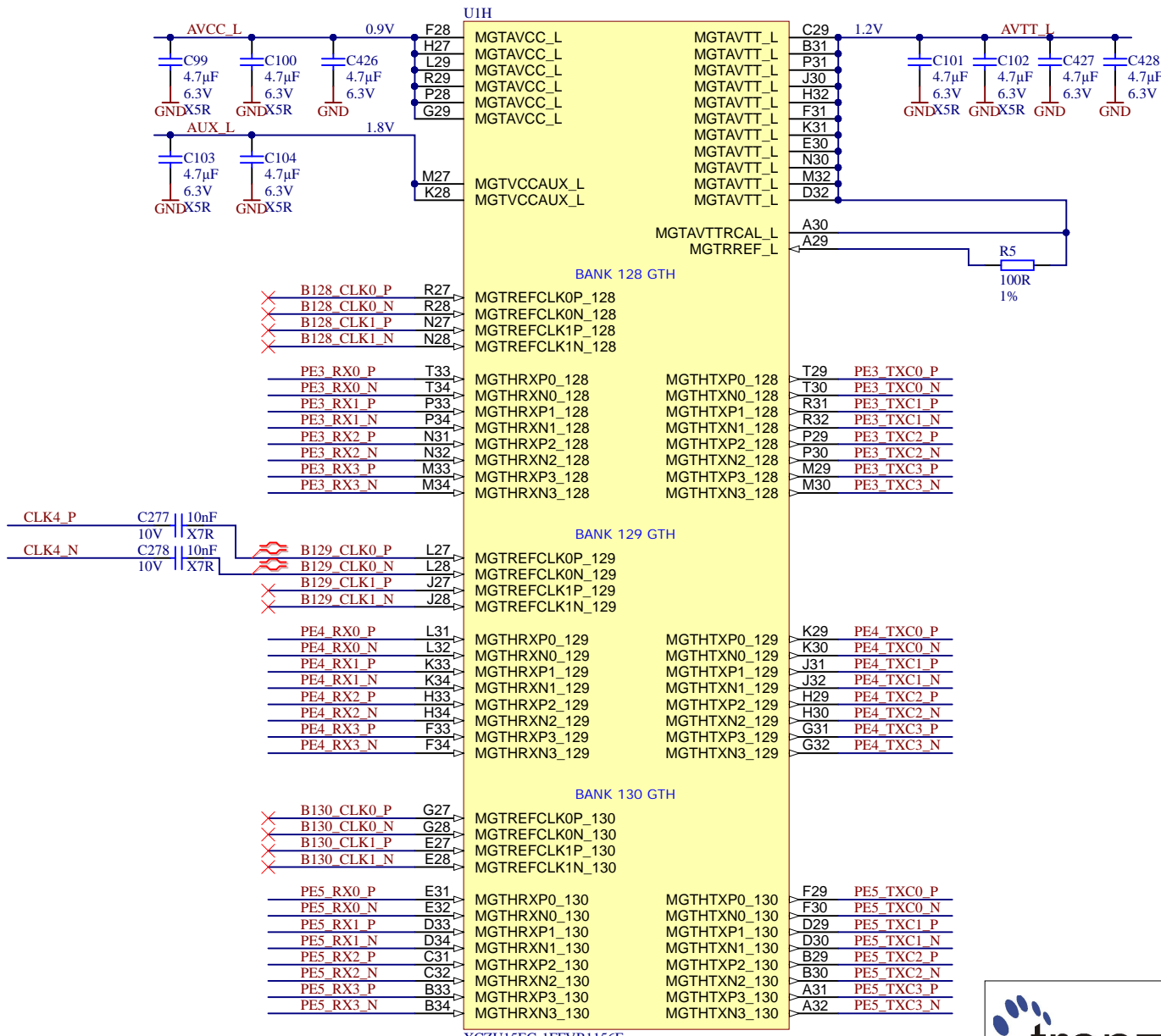
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| Title: TEC0850 - FPGA_MGT_L | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
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| Filename: ZU_MGT_L.SchDoc | | |

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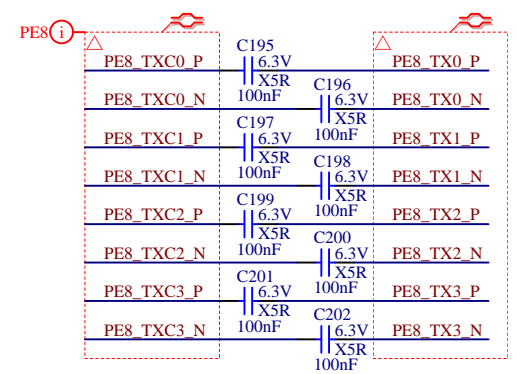
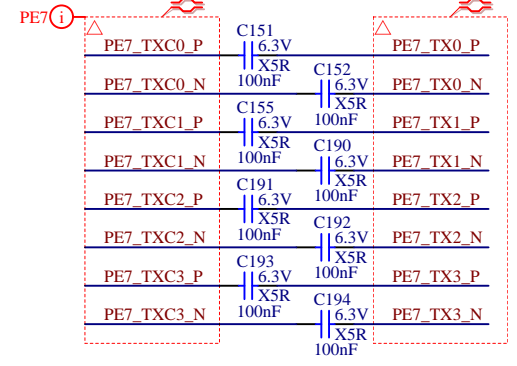
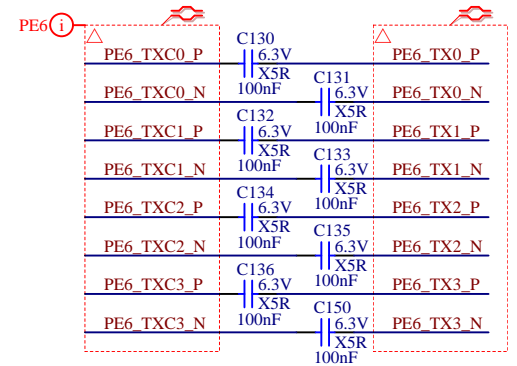
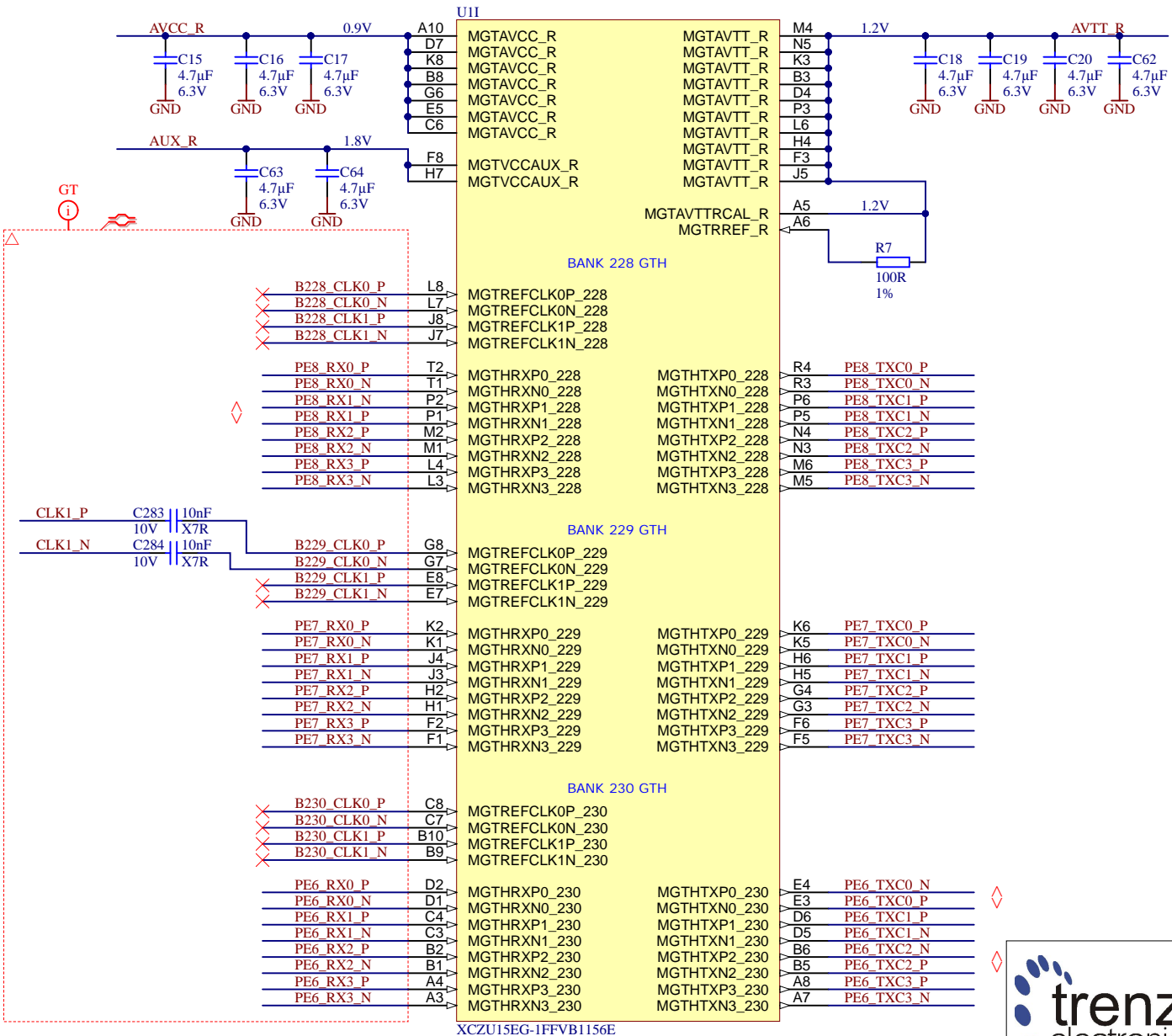
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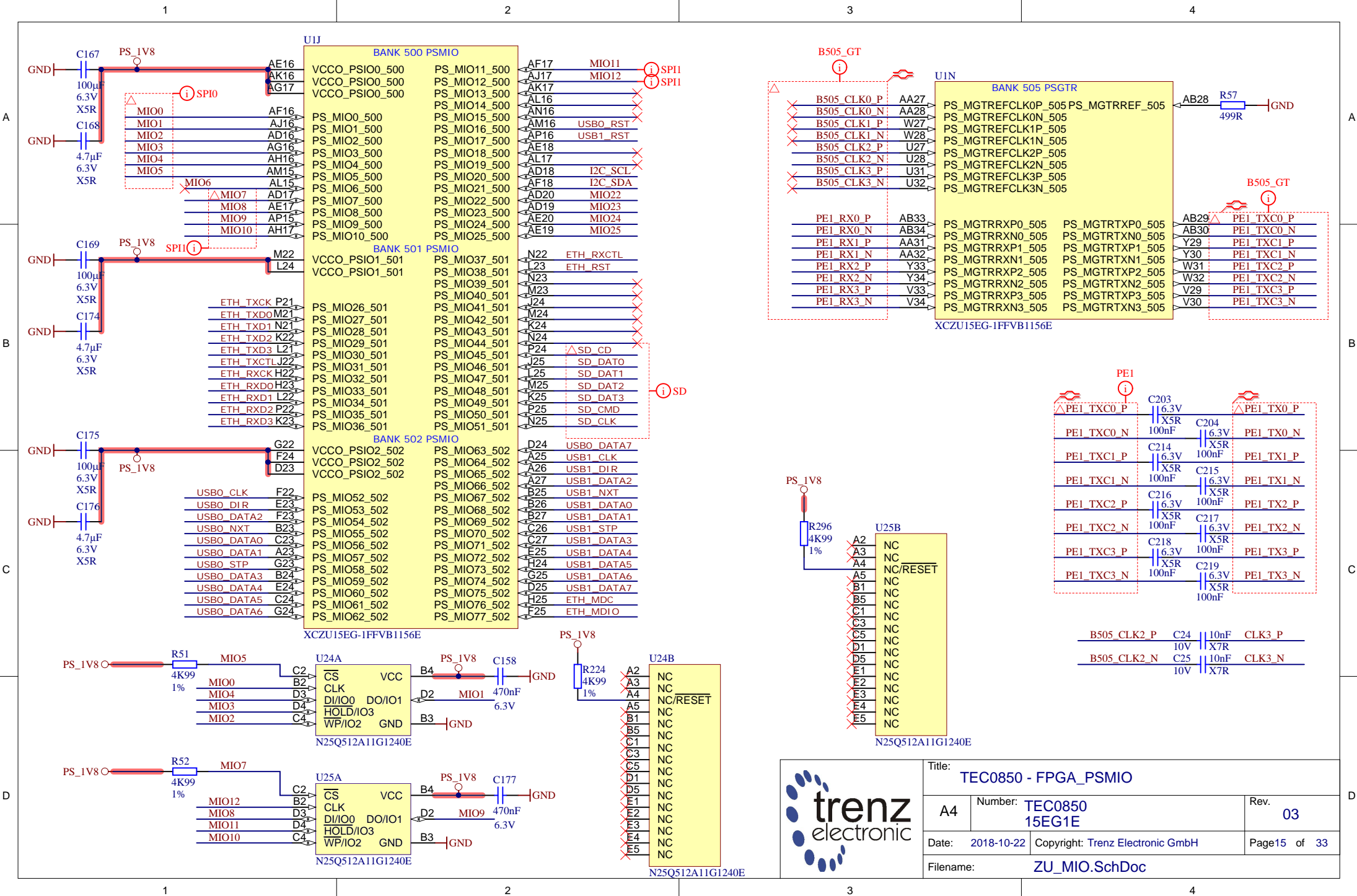
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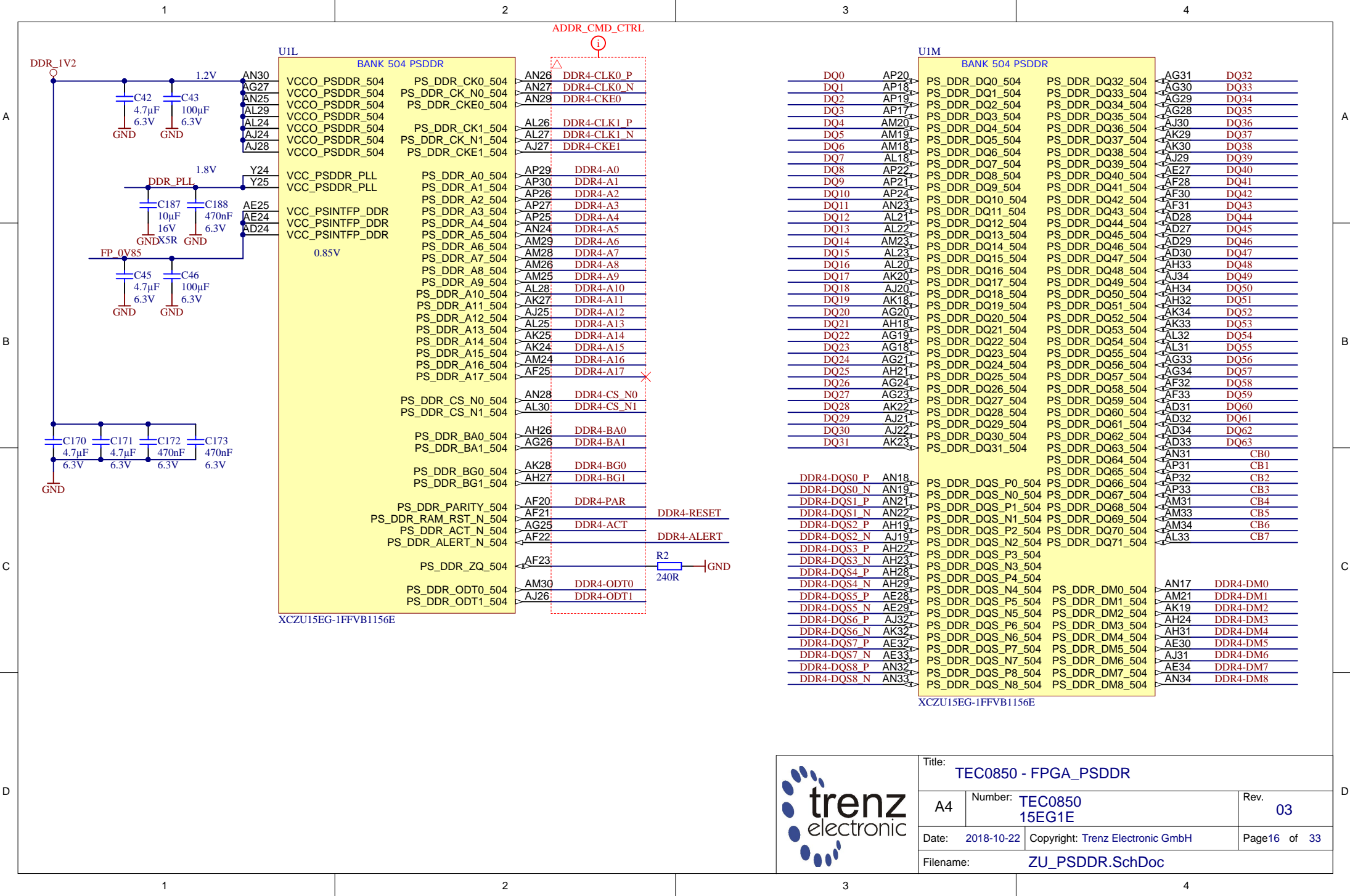
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| Title: TEC0850 - FPGA_MGT_R | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 14 of 33 |
| Filename: ZU_MGT_R.SchDoc | | |





ADDR_CMD_CTRL

UI1

U1M

| BANK 504 PSDDR | |
|----------------------|------------------|
| VCCO_PSDDR_504 | PS_DDR_CK0_504 |
| VCCO_PSDDR_504 | PS_DDR_CK_N0_504 |
| VCCO_PSDDR_504 | PS_DDR_CKE0_504 |
| VCCO_PSDDR_504 | PS_DDR_CK1_504 |
| VCCO_PSDDR_504 | PS_DDR_CK_N1_504 |
| VCCO_PSDDR_504 | PS_DDR_CKE1_504 |
| VCC_PSDDR_PLL | PS_DDR_A0_504 |
| VCC_PSDDR_PLL | PS_DDR_A1_504 |
| VCC_PSDDR_PLL | PS_DDR_A2_504 |
| VCC_PSDDR_PLL | PS_DDR_A3_504 |
| VCC_PSDDR_PLL | PS_DDR_A4_504 |
| VCC_PSDDR_PLL | PS_DDR_A5_504 |
| VCC_PSDDR_PLL | PS_DDR_A6_504 |
| VCC_PSDDR_PLL | PS_DDR_A7_504 |
| VCC_PSDDR_PLL | PS_DDR_A8_504 |
| VCC_PSDDR_PLL | PS_DDR_A9_504 |
| VCC_PSDDR_PLL | PS_DDR_A10_504 |
| VCC_PSDDR_PLL | PS_DDR_A11_504 |
| VCC_PSDDR_PLL | PS_DDR_A12_504 |
| VCC_PSDDR_PLL | PS_DDR_A13_504 |
| VCC_PSDDR_PLL | PS_DDR_A14_504 |
| VCC_PSDDR_PLL | PS_DDR_A15_504 |
| VCC_PSDDR_PLL | PS_DDR_A16_504 |
| VCC_PSDDR_PLL | PS_DDR_A17_504 |
| PS_DDR_CS_N0_504 | |
| PS_DDR_CS_N1_504 | |
| PS_DDR_BA0_504 | |
| PS_DDR_BA1_504 | |
| PS_DDR_BG0_504 | |
| PS_DDR_BG1_504 | |
| PS_DDR_PARITY_504 | |
| PS_DDR_RAM_RST_N_504 | |
| PS_DDR_ACT_N_504 | |
| PS_DDR_ALERT_N_504 | |
| PS_DDR_ZQ_504 | |
| PS_DDR_ODT0_504 | |
| PS_DDR_ODT1_504 | |

XCZU15EG-1FFVB1156E

| | |
|------|-------------|
| AN26 | DDR4-CLK0_P |
| AN27 | DDR4-CLK0_N |
| AN29 | DDR4-CKE0 |
| AL26 | DDR4-CLK1_P |
| AL27 | DDR4-CLK1_N |
| AJ27 | DDR4-CKE1 |
| AP29 | DDR4-A0 |
| AP30 | DDR4-A1 |
| AP26 | DDR4-A2 |
| AP27 | DDR4-A3 |
| AP25 | DDR4-A4 |
| AN24 | DDR4-A5 |
| AM29 | DDR4-A6 |
| AM28 | DDR4-A7 |
| AM26 | DDR4-A8 |
| AM25 | DDR4-A9 |
| AL28 | DDR4-A10 |
| AK27 | DDR4-A11 |
| AJ25 | DDR4-A12 |
| AL25 | DDR4-A13 |
| AK25 | DDR4-A14 |
| AK24 | DDR4-A15 |
| AM24 | DDR4-A16 |
| AF25 | DDR4-A17 |
| AN28 | DDR4-CS_N0 |
| AL30 | DDR4-CS_N1 |
| AH26 | DDR4-BA0 |
| AG26 | DDR4-BA1 |
| AK28 | DDR4-BG0 |
| AH27 | DDR4-BG1 |
| AF20 | DDR4-PAR |
| AF21 | DDR4-PAR |
| AG25 | DDR4-ACT |
| AF22 | DDR4-ACT |
| AF23 | DDR4-ACT |
| AM30 | DDR4-ODT0 |
| AJ26 | DDR4-ODT1 |

DDR4-RESET

DDR4-ALERT

R2 240R

| BANK 504 PSDDR | | | |
|-----------------|------|-----------------|-----------------|
| DQ0 | AP20 | PS_DDR_DQ0_504 | PS_DDR_DQ32_504 |
| DQ1 | AP18 | PS_DDR_DQ1_504 | PS_DDR_DQ33_504 |
| DQ2 | AP19 | PS_DDR_DQ2_504 | PS_DDR_DQ34_504 |
| DQ3 | AP17 | PS_DDR_DQ3_504 | PS_DDR_DQ35_504 |
| DQ4 | AM20 | PS_DDR_DQ4_504 | PS_DDR_DQ36_504 |
| DQ5 | AM19 | PS_DDR_DQ5_504 | PS_DDR_DQ37_504 |
| DQ6 | AM18 | PS_DDR_DQ6_504 | PS_DDR_DQ38_504 |
| DQ7 | AL18 | PS_DDR_DQ7_504 | PS_DDR_DQ39_504 |
| DQ8 | AP22 | PS_DDR_DQ8_504 | PS_DDR_DQ40_504 |
| DQ9 | AP21 | PS_DDR_DQ9_504 | PS_DDR_DQ41_504 |
| DQ10 | AP24 | PS_DDR_DQ10_504 | PS_DDR_DQ42_504 |
| DQ11 | AM23 | PS_DDR_DQ11_504 | PS_DDR_DQ43_504 |
| DQ12 | AL21 | PS_DDR_DQ12_504 | PS_DDR_DQ44_504 |
| DQ13 | AL22 | PS_DDR_DQ13_504 | PS_DDR_DQ45_504 |
| DQ14 | AM23 | PS_DDR_DQ14_504 | PS_DDR_DQ46_504 |
| DQ15 | AL23 | PS_DDR_DQ15_504 | PS_DDR_DQ47_504 |
| DQ16 | AL20 | PS_DDR_DQ16_504 | PS_DDR_DQ48_504 |
| DQ17 | AK20 | PS_DDR_DQ17_504 | PS_DDR_DQ49_504 |
| DQ18 | AJ20 | PS_DDR_DQ18_504 | PS_DDR_DQ50_504 |
| DQ19 | AK18 | PS_DDR_DQ19_504 | PS_DDR_DQ51_504 |
| DQ20 | AG20 | PS_DDR_DQ20_504 | PS_DDR_DQ52_504 |
| DQ21 | AH18 | PS_DDR_DQ21_504 | PS_DDR_DQ53_504 |
| DQ22 | AG19 | PS_DDR_DQ22_504 | PS_DDR_DQ54_504 |
| DQ23 | AG18 | PS_DDR_DQ23_504 | PS_DDR_DQ55_504 |
| DQ24 | AG21 | PS_DDR_DQ24_504 | PS_DDR_DQ56_504 |
| DQ25 | AH21 | PS_DDR_DQ25_504 | PS_DDR_DQ57_504 |
| DQ26 | AG24 | PS_DDR_DQ26_504 | PS_DDR_DQ58_504 |
| DQ27 | AG23 | PS_DDR_DQ27_504 | PS_DDR_DQ59_504 |
| DQ28 | AK22 | PS_DDR_DQ28_504 | PS_DDR_DQ60_504 |
| DQ29 | AJ21 | PS_DDR_DQ29_504 | PS_DDR_DQ61_504 |
| DQ30 | AJ22 | PS_DDR_DQ30_504 | PS_DDR_DQ62_504 |
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| PS_DDR_DQ97_504 | | | |
| PS_DDR_DQ98_504 | | | |
| PS_DDR_DQ99_504 | | | |

XCZU15EG-1FFVB1156E



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|------------------------------------|---|-----------------------------|
| Title: TEC0850 - FPGA_PSDDR | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 16 of 33 |
| Filename: ZU_PSDDR.SchDoc | | |

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A

A

B

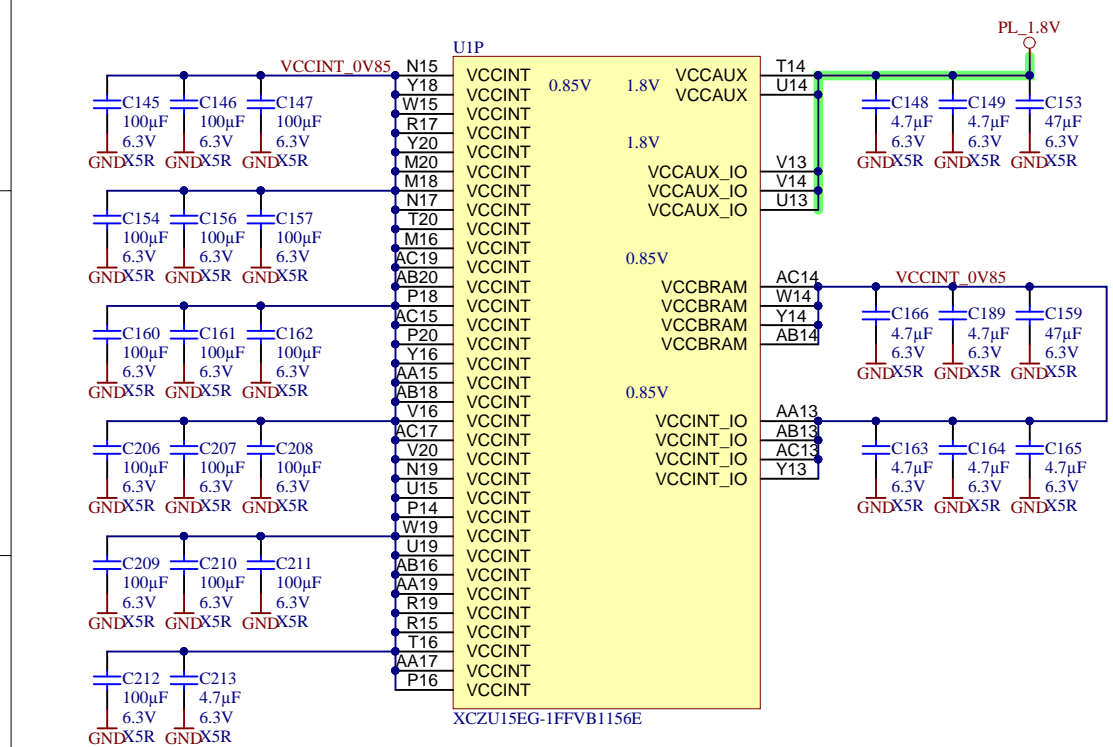
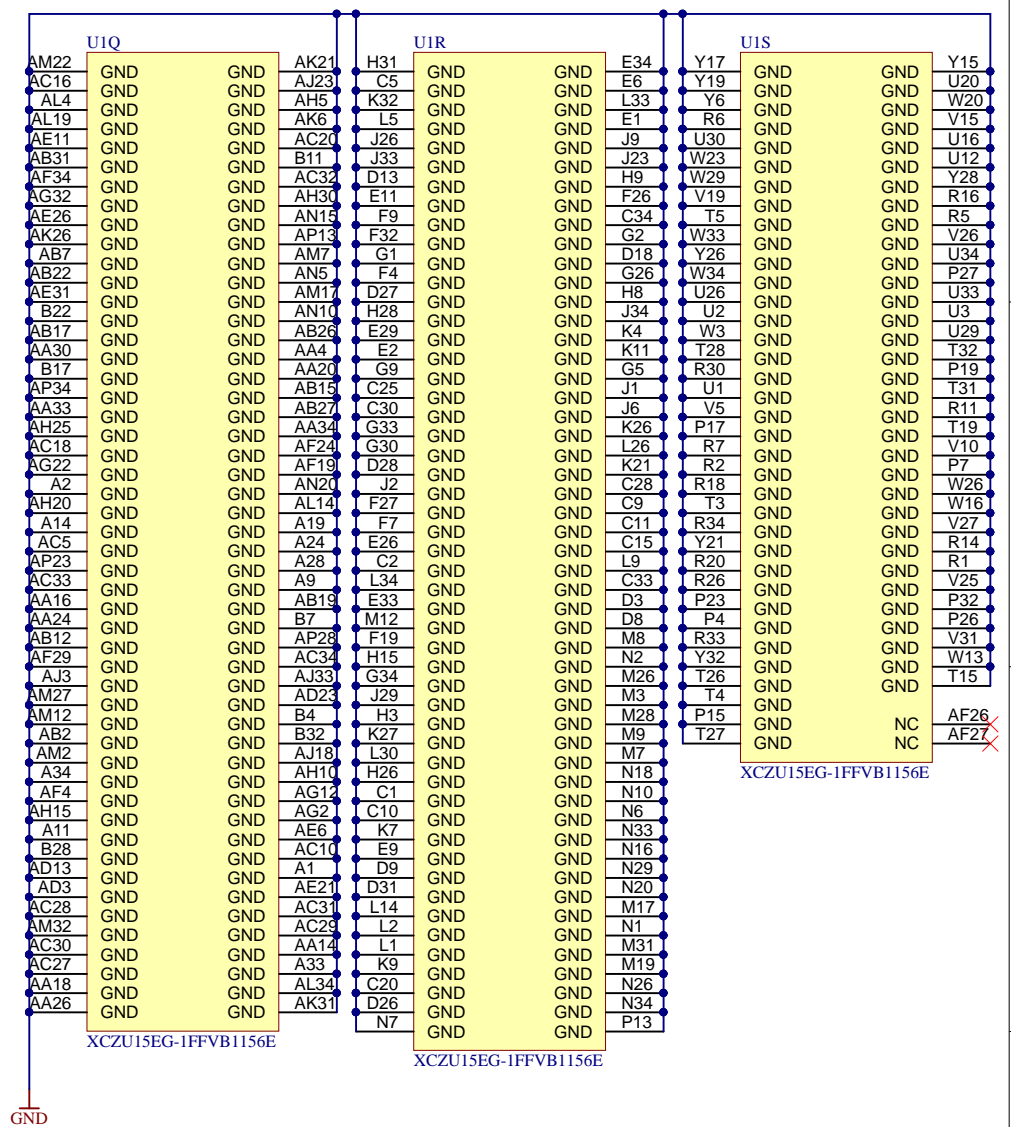
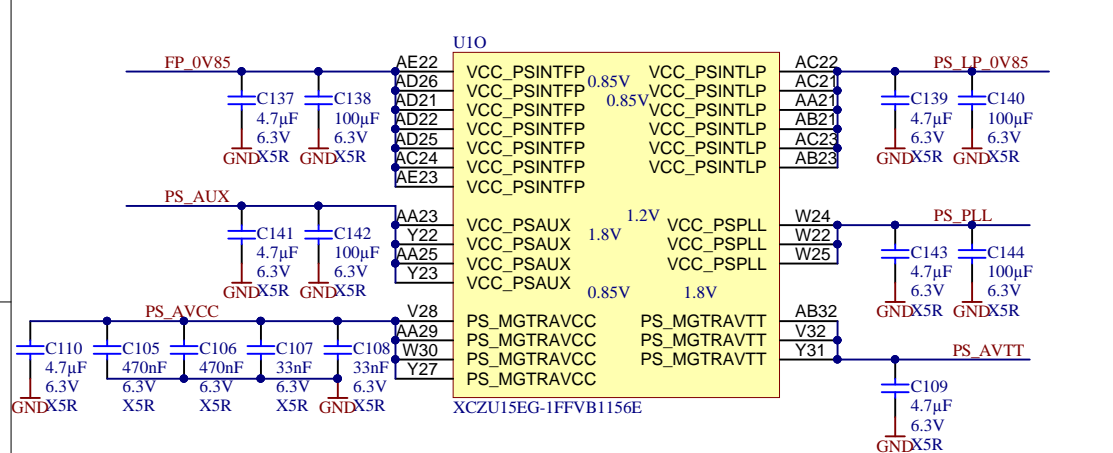
B

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C

D

D



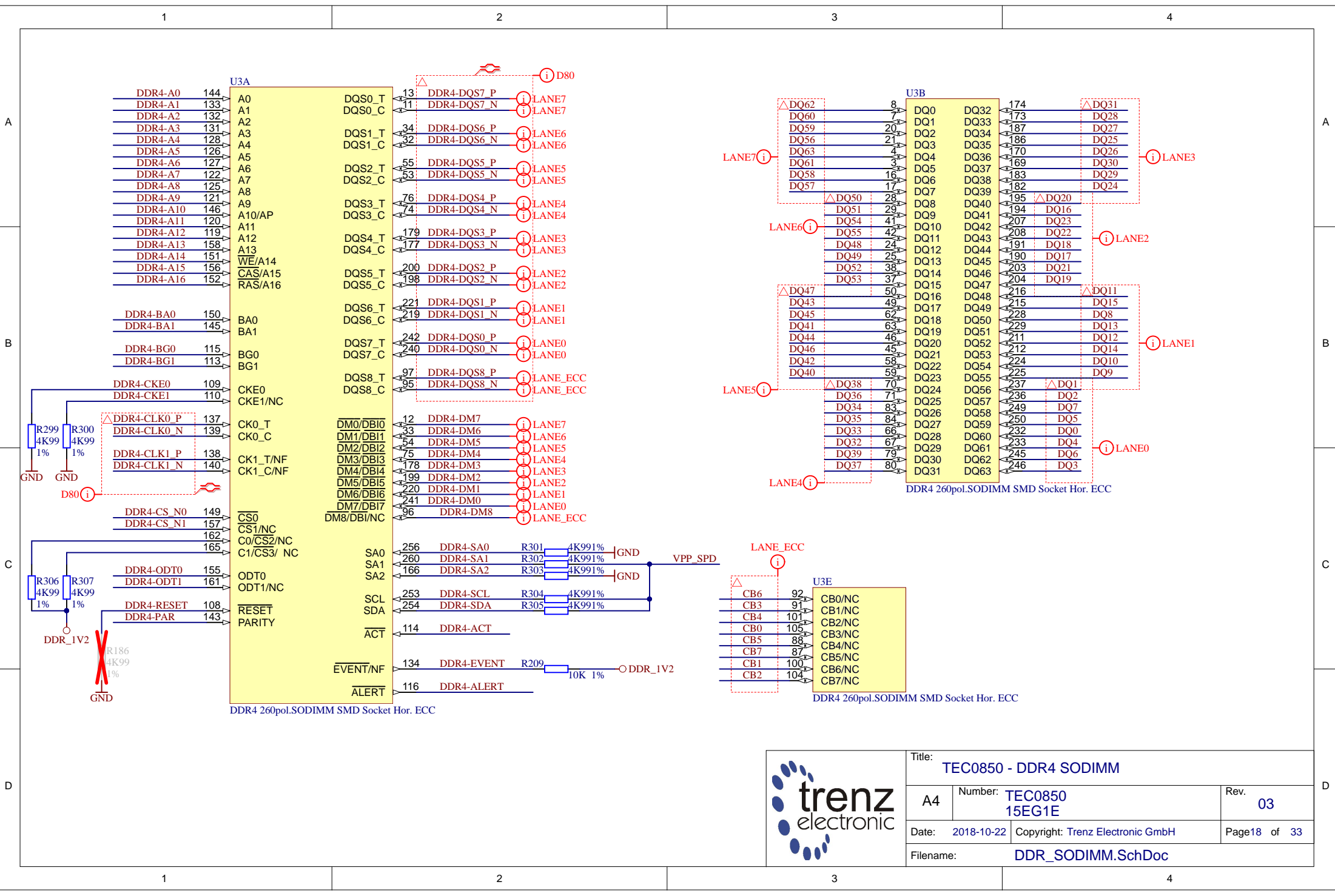
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| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 17 of 33 |
| Filename: ZU_PWR.SchDoc | | |


1

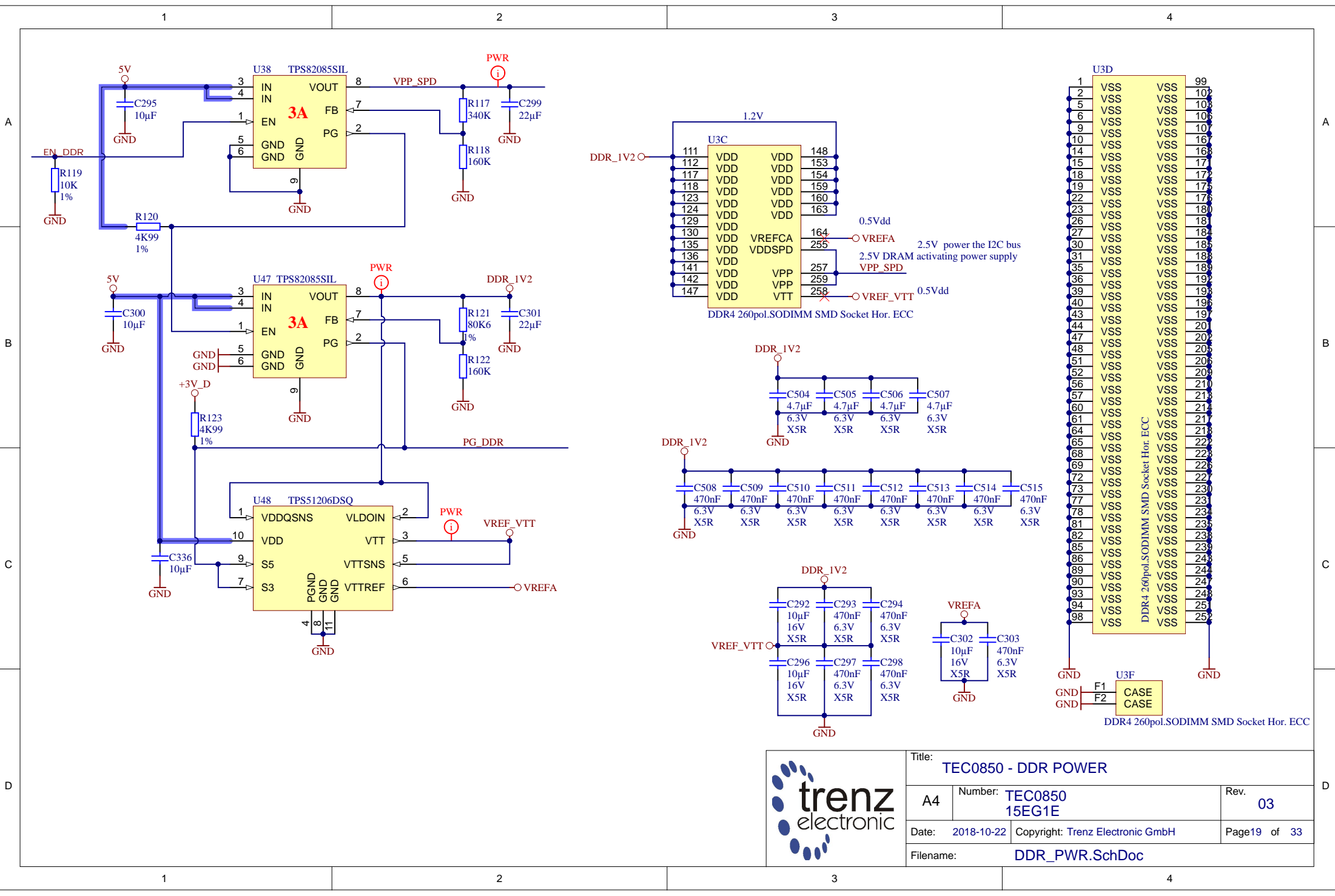
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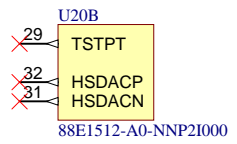
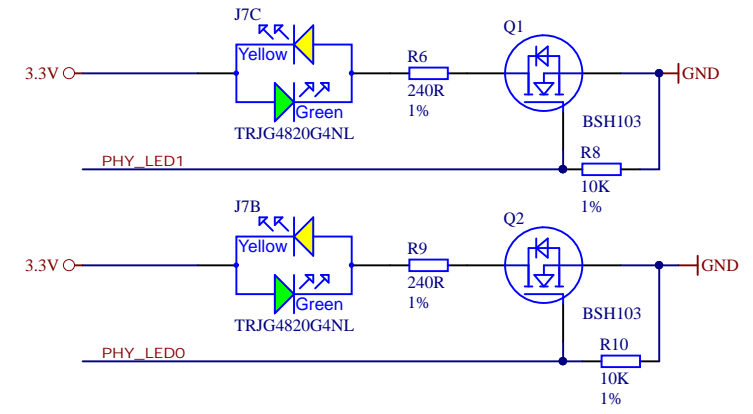
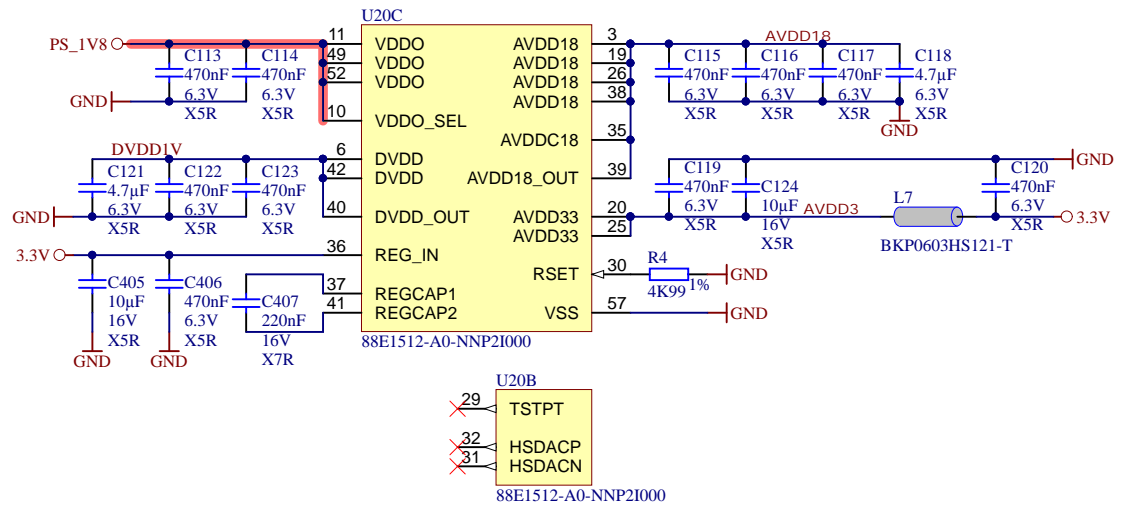
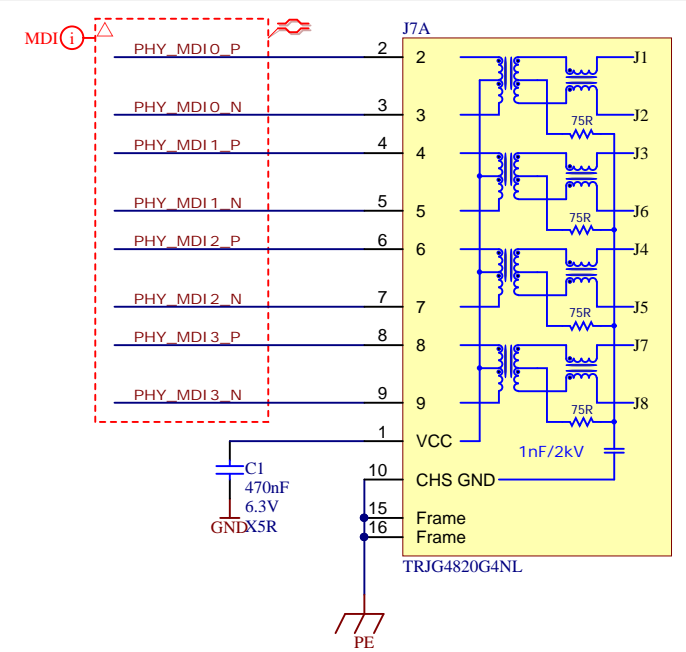
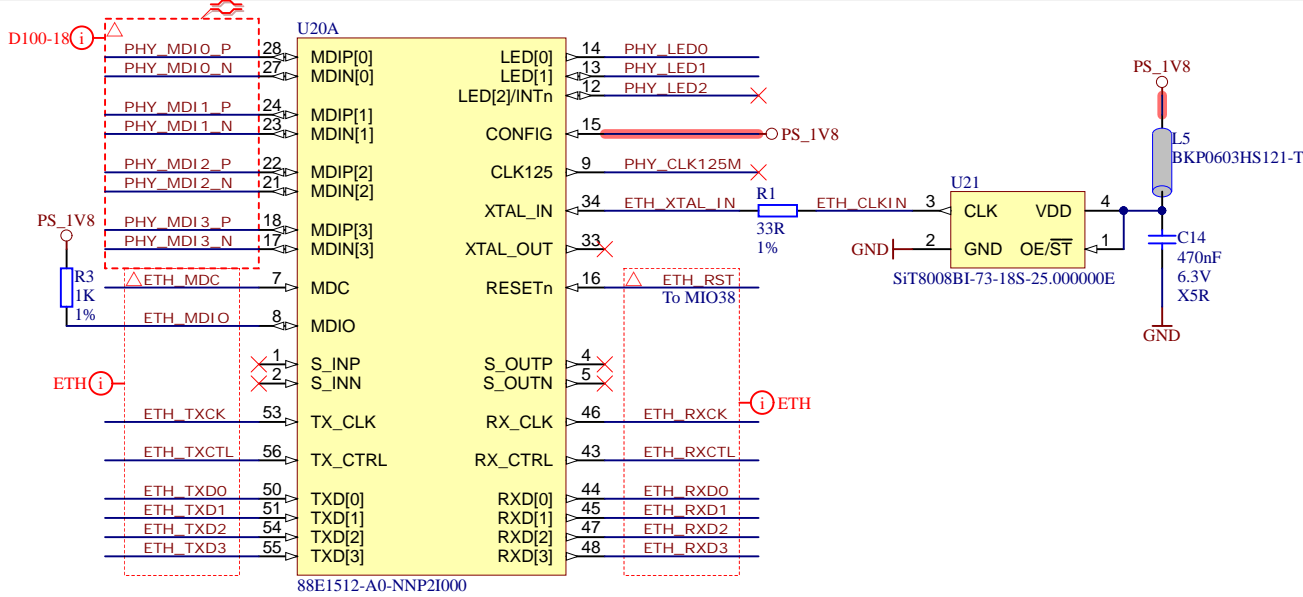
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| | | | A4 | Number: TEC0850 15EG1E |
| Date: 2018-10-22 | | Copyright: Trenz Electronic GmbH | | Page18 of 33 |
| Filename: DDR_SODIMM.SchDoc | | | | |



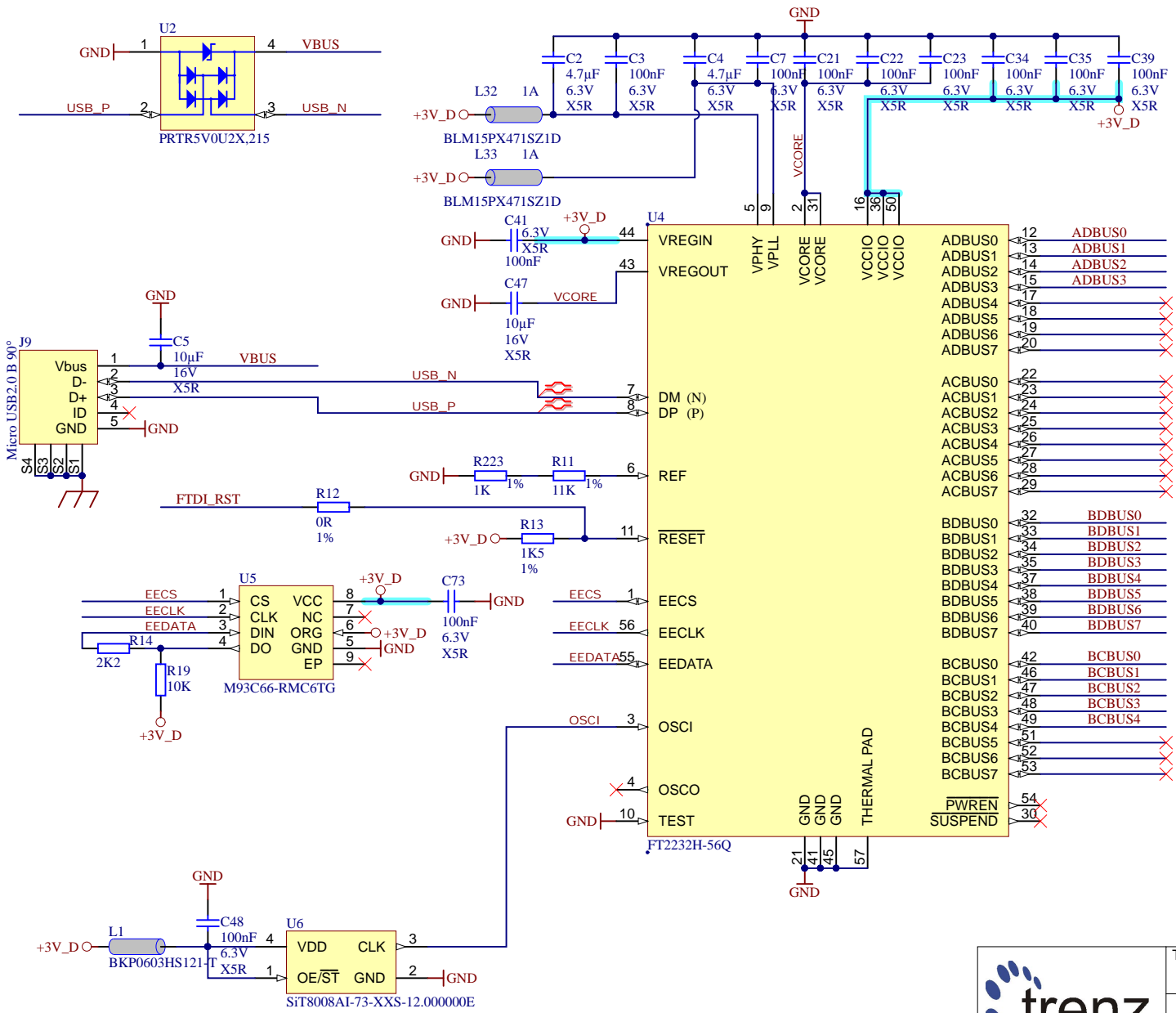
trenz electronic


Title: **TEC0850 - DDR POWER**

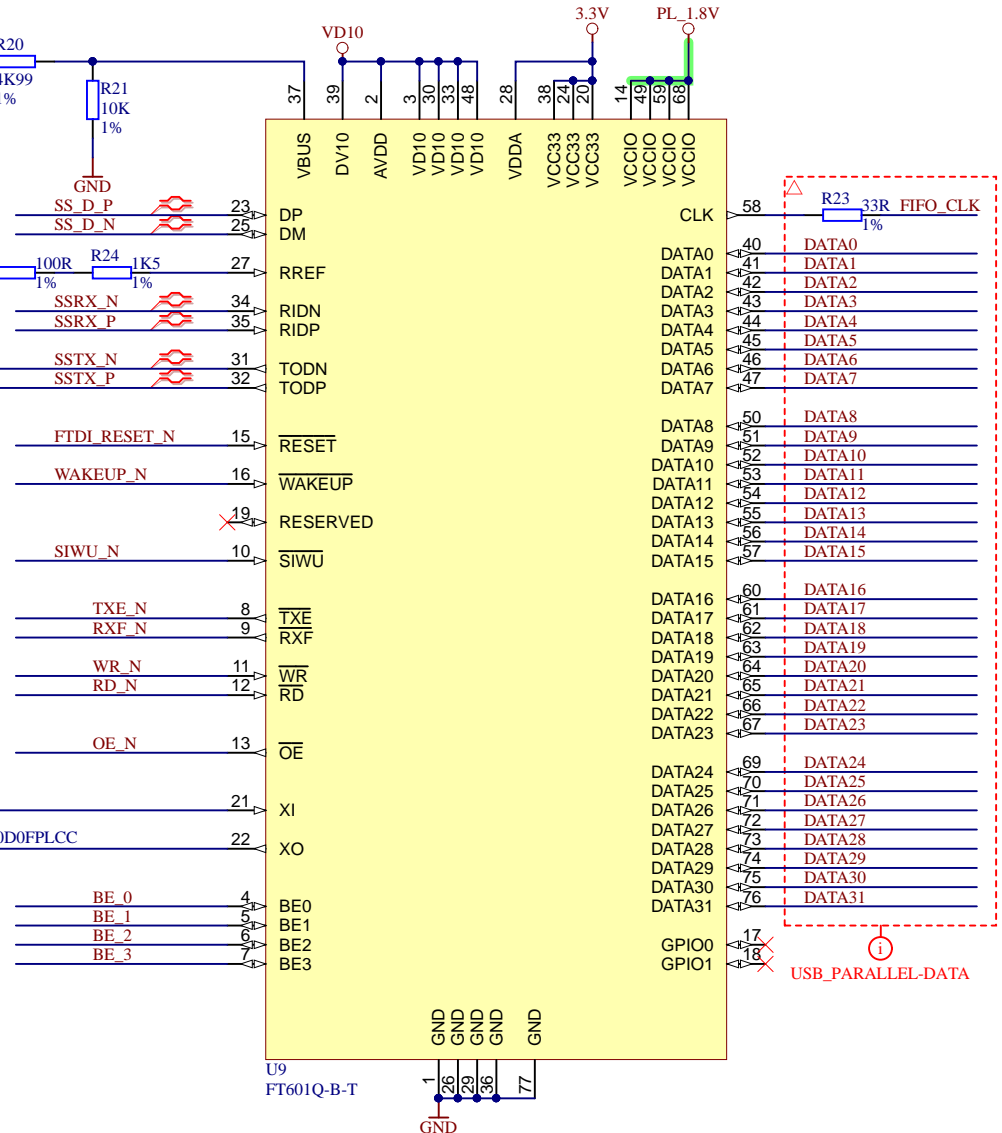
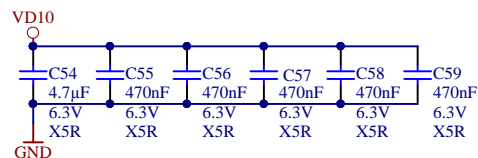
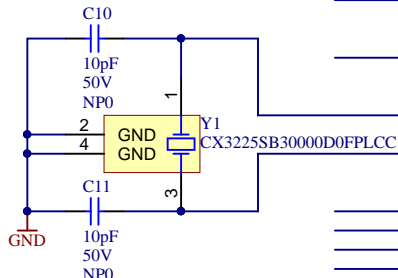
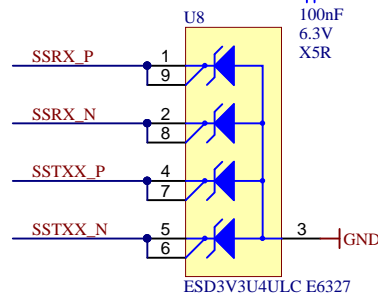
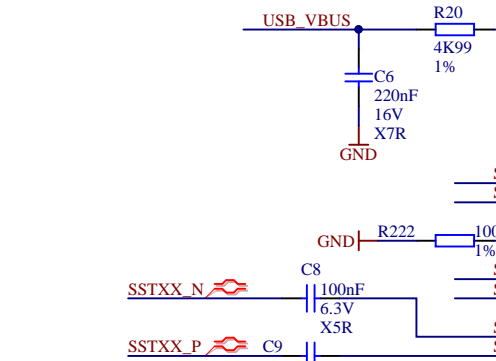
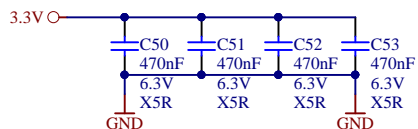
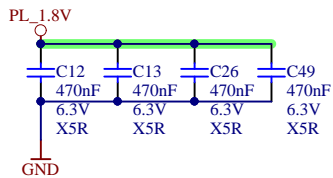
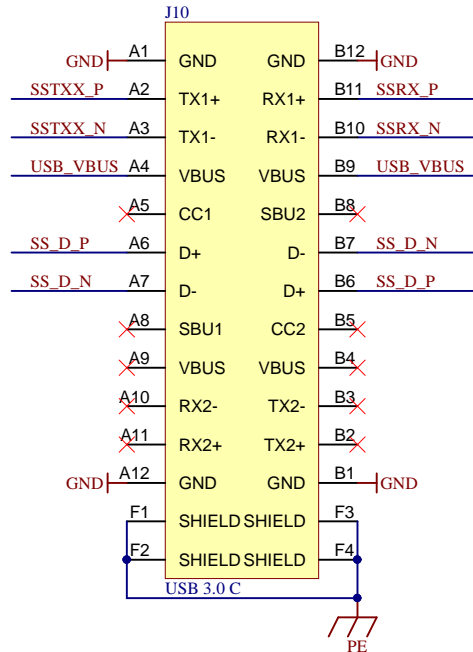
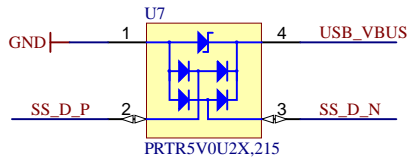
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| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 19 of 33 |
| Filename: DDR_PWR.SchDoc | | |



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|---------------------------|----------------------------------|--------------|
| Title: TEC0850 - ETH | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page20 of 33 |
| Filename: Ethernet.SchDoc | | |



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|  | | | Title: TEC0850 - FTDI | |
| | | | A4 | Number: TEC0850 15EG1E |
| Date: 2018-10-22 | | Copyright: Trenz Electronic GmbH | | Page 21 of 33 |
| Filename: FTDI.SchDoc | | | | |



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|--------------------------------|---|-----------------------------|
| Title: TEC0850 - USB3.0 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 22 of 33 |
| Filename: USB30.SchDoc | | |

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A

A

B

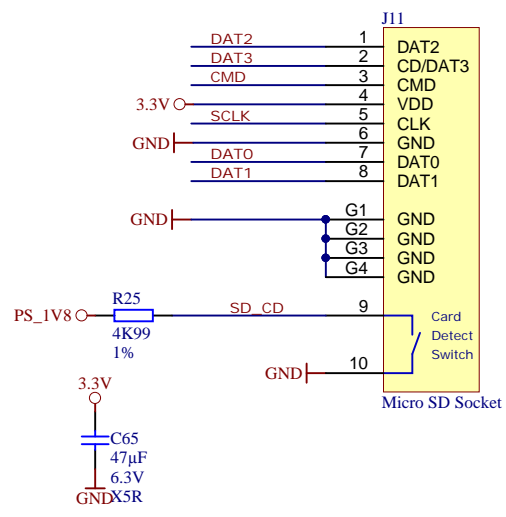
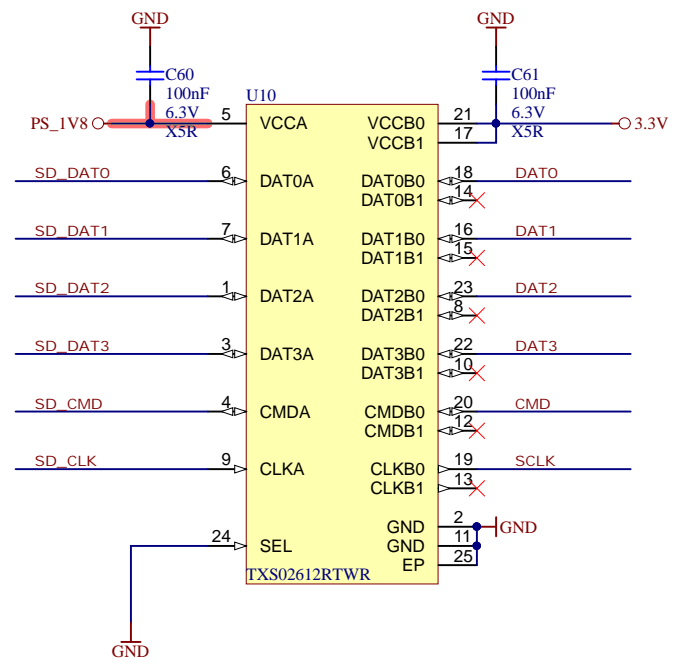
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C

C

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D



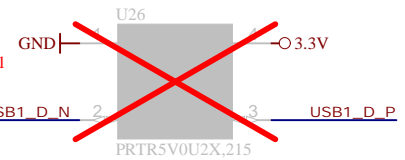
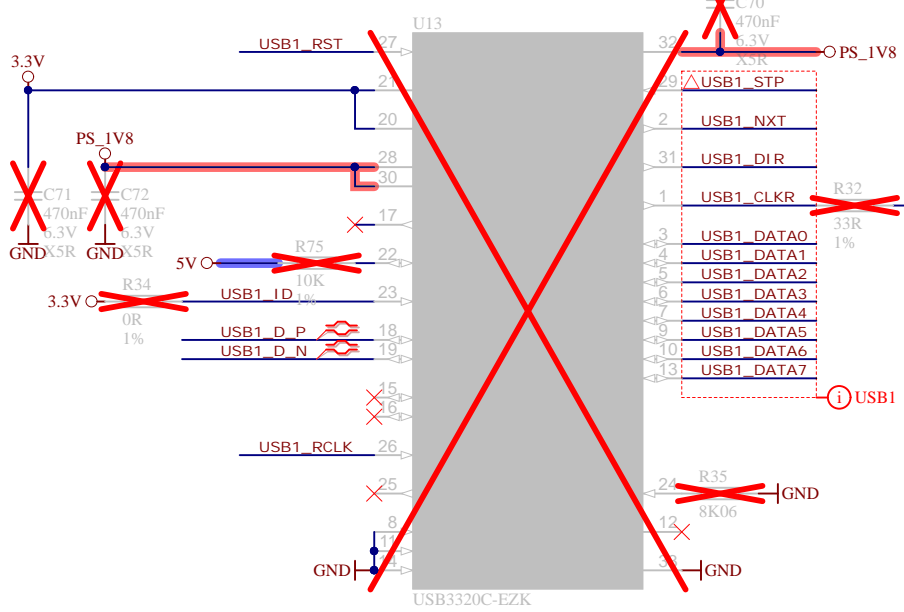
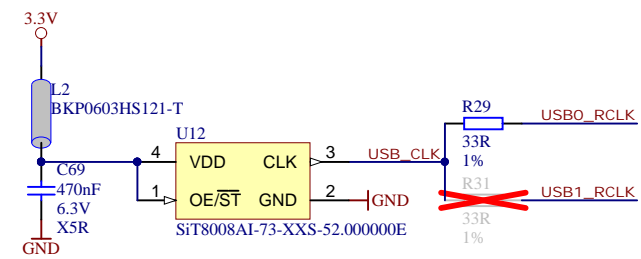
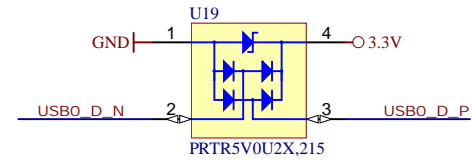
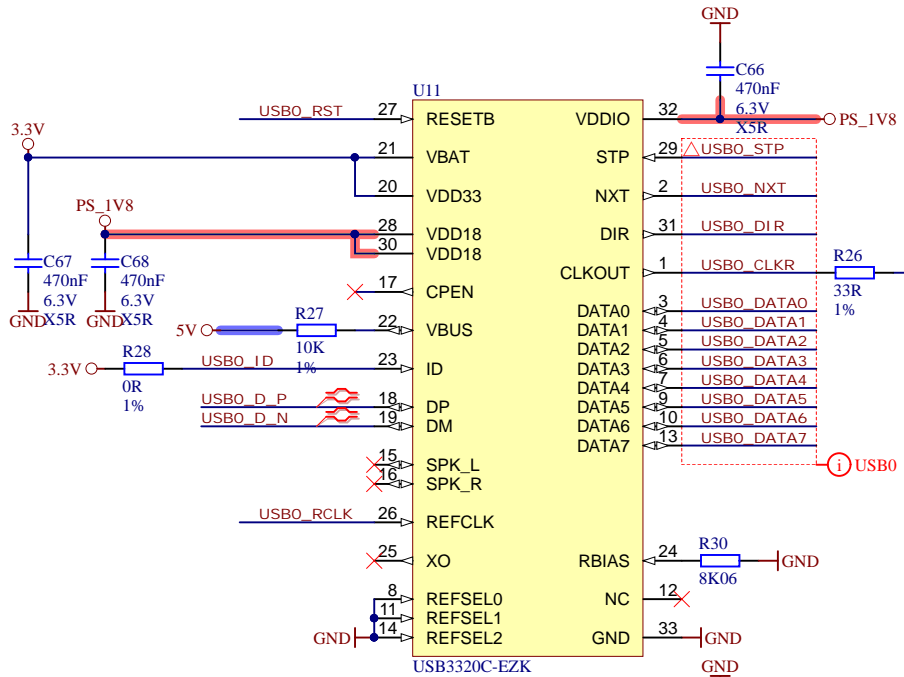
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| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 23 of 33 |
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1

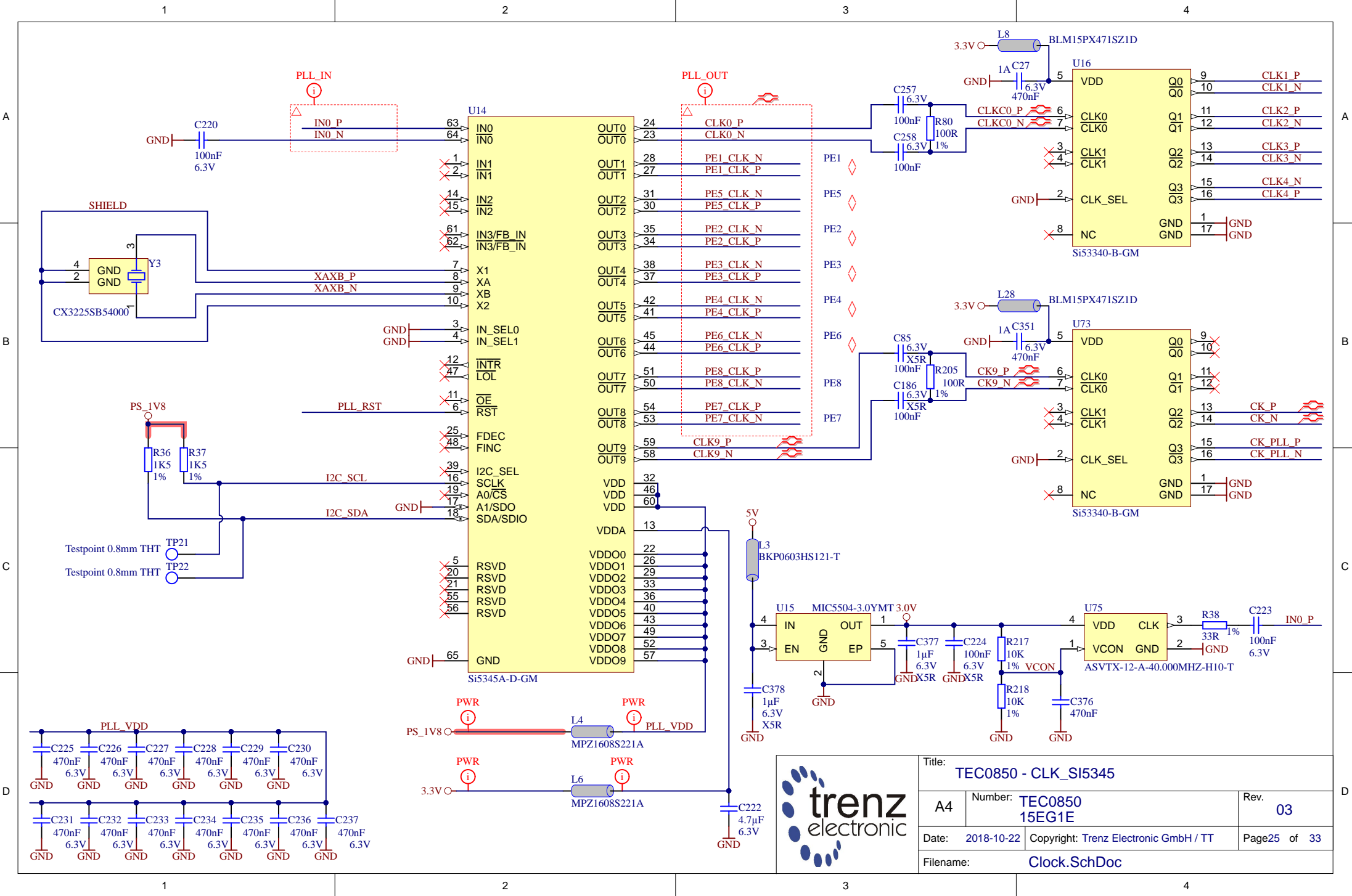
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3

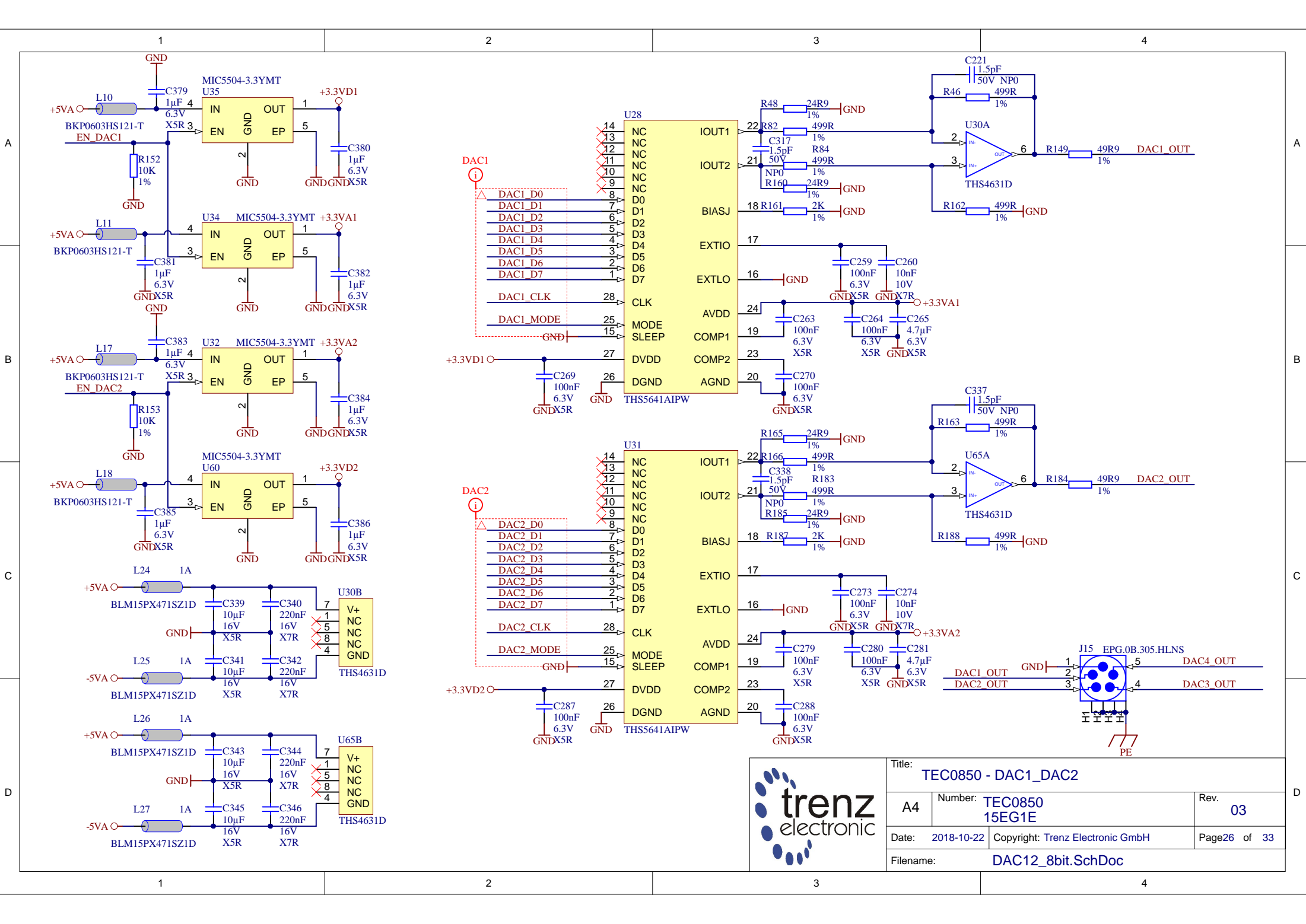
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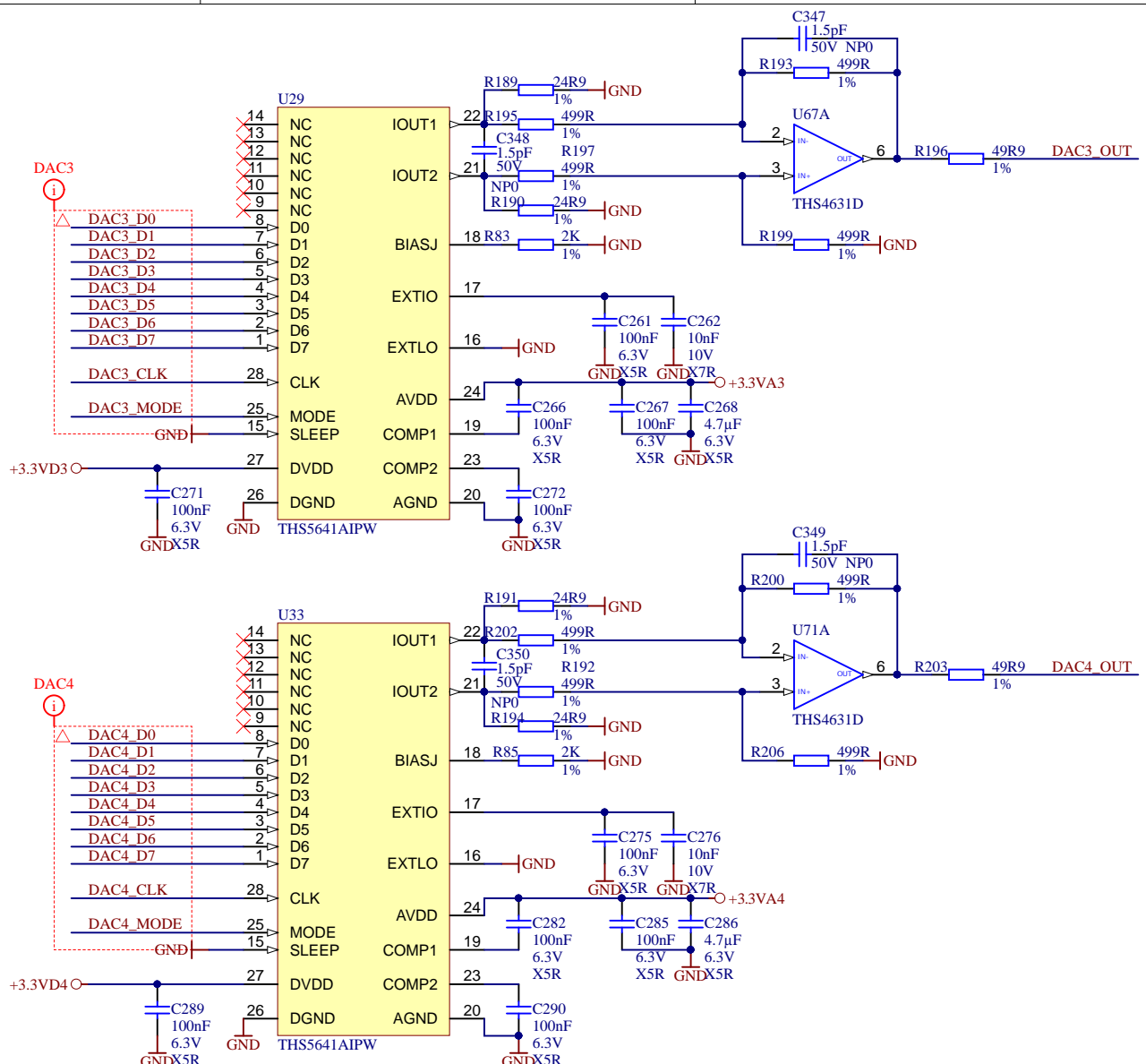
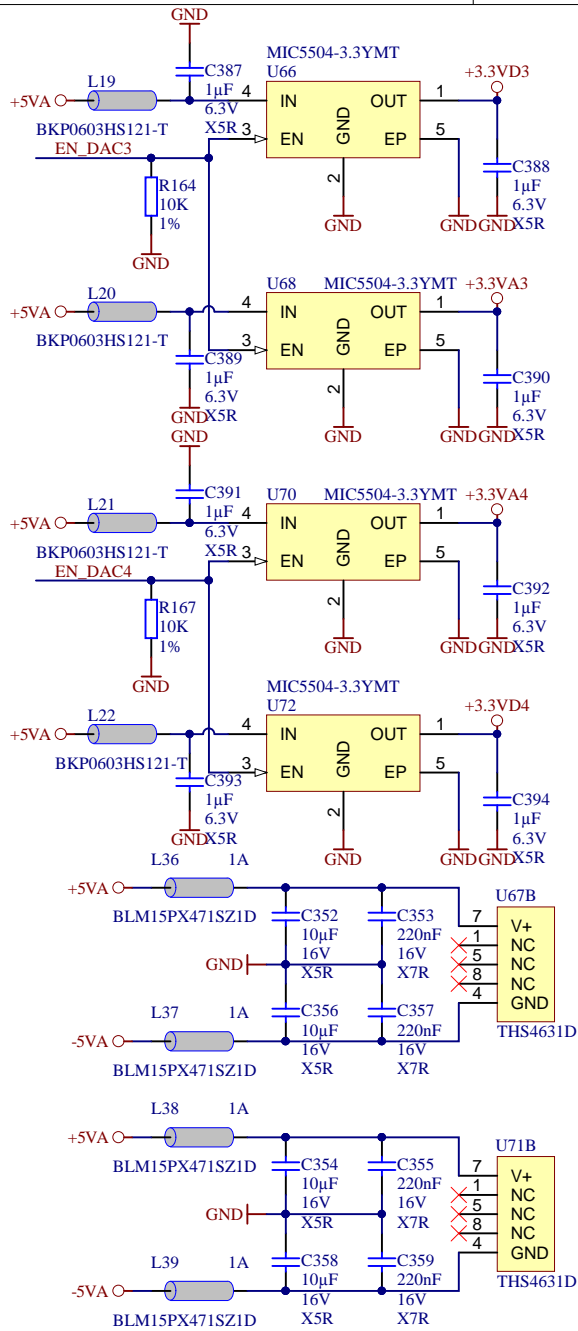
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| | | A4 | Number: TEC0850 15EG1E |
| Date: 2018-10-22 | | Copyright: Trenz Electronic GmbH | |
| Filename: USB-PHY.SchDoc | | Page 24 of 33 | |




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| Title: TEC0850 - CLK_SI5345 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH / TT | Page 25 of 33 |
| Filename: Clock.SchDoc | | |

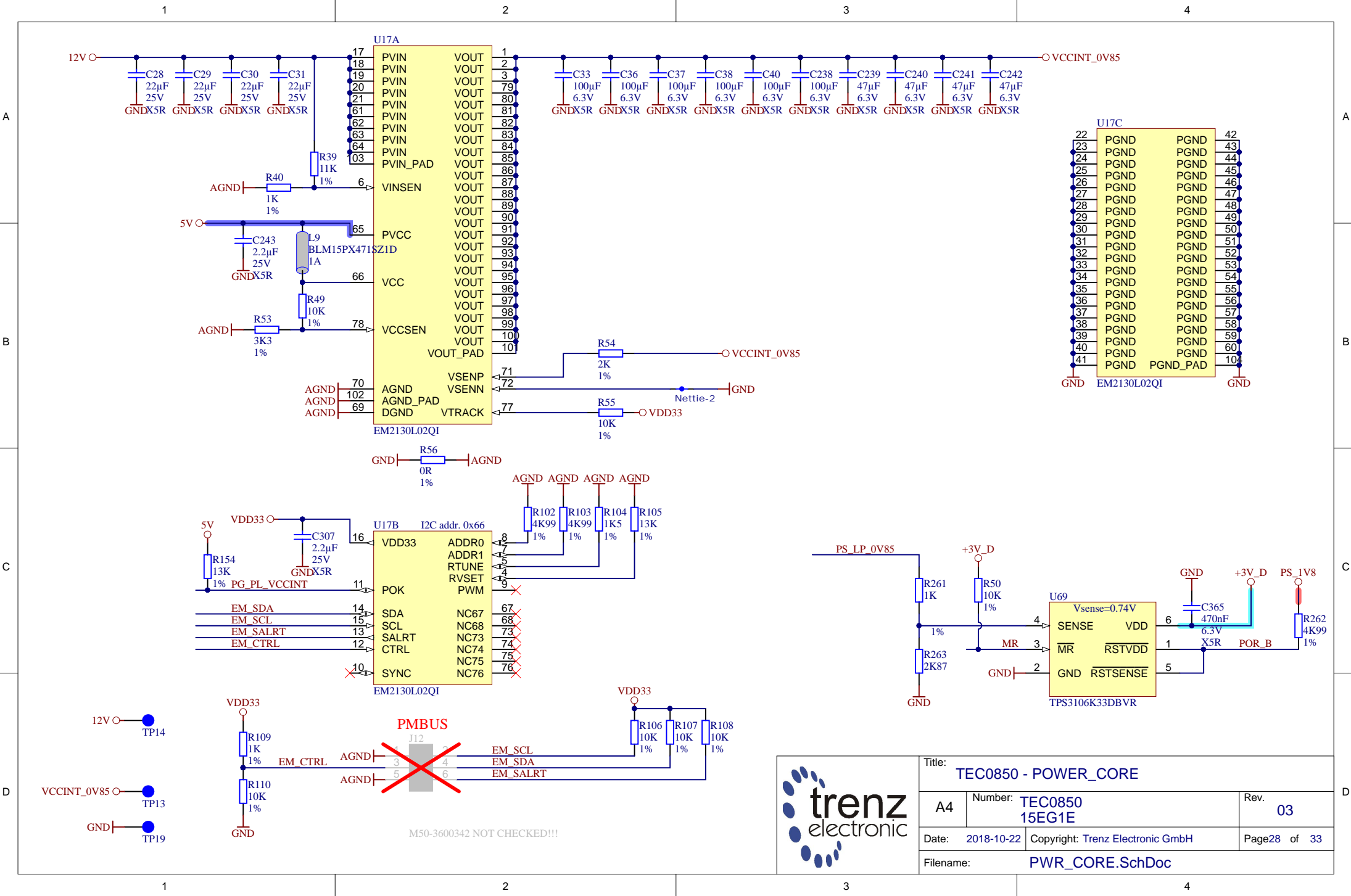



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| Title: TEC0850 - DAC1_DAC2 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 26 of 33 |
| Filename: DAC12_8bit.SchDoc | | |

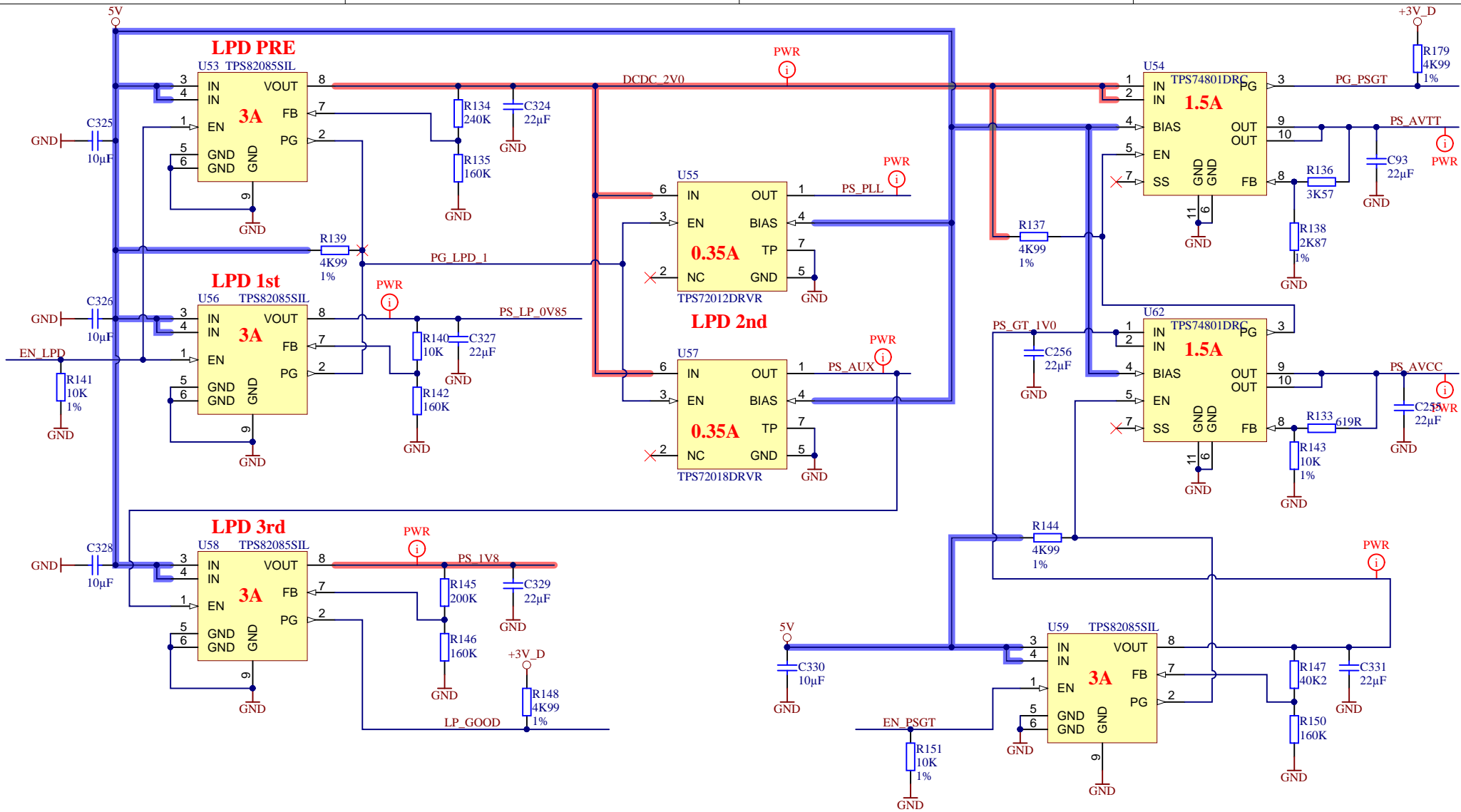




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| Title: TEC0850 - DAC3_DAC4 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH | Page 27 of 33 |
| Filename: DAC34_8bit.SchDoc | | |



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|---|--|----------------------------------|-----------------------------|------------------------|
|  | | | Title: TEC0850 - POWER_CORE | |
| | | | A4 | Number: TEC0850 15EG1E |
| Date: 2018-10-22 | | Copyright: Trenz Electronic GmbH | | Page 28 of 33 |
| Filename: PWR_CORE.SchDoc | | | | |



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|-----------------------------|---------------------------------------|---------------|
| Title: TEC0850 - POWER1 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH / TT | Page 29 of 33 |
| Filename: POWER_PSLP.schdoc | | |

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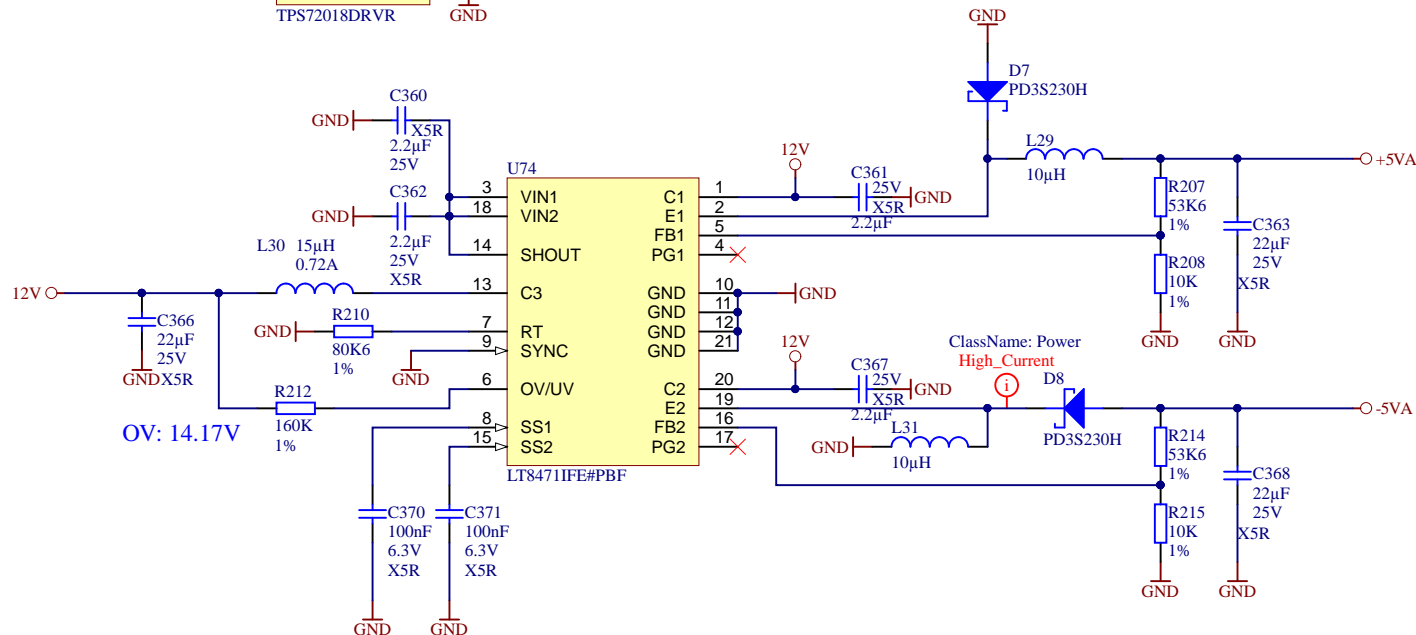
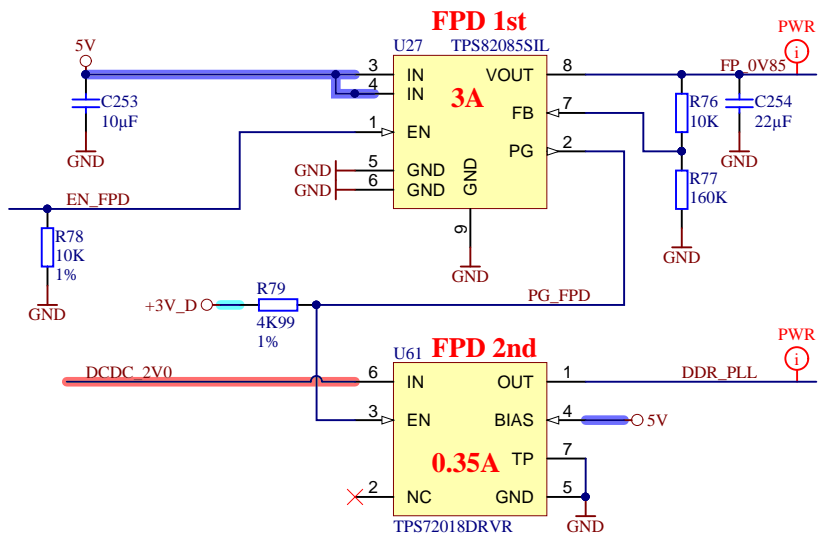
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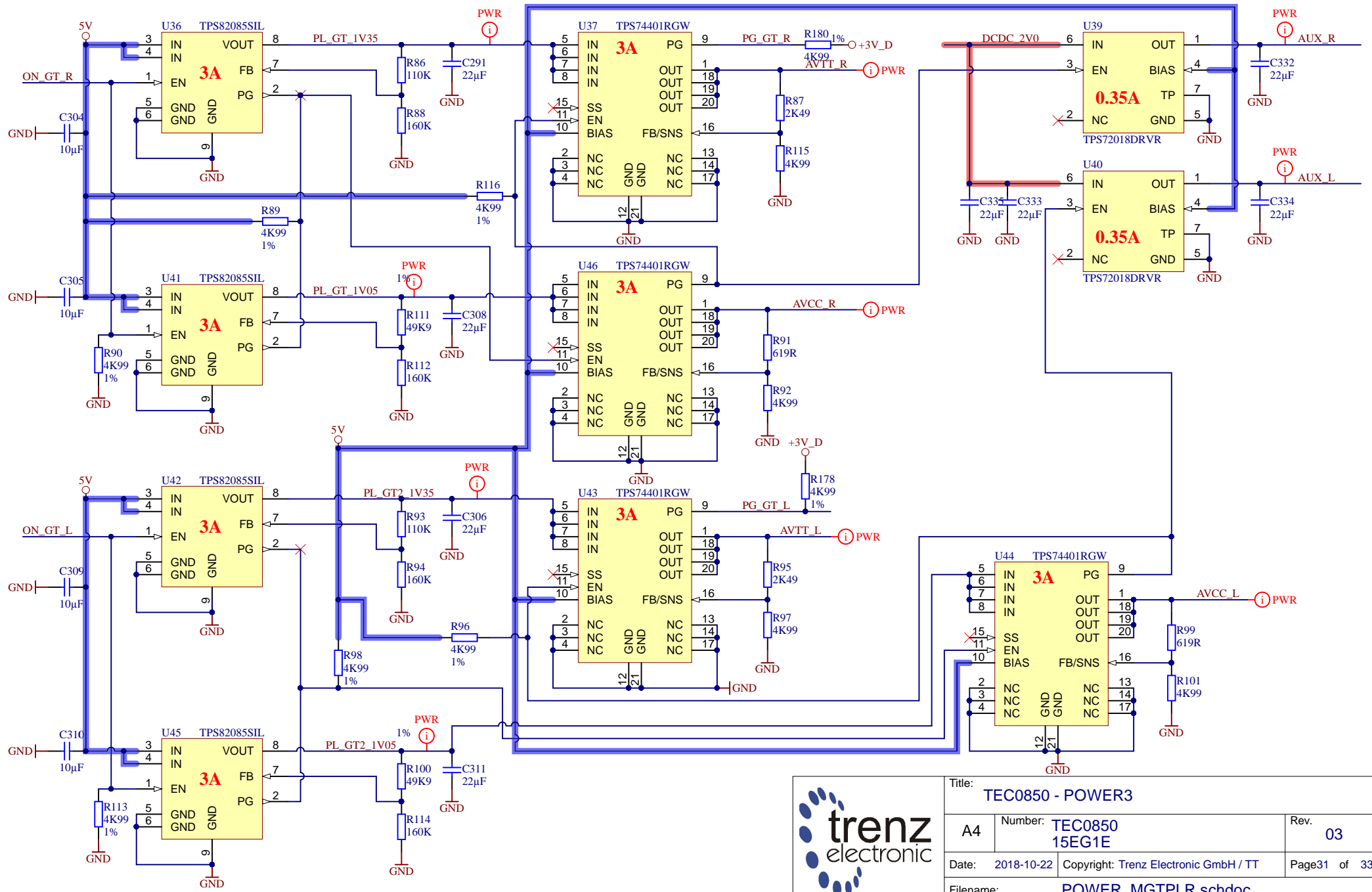
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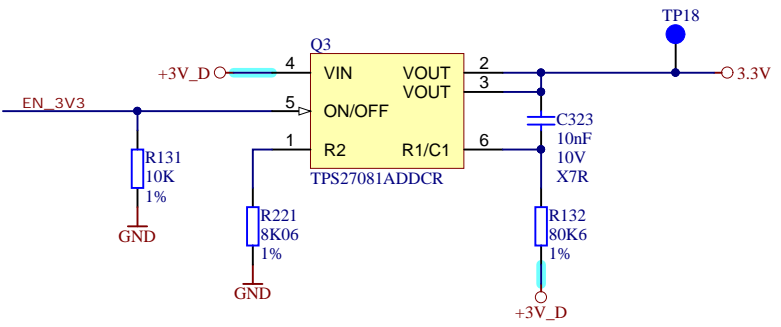
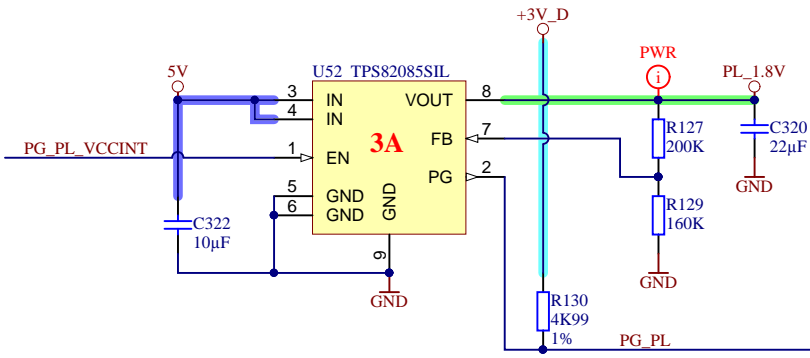
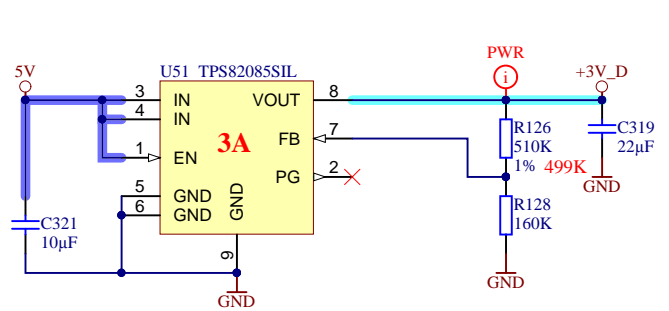
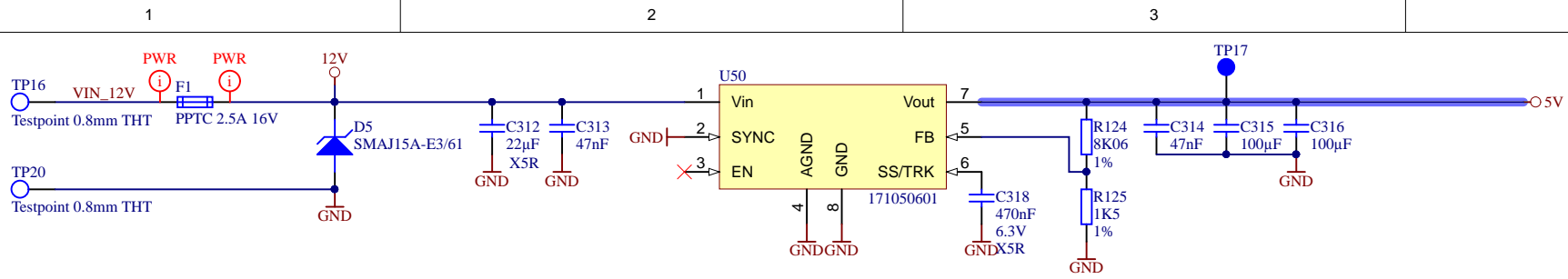
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| | Date: 2018-10-22 | Copyright: Trenz Electronic GmbH / TT |
| | Rev. 03 | Page30 of 33 |
| Filename: POWER_PSFP.schdoc | | |



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| Title: TEC0850 - POWER3 | | |
| A4 | Number: TEC0850 15EG1E | Rev. 03 |
| Date: 2018-10-22 | Copyright: Trenz Electronic GmbH / TT | |
| Page 31 of 33 | | Page 31 of 33 |
| Filename: POWER_MGTPLR.schdoc | | |



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|---|-------------------------------|---------------------------------------|---------------|
|  | Title: TEC0850 - POWER4 | | |
| | A4 | Number: TEC0850 15EG1E | Rev. 03 |
| | Date: 2018-10-22 | Copyright: Trenz Electronic GmbH / TT | Page 32 of 33 |
| | Filename: POWER_MGTPLL.schdoc | | |

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CHANGES REV01 to REV02

- 1) Fixed connection for U16 (Si53340-B-GM)
- 2) Added THT-testpoints for I2C-bus
- 3) Changed MEMS osc to TCXO osc , added LDO for TCXO osc
- 4) Use out9 from PLL, added dual output buffer ("1" -> MPSOC, B65; "2" -> J1, cPCI-serial)
- 5) Changed connector J12 (do not populated)
- 6) Added capacitors C372, C373 on the clock line (AC-coupling)
- 7) Changed OPs for DACs (LT6200IS6 -> THS4631D)
- 8) Added additional DCDC (+/-5V) for THS4631D
- 9) Added THT-testpoints for VIN/GND
- 10) full update lib

CHANGES REV02 to REV03

- 1) Fixed connection for U74 (LT8471IFE#PBF)
- 2) Added additional resistors R219/R220
- 3) Fixed connection for Y2 (CM2012-2pad)
- 4) Changed U69 (TPS3106E09DBVR -> TPS3106K33DBVR)
- 5) Changed U73 (LTC6957IDD-2#PBF -> Si53340-B-GM)
- 6) Optimized BOM
- 7) full update lib

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