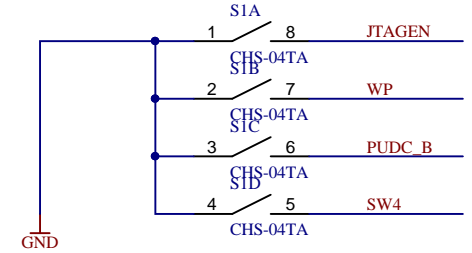
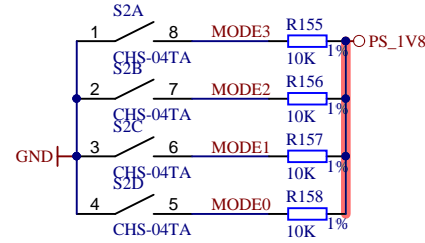
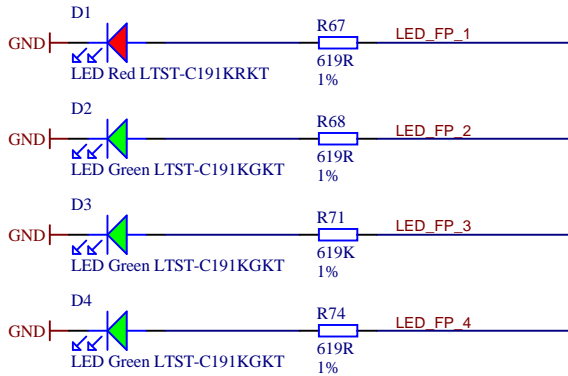
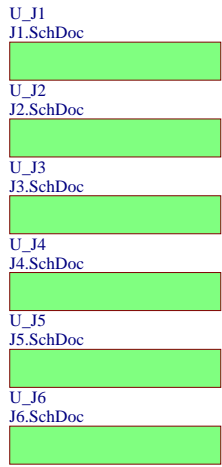
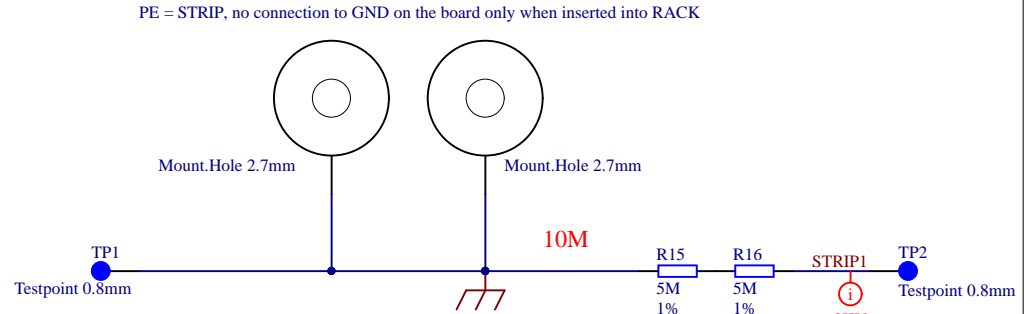
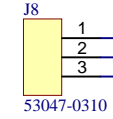
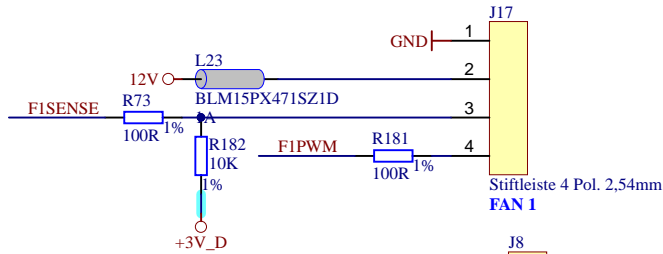
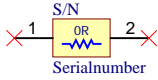


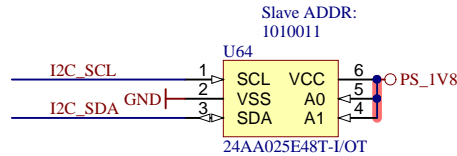
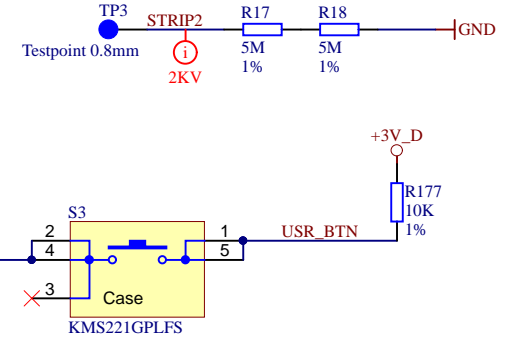
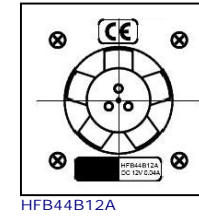
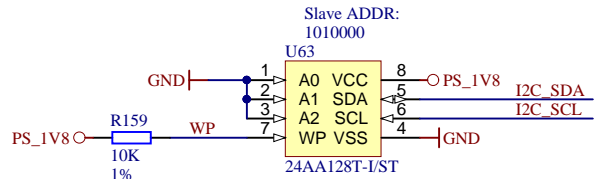
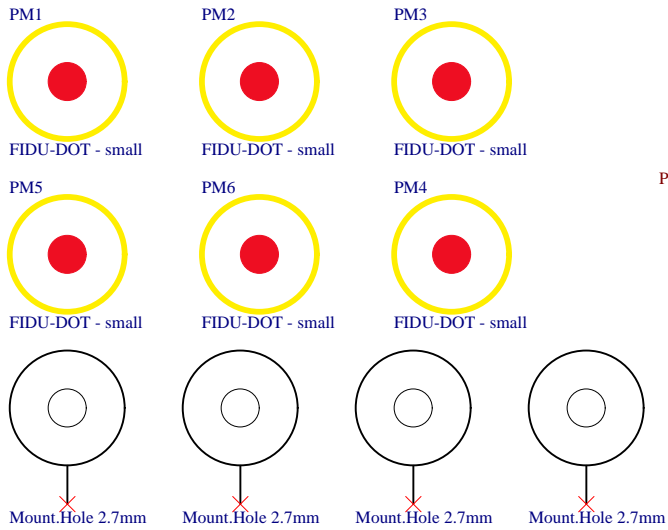
A



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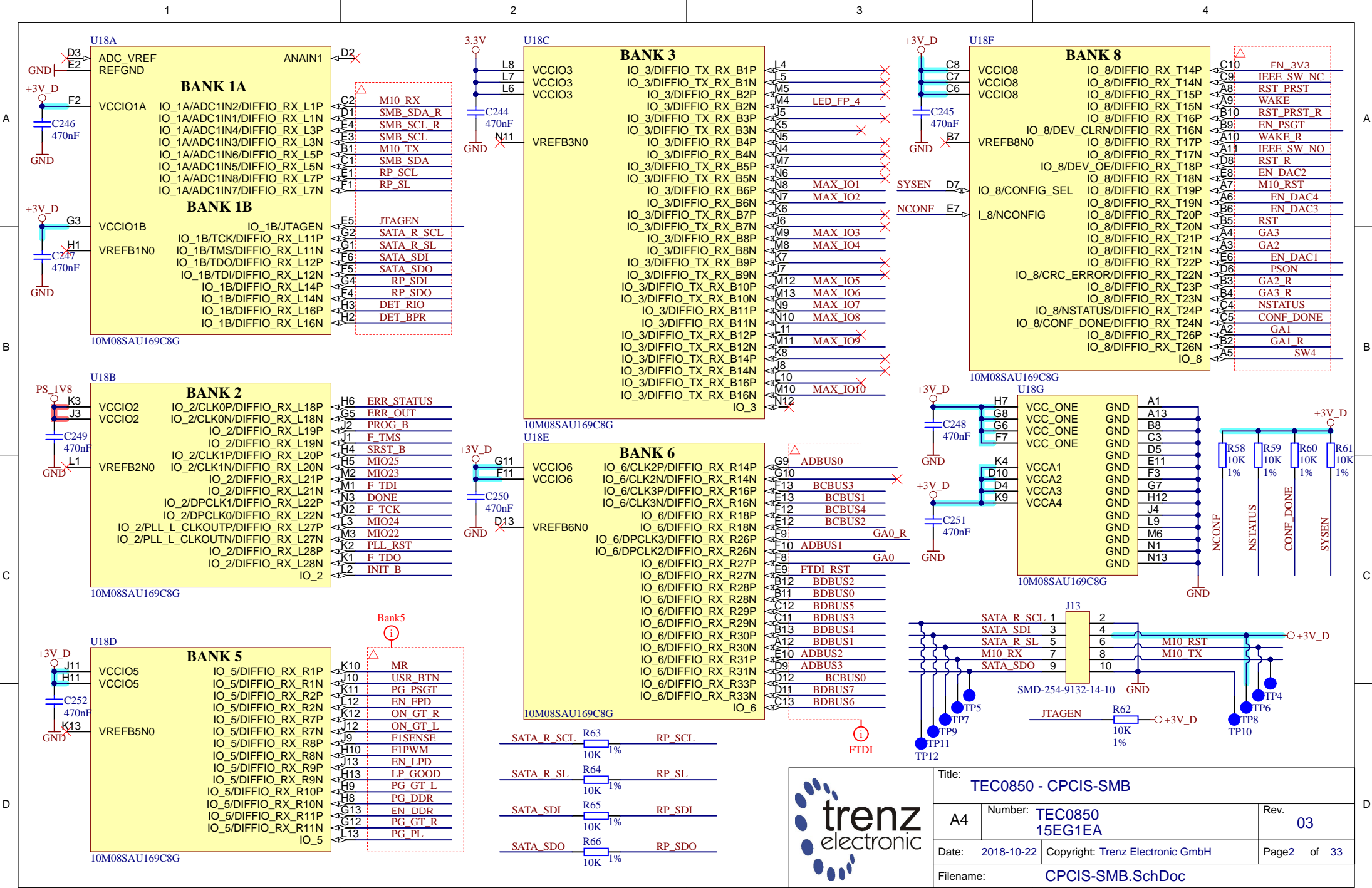


C



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				Title: <b>TEC0850 - CPCIS-SMB</b>	
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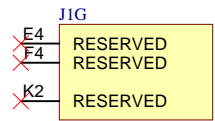
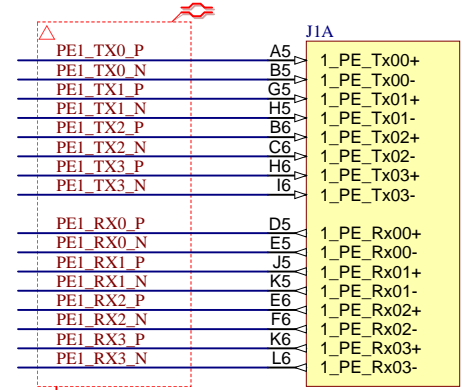
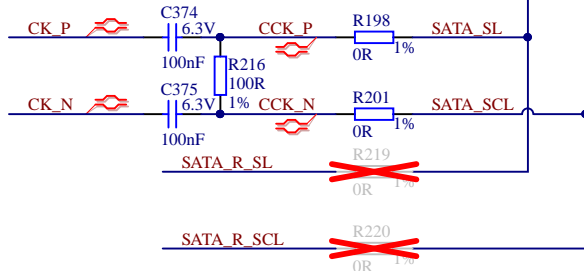
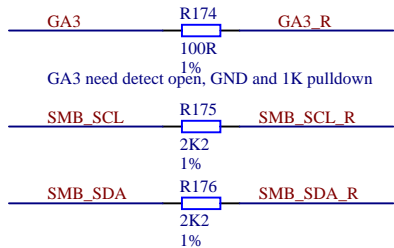
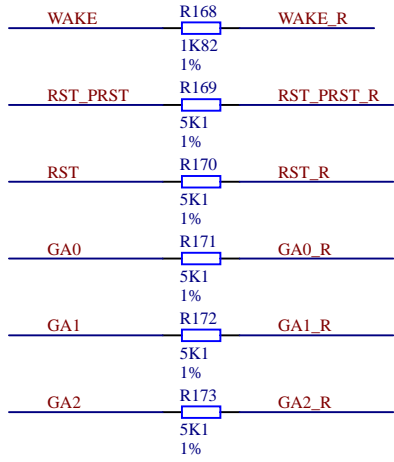
C

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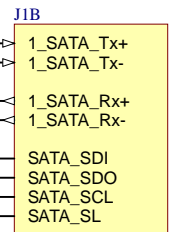
D

1.8, 2.2 and 5.1K are REQUIRED BY CPCI-S do not optimize to other values

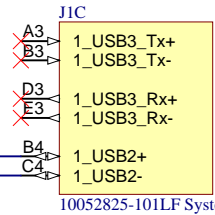


10052825-101LF System Slot P1

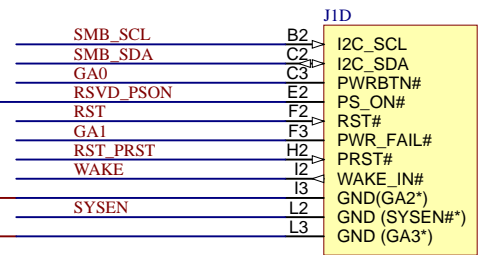
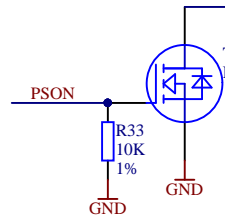
10052825-101LF System Slot P1



10052825-101LF System Slot P1

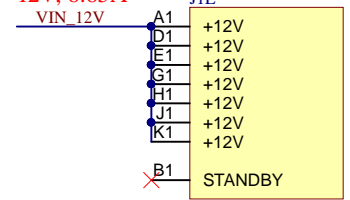


10052825-101LF System Slot P1

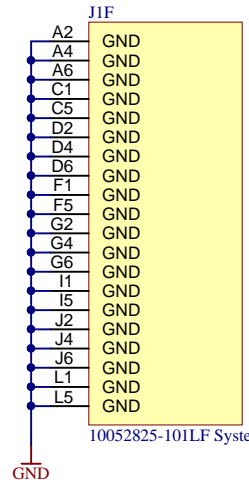


10052825-101LF System Slot P1

12V, 6.65A



10052825-101LF System Slot P1



10052825-101LF System Slot P1



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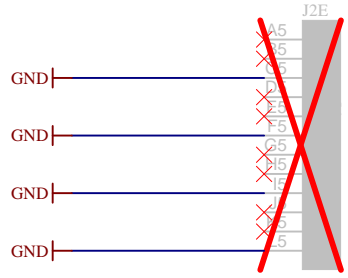
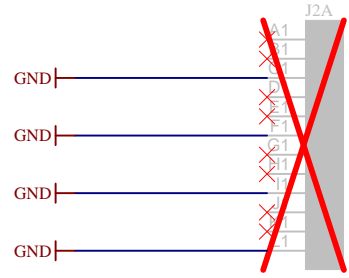
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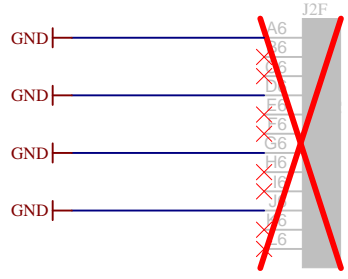
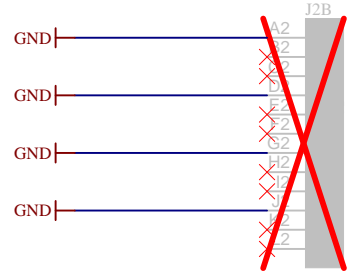
A

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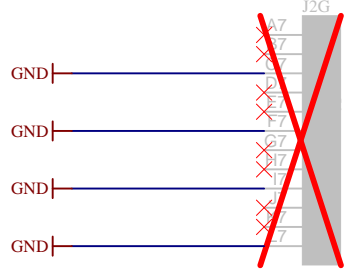
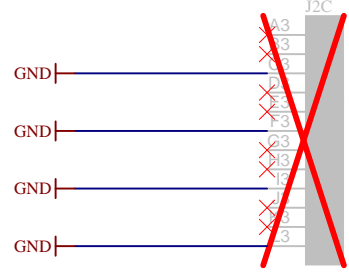
B

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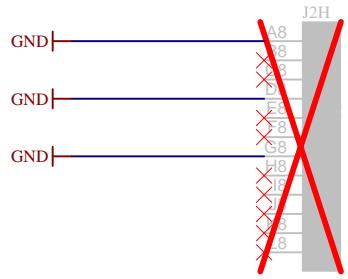
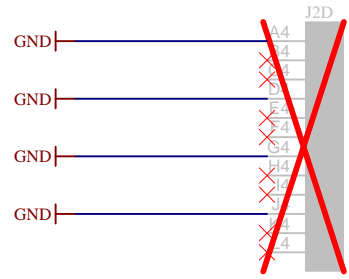
C

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Title: <b>TEC0850 - J2</b>		
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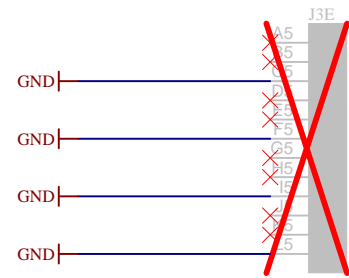
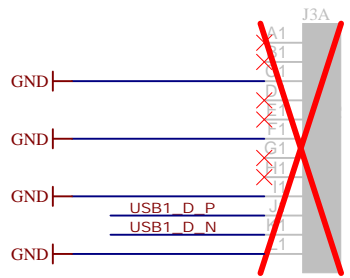
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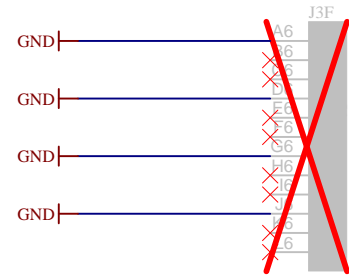
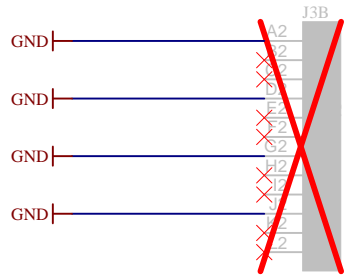
A

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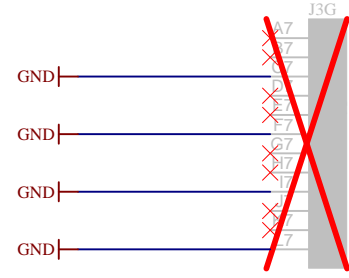
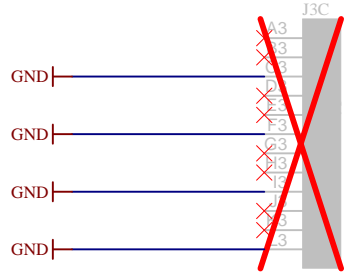
B

B



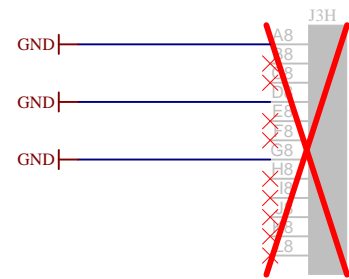
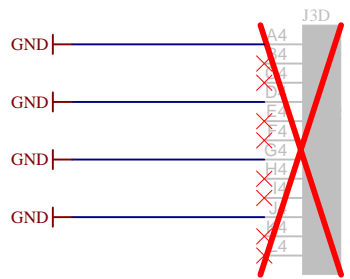
C

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Title: <b>TEC0850 - J3</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
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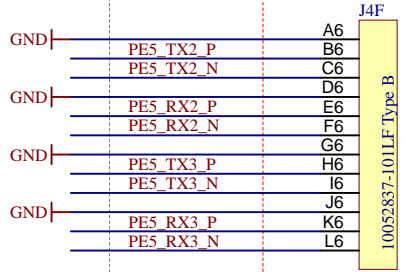
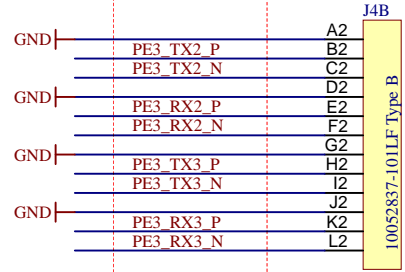
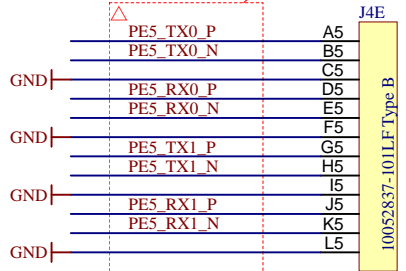
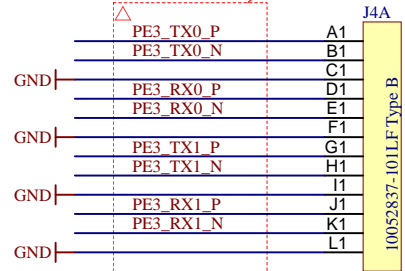
B

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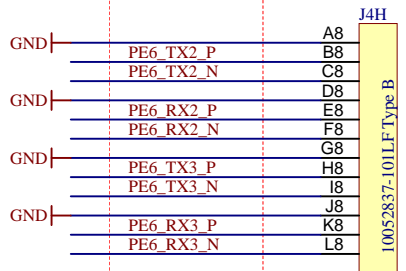
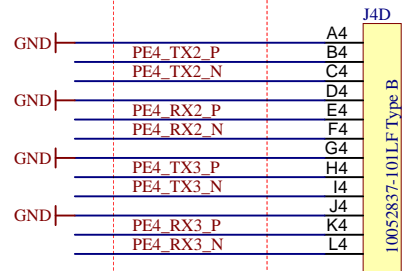
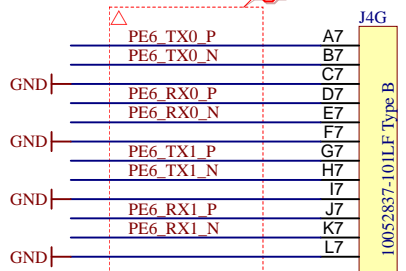
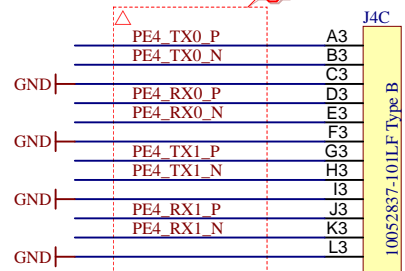
D

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PE3

PE5



PE4

PE6



Title: <b>TEC0850 - J4</b>		
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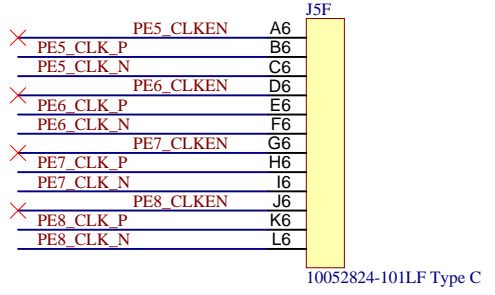
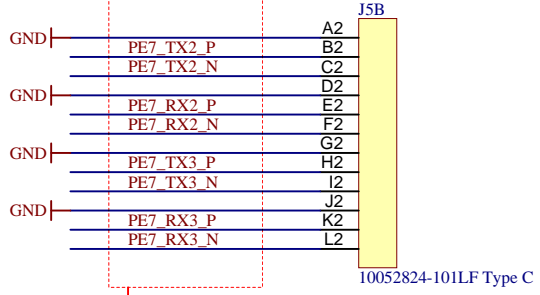
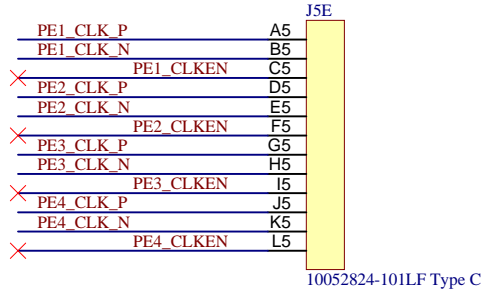
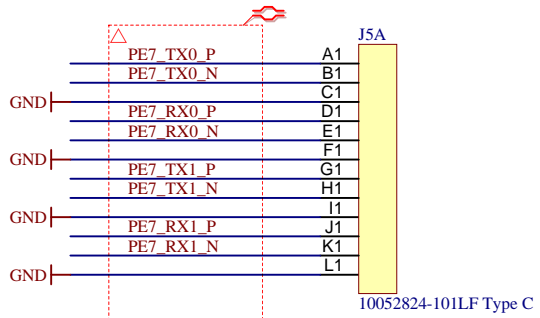
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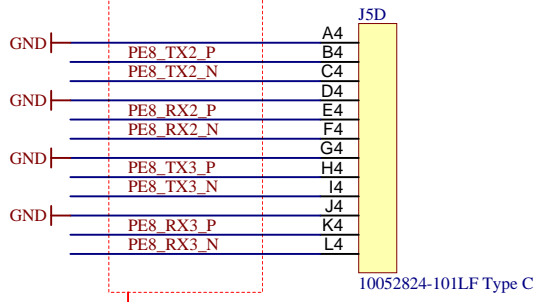
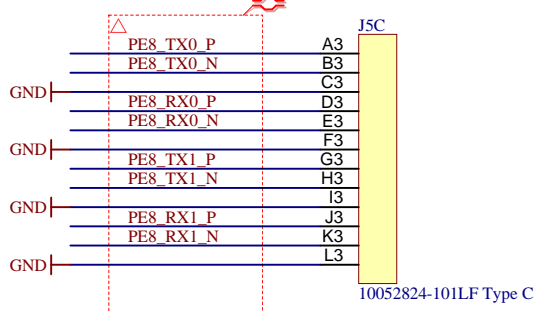
C

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PE7



①  
PE8



Title: <b>TEC0850 - J5</b>		
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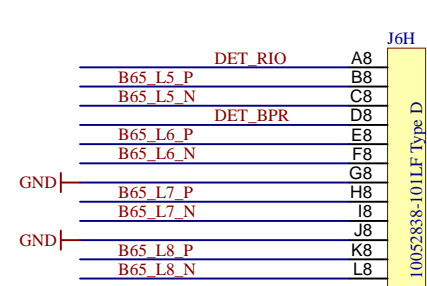
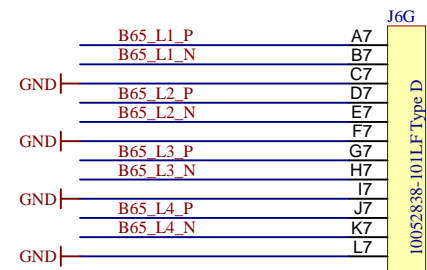
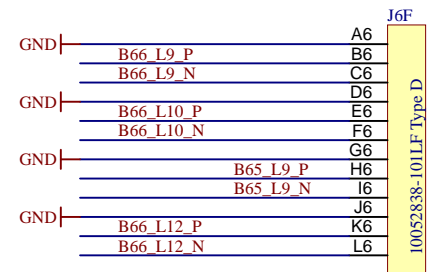
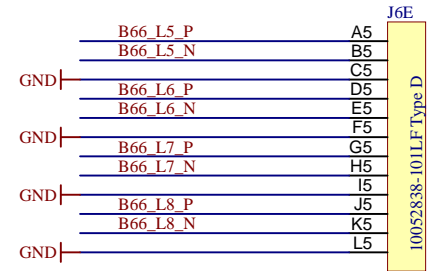
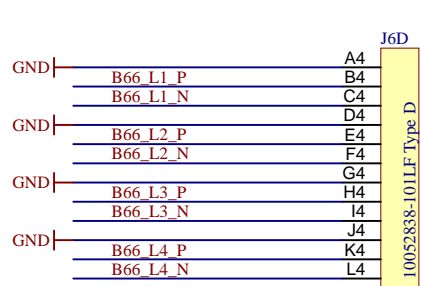
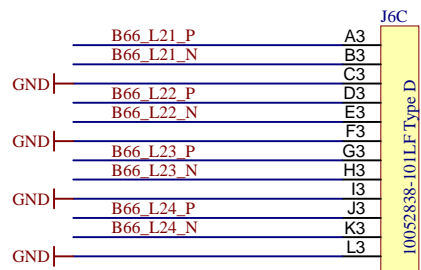
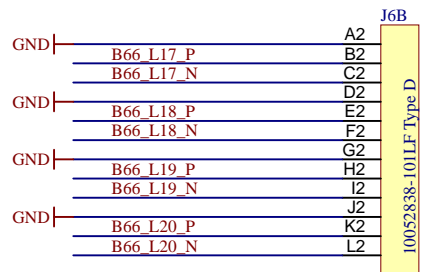
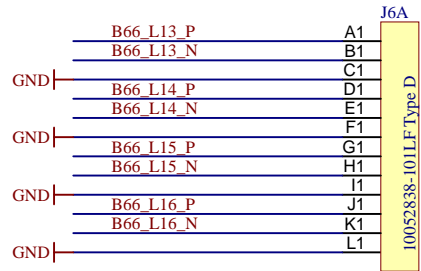
B

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Title: <b>TEC0850 - J6</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
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Filename: <b>J6.SchDoc</b>		

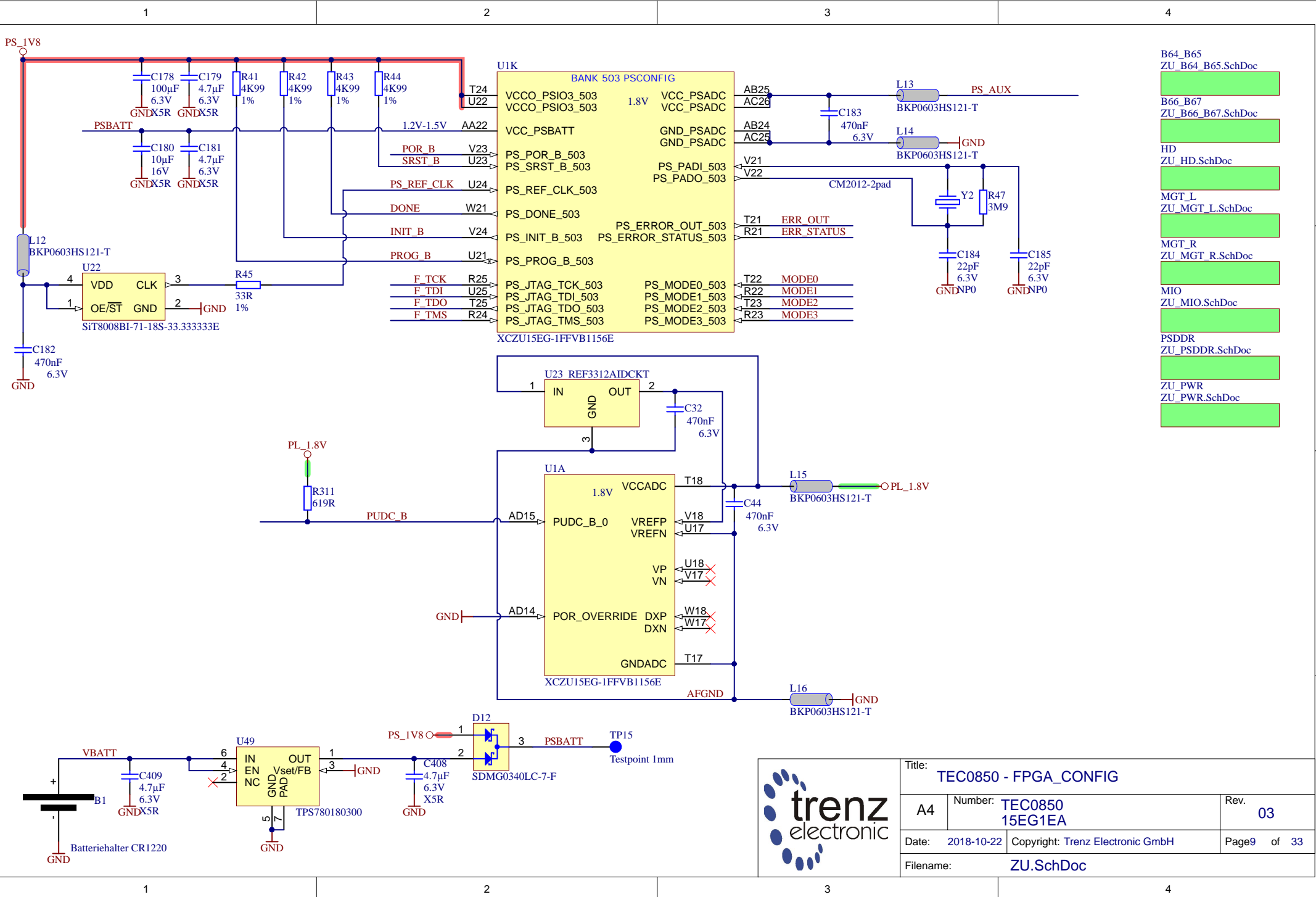
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- B64\_B65  
ZU\_B64\_B65.SchDoc
- B66\_B67  
ZU\_B66\_B67.SchDoc
- HD  
ZU\_HD.SchDoc
- MGT\_L  
ZU\_MGT\_L.SchDoc
- MGT\_R  
ZU\_MGT\_R.SchDoc
- MIO  
ZU\_MIO.SchDoc
- PSDDR  
ZU\_PSDDR.SchDoc
- ZU\_PWR  
ZU\_PWR.SchDoc



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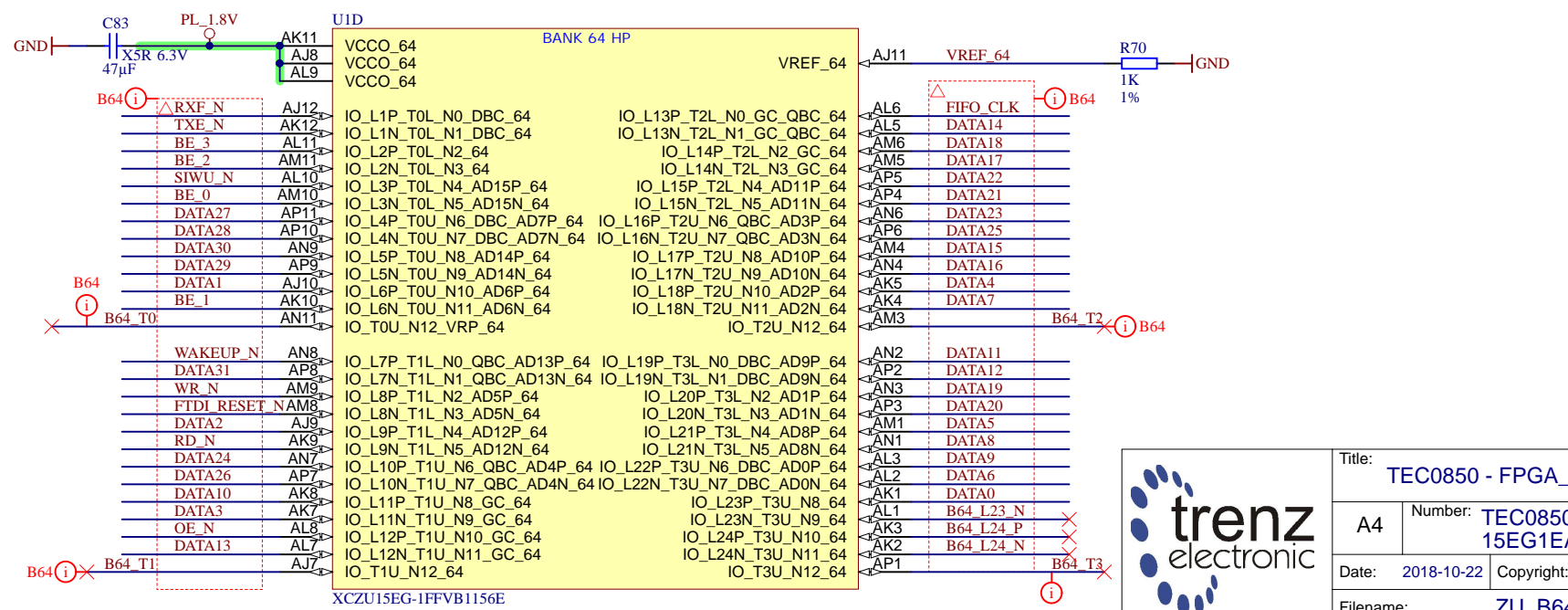
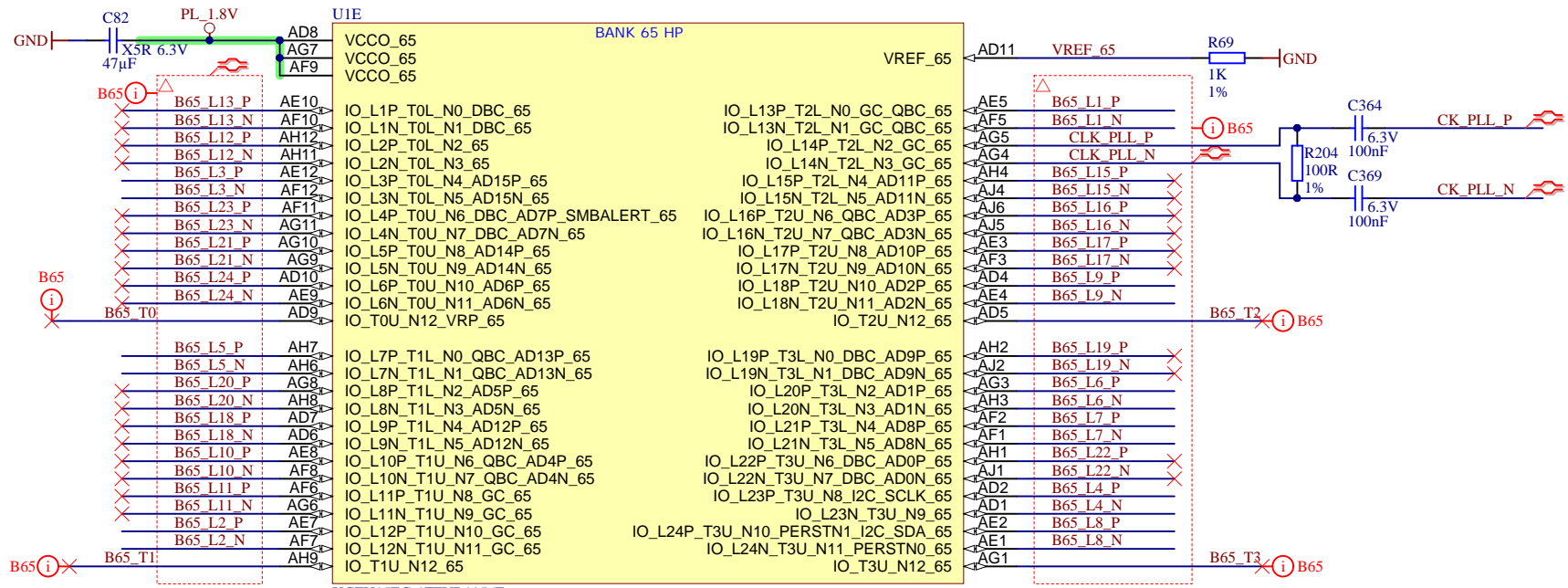
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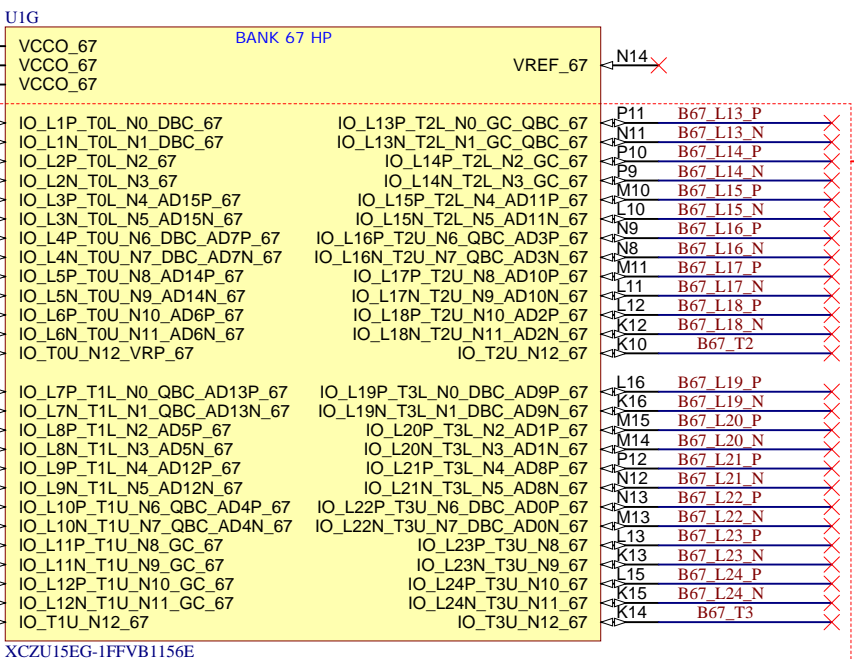
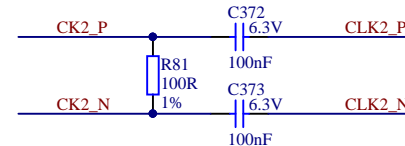
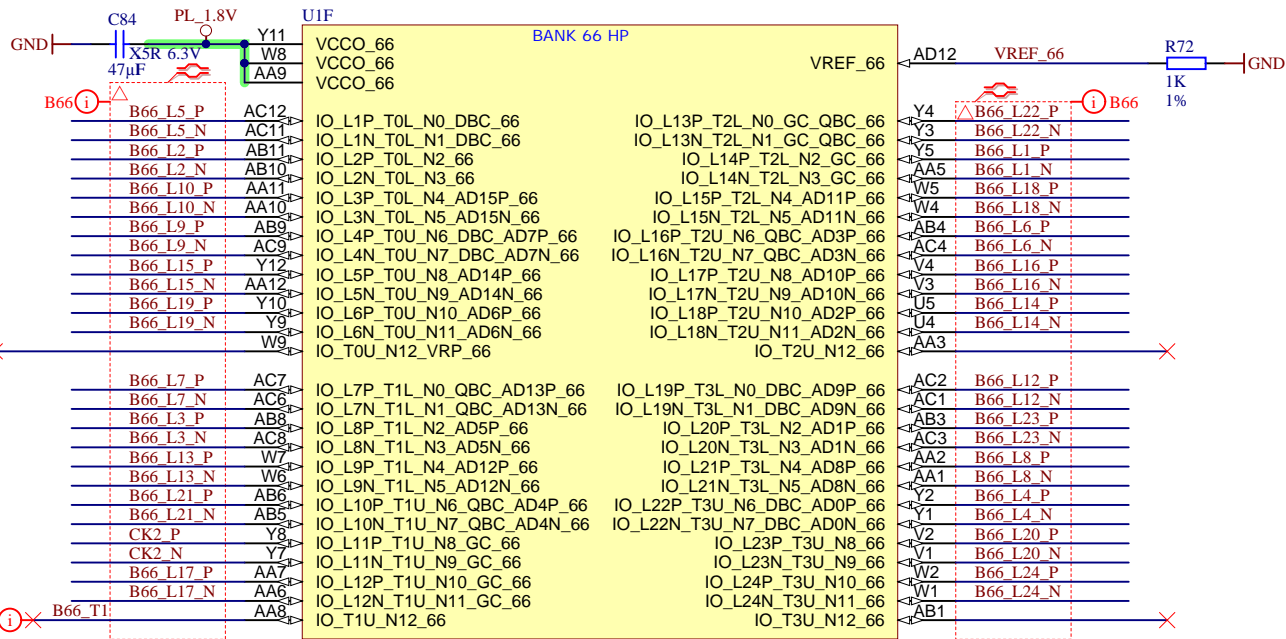
Title: <b>TEC0850 - FPGA_B64_B65</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>10</b> of <b>33</b>
Filename: <b>ZU_B64_B65.SchDoc</b>		

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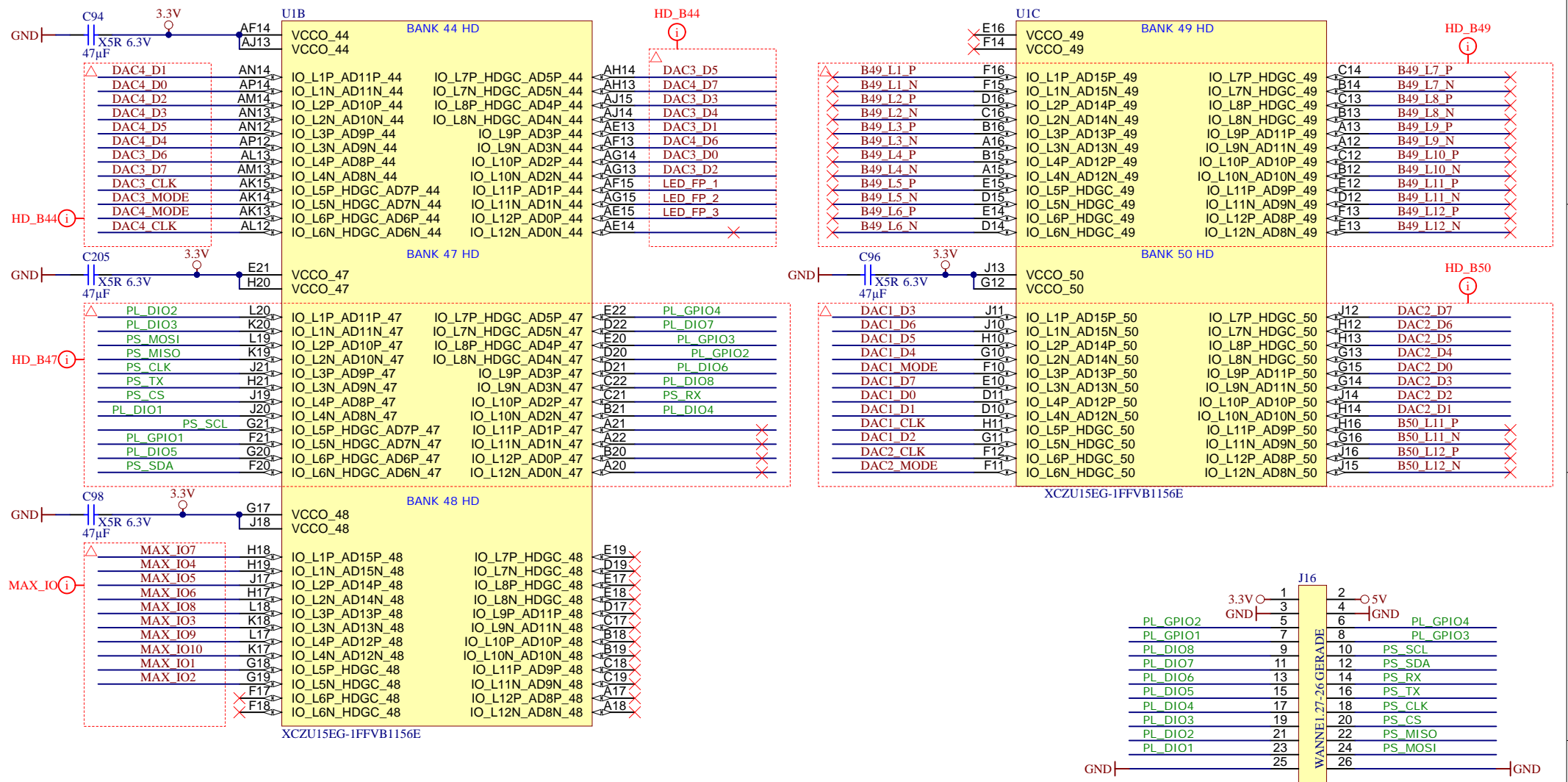
Title: <b>TEC0850 - FPGA_B66_B67</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>11</b> of <b>33</b>
Filename: <b>ZU_B66_B67.SchDoc</b>		

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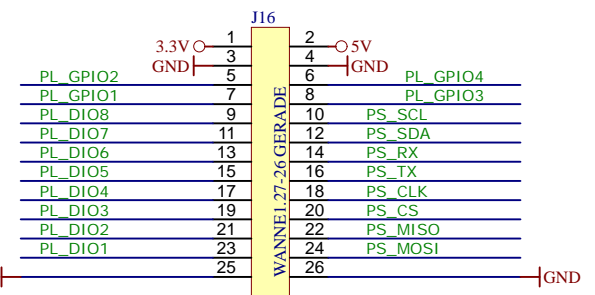
2

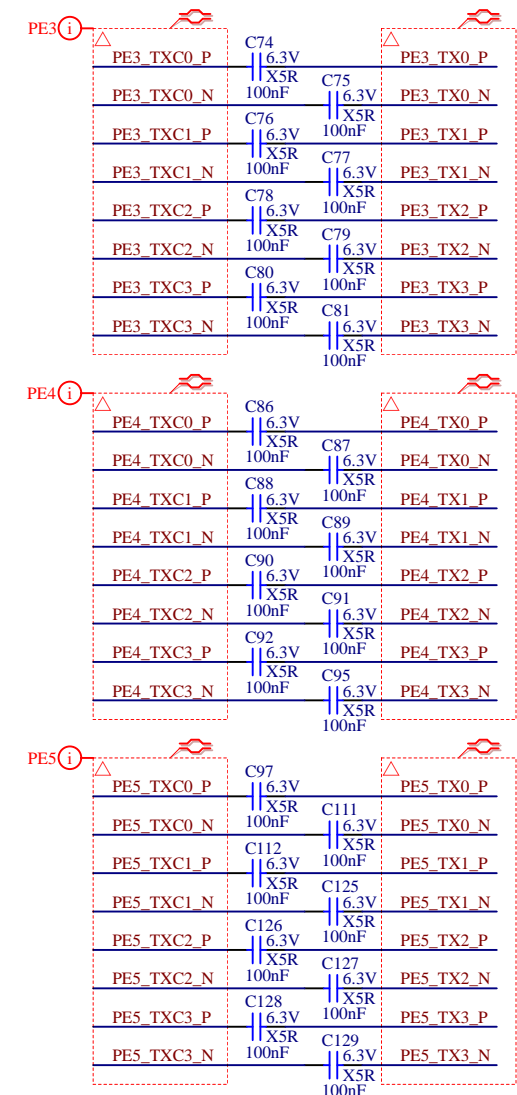
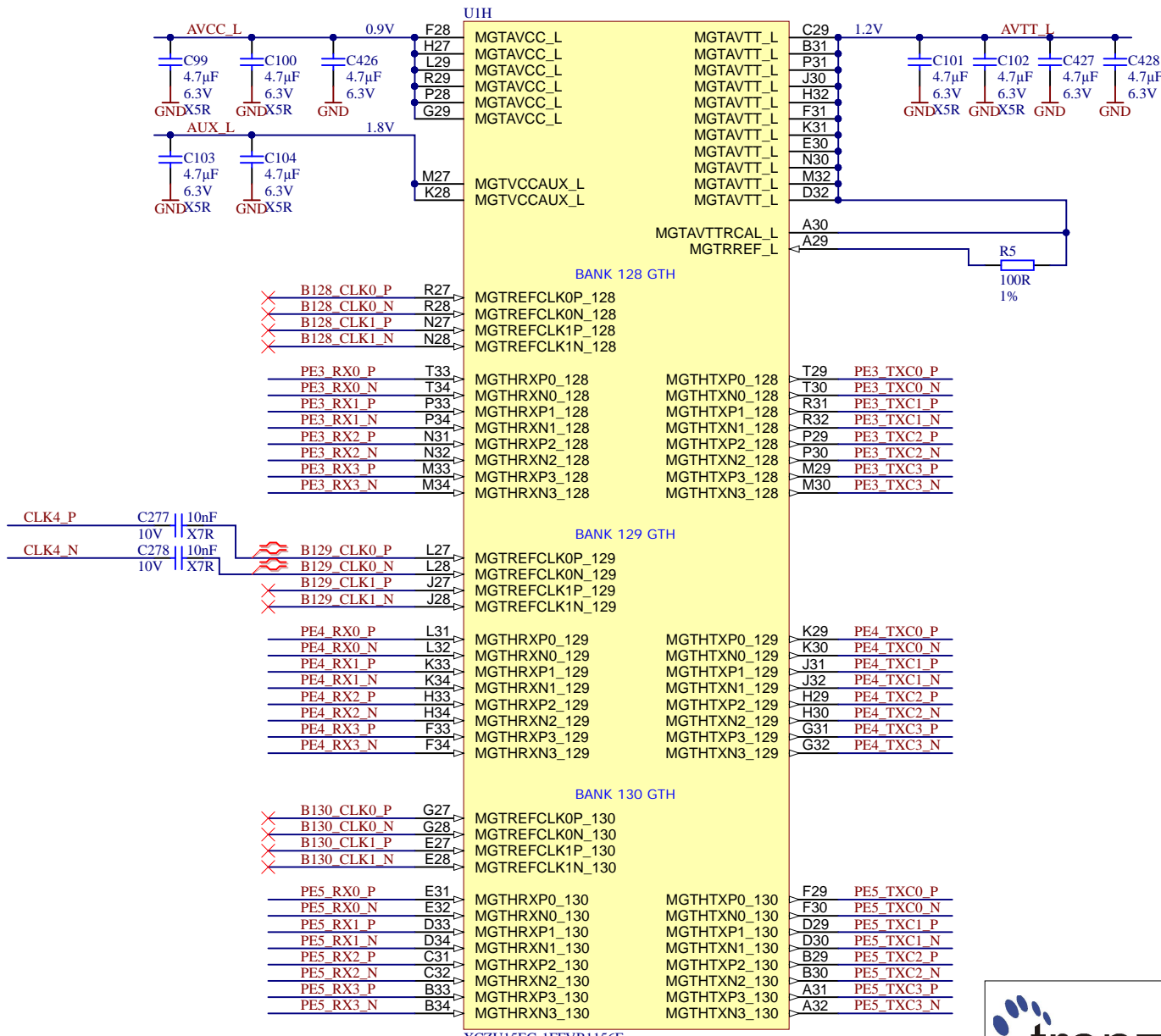
3

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Title: <b>TEC0850 - FPGA_HD</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
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A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>13</b> of <b>33</b>
Filename: <b>ZU_MGT_L.SchDoc</b>		



A

B

C

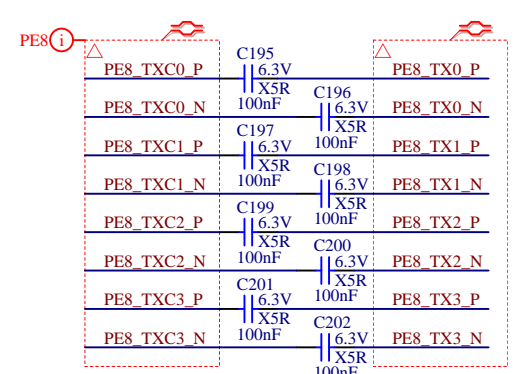
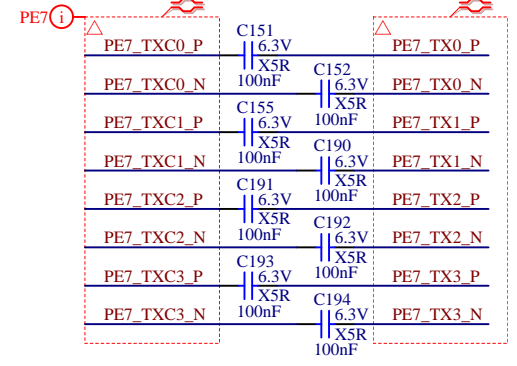
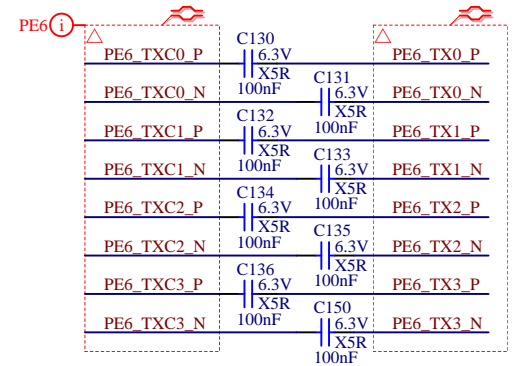
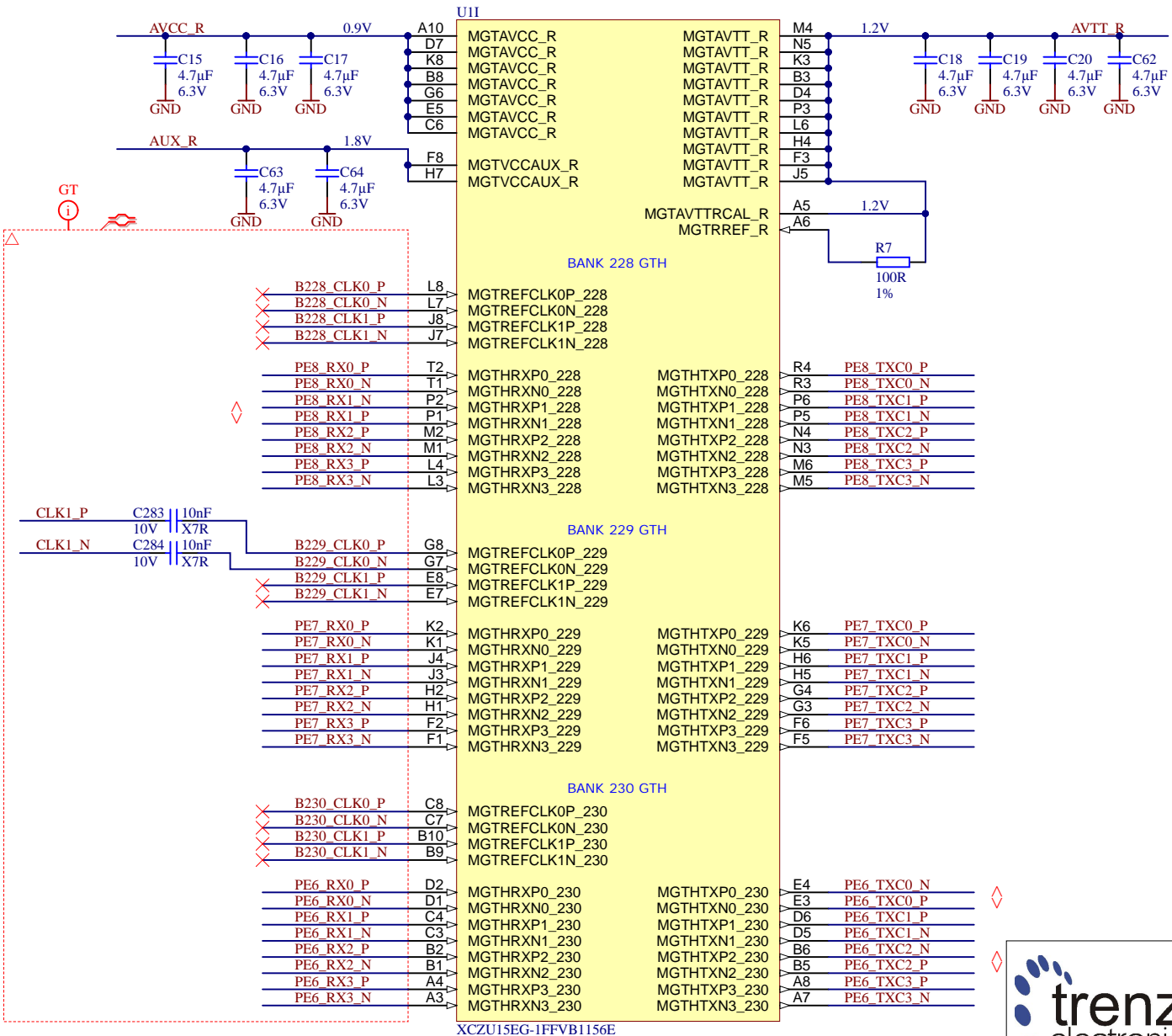
D

A

B

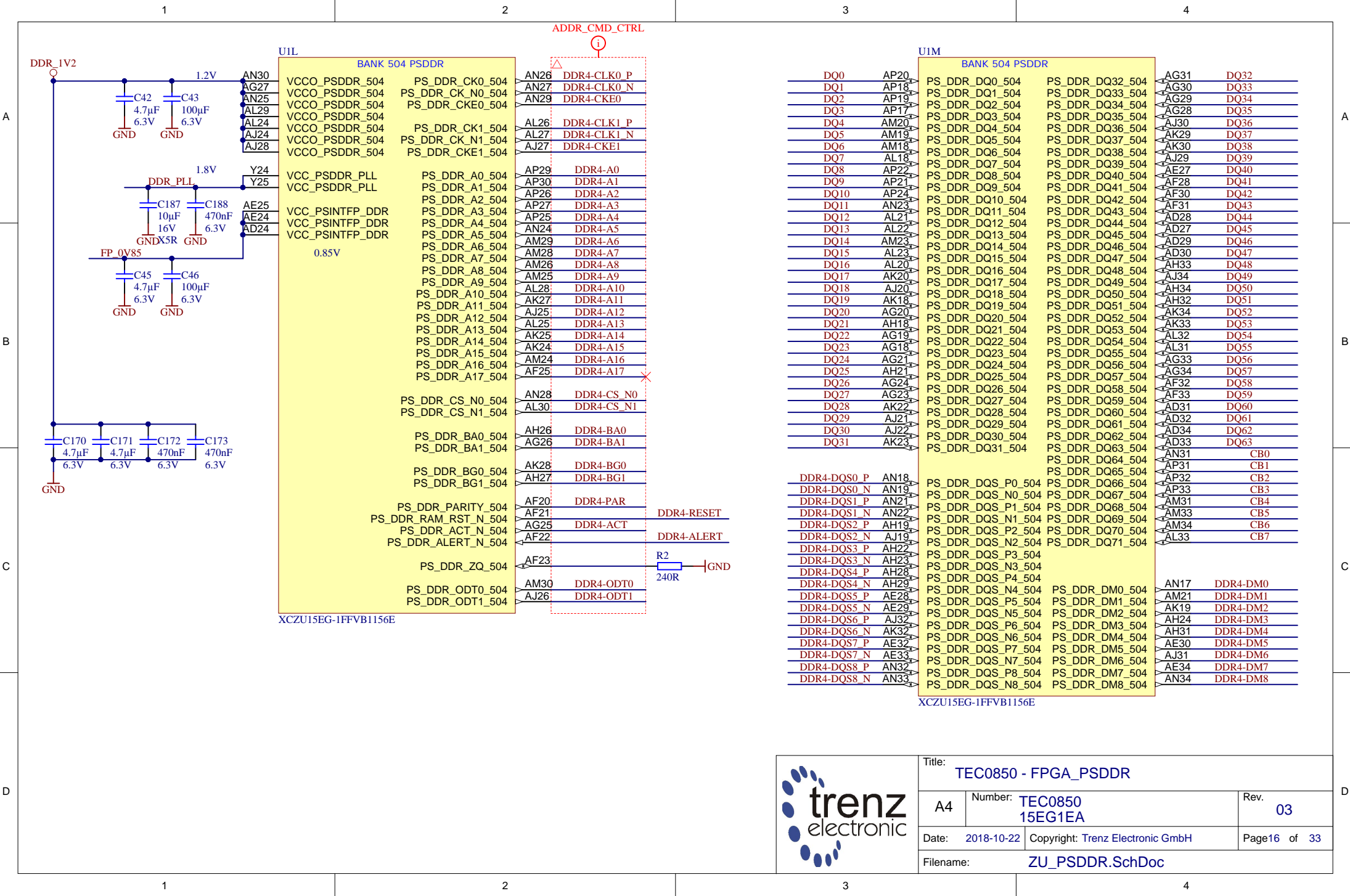
C

D



Title: <b>TEC0850 - FPGA_MGT_R</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>14</b> of <b>33</b>
Filename: <b>ZU_MGT_R.SchDoc</b>		





ADDR\_CMD\_CTRL

UI1

BANK 504 PSDDR

VCCO_PSSDR_504	PS_DDR_CK0_504
VCCO_PSSDR_504	PS_DDR_CK_N0_504
VCCO_PSSDR_504	PS_DDR_CKE0_504
VCCO_PSSDR_504	PS_DDR_CK1_504
VCCO_PSSDR_504	PS_DDR_CK_N1_504
VCCO_PSSDR_504	PS_DDR_CKE1_504
VCC_PSDDDR_PLL	PS_DDR_A0_504
VCC_PSDDDR_PLL	PS_DDR_A1_504
VCC_PSDDDR_PLL	PS_DDR_A2_504
VCC_PSDDDR_PLL	PS_DDR_A3_504
VCC_PSDDDR_PLL	PS_DDR_A4_504
VCC_PSDDDR_PLL	PS_DDR_A5_504
VCC_PSDDDR_PLL	PS_DDR_A6_504
VCC_PSDDDR_PLL	PS_DDR_A7_504
VCC_PSDDDR_PLL	PS_DDR_A8_504
VCC_PSDDDR_PLL	PS_DDR_A9_504
VCC_PSDDDR_PLL	PS_DDR_A10_504
VCC_PSDDDR_PLL	PS_DDR_A11_504
VCC_PSDDDR_PLL	PS_DDR_A12_504
VCC_PSDDDR_PLL	PS_DDR_A13_504
VCC_PSDDDR_PLL	PS_DDR_A14_504
VCC_PSDDDR_PLL	PS_DDR_A15_504
VCC_PSDDDR_PLL	PS_DDR_A16_504
VCC_PSDDDR_PLL	PS_DDR_A17_504
PS_DDR_CS_N0_504	
PS_DDR_CS_N1_504	
PS_DDR_BA0_504	
PS_DDR_BA1_504	
PS_DDR_BG0_504	
PS_DDR_BG1_504	
PS_DDR_PARITY_504	
PS_DDR_RAM_RST_N_504	
PS_DDR_ACT_N_504	
PS_DDR_ALERT_N_504	
PS_DDR_ZQ_504	
PS_DDR_ODT0_504	
PS_DDR_ODT1_504	

0.85V

XCZU15EG-1FFVB1156E

U1M

BANK 504 PSDDR

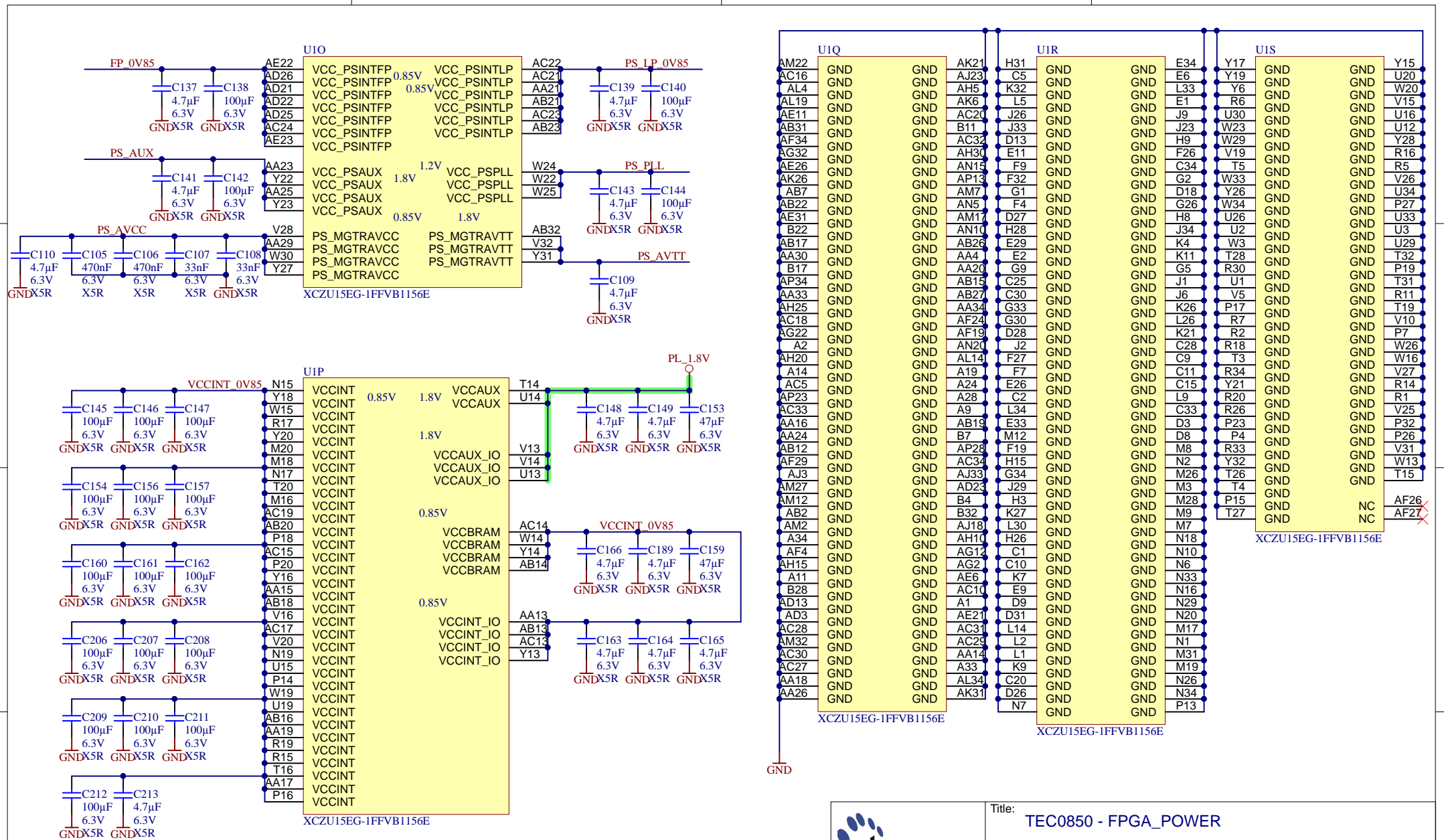
DQ0	AP20	PS_DDR_DQ0_504	PS_DDR_DQ32_504	AG31	DQ32
DQ1	AP18	PS_DDR_DQ1_504	PS_DDR_DQ33_504	AG30	DQ33
DQ2	AP19	PS_DDR_DQ2_504	PS_DDR_DQ34_504	AG29	DQ34
DQ3	AP17	PS_DDR_DQ3_504	PS_DDR_DQ35_504	AG28	DQ35
DQ4	AM20	PS_DDR_DQ4_504	PS_DDR_DQ36_504	AJ30	DQ36
DQ5	AM19	PS_DDR_DQ5_504	PS_DDR_DQ37_504	AK29	DQ37
DQ6	AM18	PS_DDR_DQ6_504	PS_DDR_DQ38_504	AK30	DQ38
DQ7	AL18	PS_DDR_DQ7_504	PS_DDR_DQ39_504	AJ29	DQ39
DQ8	AP22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	AE27	DQ40
DQ9	AP21	PS_DDR_DQ9_504	PS_DDR_DQ41_504	AF28	DQ41
DQ10	AP24	PS_DDR_DQ10_504	PS_DDR_DQ42_504	AF30	DQ42
DQ11	AM23	PS_DDR_DQ11_504	PS_DDR_DQ43_504	AF31	DQ43
DQ12	AL21	PS_DDR_DQ12_504	PS_DDR_DQ44_504	AD28	DQ44
DQ13	AL22	PS_DDR_DQ13_504	PS_DDR_DQ45_504	AD27	DQ45
DQ14	AM23	PS_DDR_DQ14_504	PS_DDR_DQ46_504	AD29	DQ46
DQ15	AL23	PS_DDR_DQ15_504	PS_DDR_DQ47_504	AD30	DQ47
DQ16	AL20	PS_DDR_DQ16_504	PS_DDR_DQ48_504	AH33	DQ48
DQ17	AK20	PS_DDR_DQ17_504	PS_DDR_DQ49_504	AJ34	DQ49
DQ18	AJ20	PS_DDR_DQ18_504	PS_DDR_DQ50_504	AH34	DQ50
DQ19	AK18	PS_DDR_DQ19_504	PS_DDR_DQ51_504	AH32	DQ51
DQ20	AG20	PS_DDR_DQ20_504	PS_DDR_DQ52_504	AK34	DQ52
DQ21	AH18	PS_DDR_DQ21_504	PS_DDR_DQ53_504	AK33	DQ53
DQ22	AG19	PS_DDR_DQ22_504	PS_DDR_DQ54_504	AL32	DQ54
DQ23	AG18	PS_DDR_DQ23_504	PS_DDR_DQ55_504	AL31	DQ55
DQ24	AG21	PS_DDR_DQ24_504	PS_DDR_DQ56_504	AG33	DQ56
DQ25	AH21	PS_DDR_DQ25_504	PS_DDR_DQ57_504	AG34	DQ57
DQ26	AG24	PS_DDR_DQ26_504	PS_DDR_DQ58_504	AF32	DQ58
DQ27	AG23	PS_DDR_DQ27_504	PS_DDR_DQ59_504	AF33	DQ59
DQ28	AK22	PS_DDR_DQ28_504	PS_DDR_DQ60_504	AD31	DQ60
DQ29	AJ21	PS_DDR_DQ29_504	PS_DDR_DQ61_504	AD32	DQ61
DQ30	AJ22	PS_DDR_DQ30_504	PS_DDR_DQ62_504	AD34	DQ62
DQ31	AK23	PS_DDR_DQ31_504	PS_DDR_DQ63_504	AD33	DQ63
			PS_DDR_DQ64_504	AN31	CB0
			PS_DDR_DQ65_504	AP31	CB1
			PS_DDR_DQ66_504	AP32	CB2
			PS_DDR_DQ67_504	AP33	CB3
			PS_DDR_DQ68_504	AM31	CB4
			PS_DDR_DQ69_504	AM33	CB5
			PS_DDR_DQ70_504	AM34	CB6
			PS_DDR_DQ71_504	AL33	CB7
DDR4-DQS0 P	AN18	PS_DDR_DQS_P0_504	PS_DDR_DQ65_504	AN17	DDR4-DM0
DDR4-DQS0 N	AN19	PS_DDR_DQS_N0_504	PS_DDR_DQ66_504	AM21	DDR4-DM1
DDR4-DQS1 P	AN21	PS_DDR_DQS_P1_504	PS_DDR_DQ67_504	AK19	DDR4-DM2
DDR4-DQS1 N	AN22	PS_DDR_DQS_N1_504	PS_DDR_DQ68_504	AH24	DDR4-DM3
DDR4-DQS2 P	AH19	PS_DDR_DQS_P2_504	PS_DDR_DQ69_504	AH31	DDR4-DM4
DDR4-DQS2 N	AJ19	PS_DDR_DQS_N2_504	PS_DDR_DQ70_504	AE30	DDR4-DM5
DDR4-DQS3 P	AH22	PS_DDR_DQS_P3_504	PS_DDR_DQ71_504	AJ31	DDR4-DM6
DDR4-DQS3 N	AH23	PS_DDR_DQS_N3_504		AE34	DDR4-DM7
DDR4-DQS4 P	AH28	PS_DDR_DQS_P4_504		AN34	DDR4-DM8
DDR4-DQS4 N	AH29	PS_DDR_DQS_N4_504	PS_DDR_DM0_504		
DDR4-DQS5 P	AE28	PS_DDR_DQS_P5_504	PS_DDR_DM1_504		
DDR4-DQS5 N	AE29	PS_DDR_DQS_N5_504	PS_DDR_DM2_504		
DDR4-DQS6 P	AJ32	PS_DDR_DQS_P6_504	PS_DDR_DM3_504		
DDR4-DQS6 N	AK32	PS_DDR_DQS_N6_504	PS_DDR_DM4_504		
DDR4-DQS7 P	AE32	PS_DDR_DQS_P7_504	PS_DDR_DM5_504		
DDR4-DQS7 N	AE33	PS_DDR_DQS_N7_504	PS_DDR_DM6_504		
DDR4-DQS8 P	AN32	PS_DDR_DQS_P8_504	PS_DDR_DM7_504		
DDR4-DQS8 N	AN33	PS_DDR_DQS_N8_504	PS_DDR_DM8_504		

XCZU15EG-1FFVB1156E



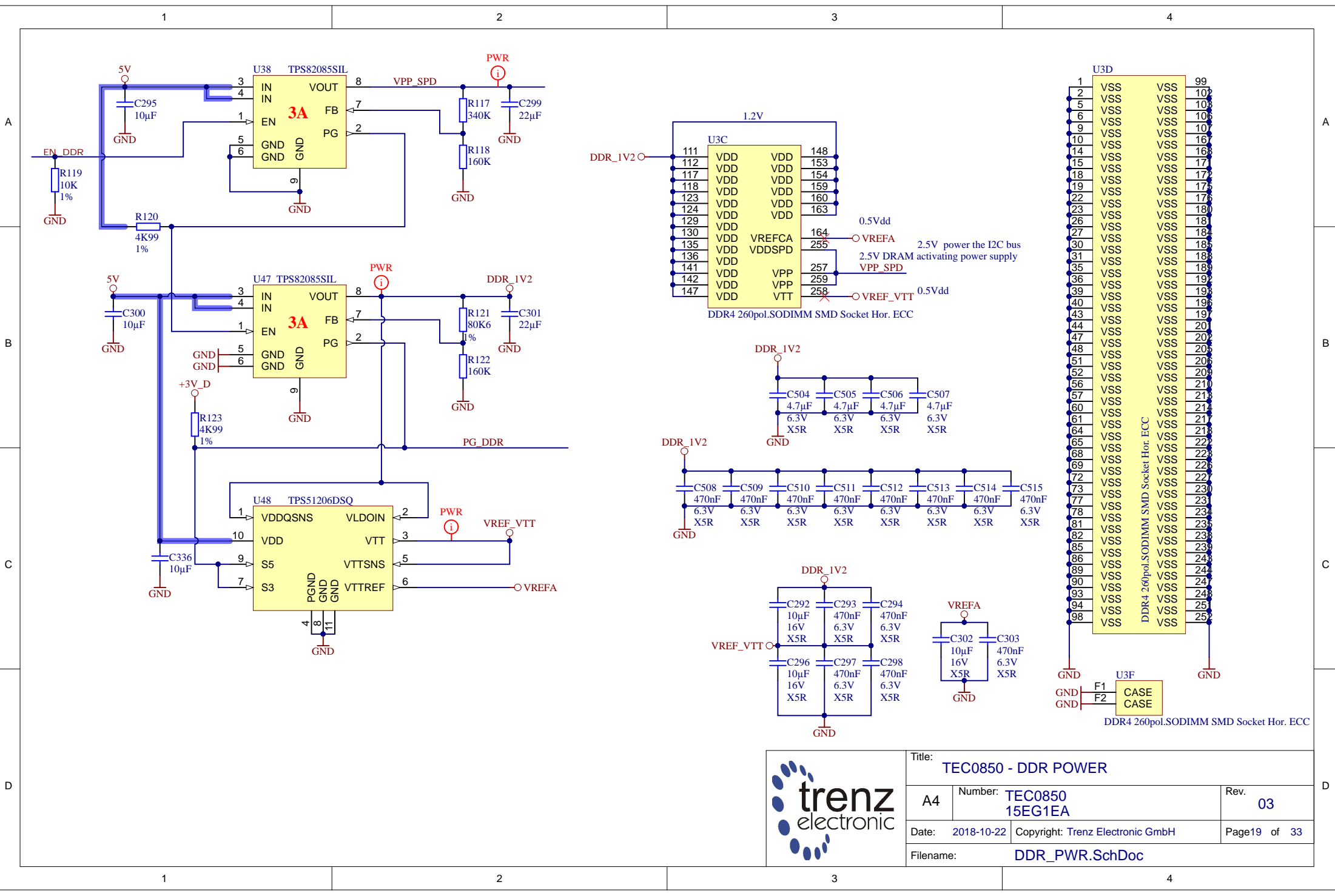
Title: <b>TEC0850 - FPGA_PSDDR</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>16</b> of <b>33</b>
Filename: <b>ZU_PSDDR.SchDoc</b>		



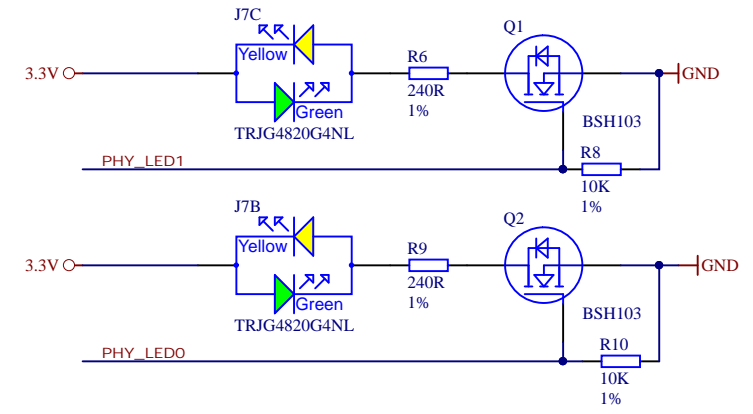
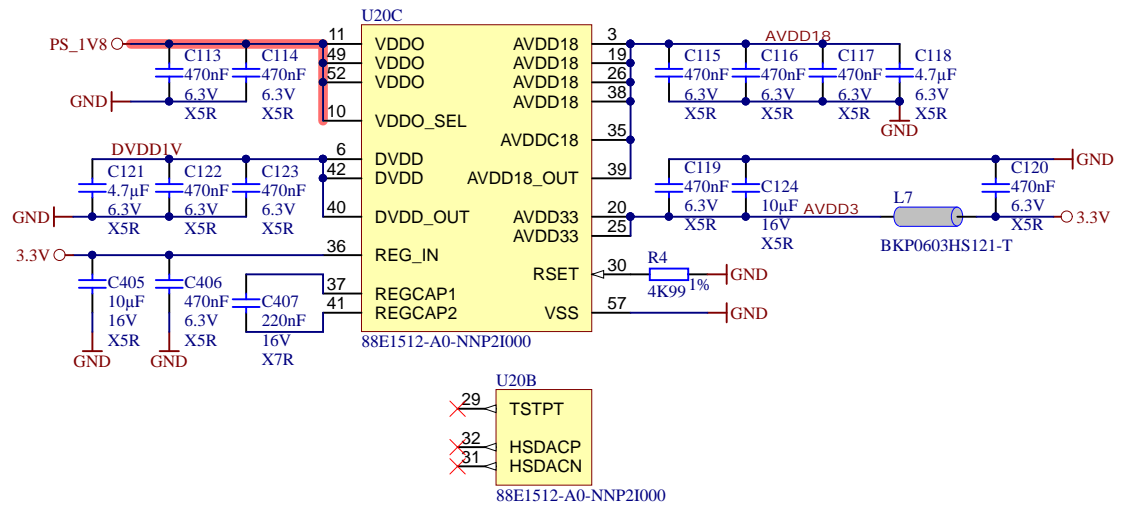
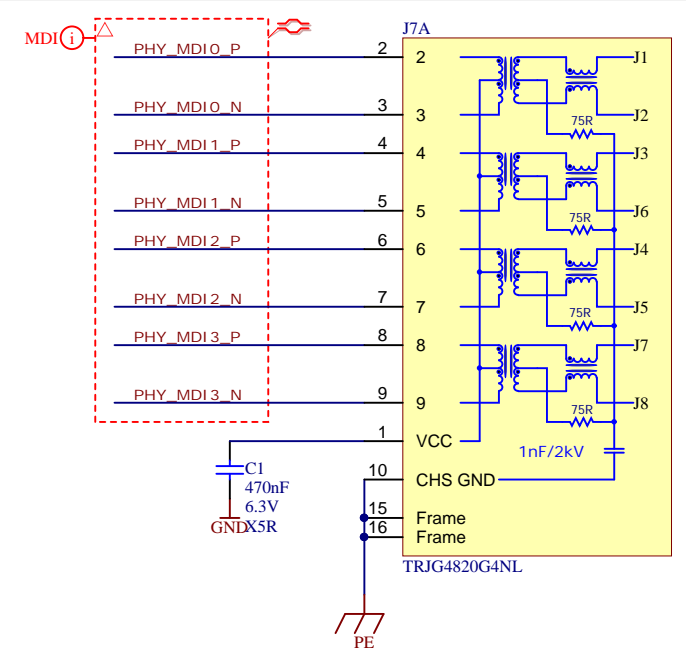
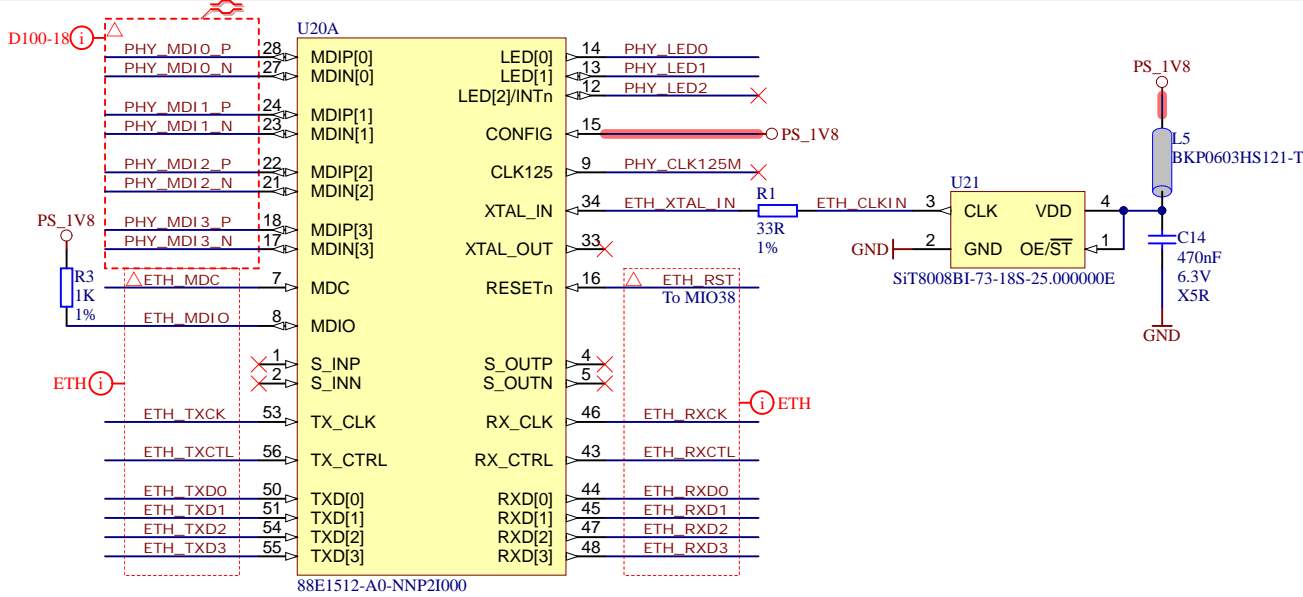


Title: <b>TEC0850 - FPGA_POWER</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	
Filename: <b>ZU_PWR.SchDoc</b>		Page <b>17</b> of <b>33</b>





Title: <b>TEC0850 - DDR POWER</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>19</b> of <b>33</b>
Filename: <b>DDR_PWR.SchDoc</b>		



Title: TEC0850 - ETH		
A4	Number: TEC0850 15EG1EA	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page 20 of 33
Filename: Ethernet.SchDoc		

1

2

3

4

A

A

B

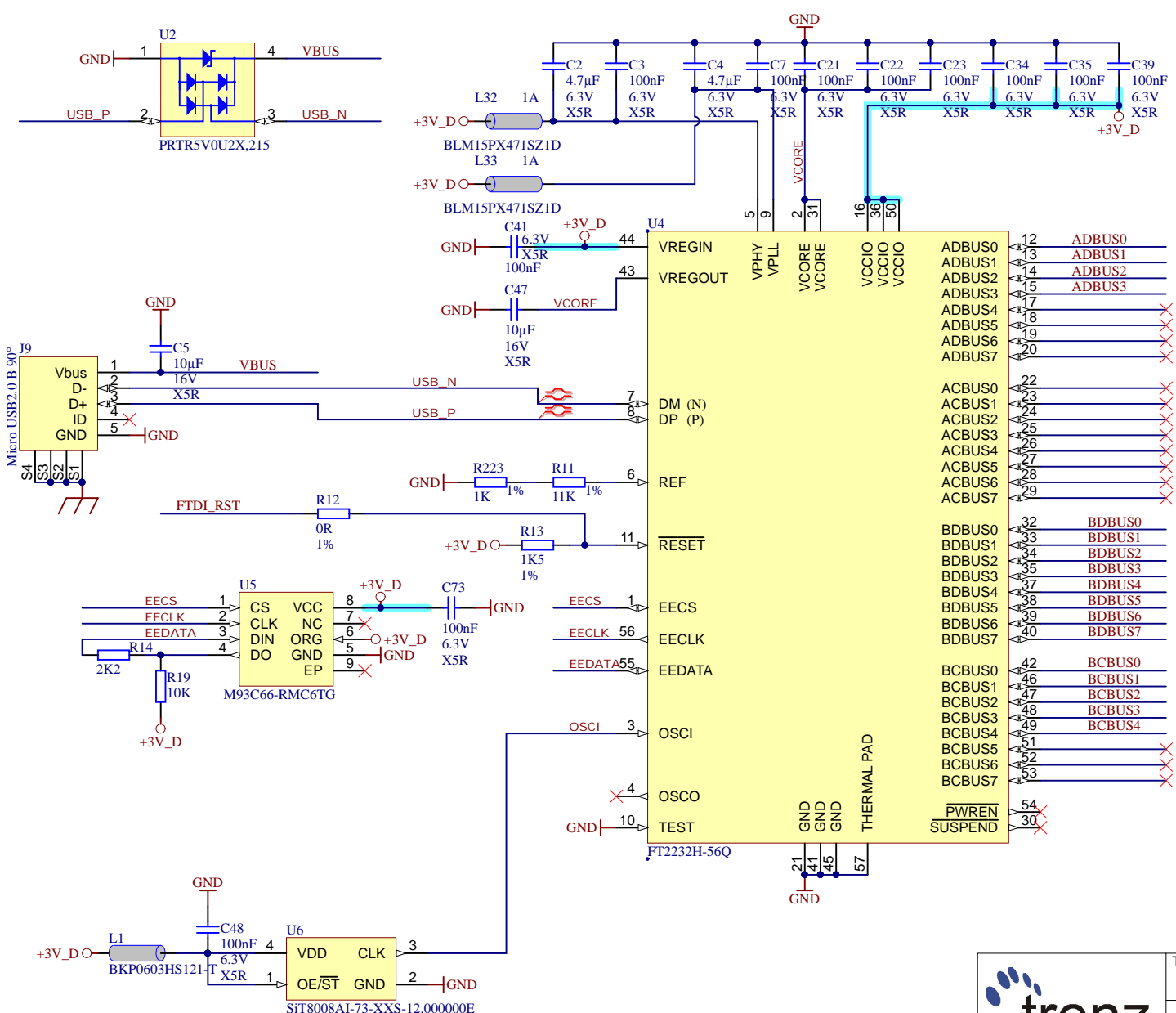

B

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C

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D

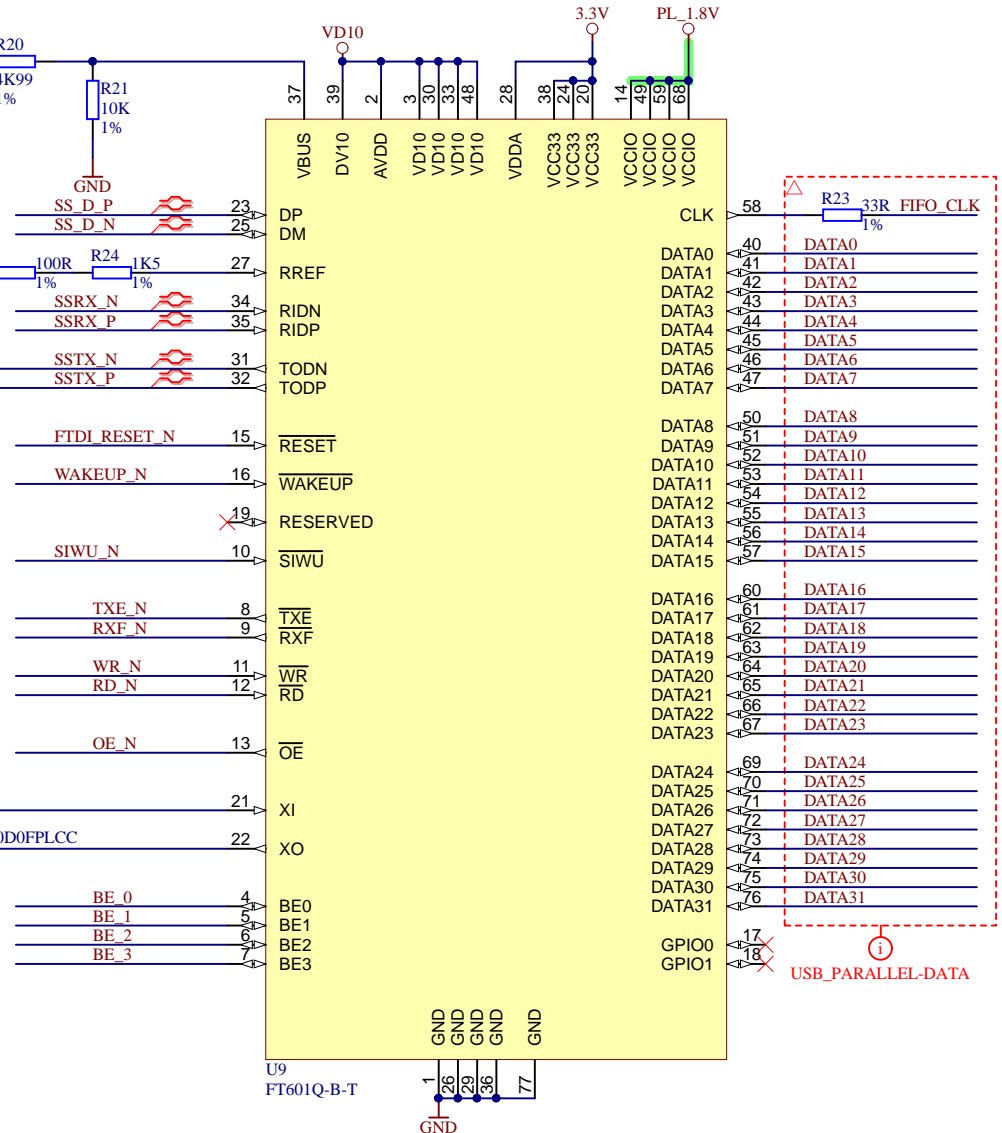
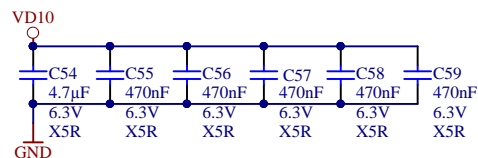
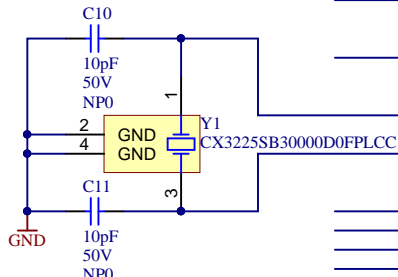
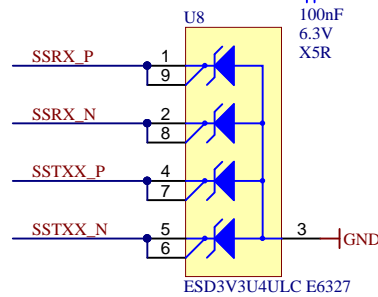
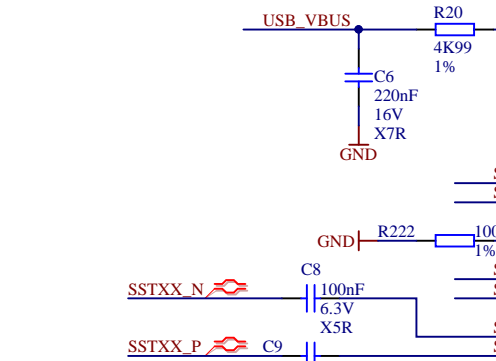
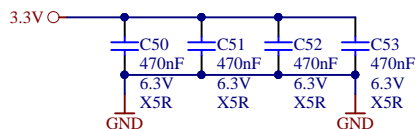
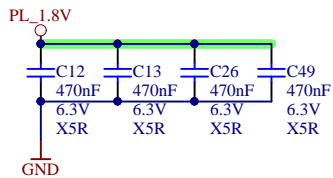
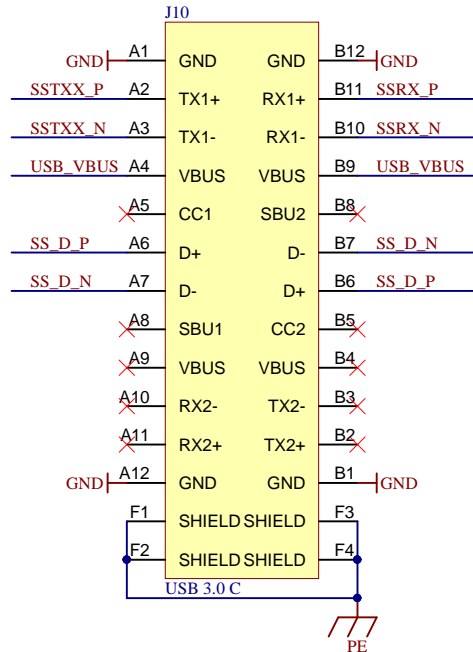
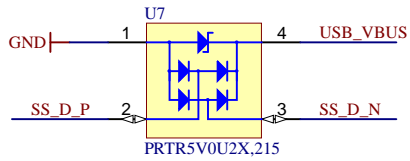
Title: TEC0850 - FTDI		
A4	Number: TEC0850 15EG1EA	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page 21 of 33
Filename: FTDI.SchDoc		

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Title: TEC0850 - USB3.0

A4	Number: TEC0850 15EG1EA	Rev. 03
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Filename: USB30.SchDoc		

1

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A

A

B

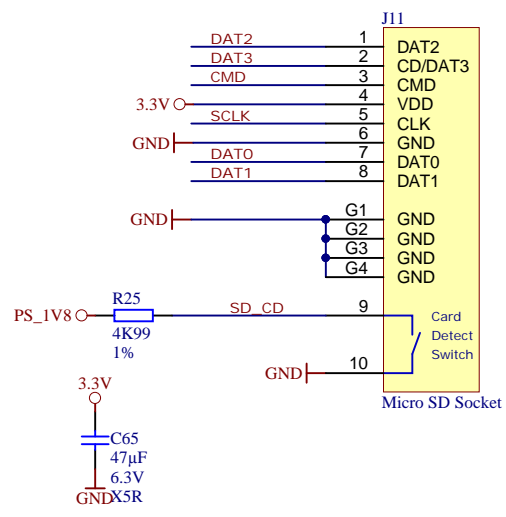
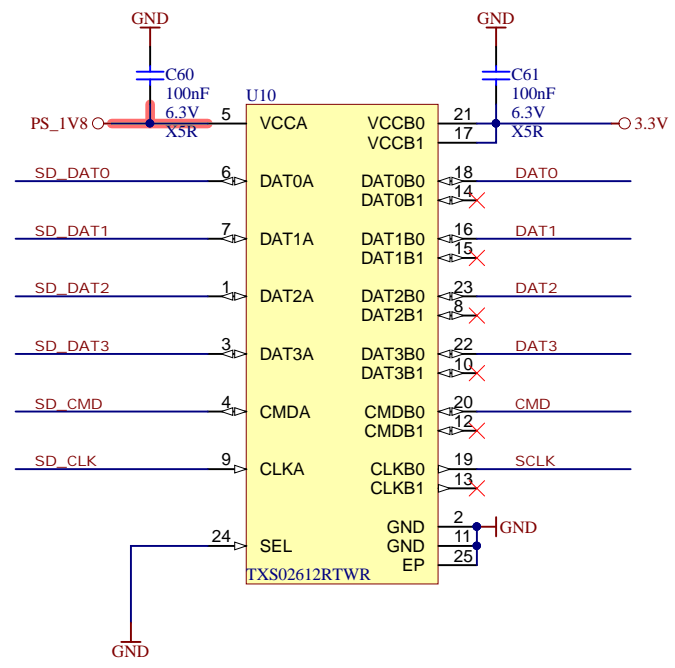
B

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C

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D



Title: <b>TEC0850 - SDCard</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>23</b> of <b>33</b>
Filename: <b>SDCard.SchDoc</b>		

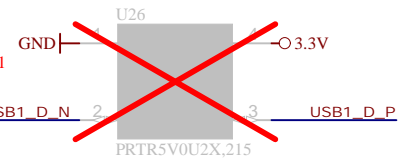
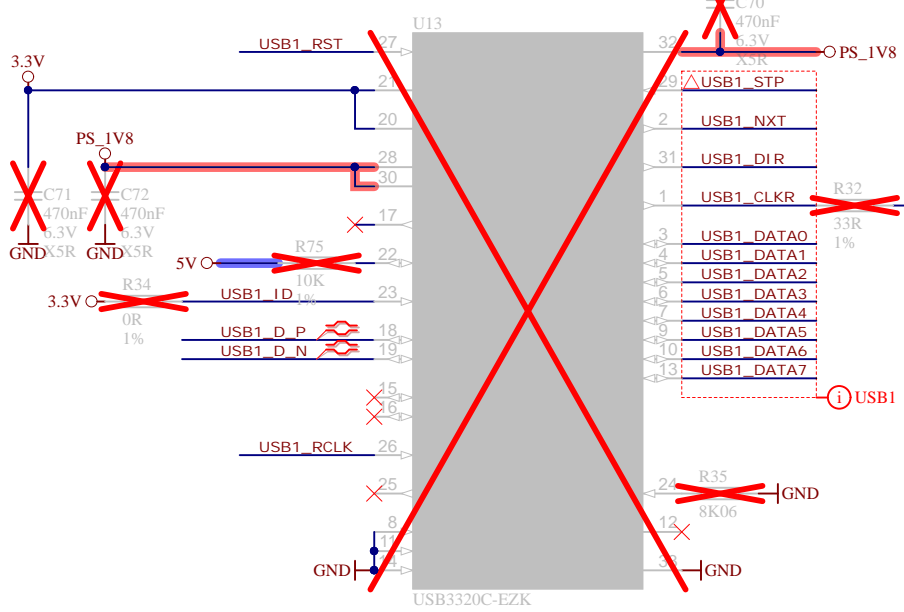
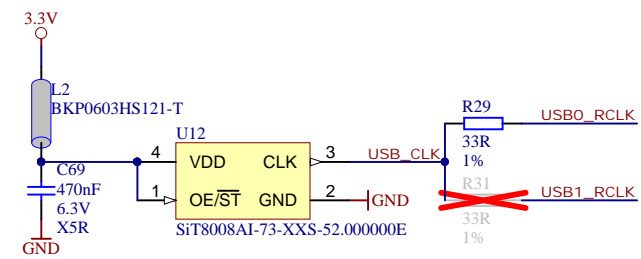
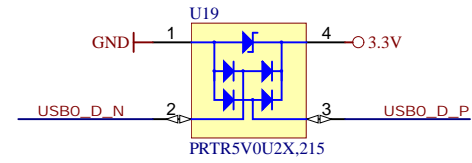
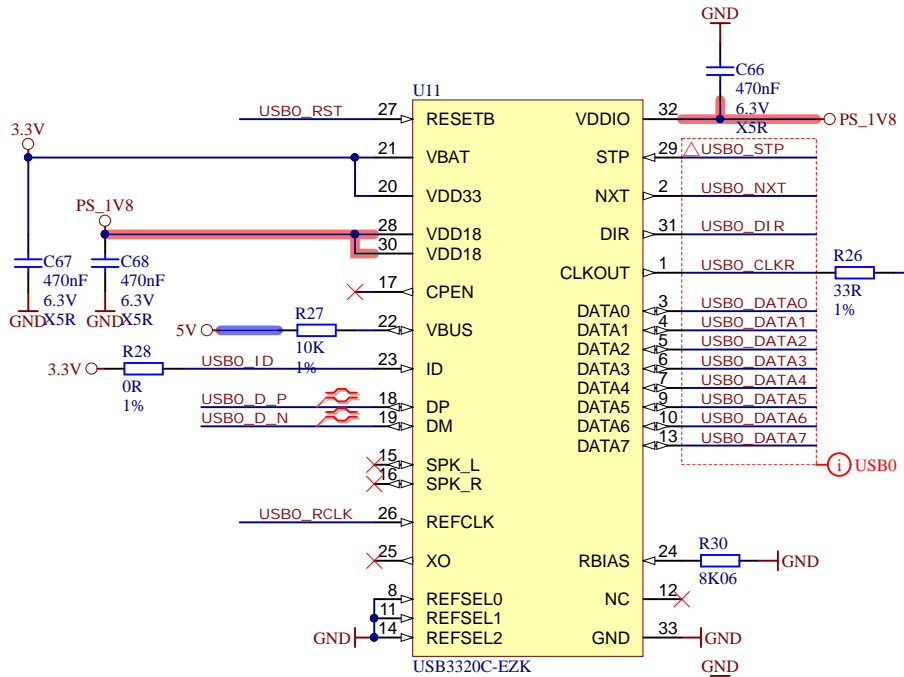
1

2

3

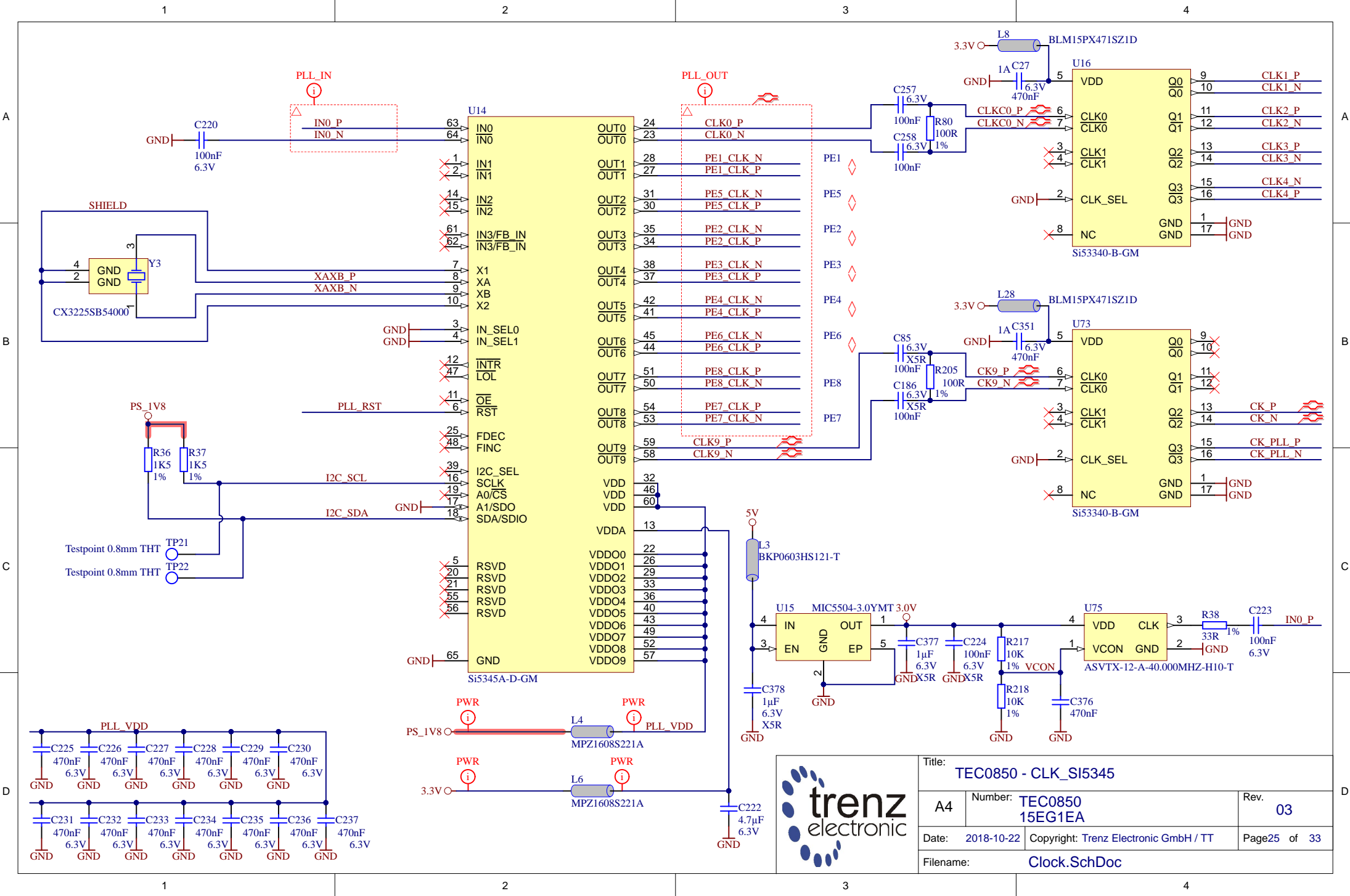
4





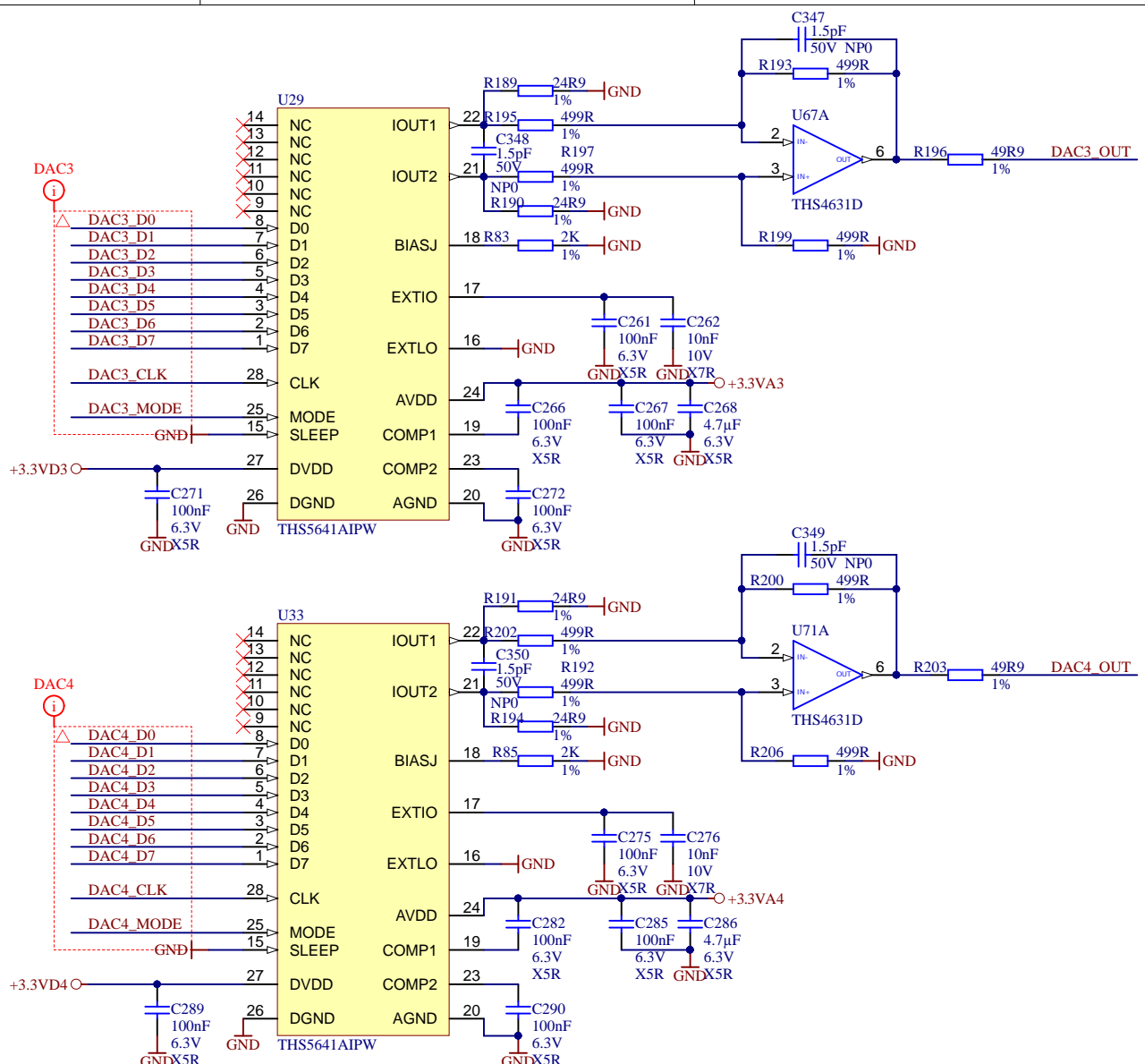
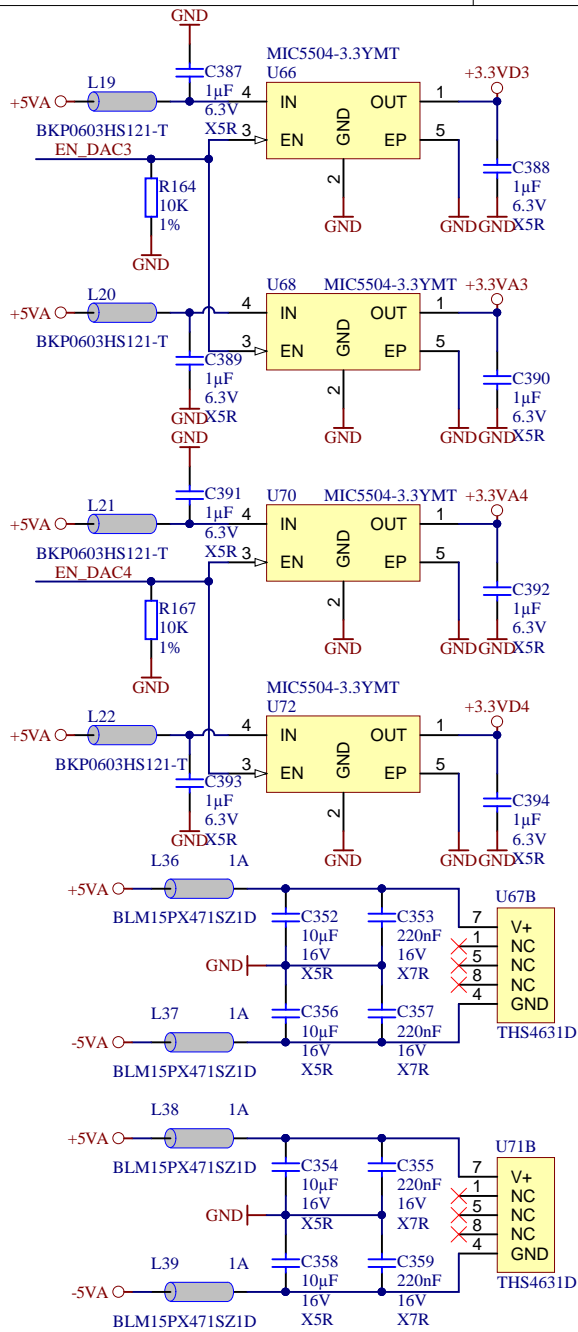
Title: <b>TEC0850 - USB_PHY</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>24</b> of <b>33</b>
Filename: <b>USB-PHY.SchDoc</b>		





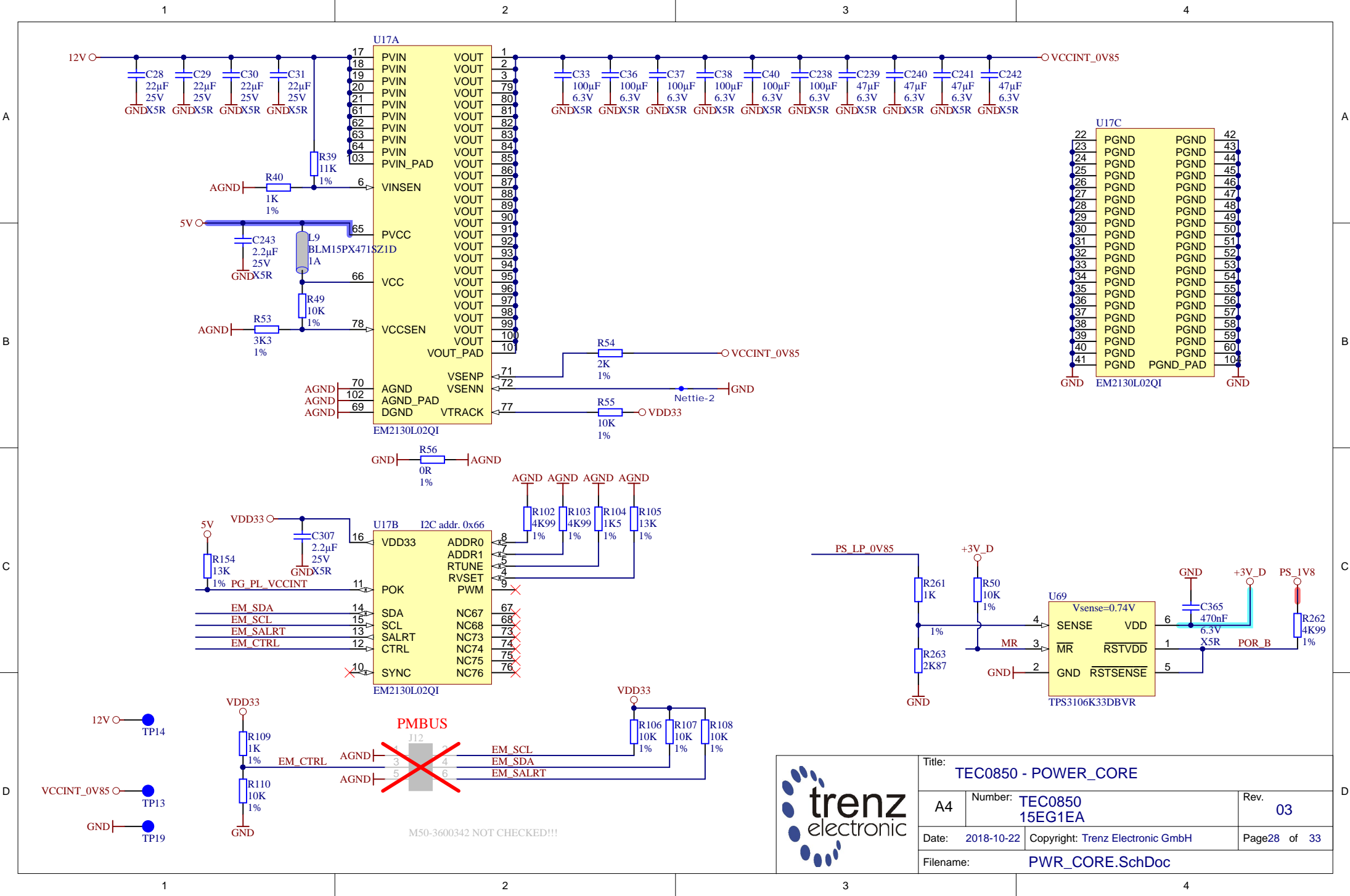
Title: TEC0850 - CLK_SI5345		
A4	Number: TEC0850 15EG1EA	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH / TT	Page 25 of 33
Filename: Clock.SchDoc		





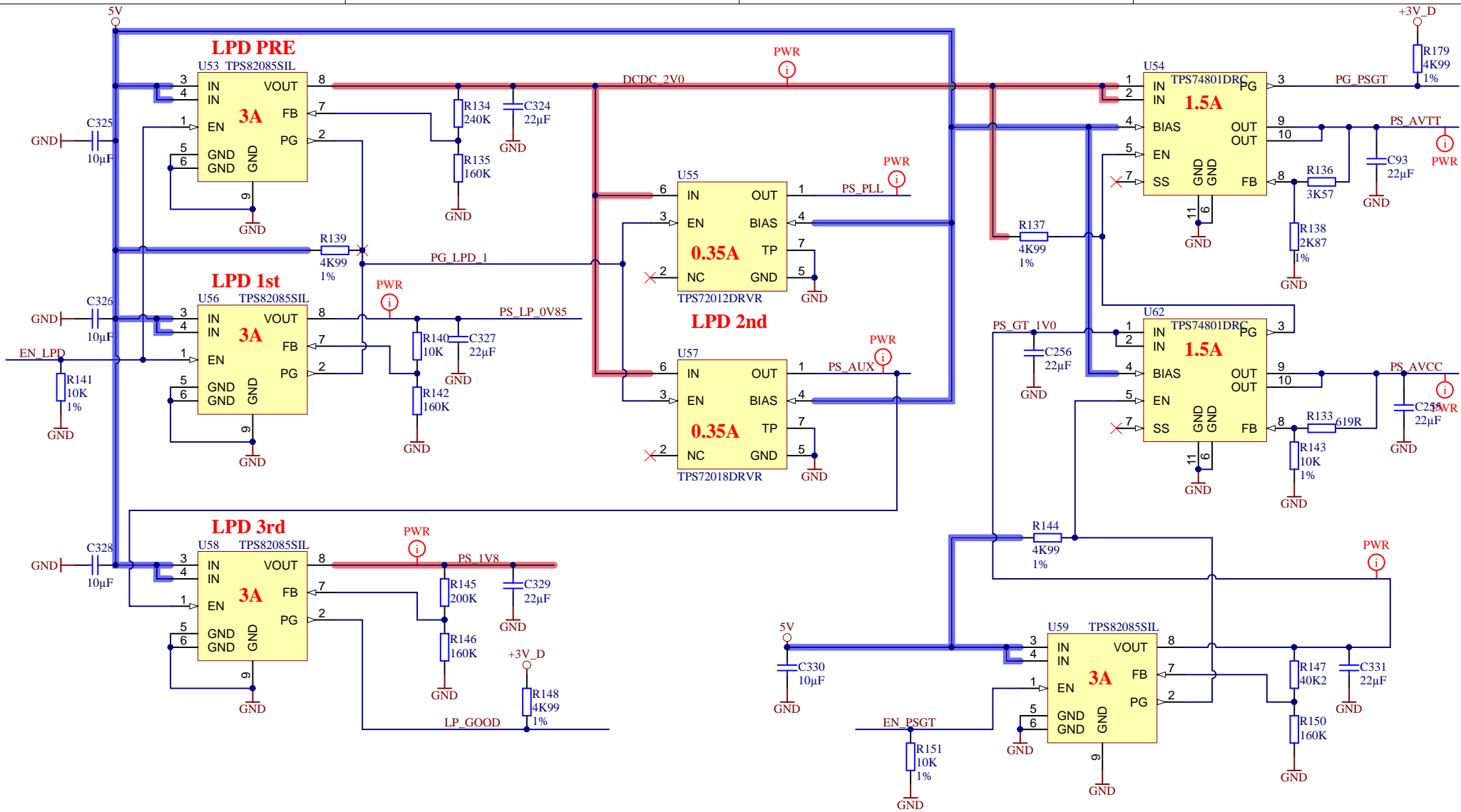
Title: **TEC0850 - DAC3\_DAC4**

A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	
Filename: <b>DAC34_8bit.SchDoc</b>		Page 27 of 33



Title: <b>TEC0850 - POWER_CORE</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>28</b> of <b>33</b>
Filename: <b>PWR_CORE.SchDoc</b>		

M50-3600342 NOT CHECKED!!!



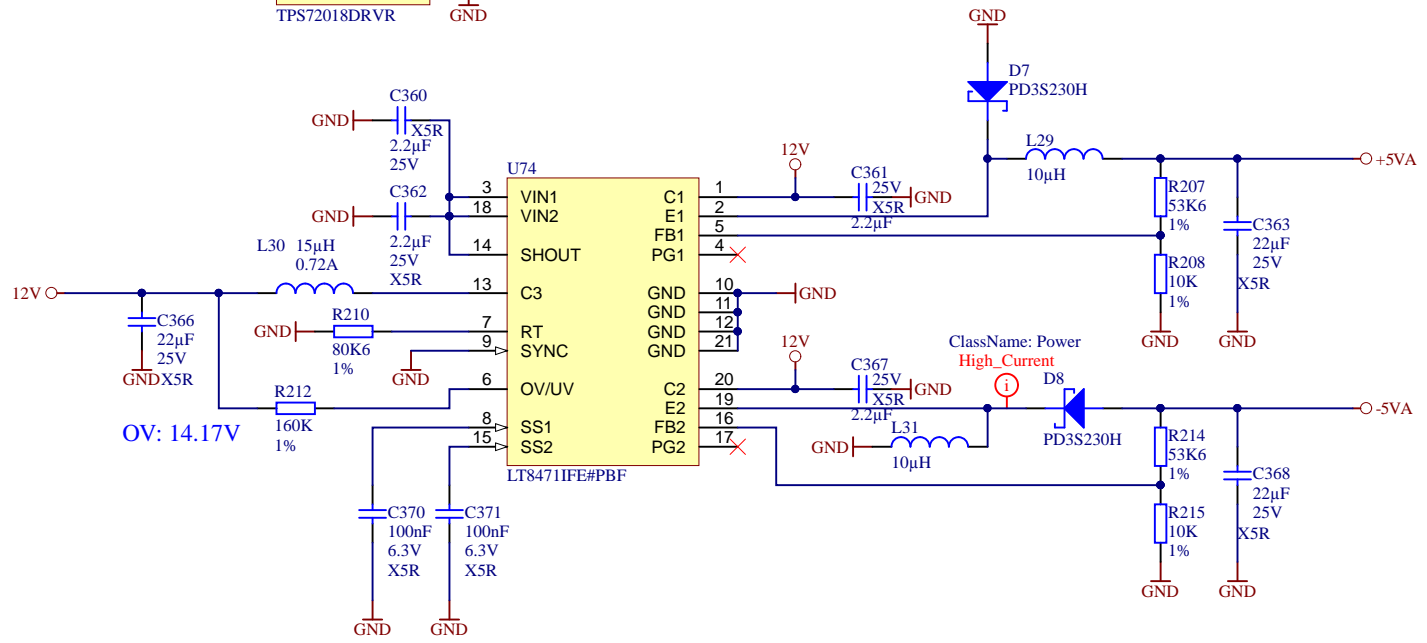
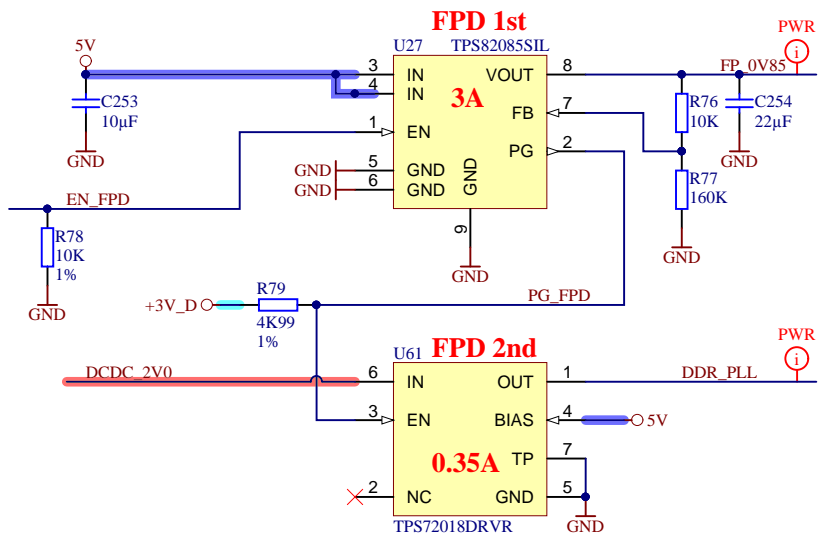
Title: <b>TEC0850 - POWER1</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>29</b> of <b>33</b>
Filename: <b>POWER_PSLP.schdoc</b>		

1

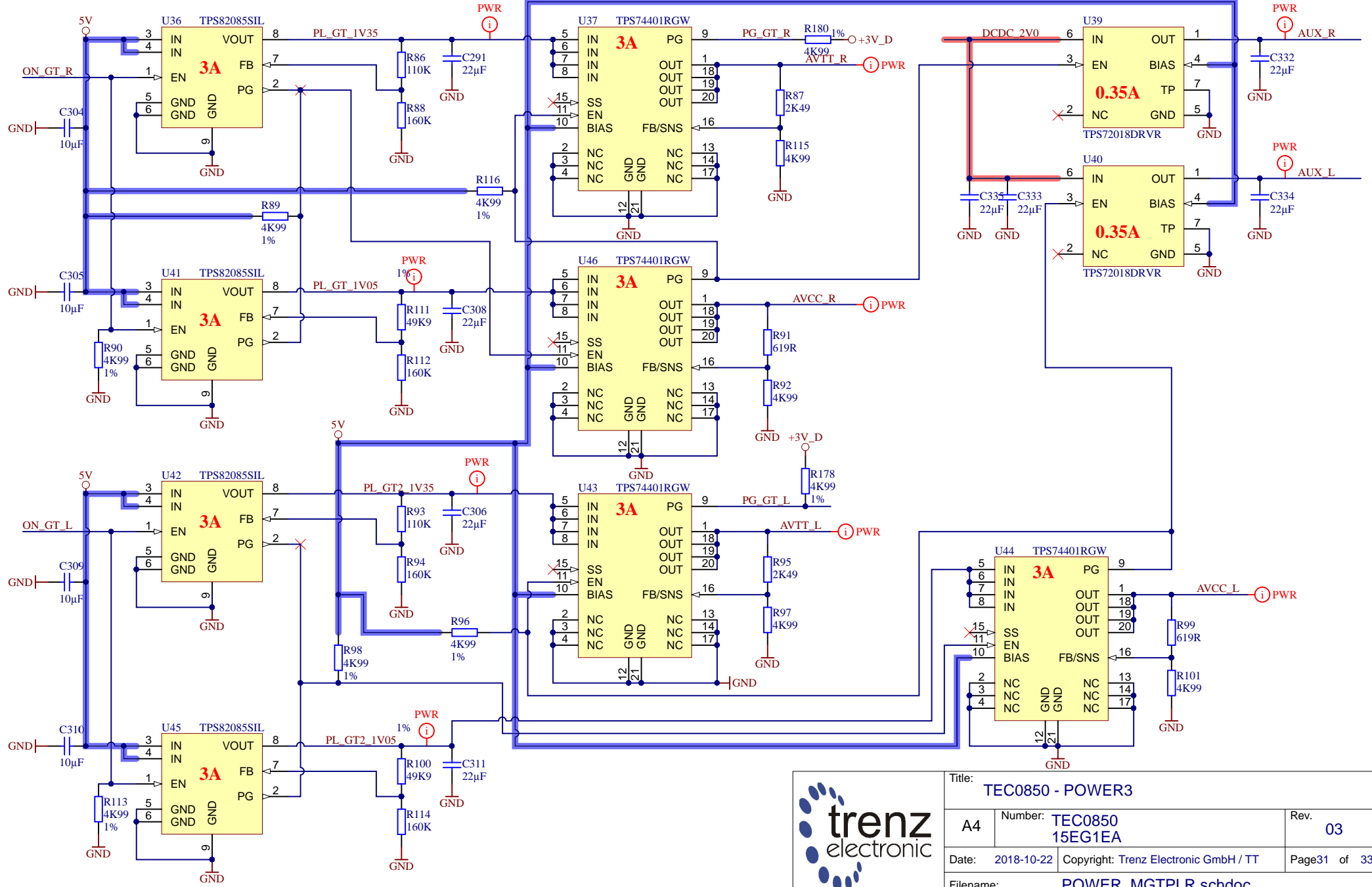
2

3

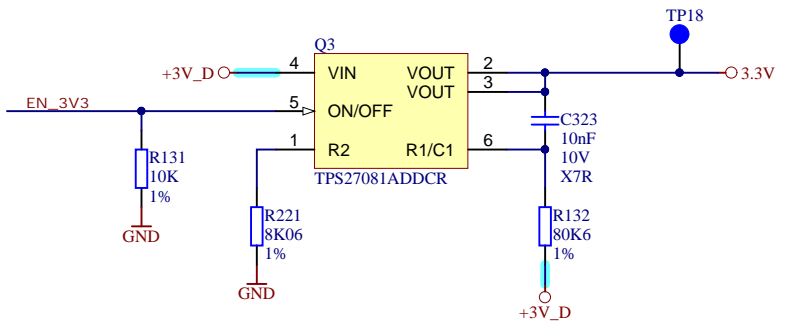
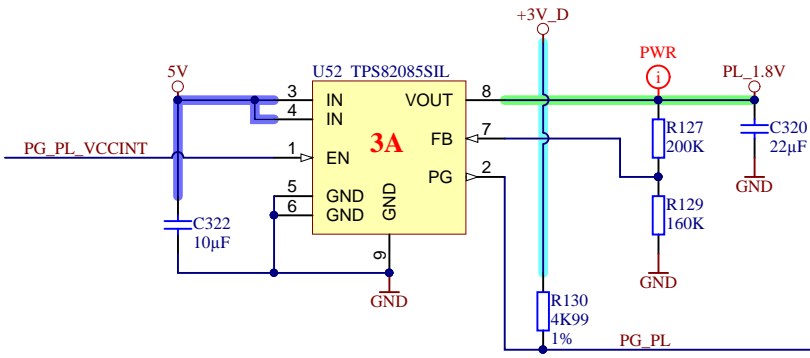
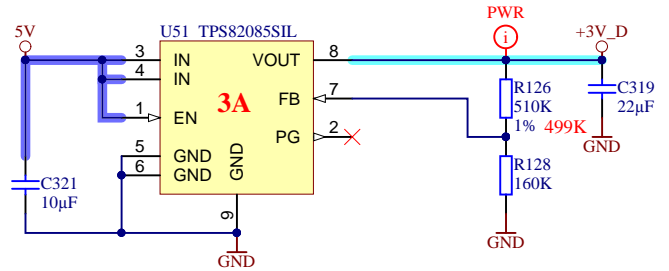
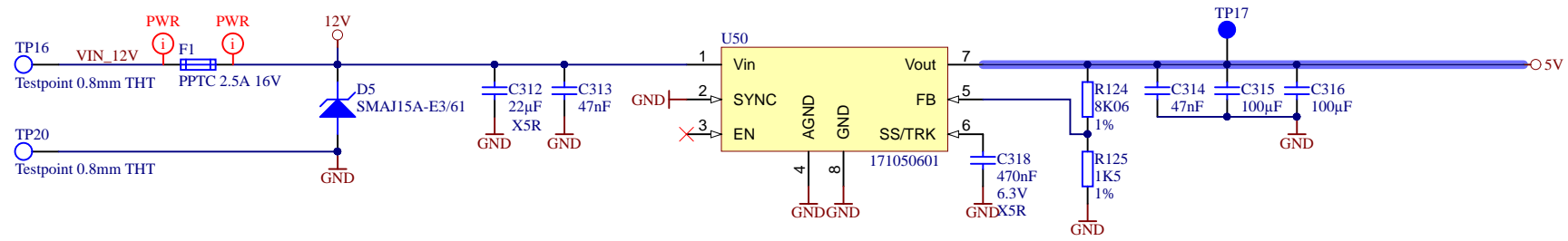
4



	Title: TEC0850 - POWER2		
	A4	Number: TEC0850 15EG1EA	Rev. 03
	Date: 2018-10-22	Copyright: Trenz Electronic GmbH / TT	Page30 of 33
	Filename: POWER_PSFP.schdoc		



Title: <b>TEC0850 - POWER3</b>		
A4	Number: <b>TEC0850 15EG1EA</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: Trenz Electronic GmbH / TT	
Page 31		of 33
Filename: <b>POWER_MGTPLR.schdoc</b>		



Title: TEC0850 - POWER4		
A4	Number: TEC0850 15EG1EA	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH / TT	Page 32 of 33
Filename: POWER_MGTPLL.schdoc		



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CHANGES REV01 to REV02

- 1) Fixed connection for U16 (Si53340-B-GM)
- 2) Added THT-testpoints for I2C-bus
- 3) Changed MEMS osc to TCXO osc , added LDO for TCXO osc
- 4) Use out9 from PLL, added dual output buffer ("1" -> MPSOC, B65; "2" -> J1, cPCI-serial)
- 5) Changed connector J12 (do not populated)
- 6) Added capacitors C372, C373 on the clock line (AC-coupling)
- 7) Changed OPs for DACs (LT6200IS6 -> THS4631D)
- 8) Added additional DCDC (+/-5V) for THS4631D
- 9) Added THT-testpoints for VIN/GND
- 10) full update lib

CHANGES REV02 to REV03

- 1) Fixed connection for U74 (LT8471IFE#PBF)
- 2) Added additional resistors R219/R220
- 3) Fixed connection for Y2 (CM2012-2pad)
- 4) Changed U69 (TPS3106E09DBVR -> TPS3106K33DBVR)
- 5) Changed U73 (LTC6957IDD-2#PBF -> Si53340-B-GM)
- 6) Optimized BOM
- 7) full update lib

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		Title: <b>TEC0850 - Changes list</b>	
		A4	Number: <b>TEC0850 15EG1EA</b>
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