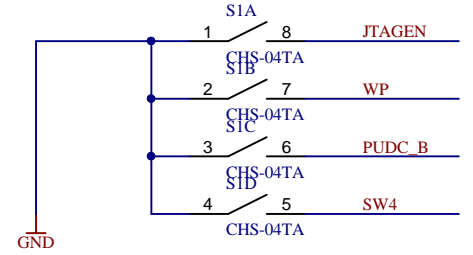
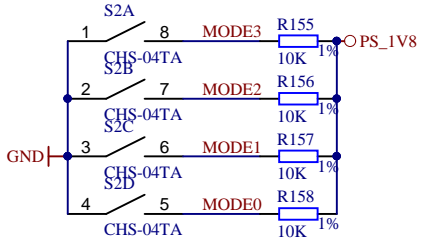
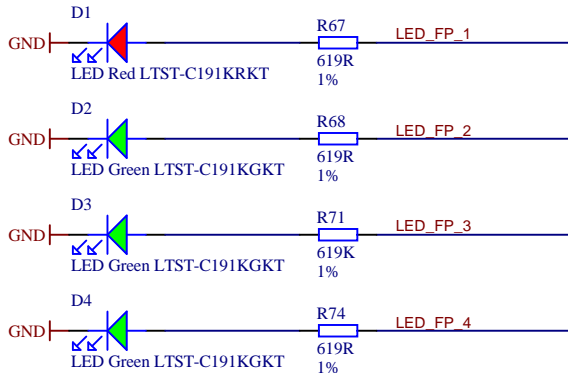
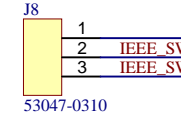
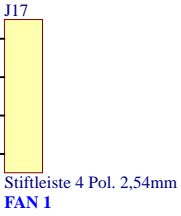
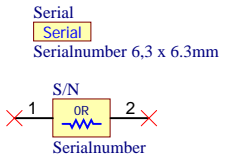
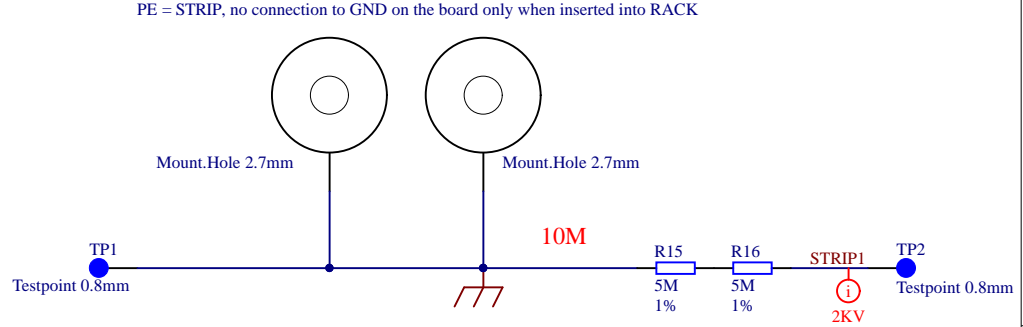
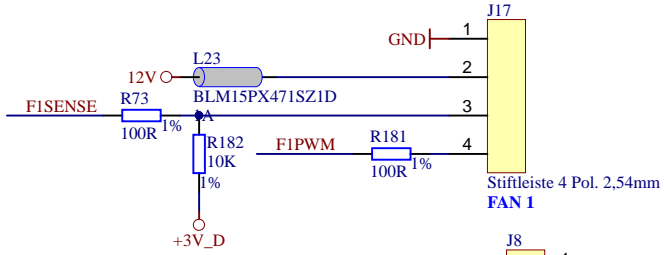


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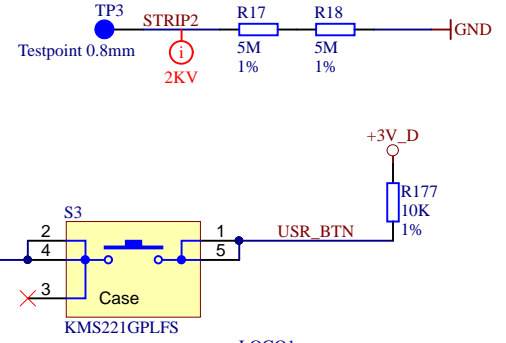
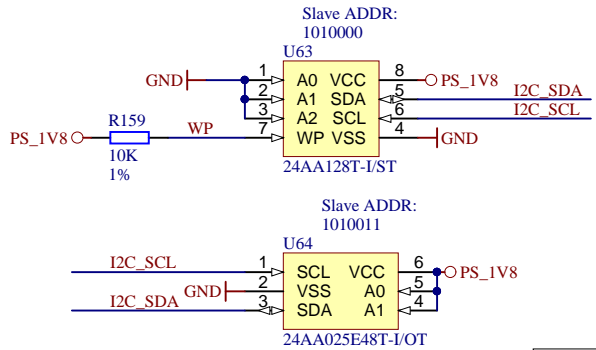
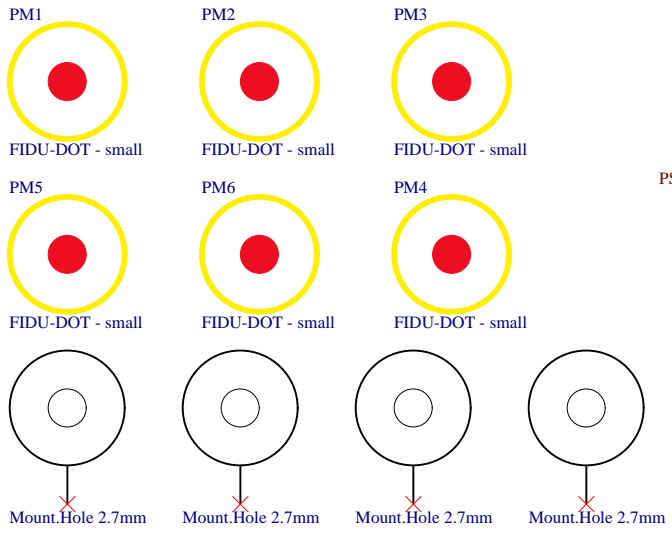
- U\_J1  
J1.SchDoc
- U\_J2  
J2.SchDoc
- U\_J3  
J3.SchDoc
- U\_J4  
J4.SchDoc
- U\_J5  
J5.SchDoc
- U\_J6  
J6.SchDoc



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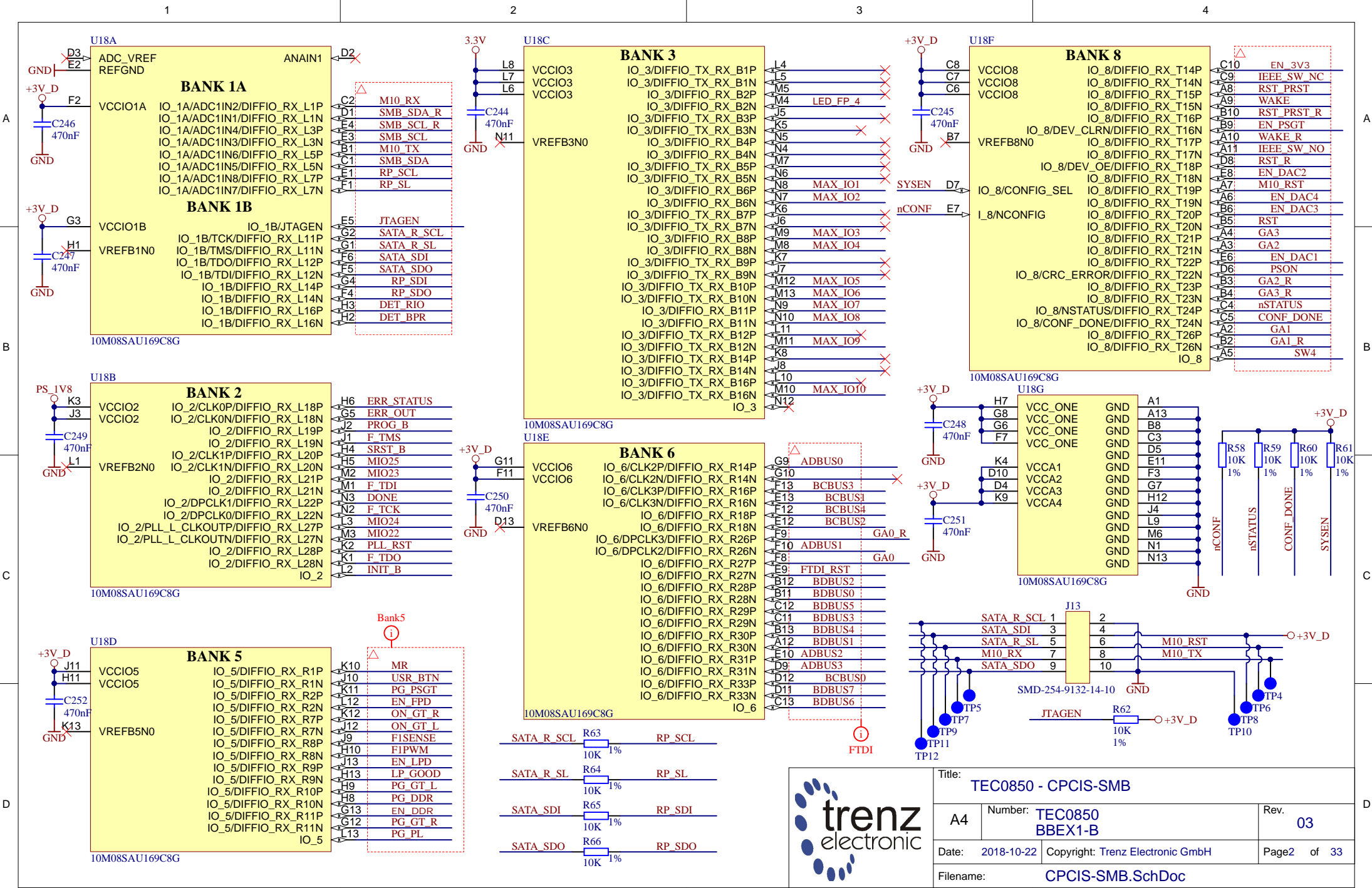
LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

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Assembly variant	BBEX1-B
Created by	VY
Modified by	VY
Modified at	2020-11-13
SVN Revision	8527



Title: TEC0850 - CPCIS-MAIN		
A4	Number: TEC0850 BBEX1-B	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page1 of 33
Filename: CPCIS-MAIN.SchDoc		



Title: <b>TEC0850 - CPCIS-SMB</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page2 of 33
Filename: <b>CPCIS-SMB.SchDoc</b>		

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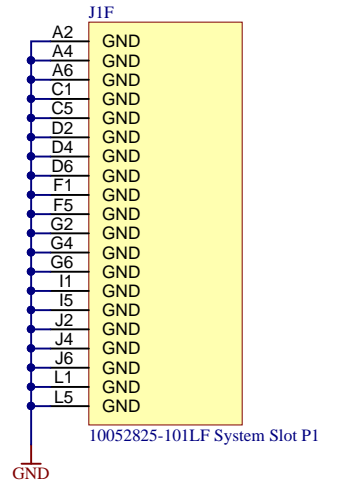
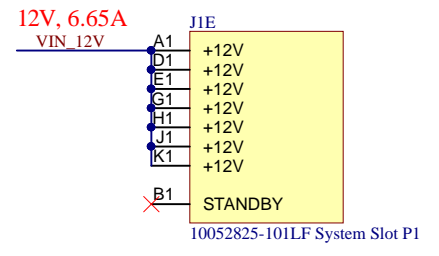
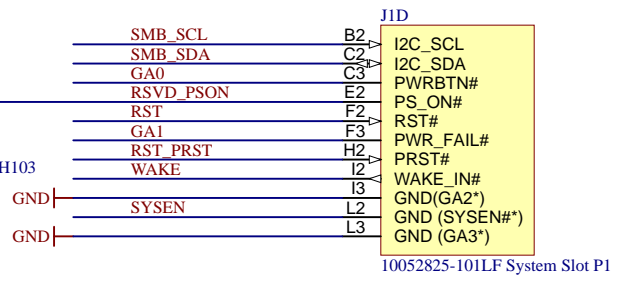
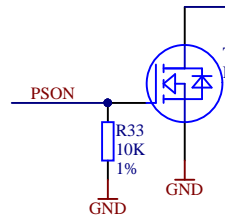
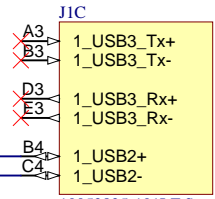
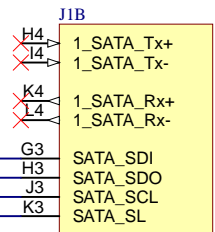
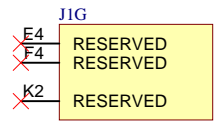
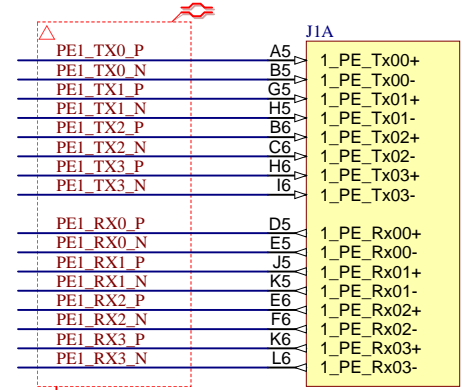
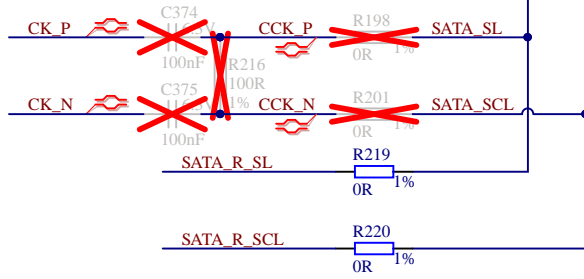
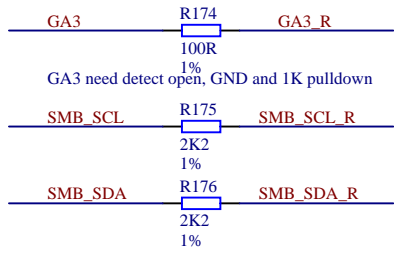
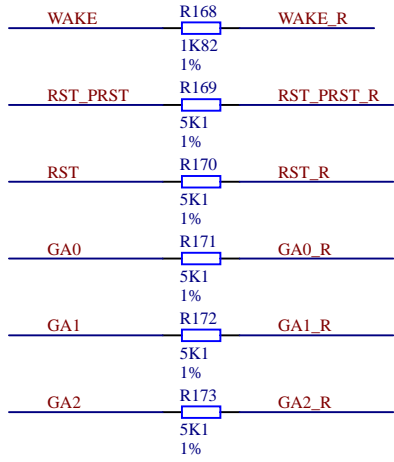
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1.8, 2.2 and 5.1K are REQUIRED BY CPCI-S do not optimize to other values



Title: TEC0850 - J1		
A4	Number: TEC0850 BBEX1-B	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page3 of 33
Filename: J1.SchDoc		

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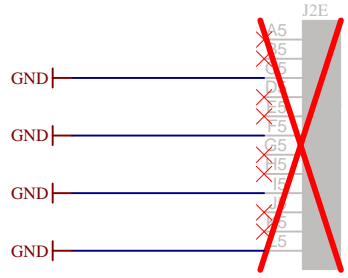
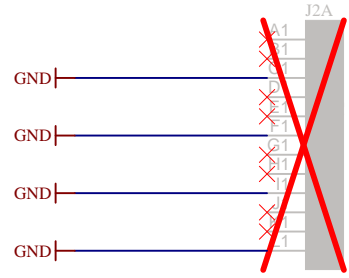
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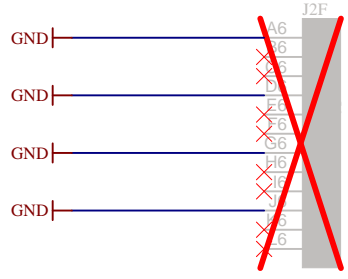
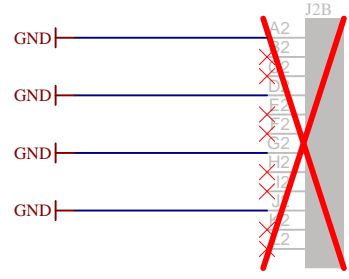
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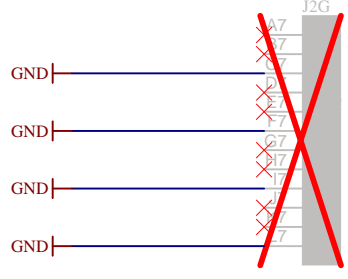
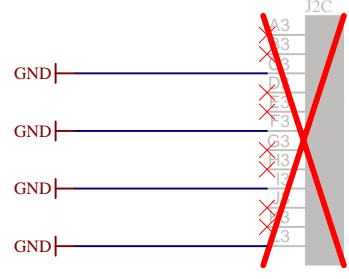
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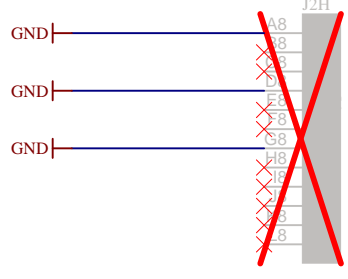
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Title: <b>TEC0850 - J2</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>4</b> of <b>33</b>
Filename: <b>J2.SchDoc</b>		

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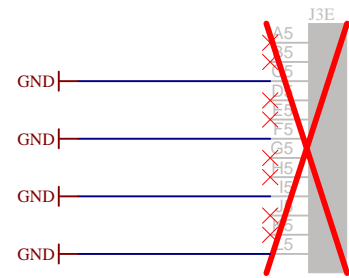
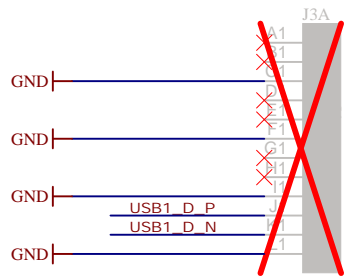
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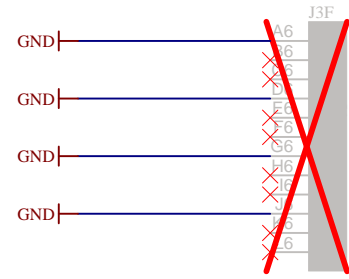
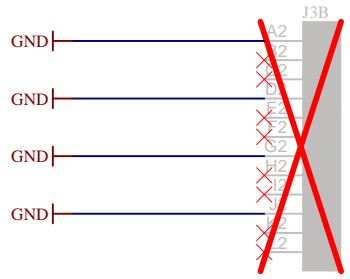
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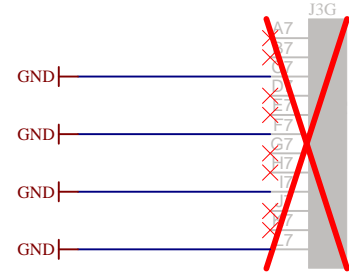
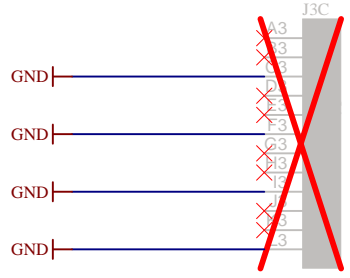
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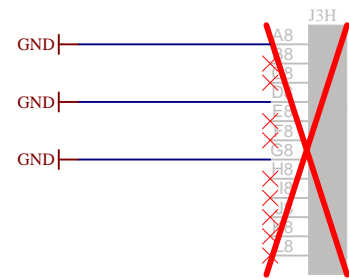
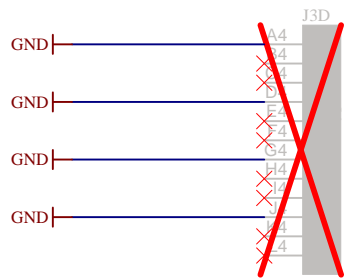

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Title: <b>TEC0850 - J3</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>5</b> of <b>33</b>
Filename: <b>J3.SchDoc</b>		

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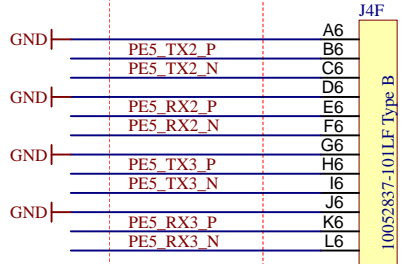
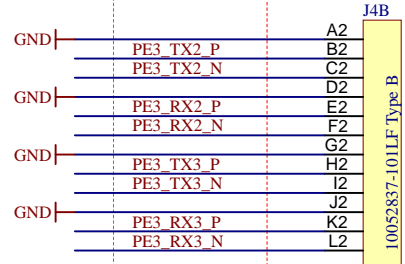
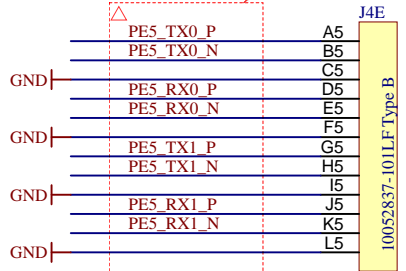
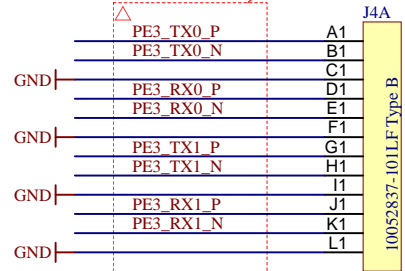
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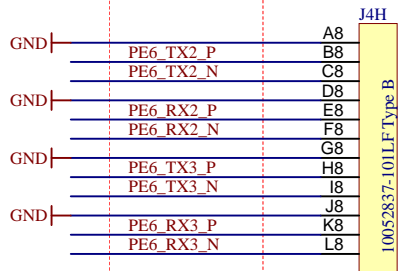
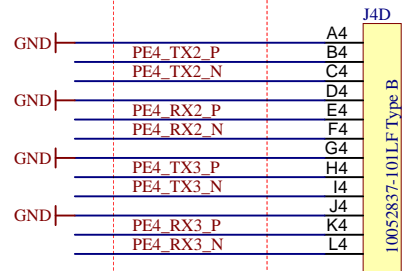
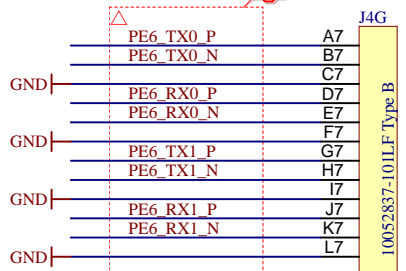
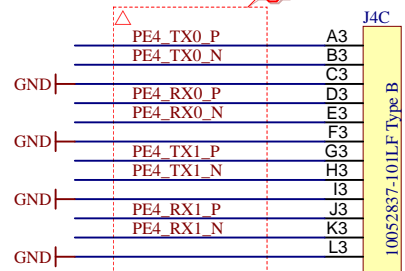
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PE3

PE5



PE4

PE6



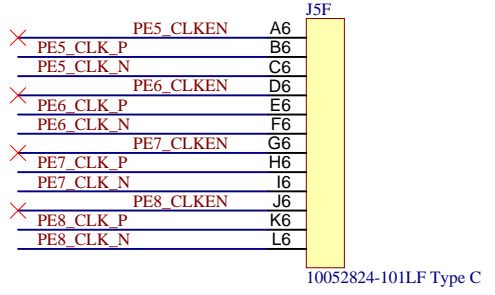
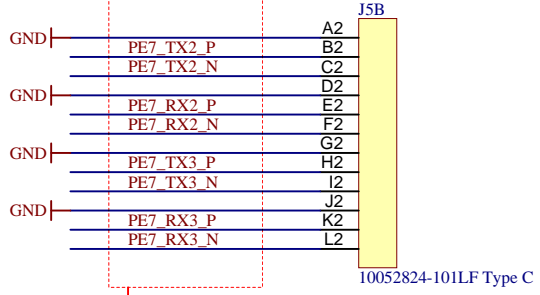
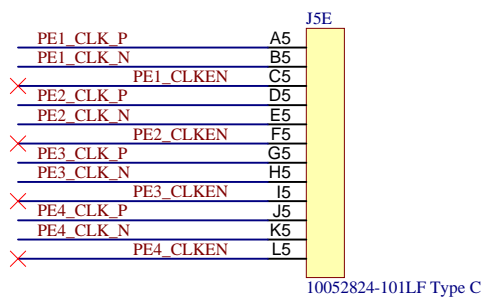
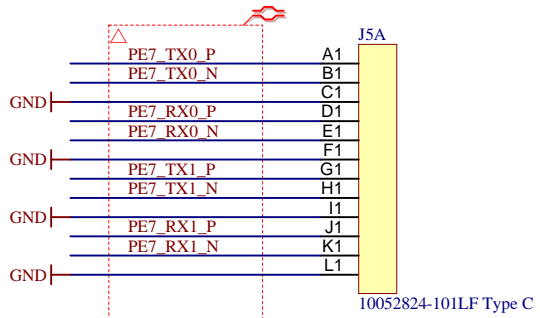
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A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>6</b> of <b>33</b>
Filename: <b>J4.SchDoc</b>		

1

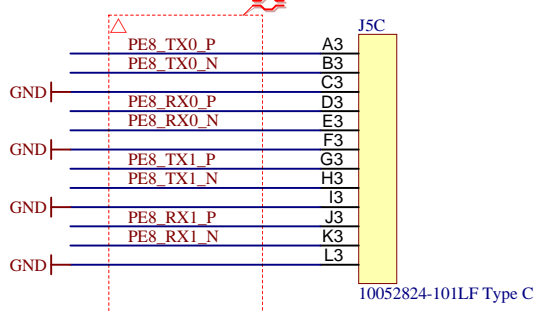
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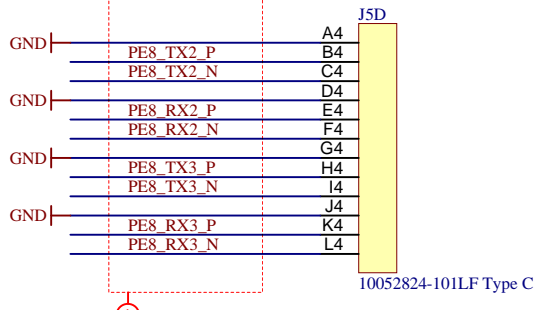
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PE7



PE8



PE8



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A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>7</b> of <b>33</b>
Filename: <b>J5.SchDoc</b>		

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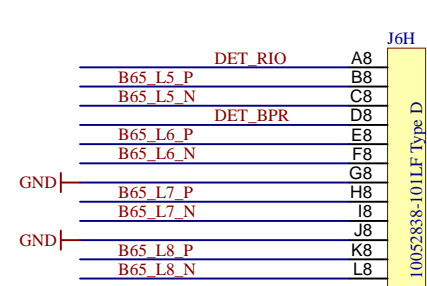
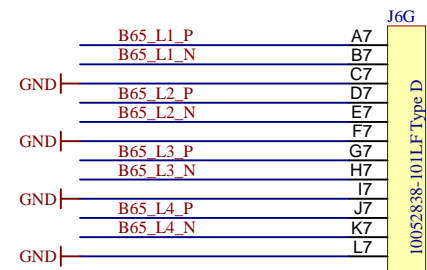
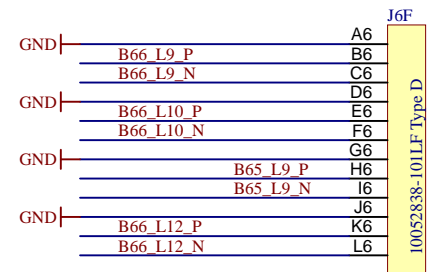
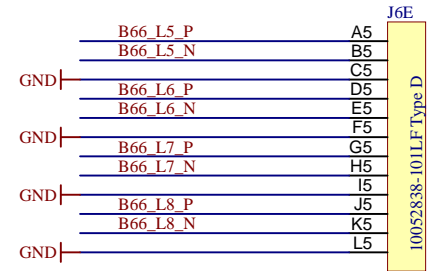
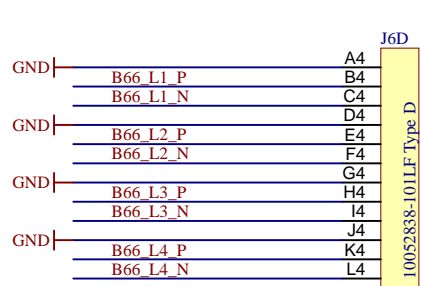
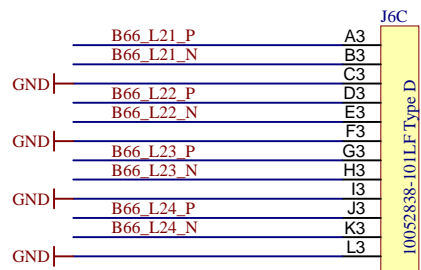
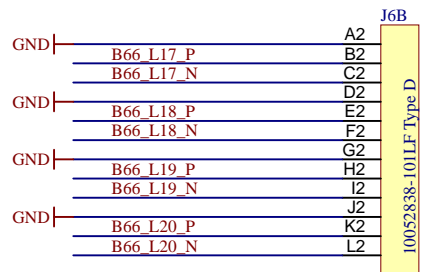
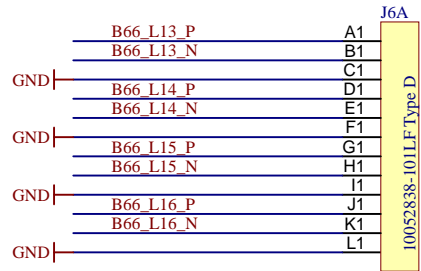
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Title: <b>TEC0850 - J6</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>8</b> of <b>33</b>
Filename: <b>J6.SchDoc</b>		

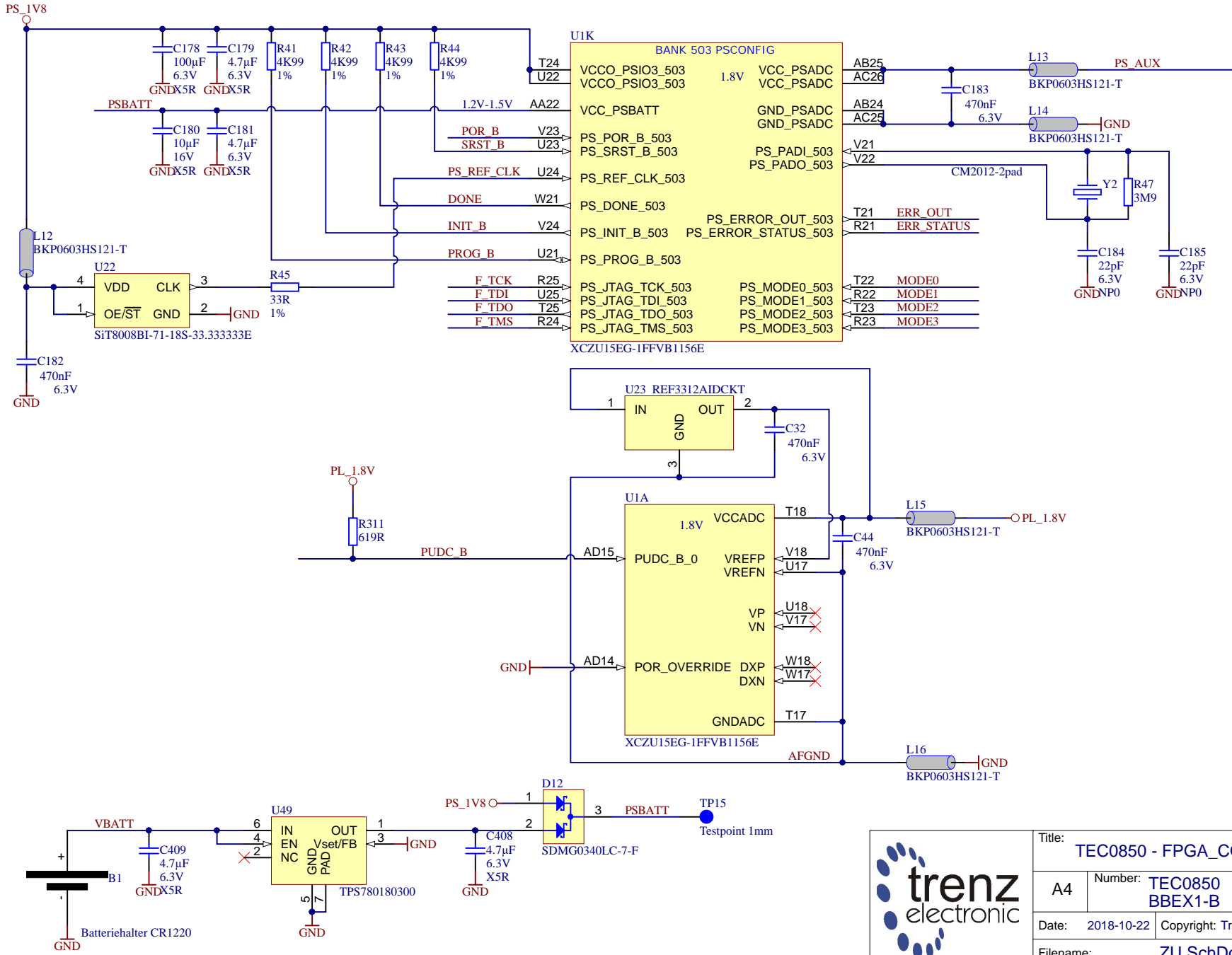
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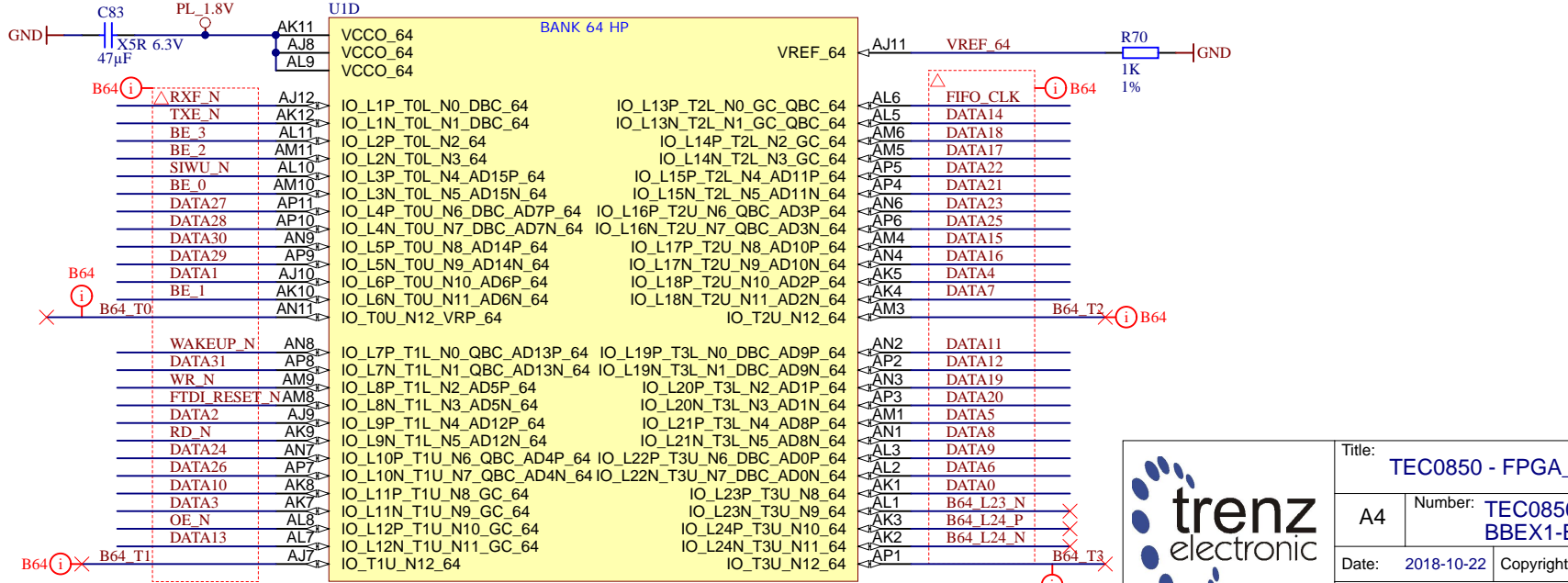
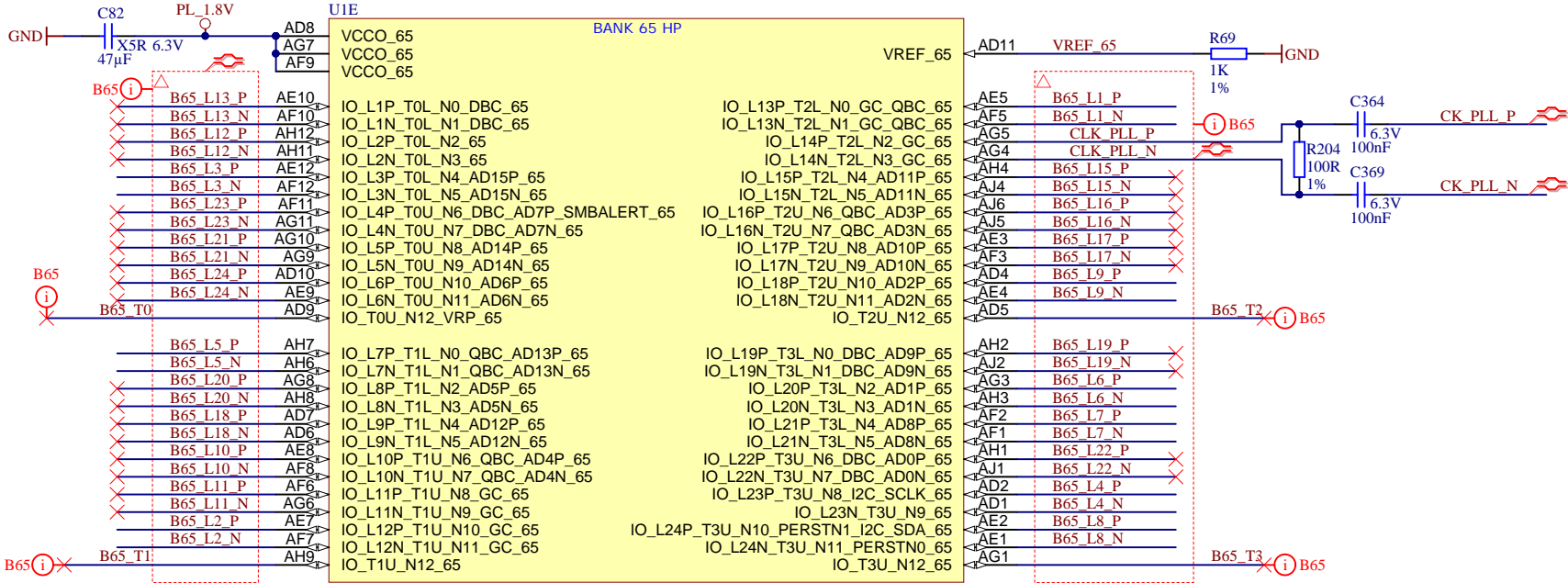




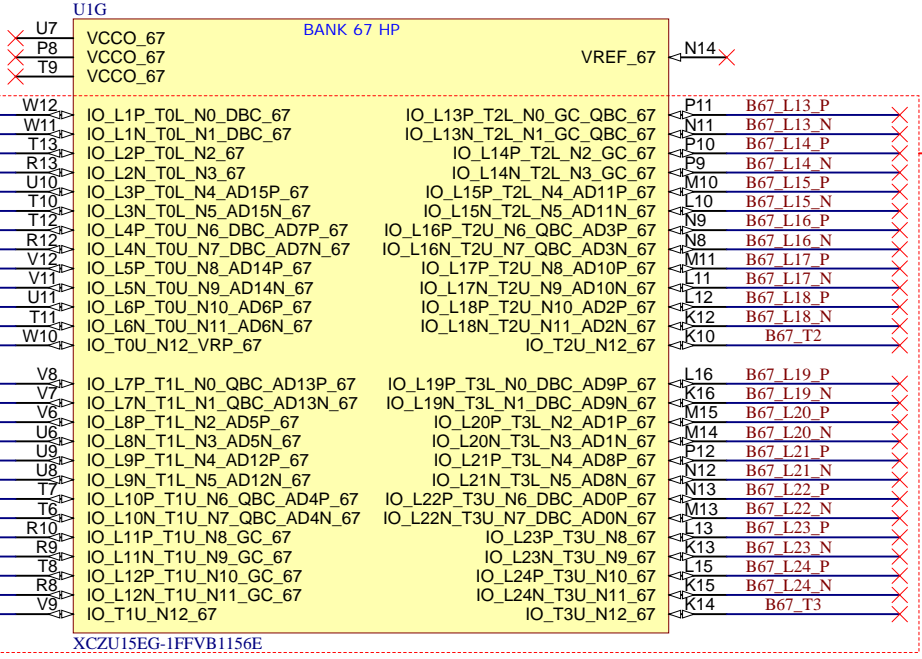
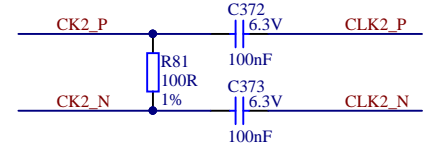
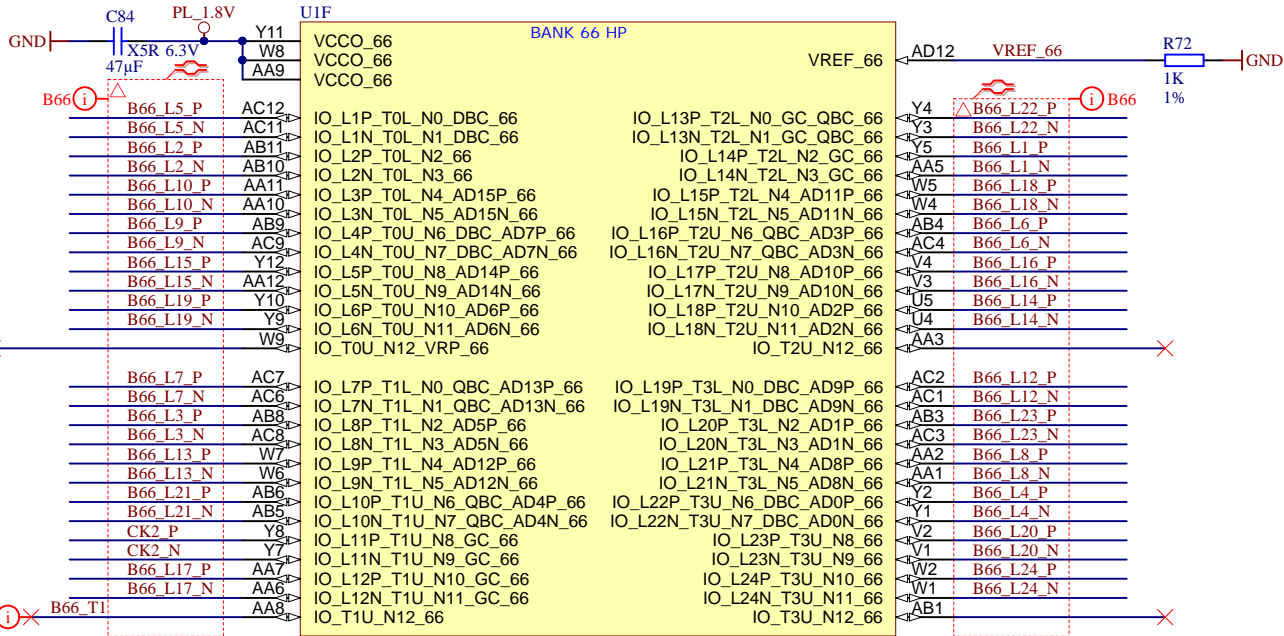
- B64\_B65  
ZU\_B64\_B65.SchDoc
- B66\_B67  
ZU\_B66\_B67.SchDoc
- HD  
ZU\_HD.SchDoc
- MGT\_L  
ZU\_MGT\_L.SchDoc
- MGT\_R  
ZU\_MGT\_R.SchDoc
- MIO  
ZU\_MIO.SchDoc
- PSDDR  
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- ZU\_PWR  
ZU\_PWR.SchDoc



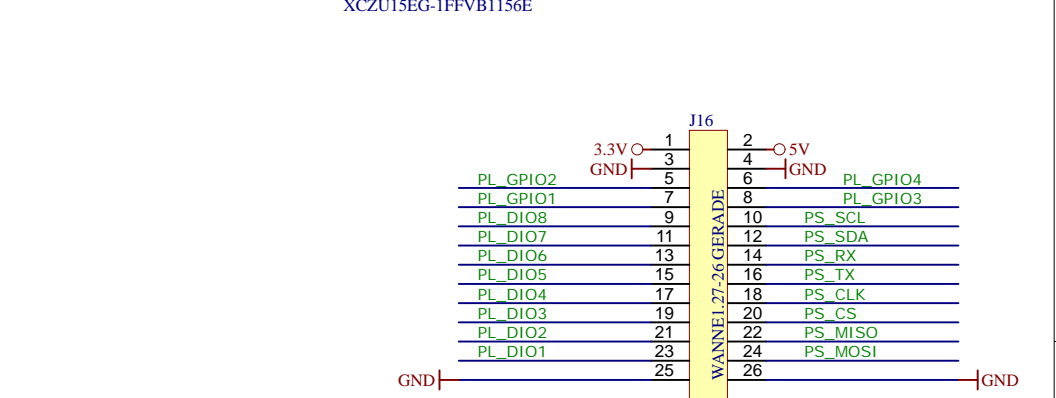
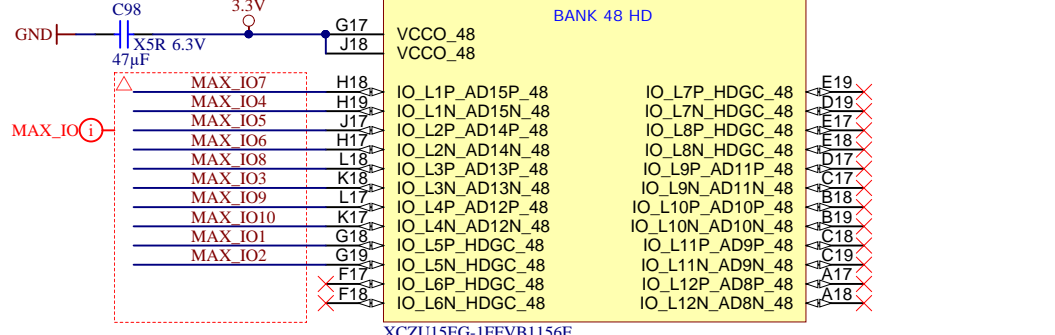
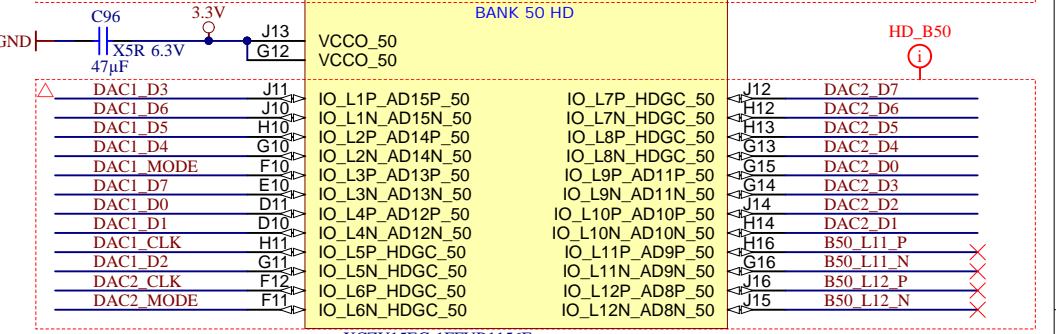
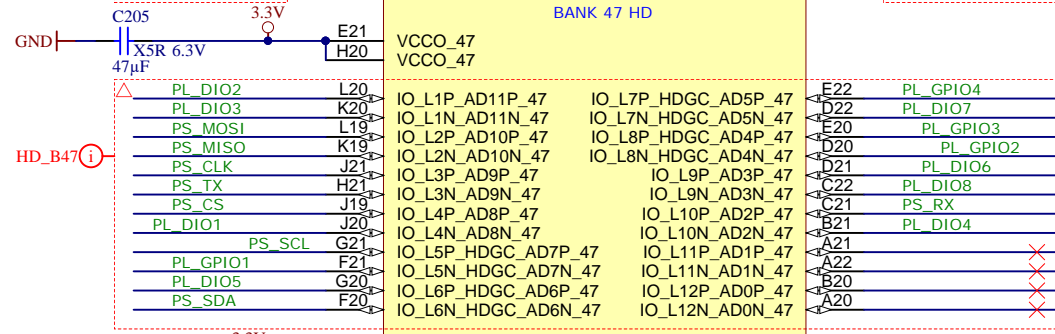
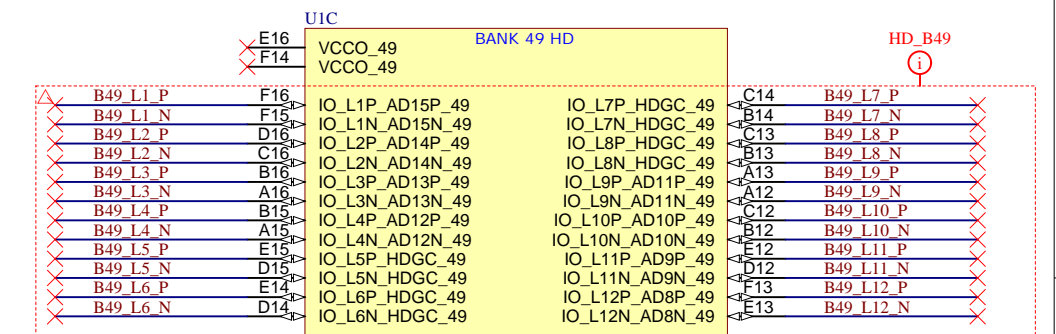
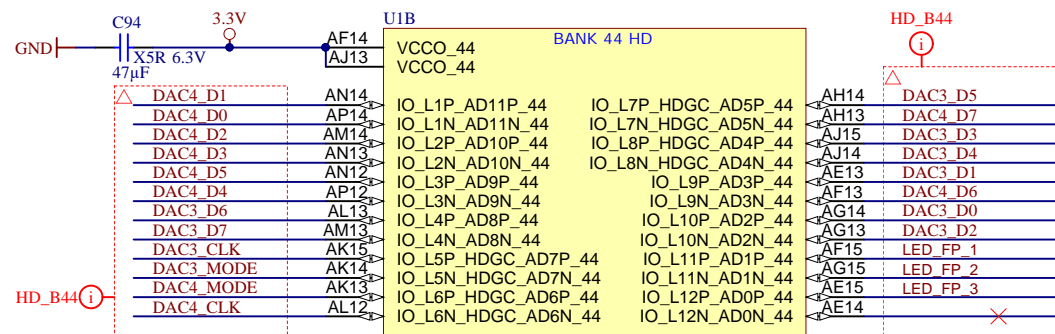
Title: TEC0850 - FPGA_CONFIG		
A4	Number: TEC0850 BBEX1-B	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page9 of 33
Filename: ZU.SchDoc		



Title: TEC0850 - FPGA_B64_B65		
A4	Number: TEC0850 BBEX1-B	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page 10 of 33
Filename: ZU_B64_B65.SchDoc		



Title: <b>TEC0850 - FPGA_B66_B67</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>11</b> of <b>33</b>
Filename: <b>ZU_B66_B67.SchDoc</b>		



XCZU15EG-1FFVB1156E

Title: **TEC0850 - FPGA\_HD**

A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>12</b> of <b>33</b>
Filename: <b>ZU_HD.SchDoc</b>		



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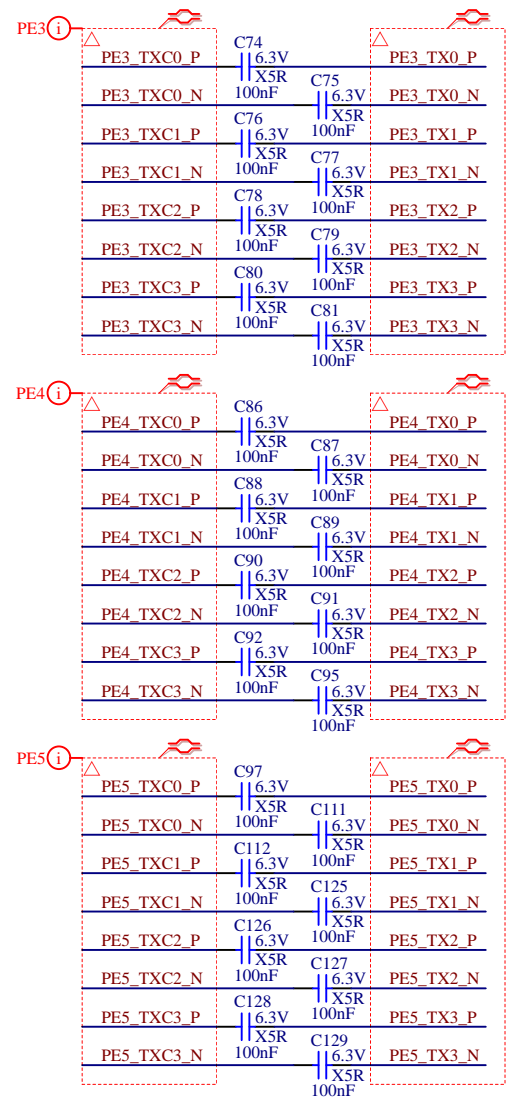
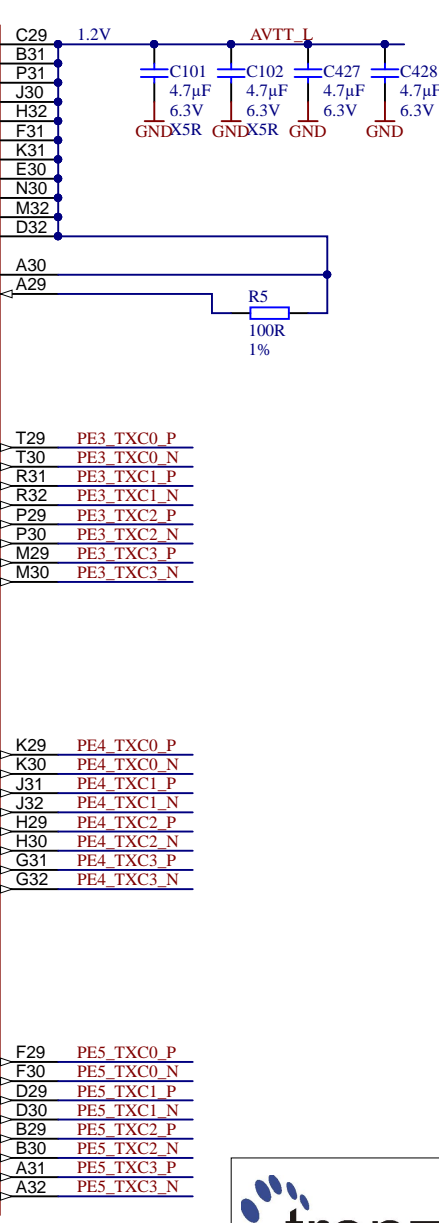
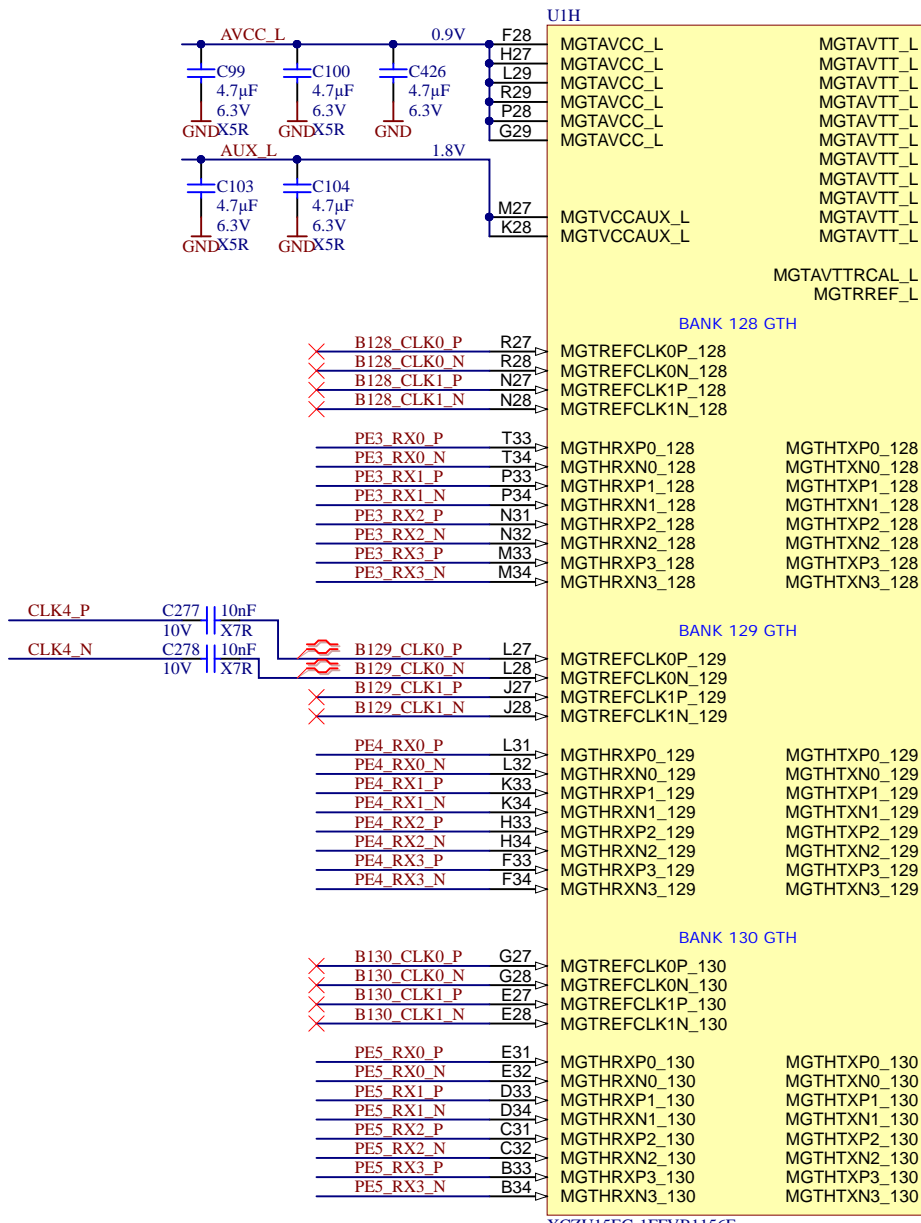
D

A

B

C

D



Title: <b>TEC0850 - FPGA_MGT_L</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: Trenz Electronic GmbH	
Page 13 of 33		
Filename: <b>ZU_MGT_L.SchDoc</b>		

A

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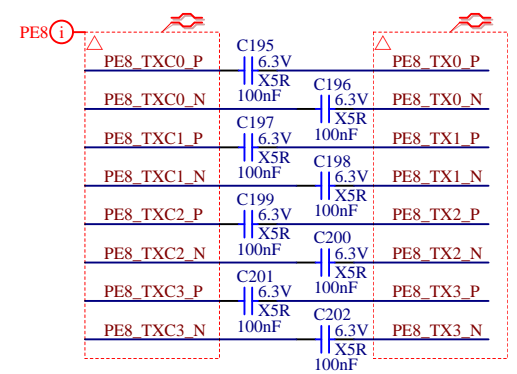
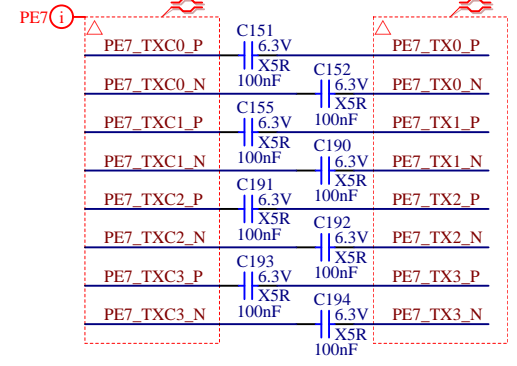
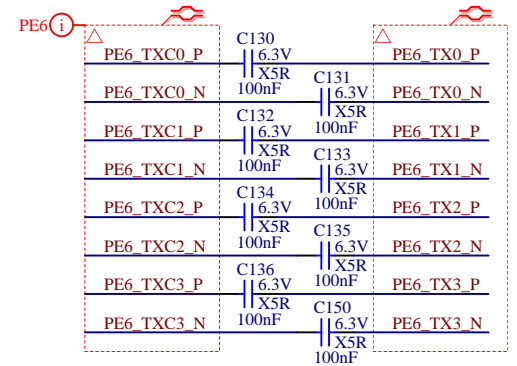
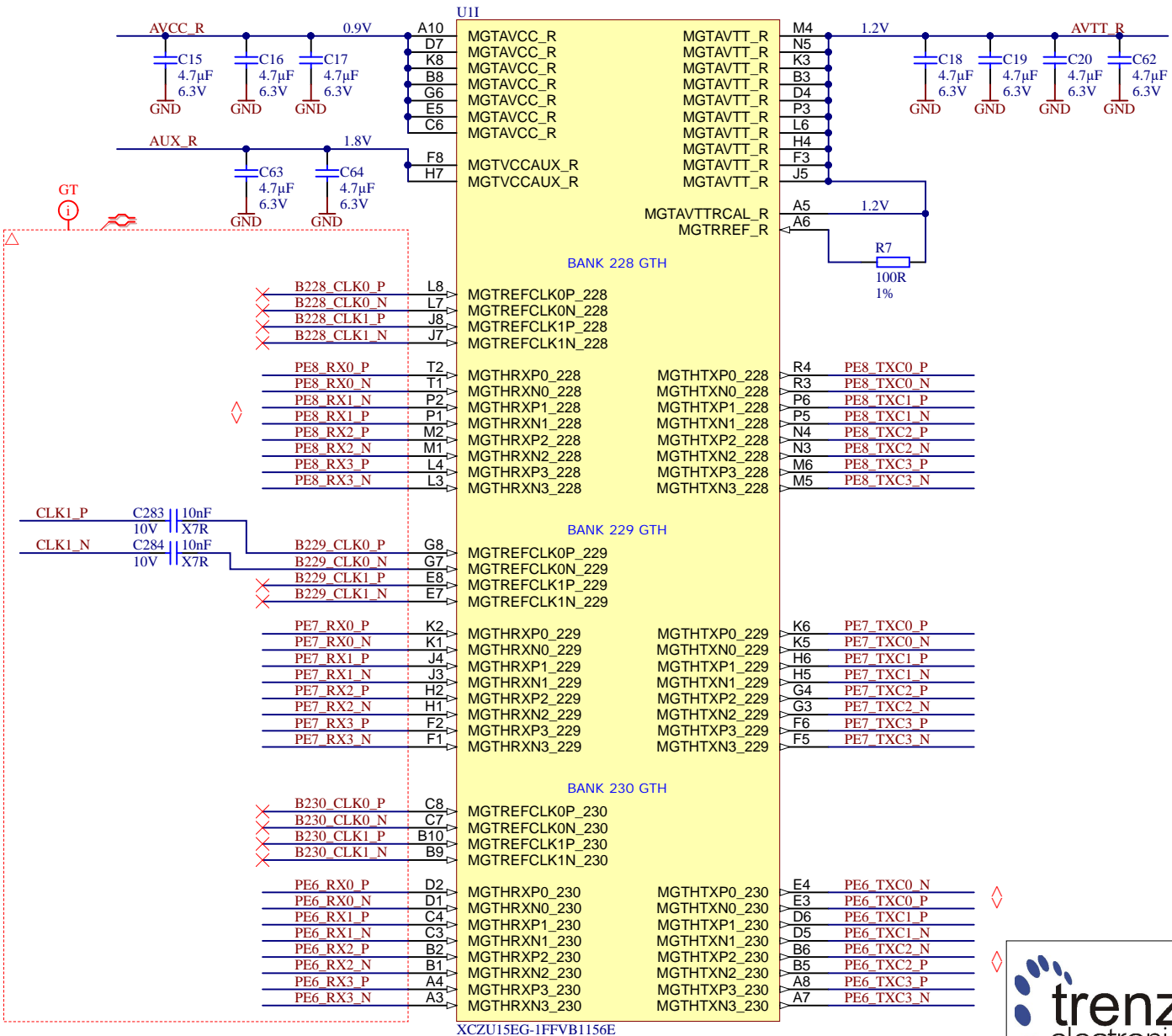
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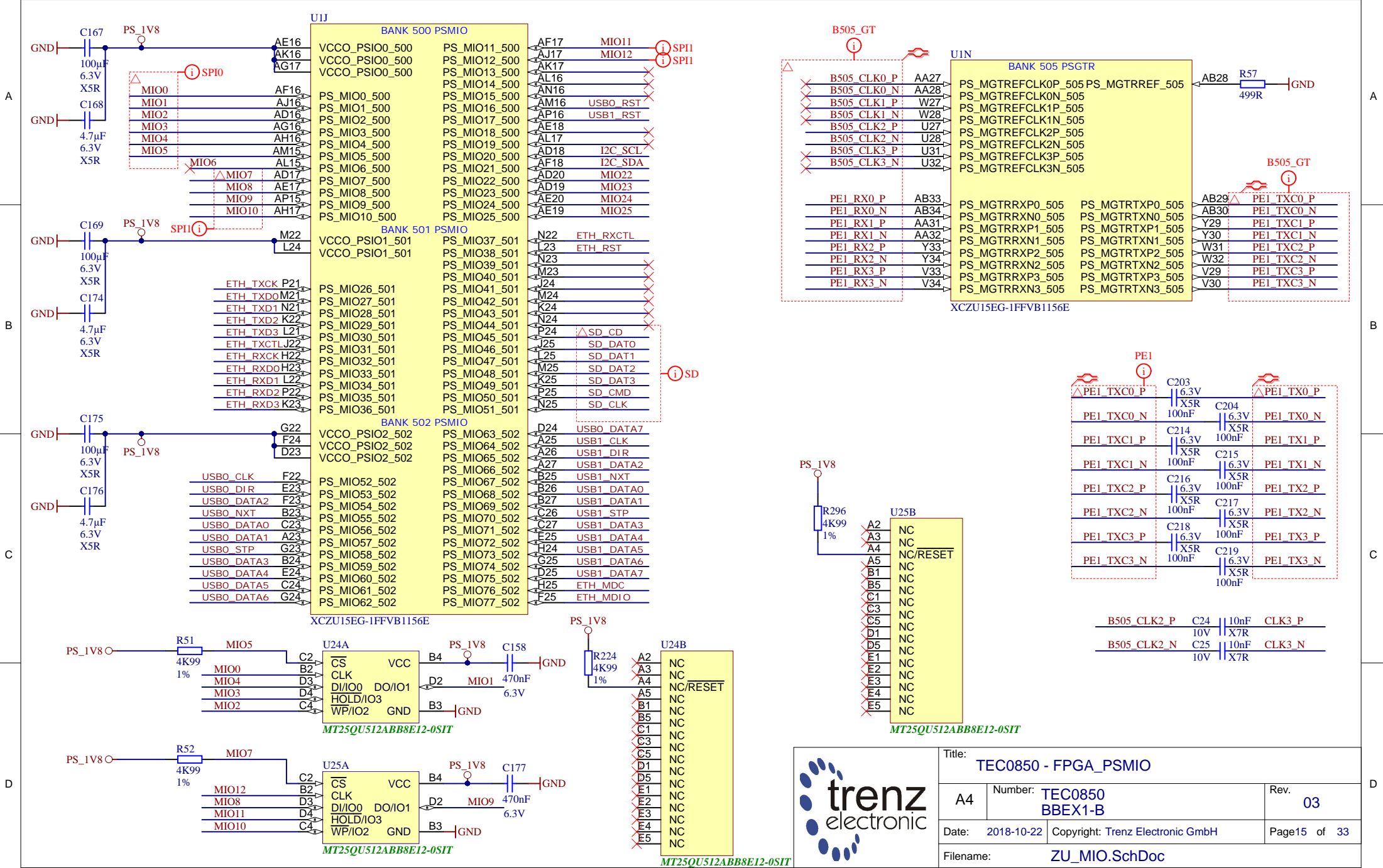
B

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Title: <b>TEC0850 - FPGA_MGT_R</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>14</b> of <b>33</b>
Filename: <b>ZU_MGT_R.SchDoc</b>		

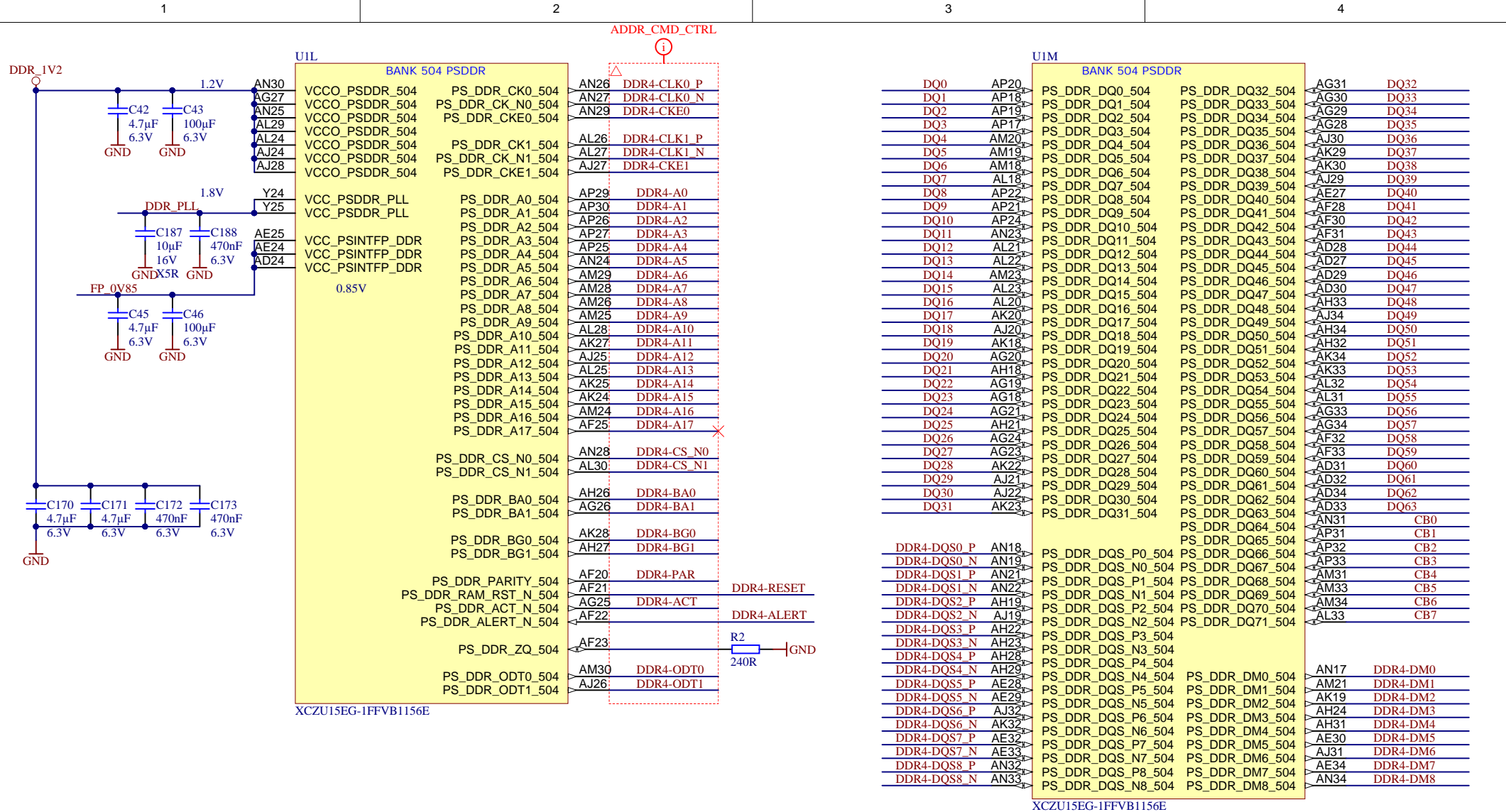



PE1_TXC0_P	C203	6.3V	X5R	100nF	PE1_TX0_N
PE1_TXC0_N	C204	6.3V	X5R	100nF	PE1_TX0_P
PE1_TXC1_P	C214	6.3V	X5R	100nF	PE1_TX1_P
PE1_TXC1_N	C215	6.3V	X5R	100nF	PE1_TX1_N
PE1_TXC2_P	C216	6.3V	X5R	100nF	PE1_TX2_P
PE1_TXC2_N	C217	6.3V	X5R	100nF	PE1_TX2_N
PE1_TXC3_P	C218	6.3V	X5R	100nF	PE1_TX3_P
PE1_TXC3_N	C219	6.3V	X5R	100nF	PE1_TX3_N

B505_CLK2_P	C24	10V	X7R	10nF	CLK3_P
B505_CLK2_N	C25	10V	X7R	10nF	CLK3_N



Title: <b>TEC0850 - FPGA_PSMIO</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>15</b> of <b>33</b>
Filename: <b>ZU_MIO.SchDoc</b>		



			Title: <b>TEC0850 - FPGA_PSDDR</b>	
			A4	Number: <b>TEC0850 BBEX1-B</b>
Date: <b>2018-10-22</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>16</b> of <b>33</b>
Filename: <b>ZU_PSDDR.SchDoc</b>				



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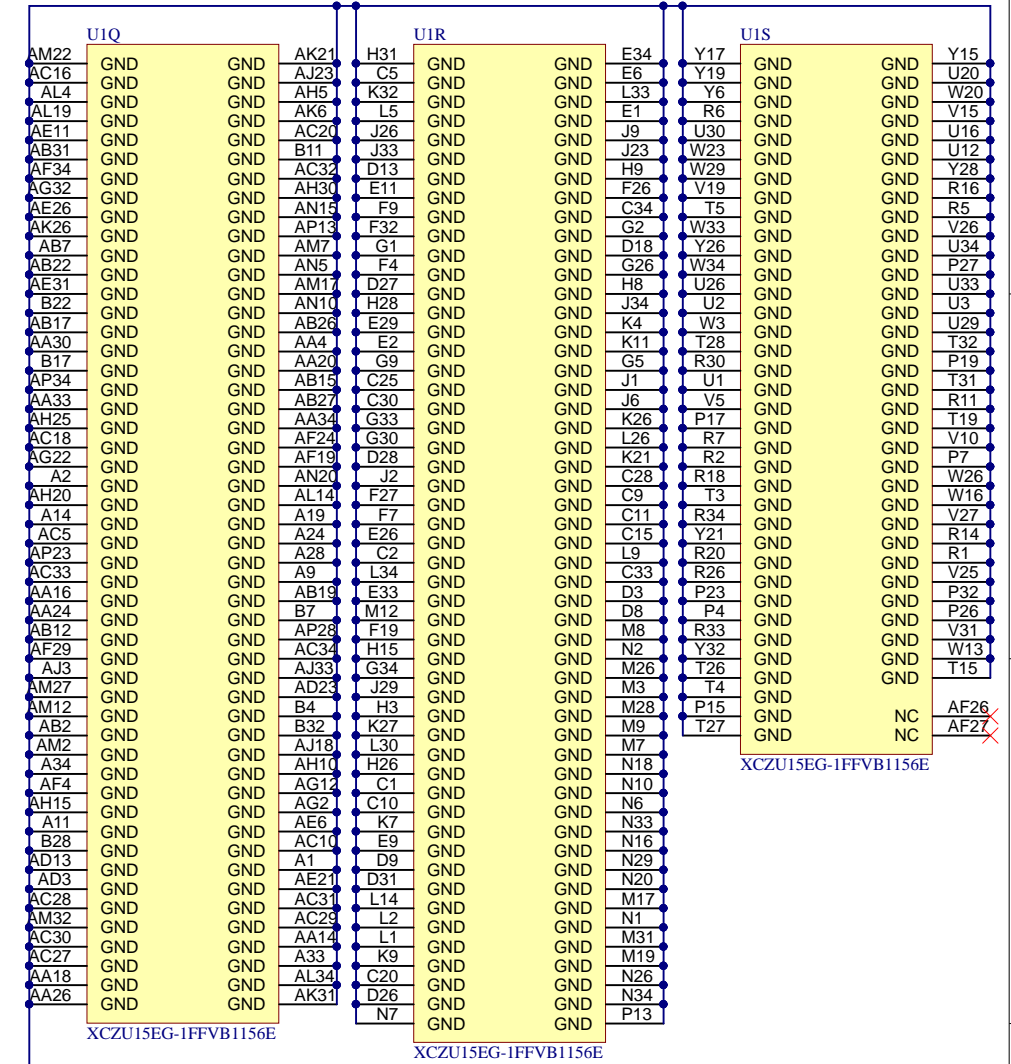
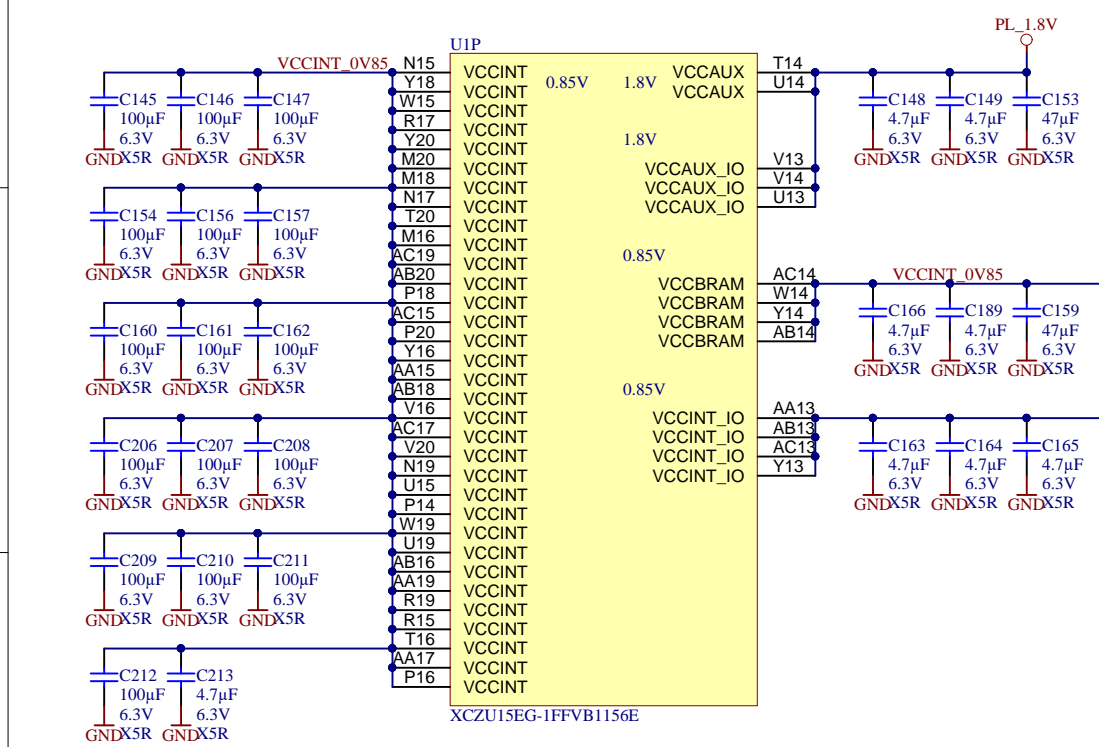
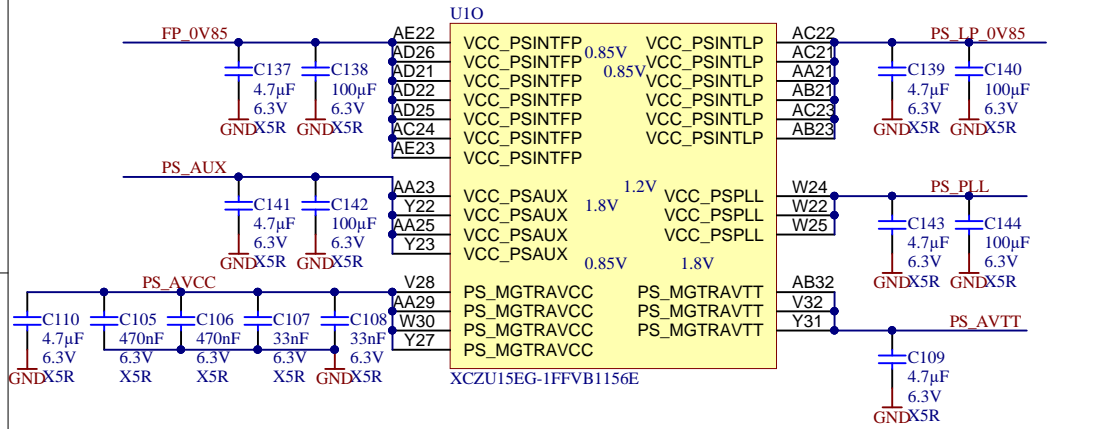
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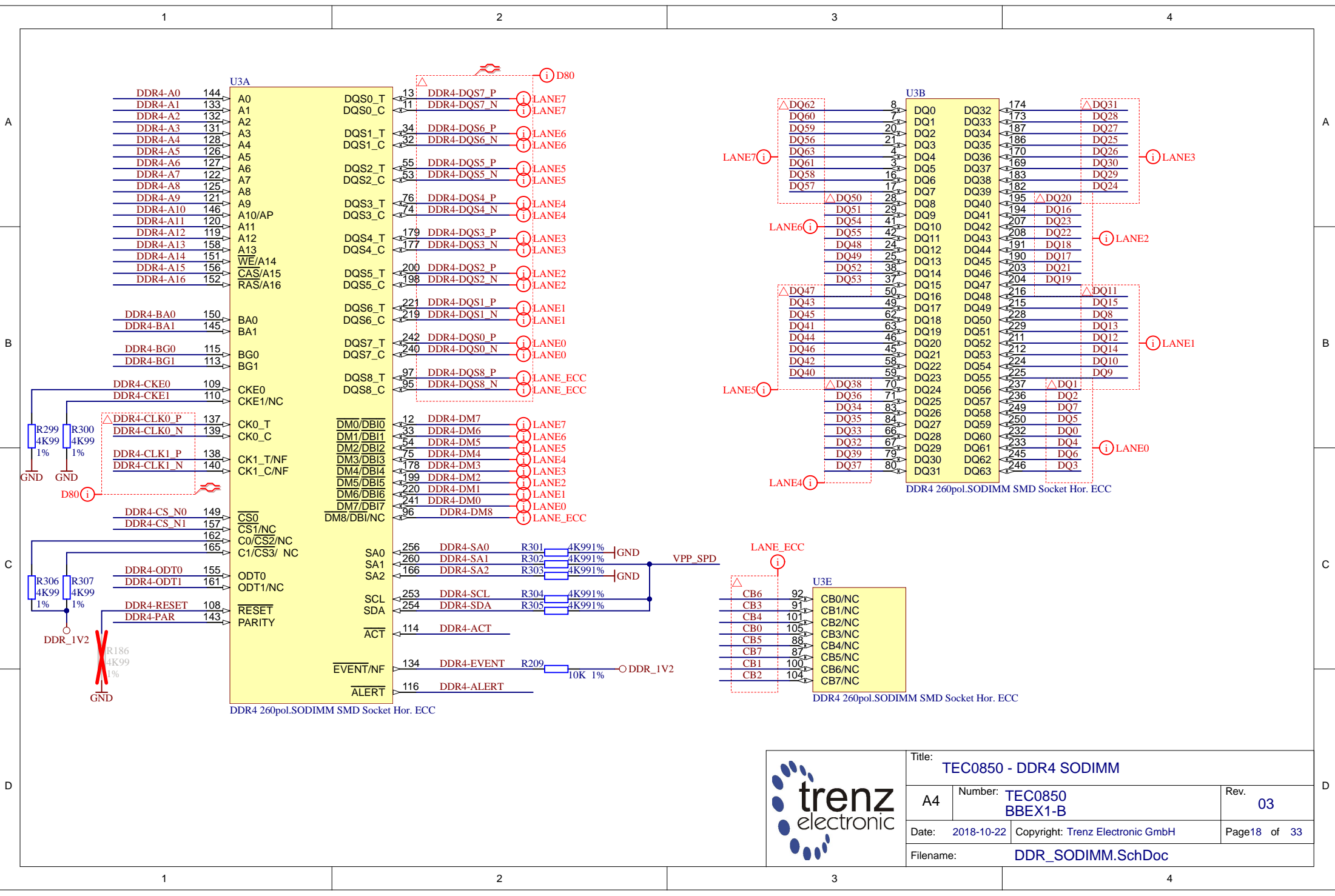
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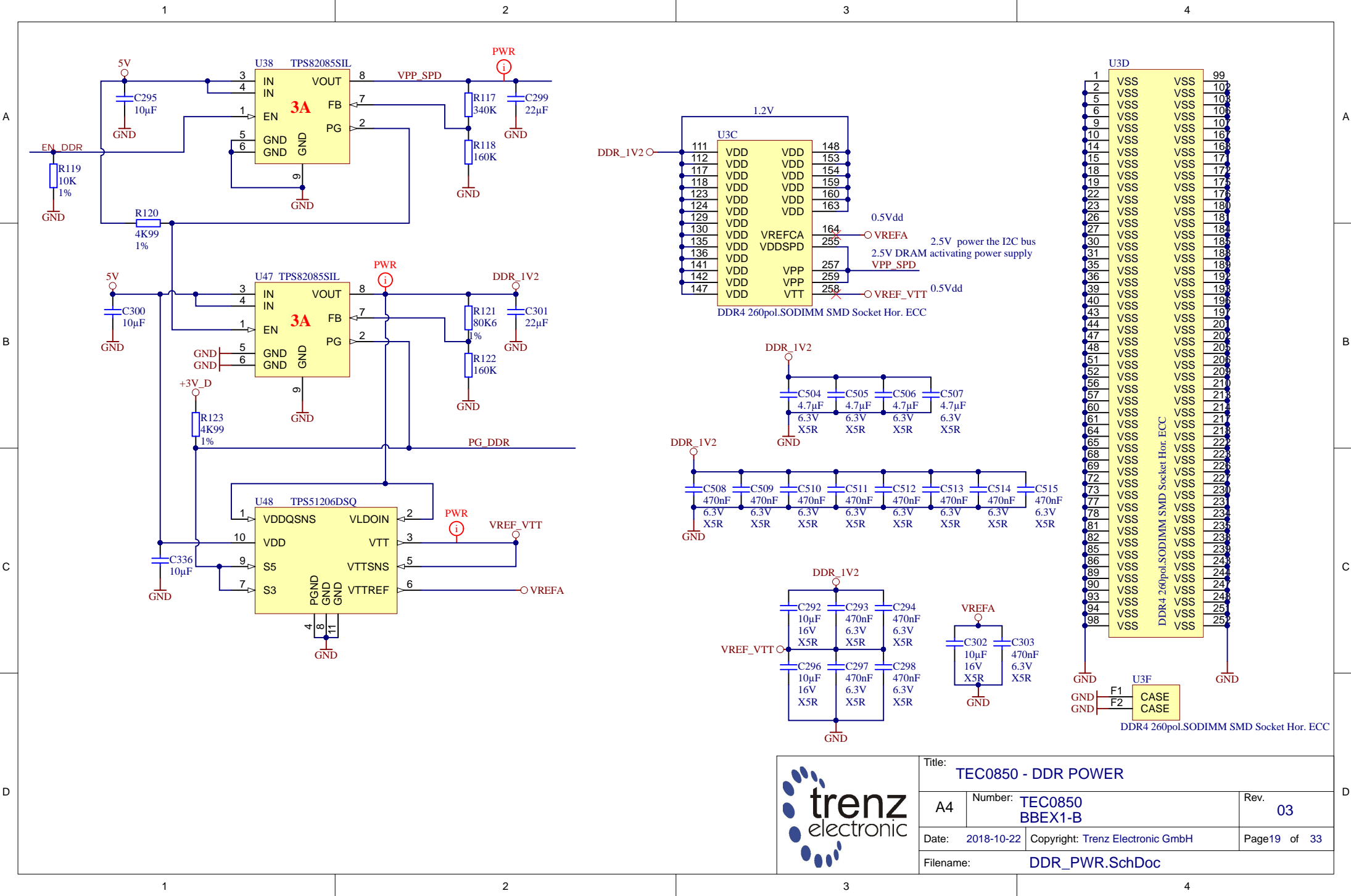
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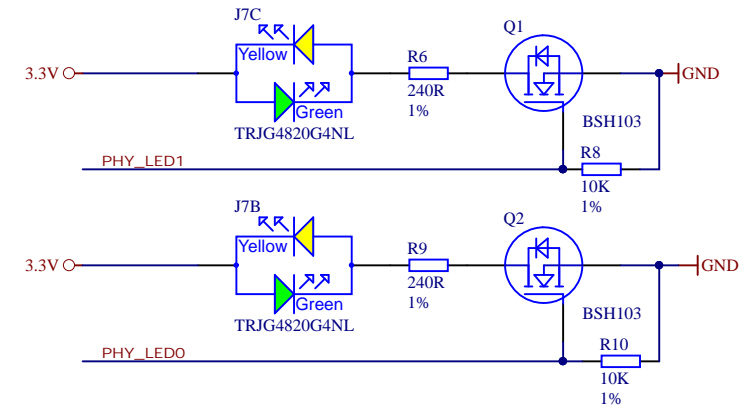
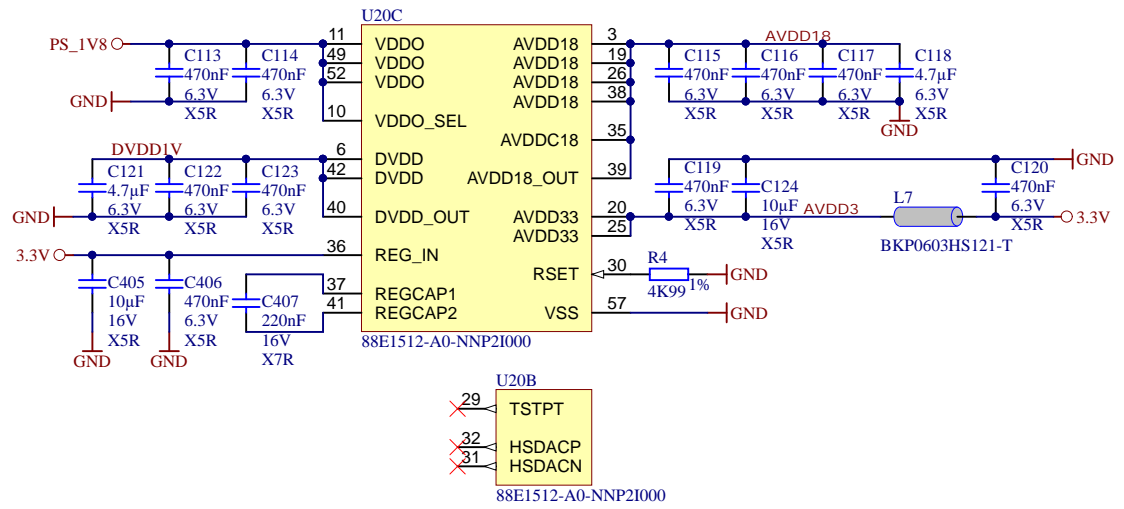
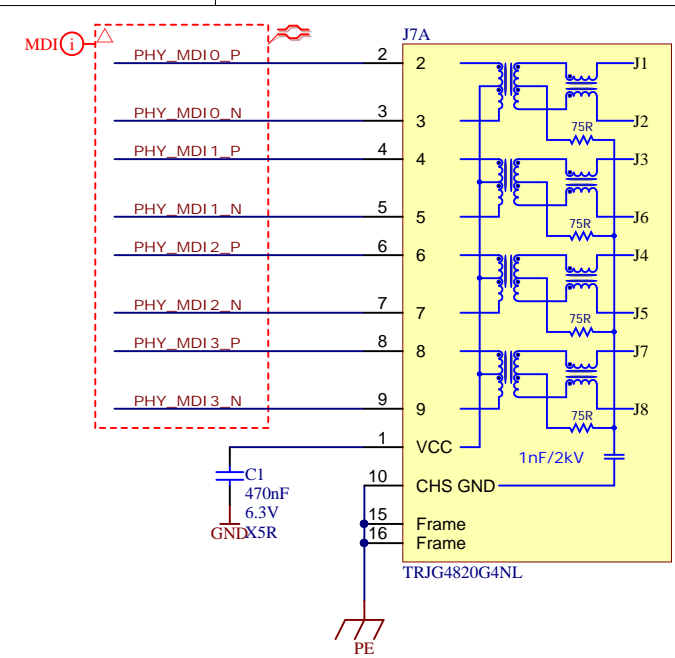
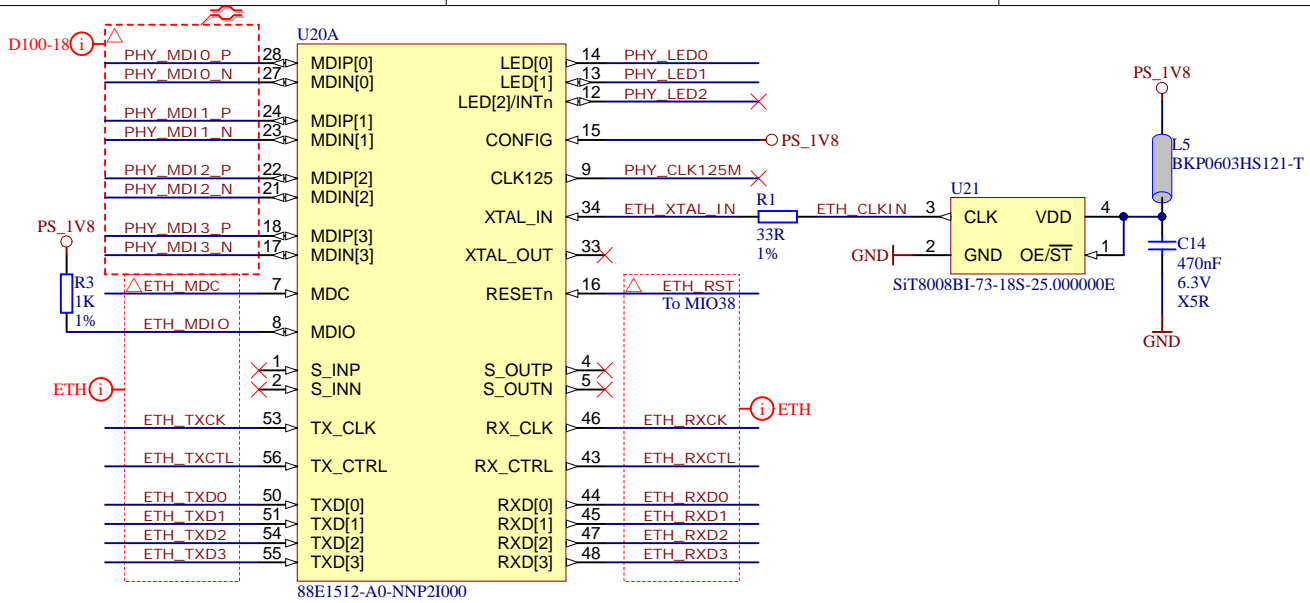
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A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>17</b> of <b>33</b>
Filename: <b>ZU_PWR.SchDoc</b>		



Title: <b>TEC0850 - DDR4 SODIMM</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page18 of 33
Filename: <b>DDR_SODIMM.SchDoc</b>		



Title: <b>TEC0850 - DDR POWER</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>19</b> of <b>33</b>
Filename: <b>DDR_PWR.SchDoc</b>		



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Title: **TEC0850 - ETH**

A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>20</b> of <b>33</b>
Filename: <b>Ethernet.SchDoc</b>		

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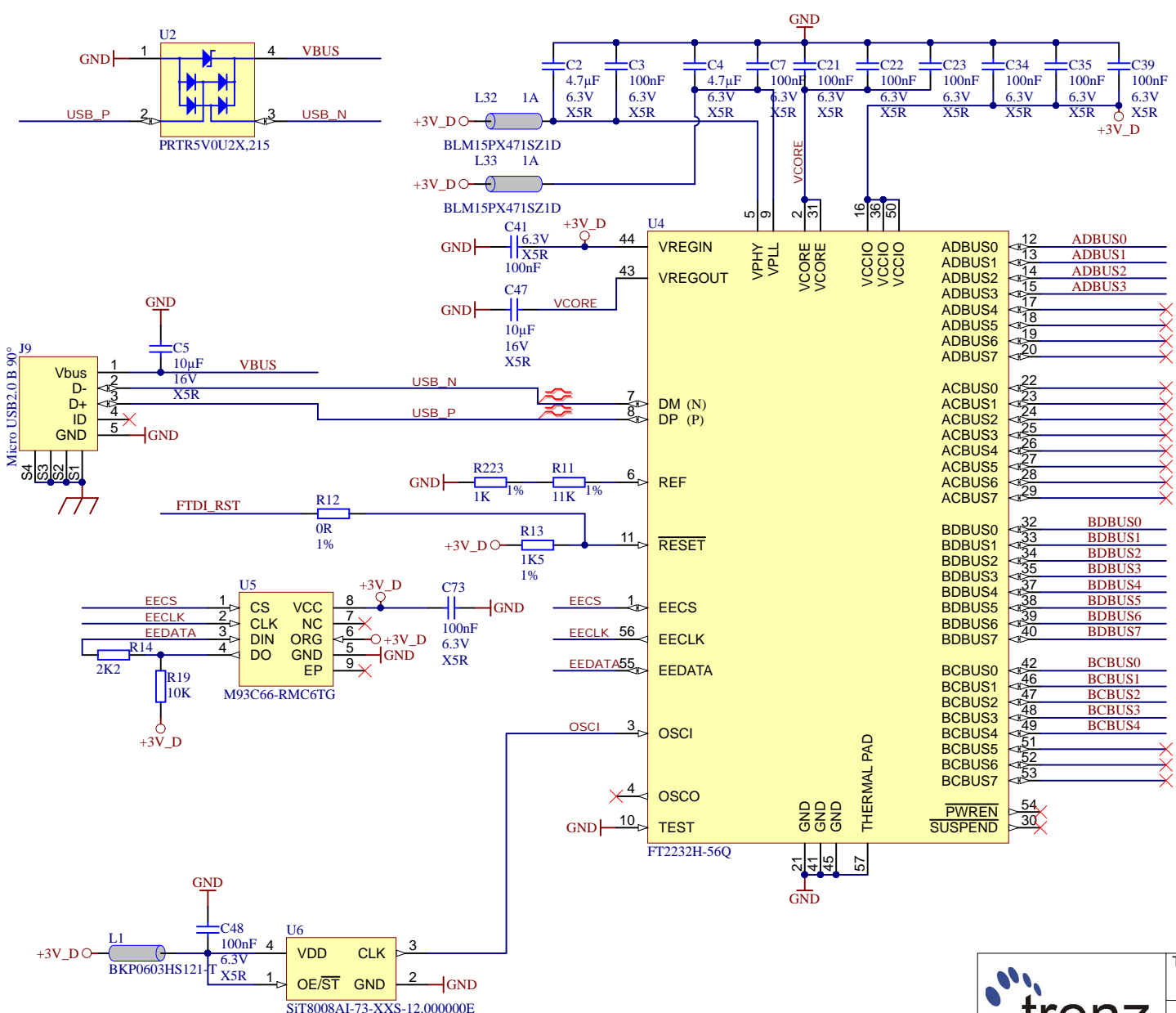
B

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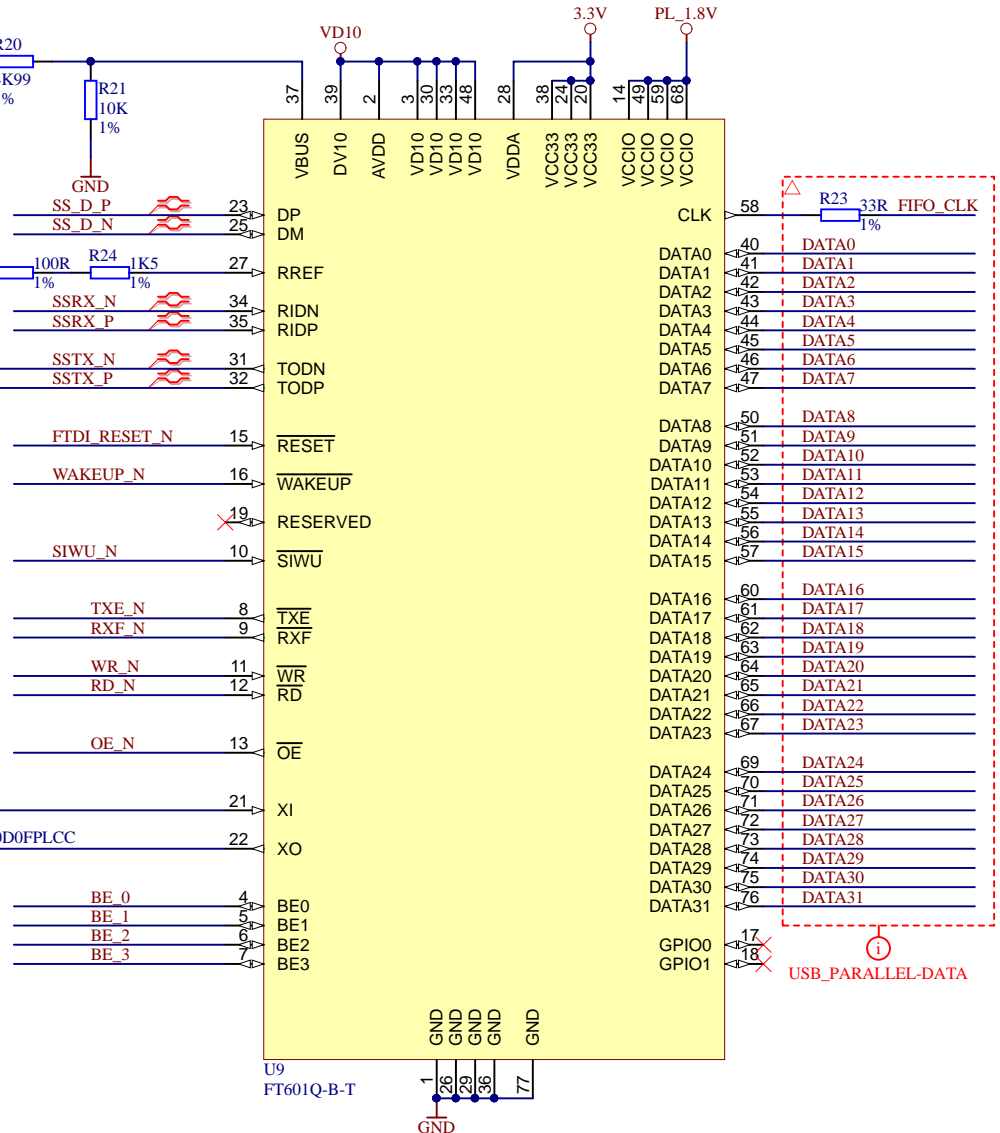
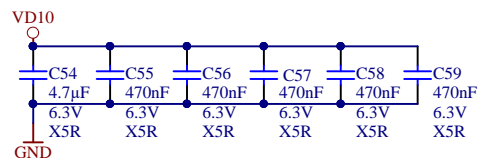
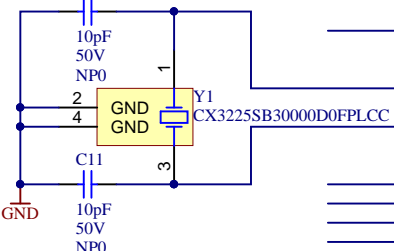
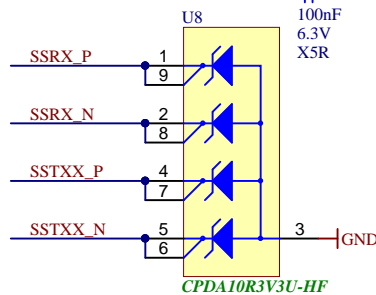
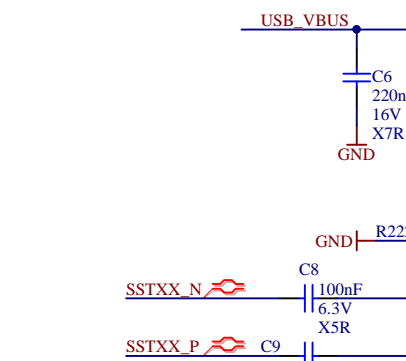
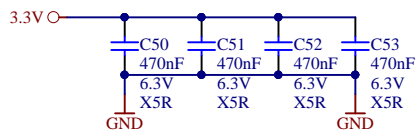
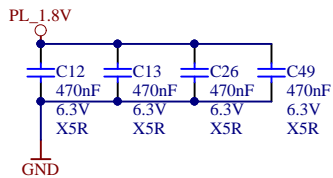
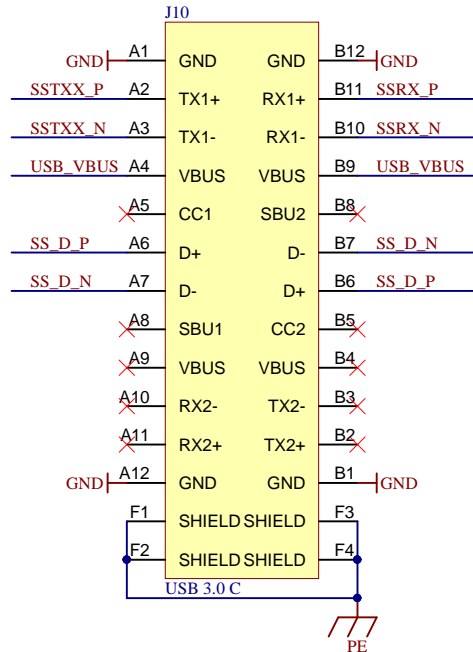
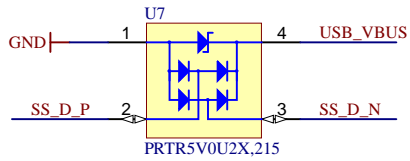
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A4	Number: TEC0850 BBEX1-B	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page 21 of 33
Filename: FTDI.SchDoc		

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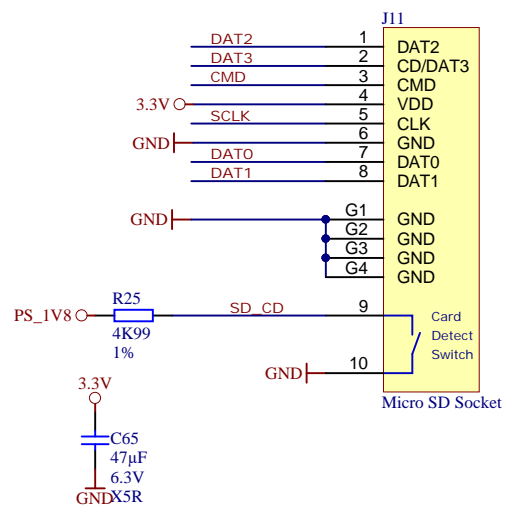
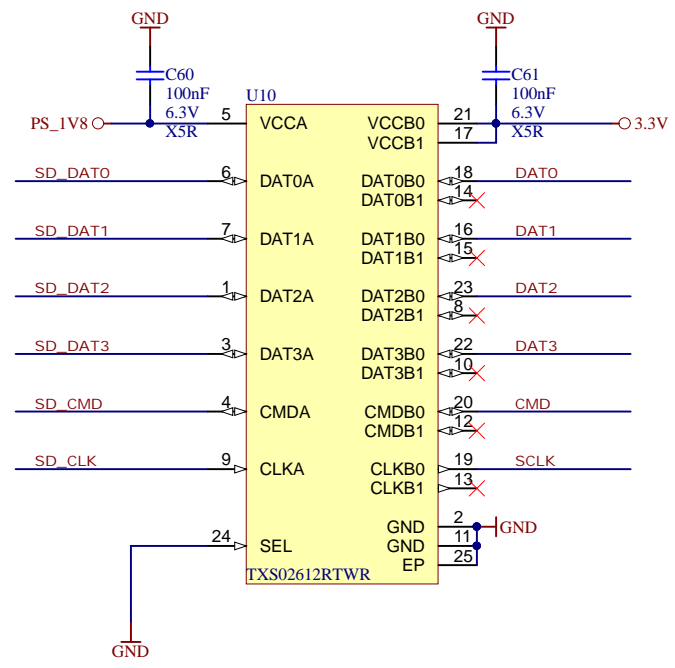
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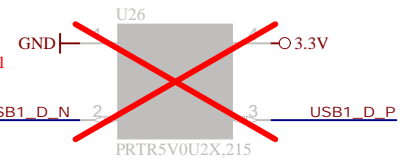
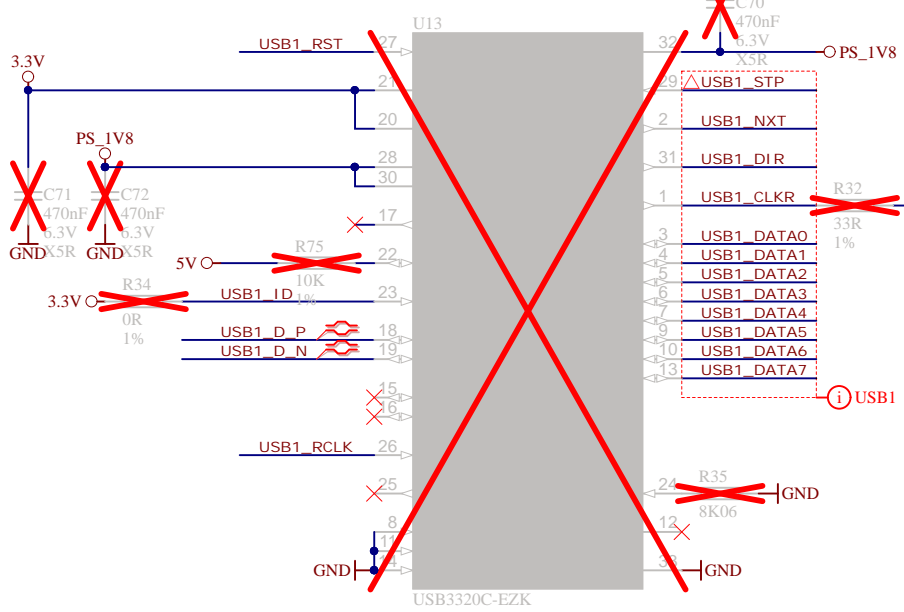
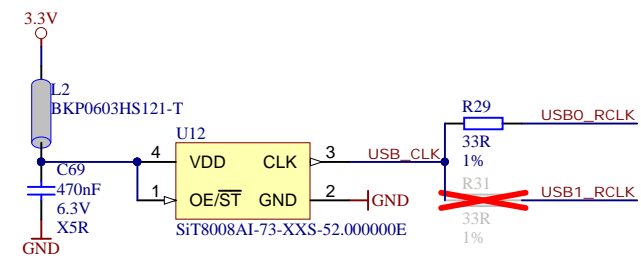
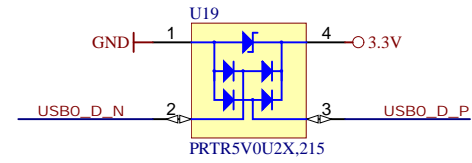
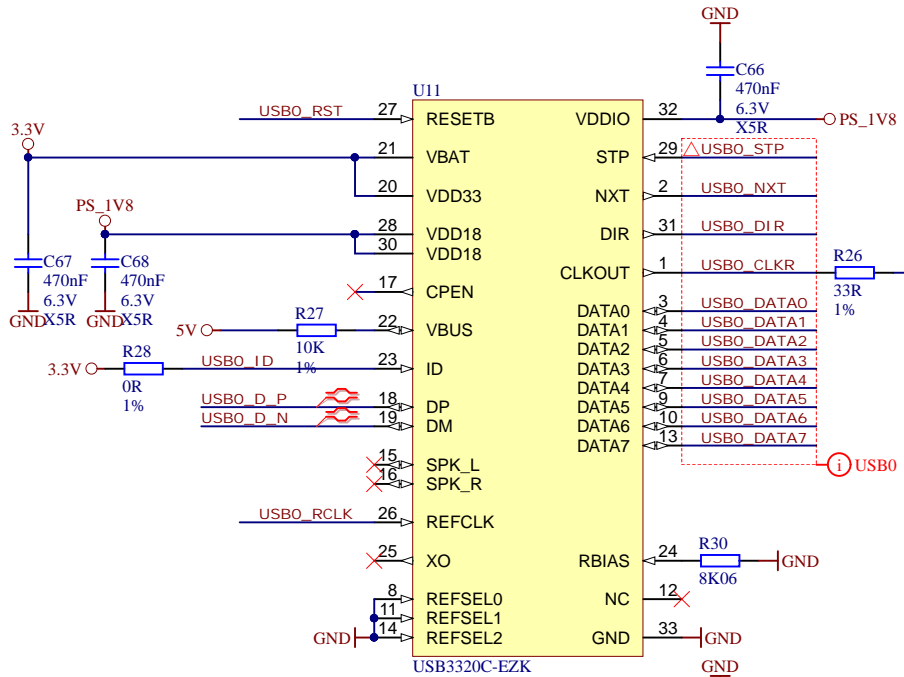


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Title: TEC0850 - USB3.0		
A4	Number: TEC0850 BBEX1-B	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page 22 of 33
Filename: USB30.SchDoc		

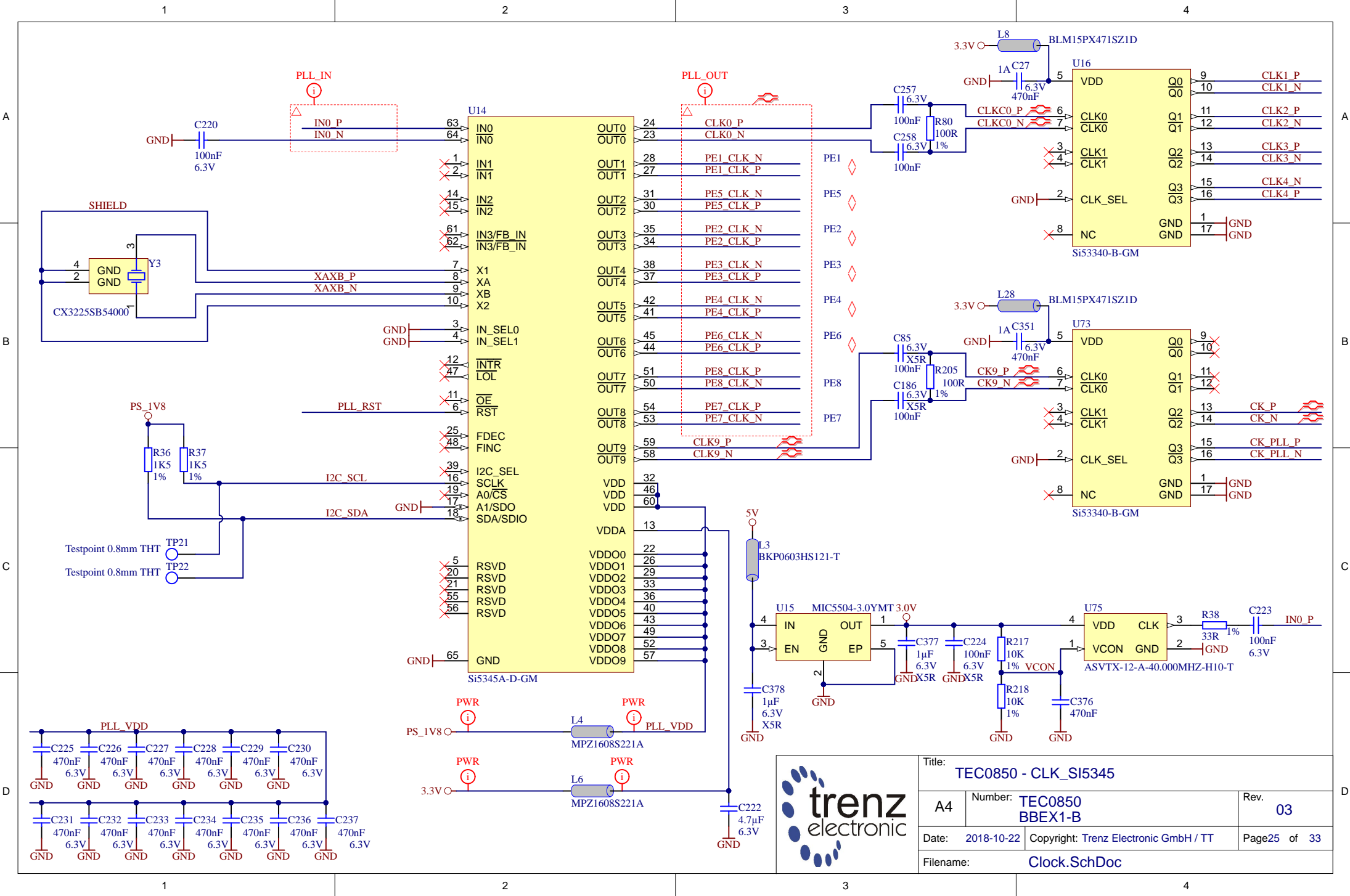


	Title: <b>TEC0850 - SDCard</b>		
	A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
	Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>23</b> of <b>33</b>
	Filename: <b>SDCard.SchDoc</b>		

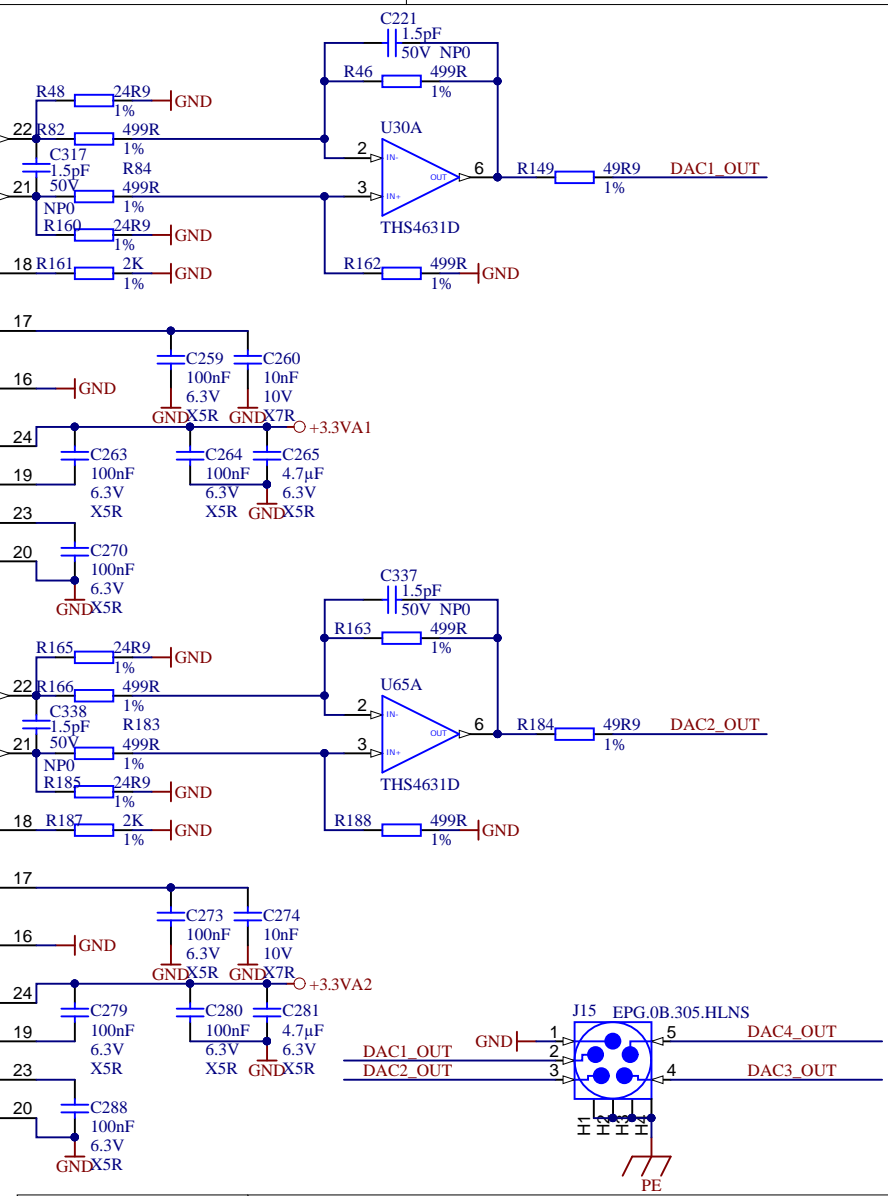
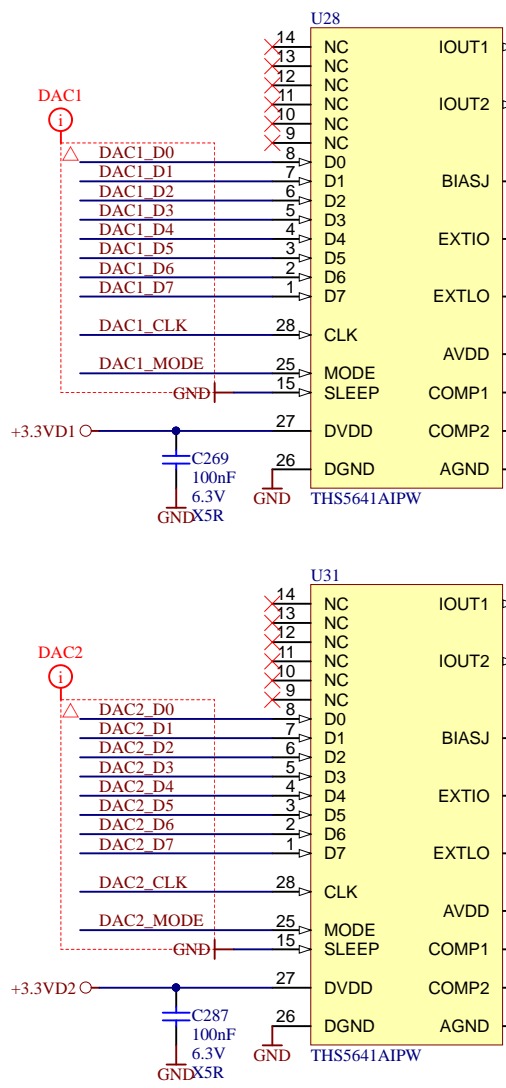
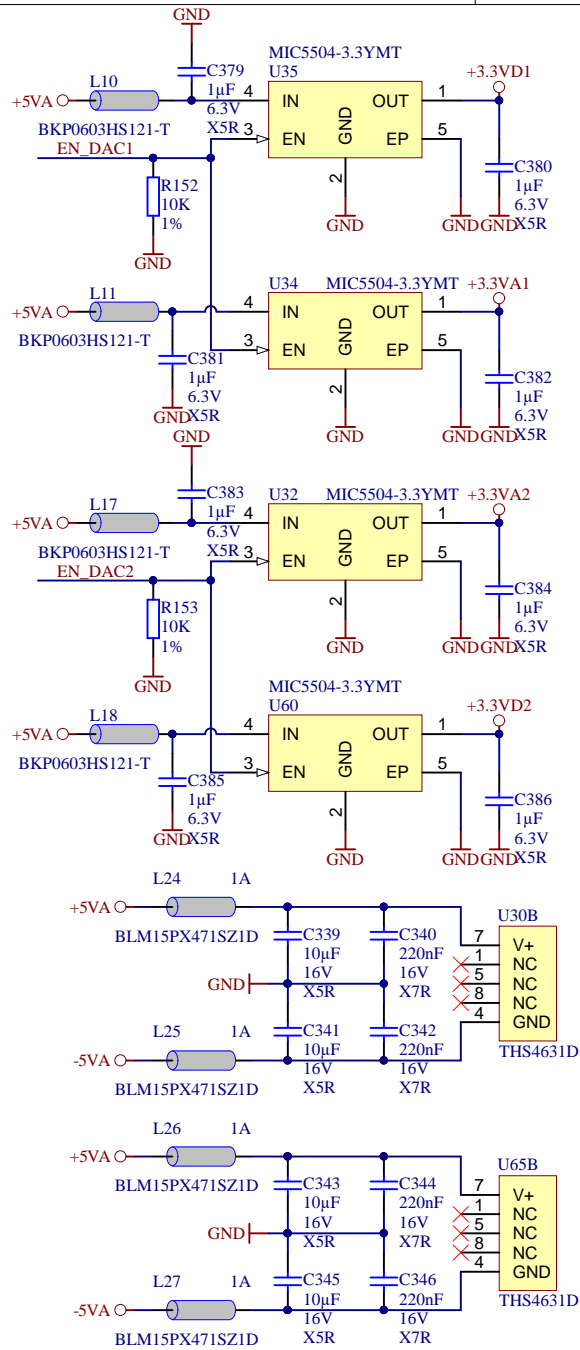


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	A4	Number: <b>TEC0850 BBEX1-B</b>
	Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>
	Page <b>24</b> of <b>33</b>	Rev. <b>03</b>
Filename: <b>USB-PHY.SchDoc</b>		

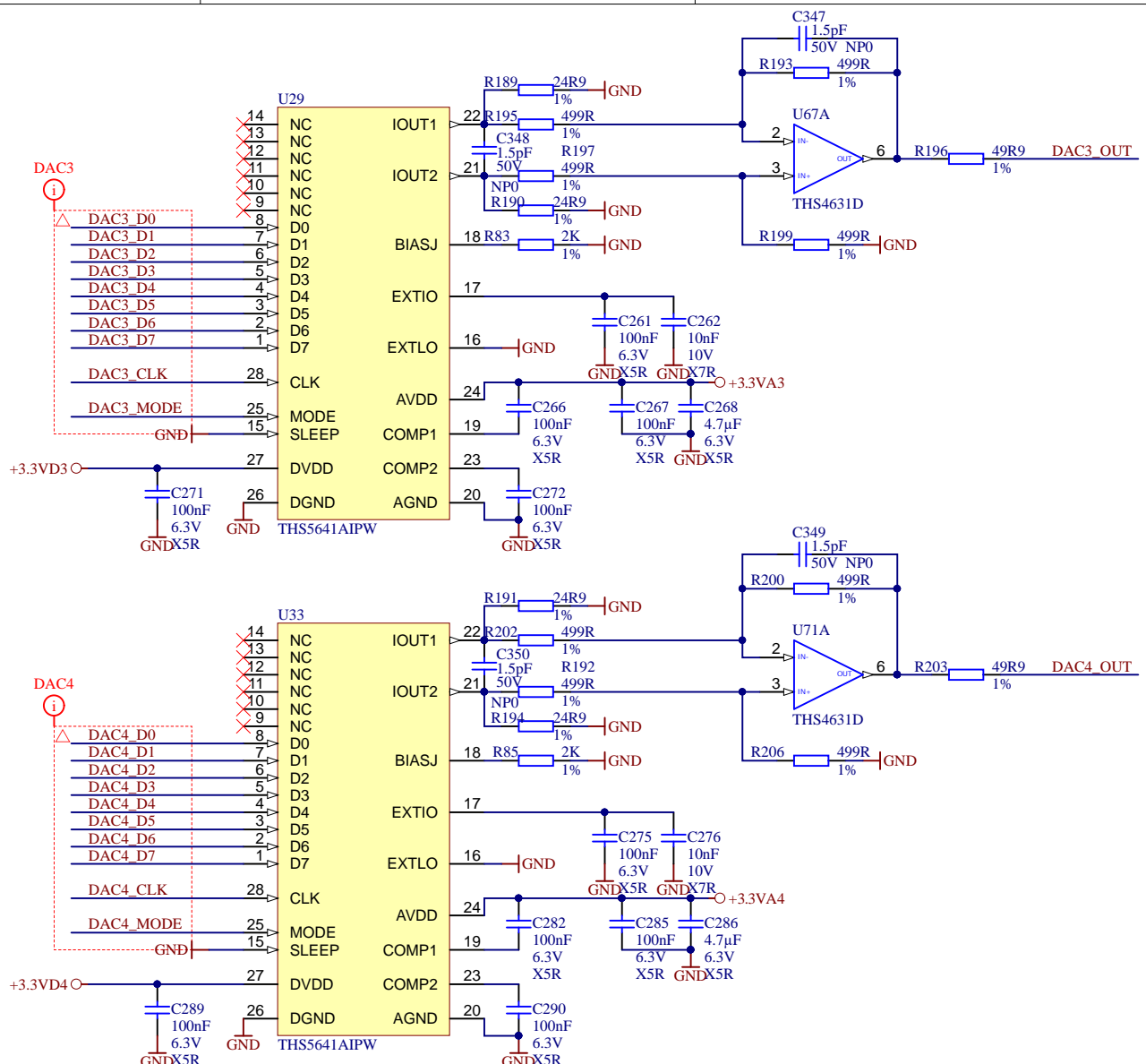
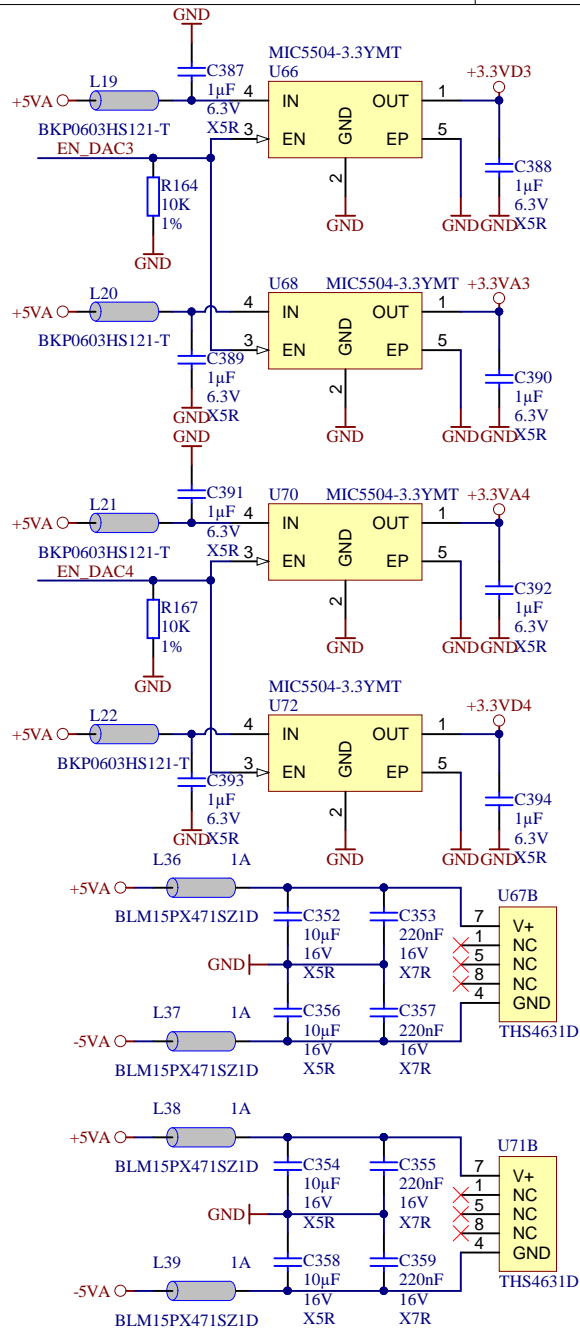





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A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>25</b> of <b>33</b>
Filename: <b>Clock.SchDoc</b>		

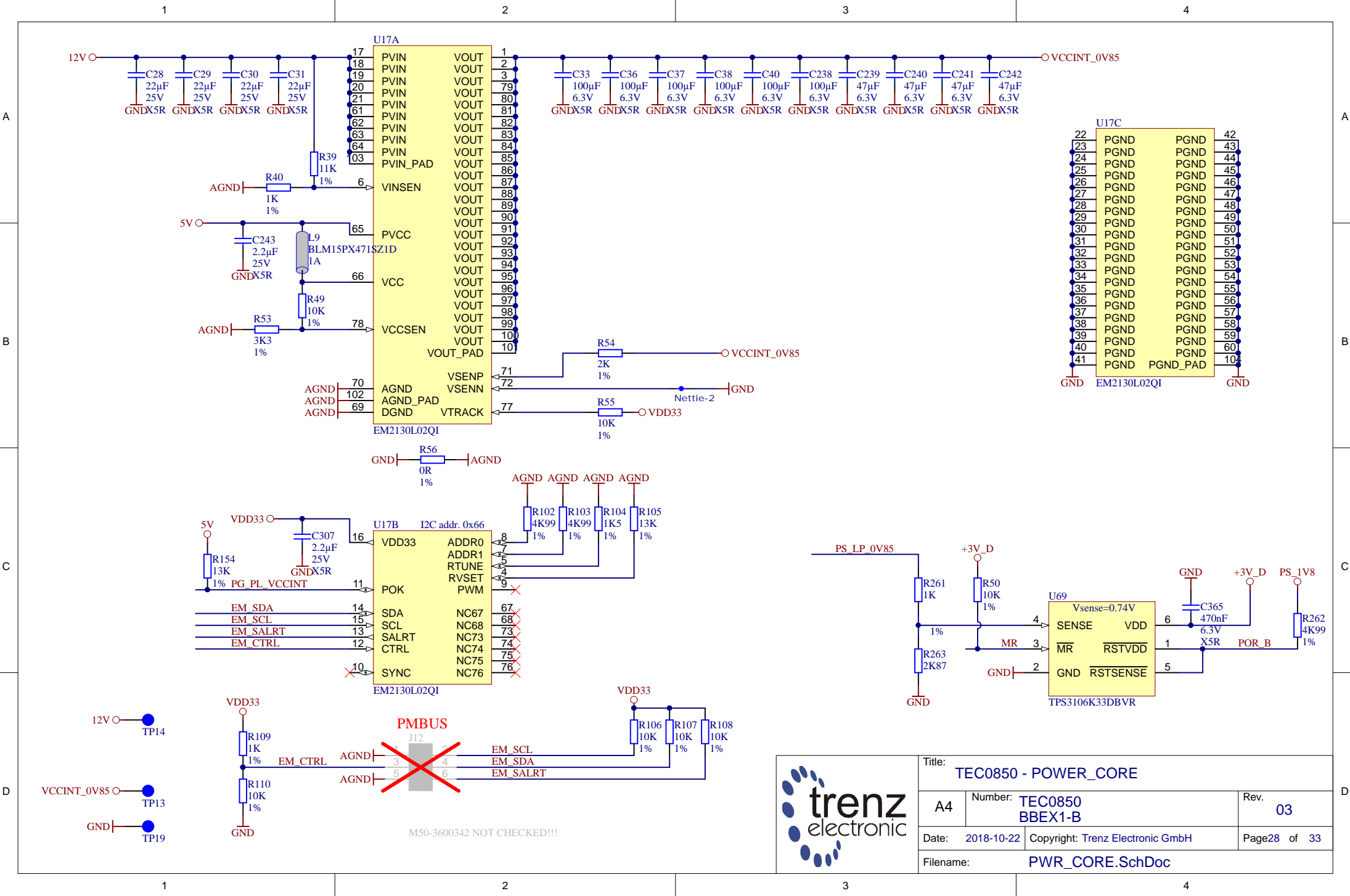


Title: TEC0850 - DAC1_DAC2		
A4	Number: TEC0850 BBEX1-B	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page 26 of 33
Filename: DAC12_8bit.SchDoc		



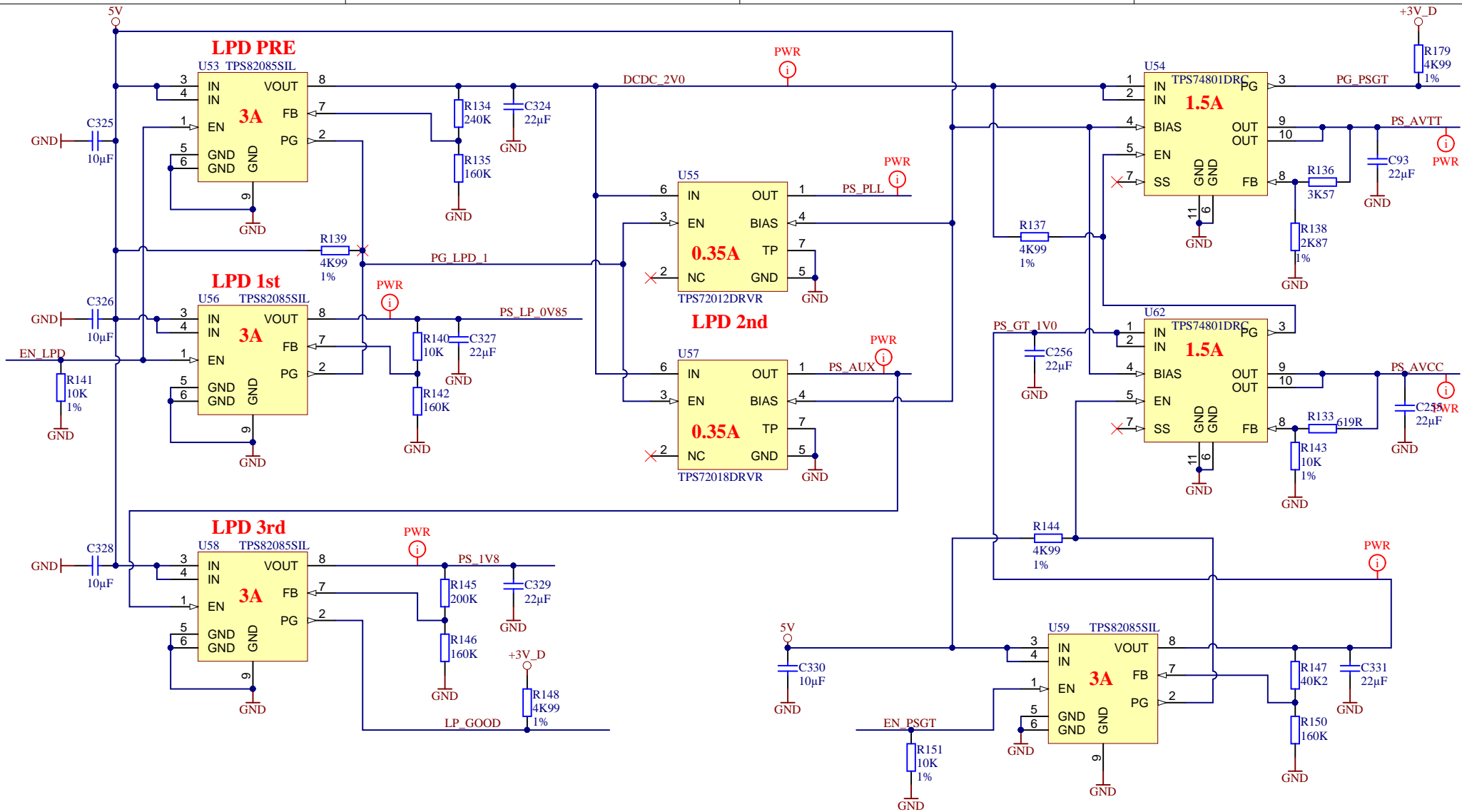



Title: <b>TEC0850 - DAC3_DAC4</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page 27 of 33
Filename: <b>DAC34_8bit.SchDoc</b>		

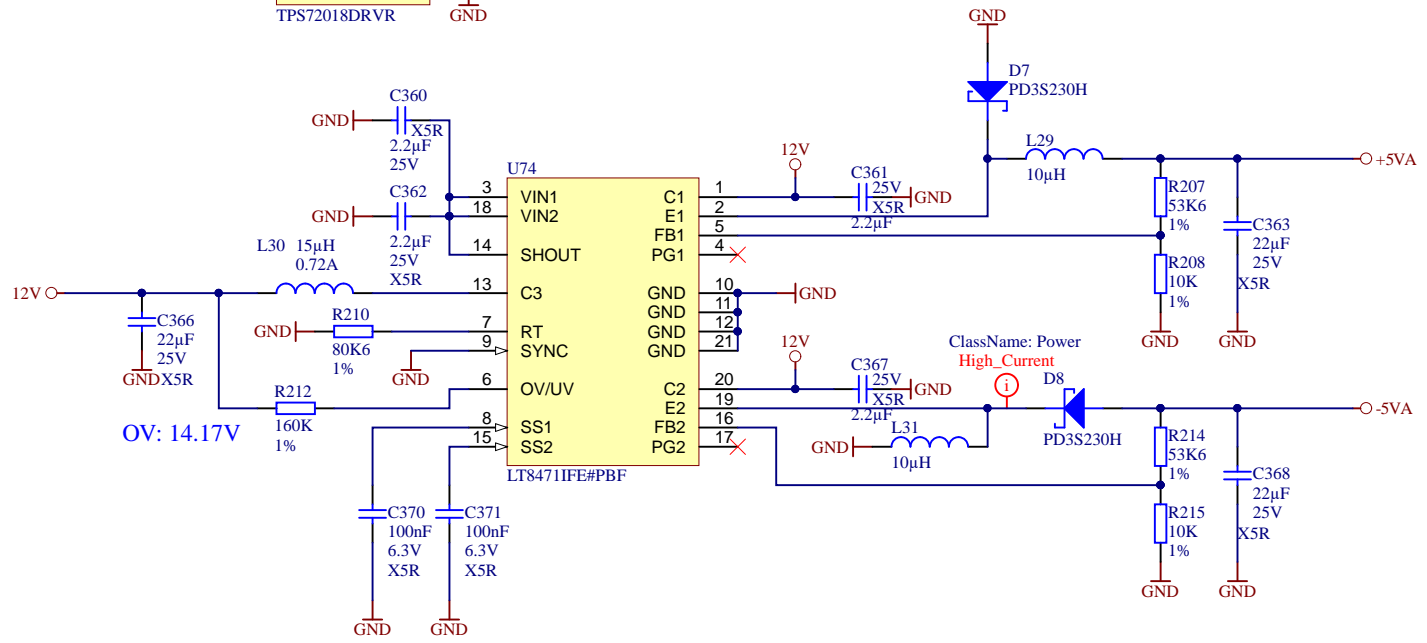
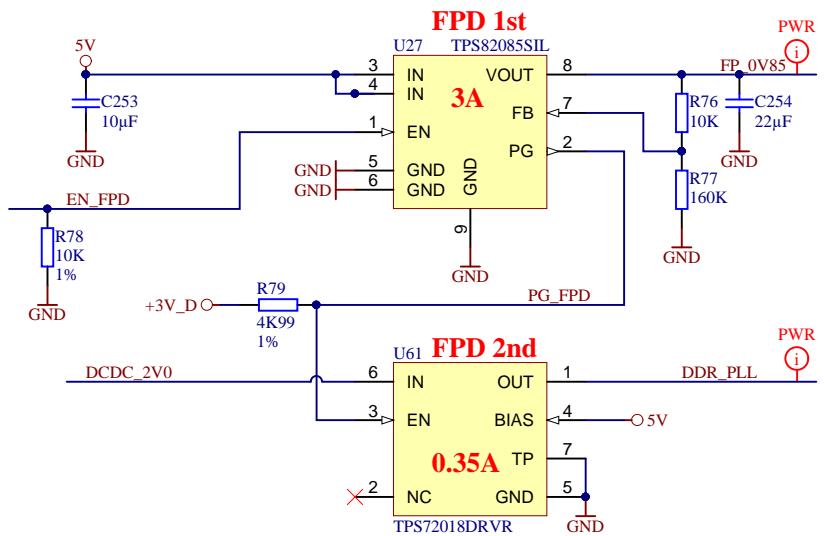



Title: <b>TEC0850 - POWER_CORE</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: Trenz Electronic GmbH	
Page 28		of 33
Filename: <b>PWR_CORE.SchDoc</b>		

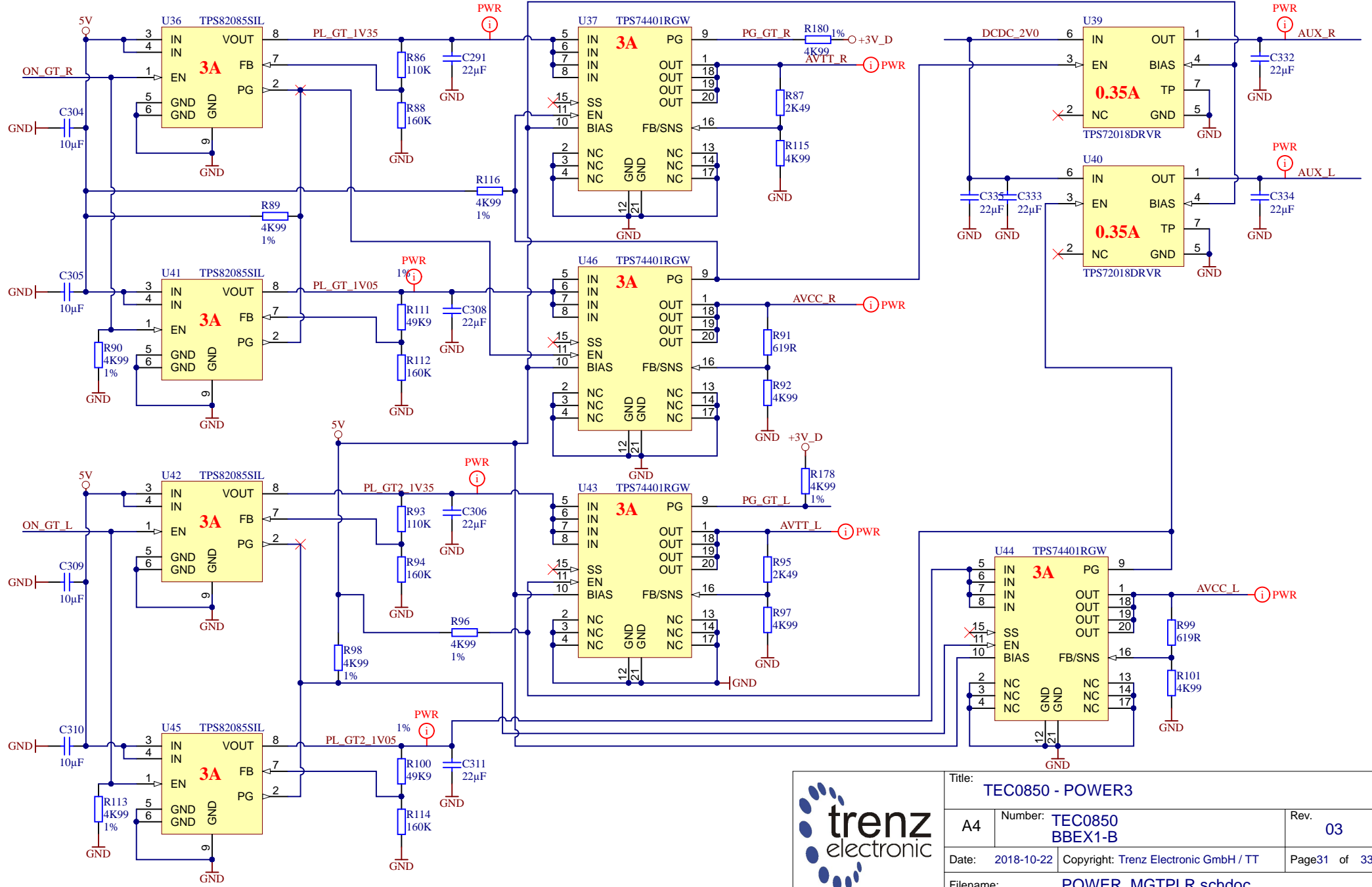
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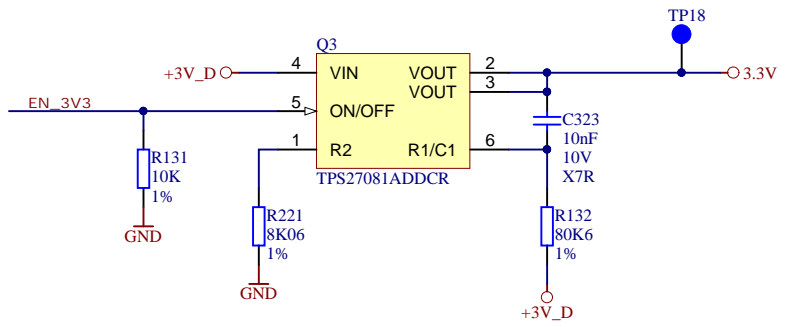
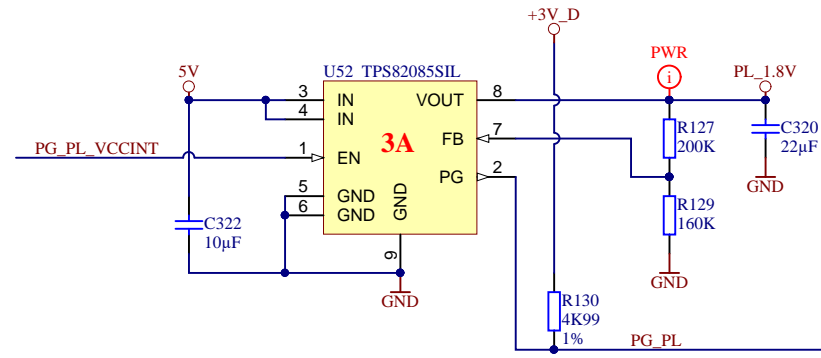
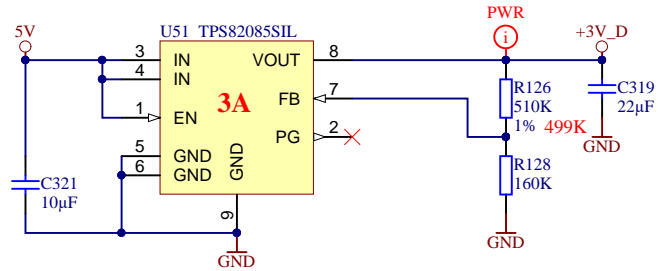
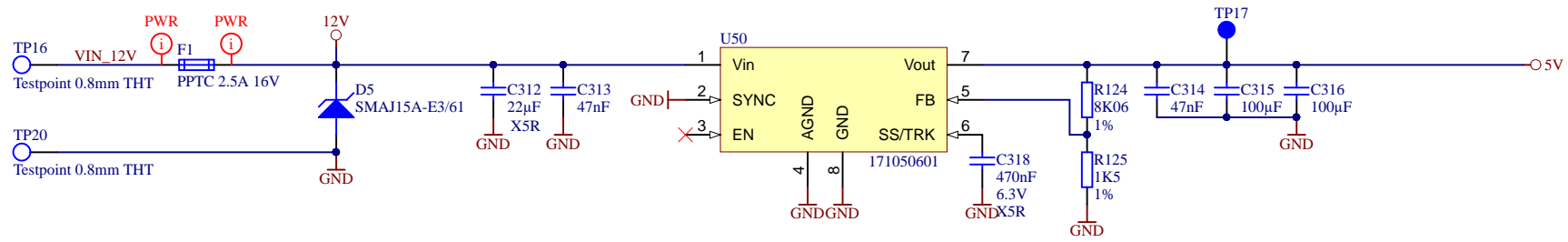
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			A4	Number: TEC0850 BBEX1-B
Date: 2018-10-22		Copyright: Trenz Electronic GmbH / TT		Page 29 of 33
Filename: POWER_PSLP.schdoc				



	Title: TEC0850 - POWER2		
	A4	Number: TEC0850 BBEX1-B	Rev. 03
	Date: 2018-10-22	Copyright: Trenz Electronic GmbH / TT	Page30 of 33
	Filename: POWER_PSFP.schdoc		



Title: <b>TEC0850 - POWER3</b>		
A4	Number: <b>TEC0850 BBEX1-B</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>31</b> of <b>33</b>
Filename: <b>POWER_MGTPLR.schdoc</b>		



	Title: TEC0850 - POWER4		
	A4	Number: TEC0850 BBEX1-B	Rev. 03
	Date: 2018-10-22	Copyright: Trenz Electronic GmbH / TT	Page 32 of 33
	Filename: POWER_MGTPLL.schdoc		



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CHANGES REV01 to REV02

- 1) Fixed connection for U16 (Si53340-B-GM)
- 2) Added THT-testpoints for I2C-bus
- 3) Changed MEMS osc to TCXO osc , added LDO for TCXO osc
- 4) Use out9 from PLL, added dual output buffer ("1" -> MPSOC, B65; "2" -> J1, cPCI-serial)
- 5) Changed connector J12 (do not populated)
- 6) Added capacitors C372, C373 on the clock line (AC-coupling)
- 7) Changed OPs for DACs (LT6200IS6 -> THS4631D)
- 8) Added additional DCDC (+/-5V) for THS4631D
- 9) Added THT-testpoints for VIN/GND
- 10) full update lib

CHANGES REV02 to REV03


- 1) Fixed connection for U74 (LT8471IFE#PBF)
- 2) Added additional resistors R219/R220
- 3) Fixed connection for Y2 (CM2012-2pad)
- 4) Changed U69 (TPS3106E09DBVR -> TPS3106K33DBVR)
- 5) Changed U73 (LTC6957IDD-2#PBF -> Si53340-B-GM)
- 6) Optimized BOM
- 7) full update lib

CHANGES REV03a

- 1) VY: replaced DDR4 SODIMM socket (b030-2604-6021-zhf -> 2309407-1)

CHANGES REV03b (19.08.2020):

- 1) VY: Protection circuit U8 ESD3V3U4ULCE6327XTSA1 replaced by CPDA10R3V3U-HF

		Title: <b>TEC0850 - Changes list</b>	
		A4	Number: <b>TEC0850 BBEX1-B</b>
Date: <b>2018-10-22</b>		Copyright: <b>Trenz Electronic GmbH</b>	
Filename: <b>Revision_Changes.SchDoc</b>		Page <b>33</b> of <b>33</b>	

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