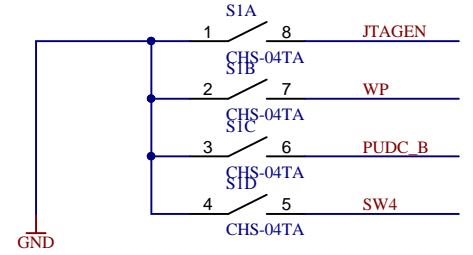
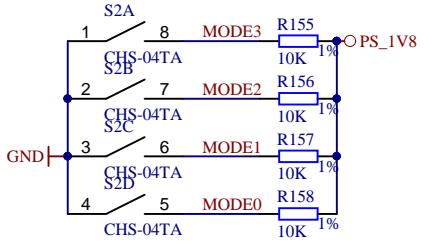
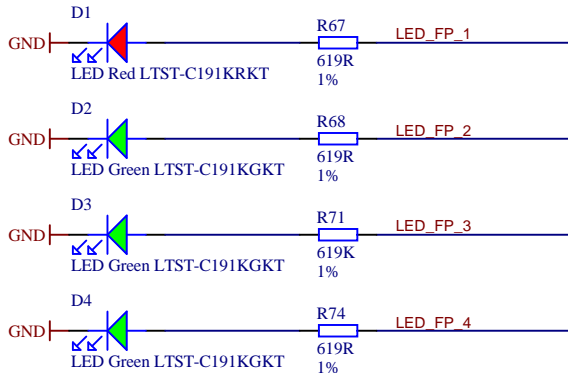
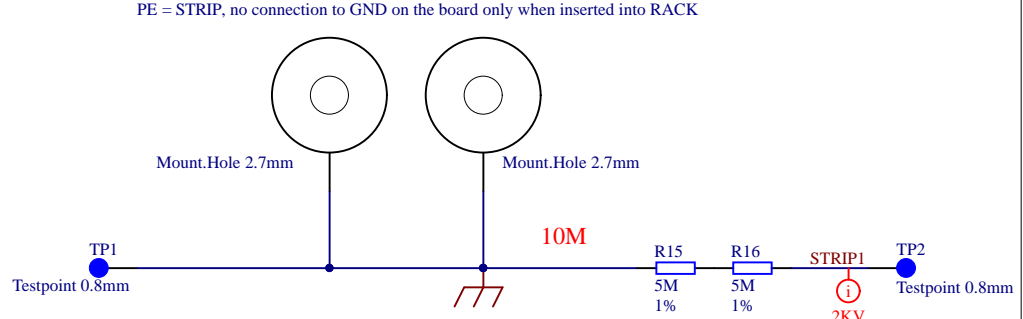
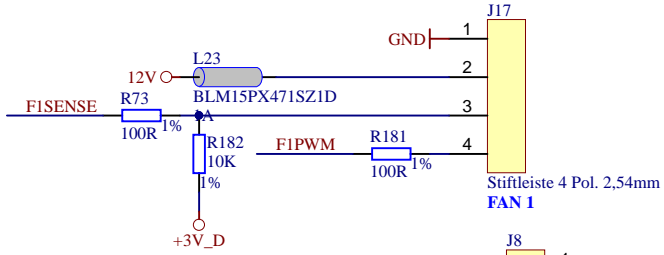


A

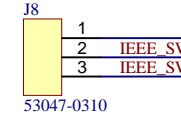
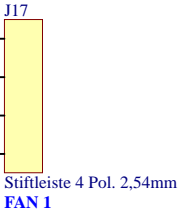
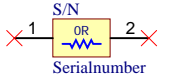
- U\_J1  
J1.SchDoc
- U\_J2  
J2.SchDoc
- U\_J3  
J3.SchDoc
- U\_J4  
J4.SchDoc
- U\_J5  
J5.SchDoc
- U\_J6  
J6.SchDoc



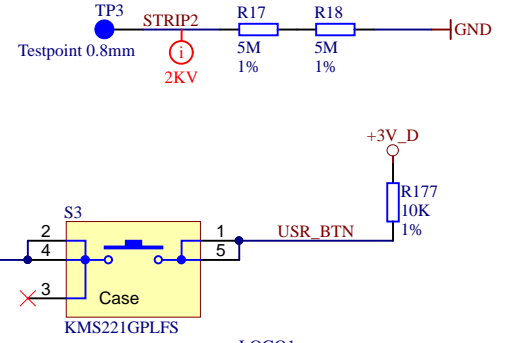
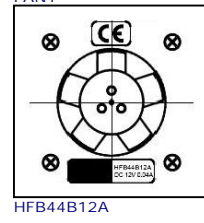
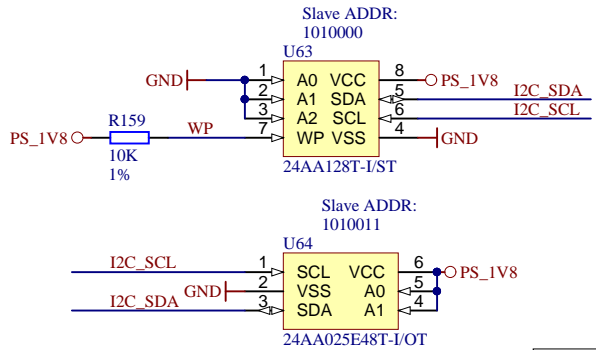
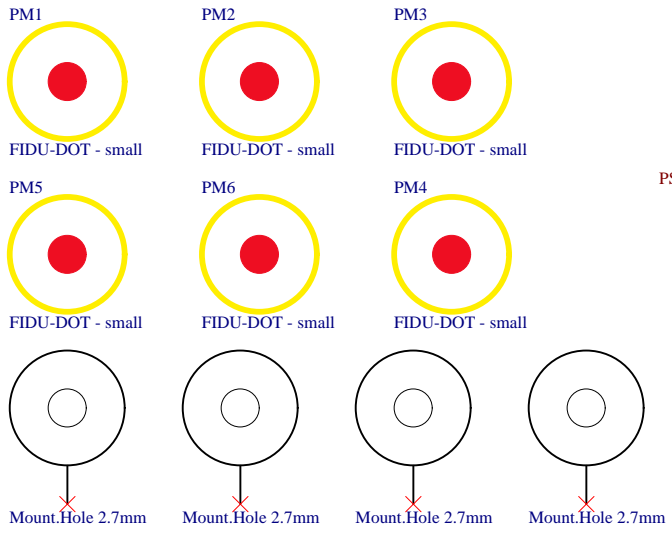
B



Serial  
Serialnummer 6,3 x 6,3mm



C



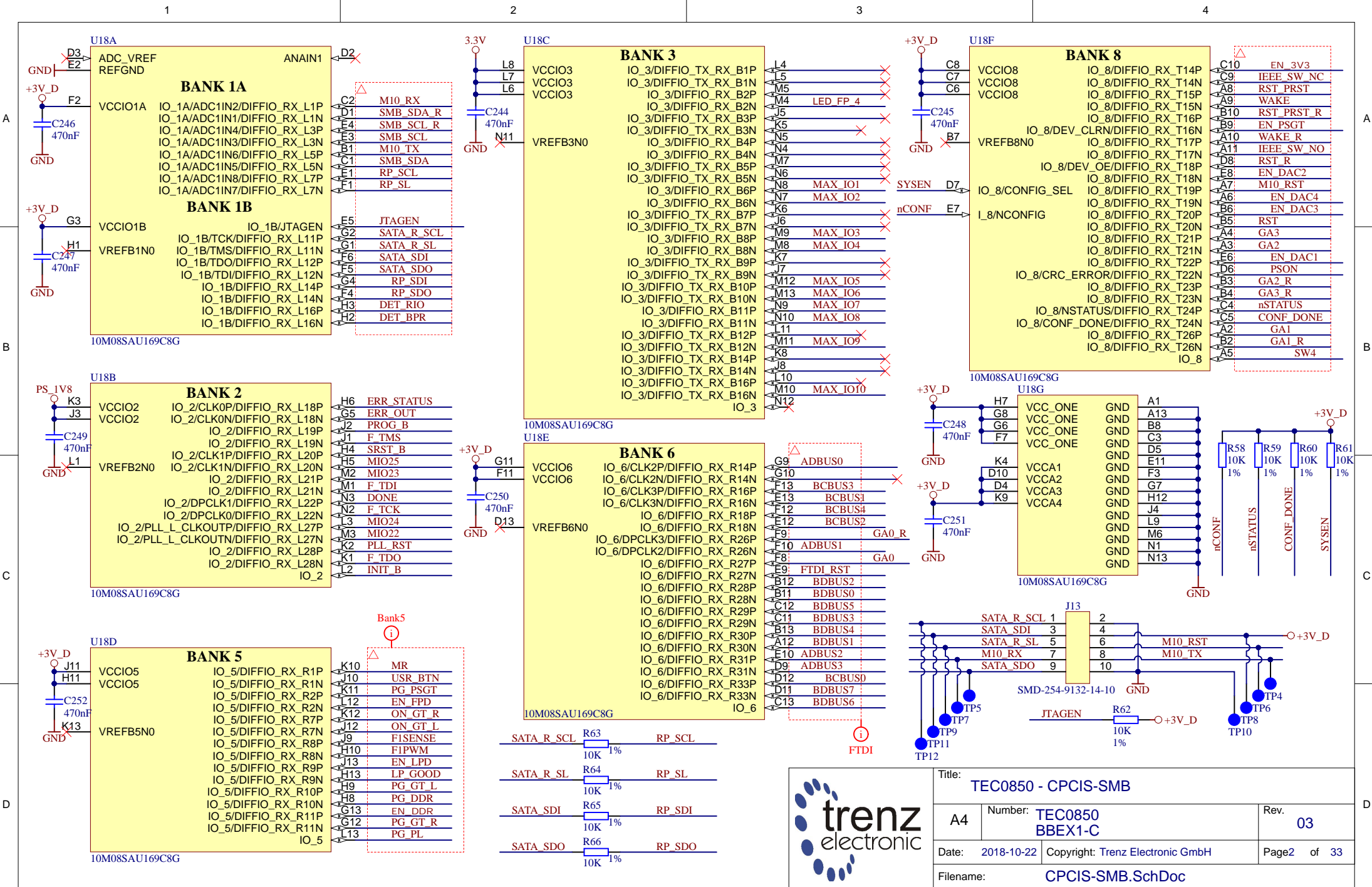
LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

D

Assembly variant	BBEX1-C
Created by	VY
Modified by	VY
Modified at	2019-09-09
SVN Revision	8527



Title: TEC0850 - CPCIS-MAIN		
A4	Number: TEC0850 BBEX1-C	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page1 of 33
Filename: CPCIS-MAIN.SchDoc		

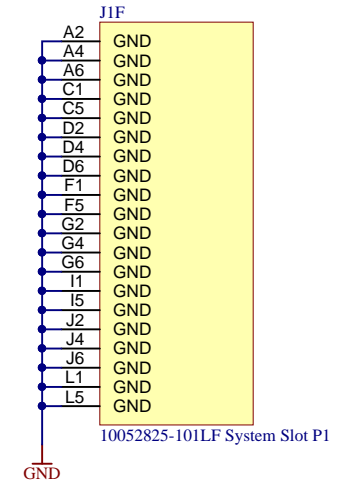
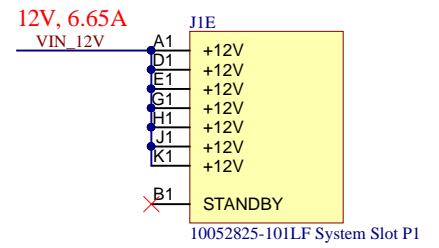
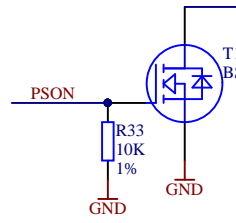
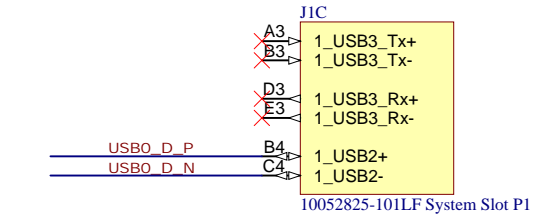
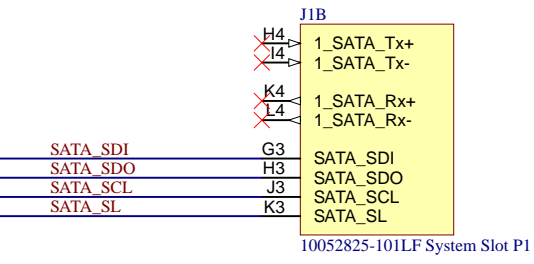
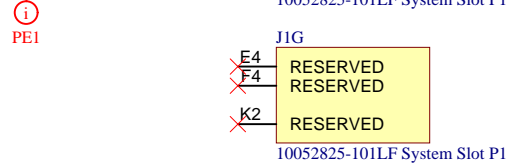
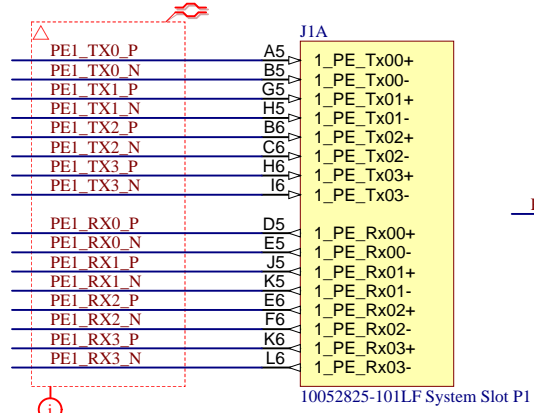
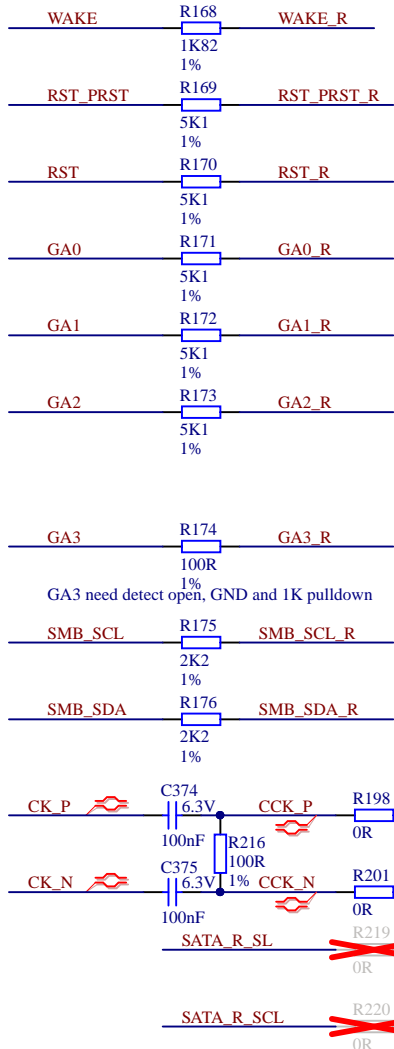


**trenz electronic**

Title: **TEC0850 - CPCIS-SMB**

A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>2</b> of <b>33</b>
Filename: <b>CPCIS-SMB.SchDoc</b>		

1.8, 2.2 and 5.1K are REQUIRED BY CPCI-S do not optimize to other values



Title: TEC0850 - J1		
A4	Number: TEC0850 BBEX1-C	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page3 of 33
Filename: J1.SchDoc		

1

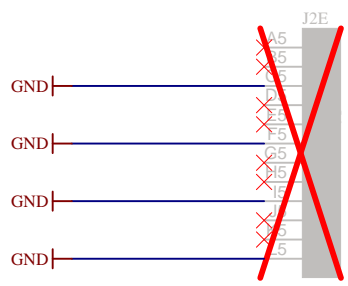
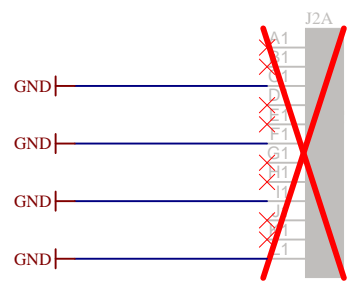
2

3

4

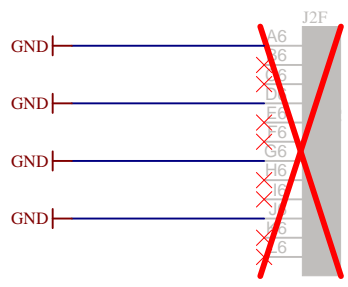
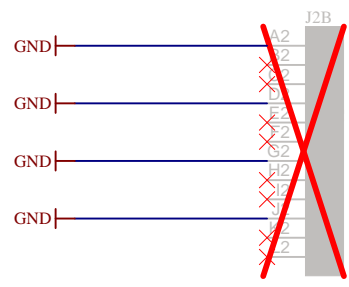
A

A



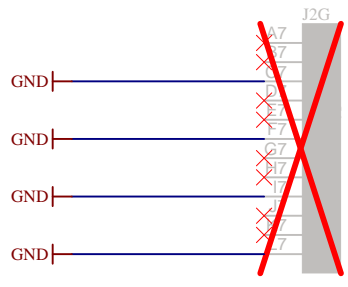
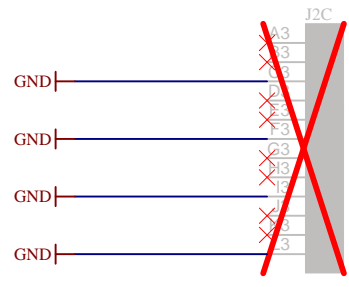
B

B



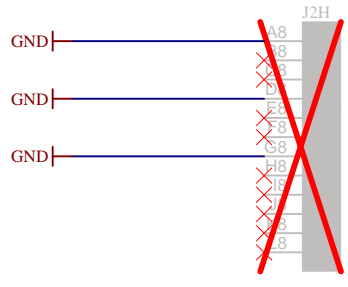
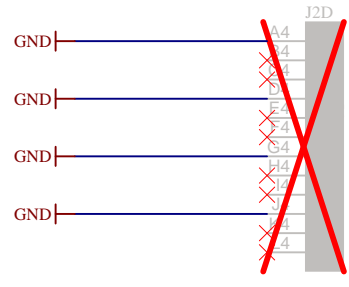
C

C



D

D



Title: <b>TEC0850 - J2</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>4</b> of <b>33</b>
Filename: <b>J2.SchDoc</b>		

1

2

3

4

1

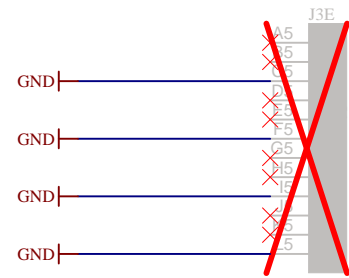
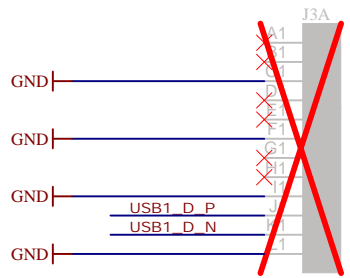
2

3

4

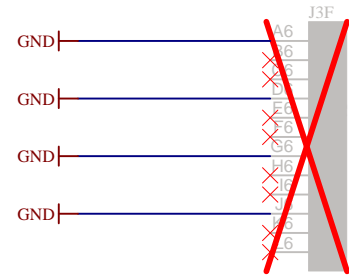
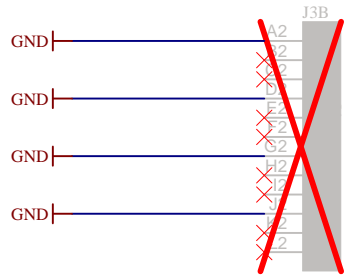
A

A



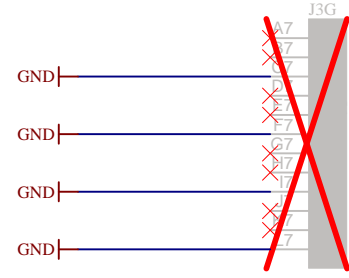
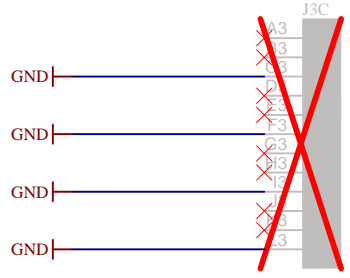
B

B



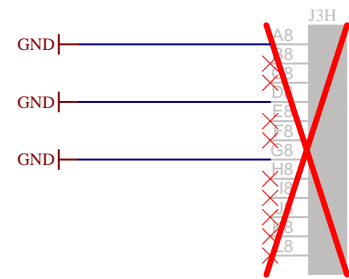
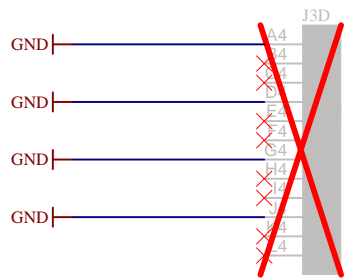
C

C



D

D



Title: <b>TEC0850 - J3</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>5</b> of <b>33</b>
Filename: <b>J3.SchDoc</b>		

1

2

3

4

1

2

3

4

A

A

B

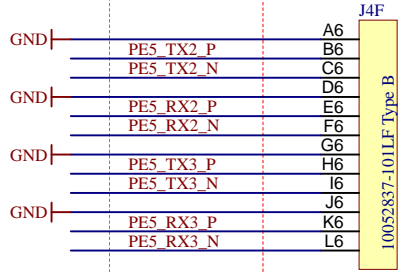
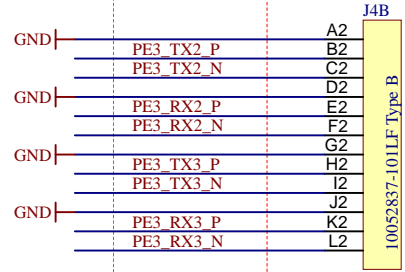
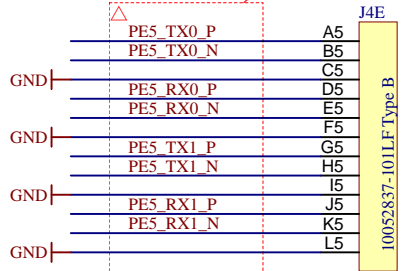
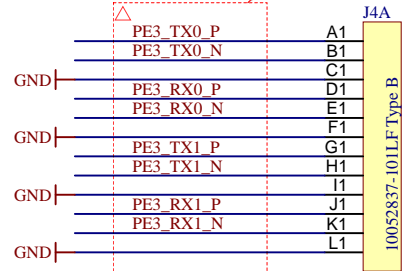
B

C

C

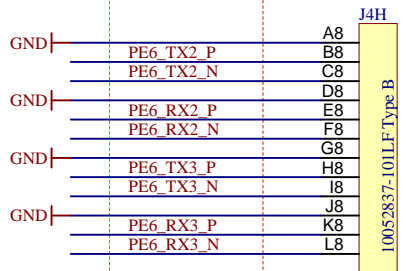
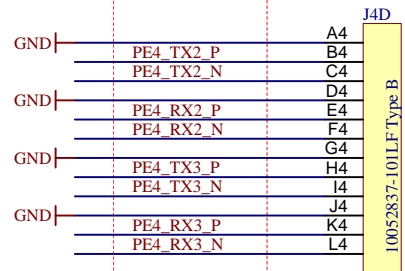
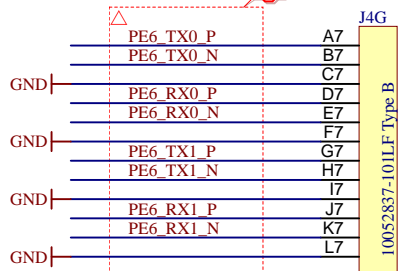
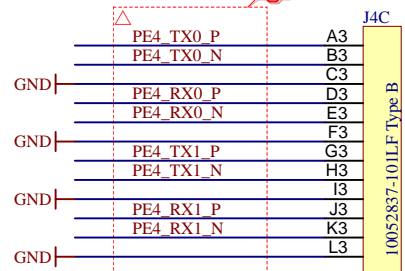
D

D



PE3

PE5



PE4

PE6



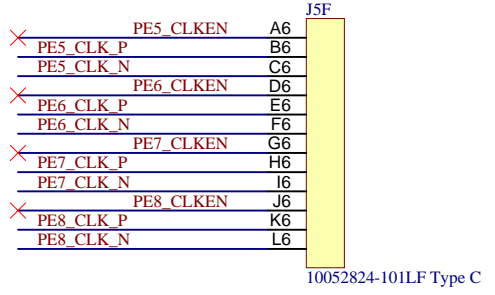
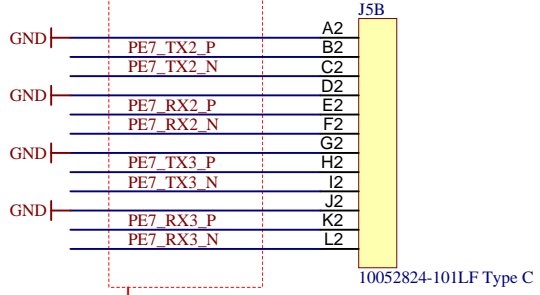
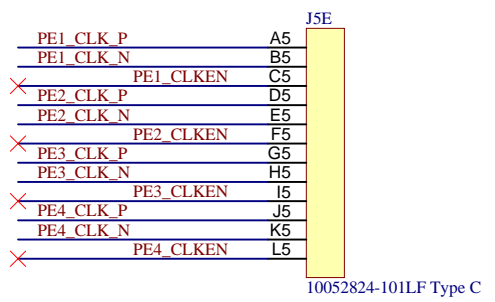
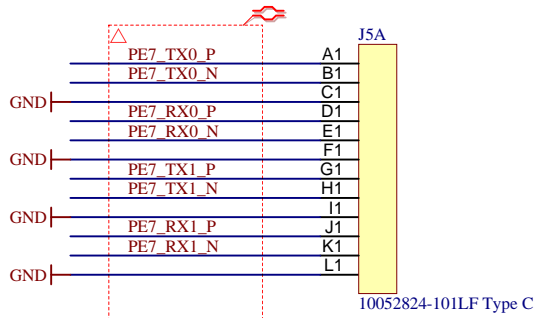
Title: <b>TEC0850 - J4</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>6</b> of <b>33</b>
Filename: <b>J4.SchDoc</b>		

1

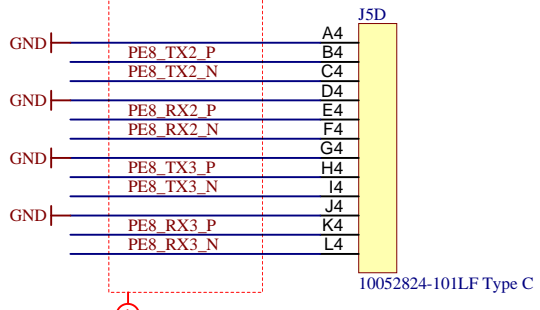
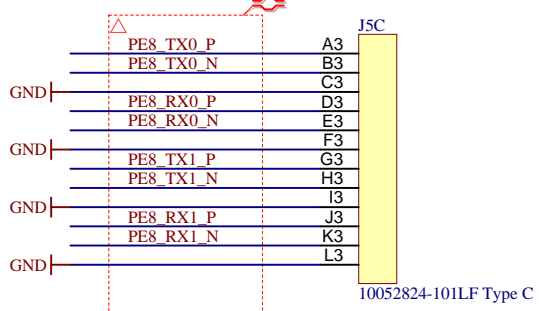
2

3

4



PE7



PE8



Title: <b>TEC0850 - J5</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>7</b> of <b>33</b>
Filename: <b>J5.SchDoc</b>		

1

2

3

4

A

A

B

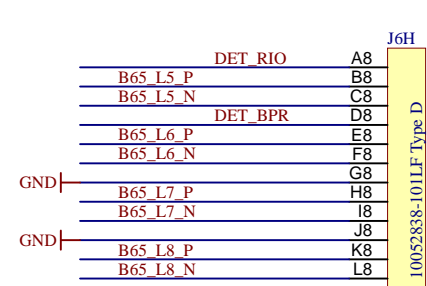
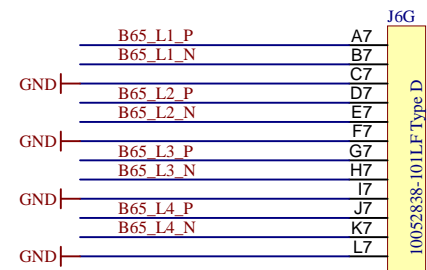
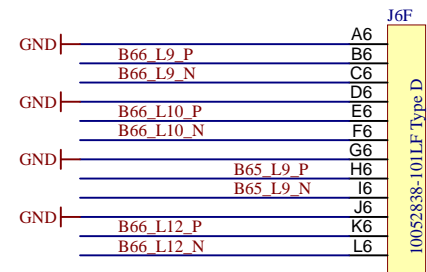
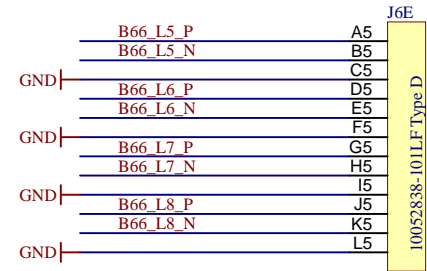
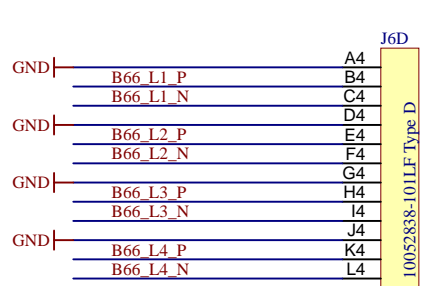
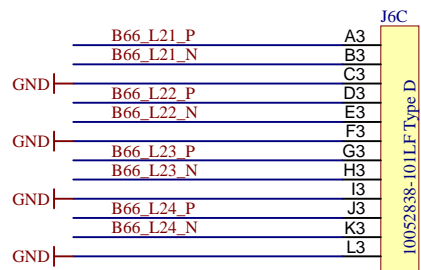
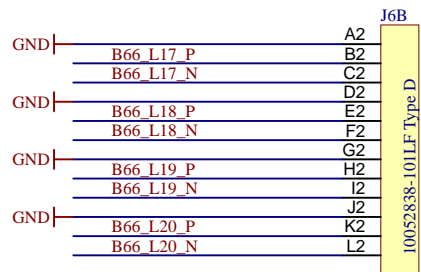
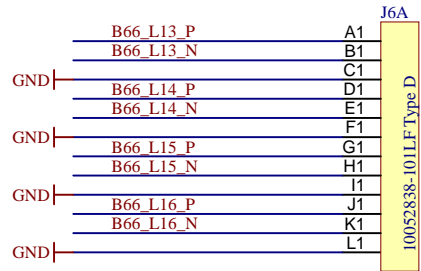
B

C

C

D

D



Title: <b>TEC0850 - J6</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>8</b> of <b>33</b>
Filename: <b>J6.SchDoc</b>		

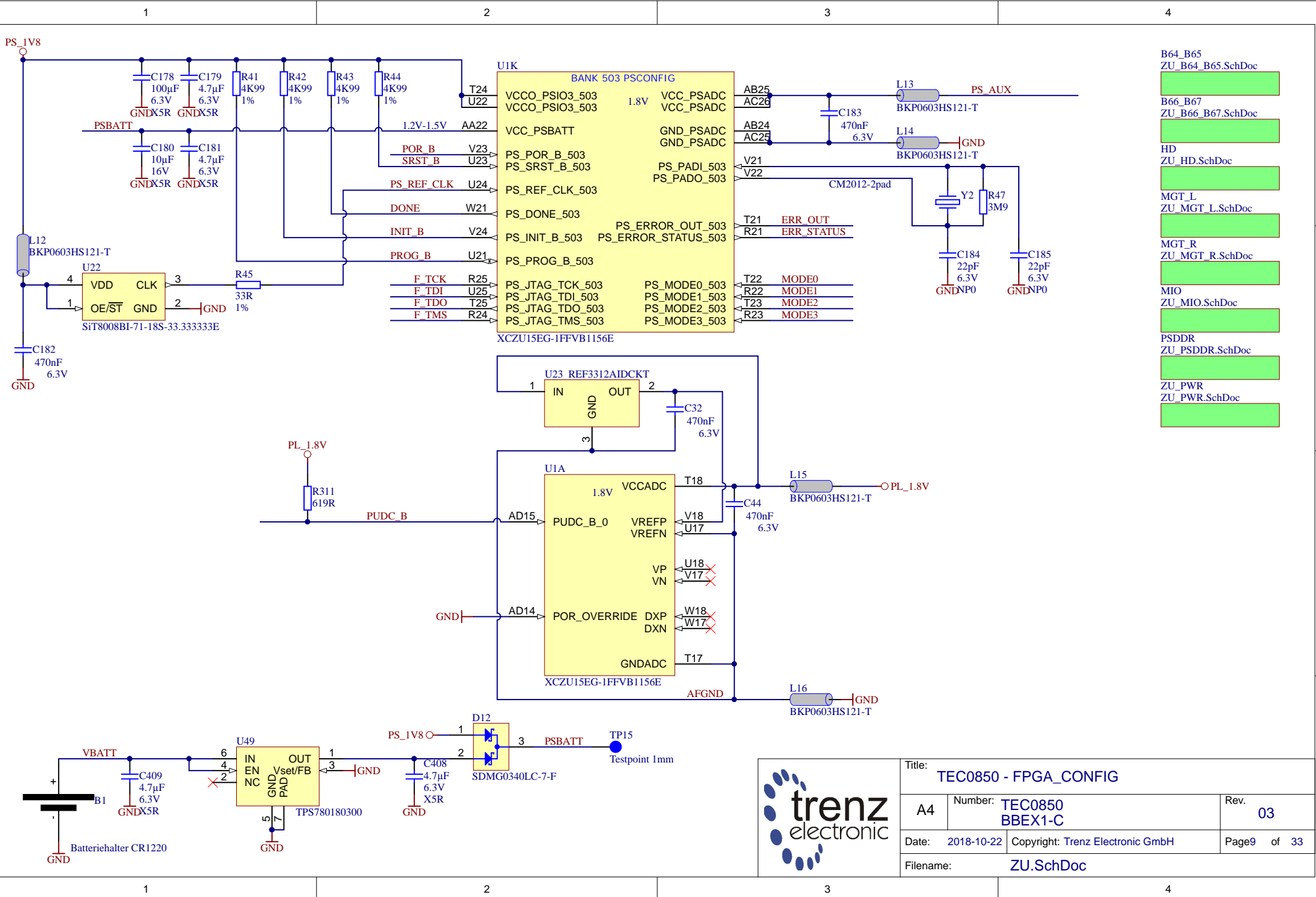
1

2

3

4

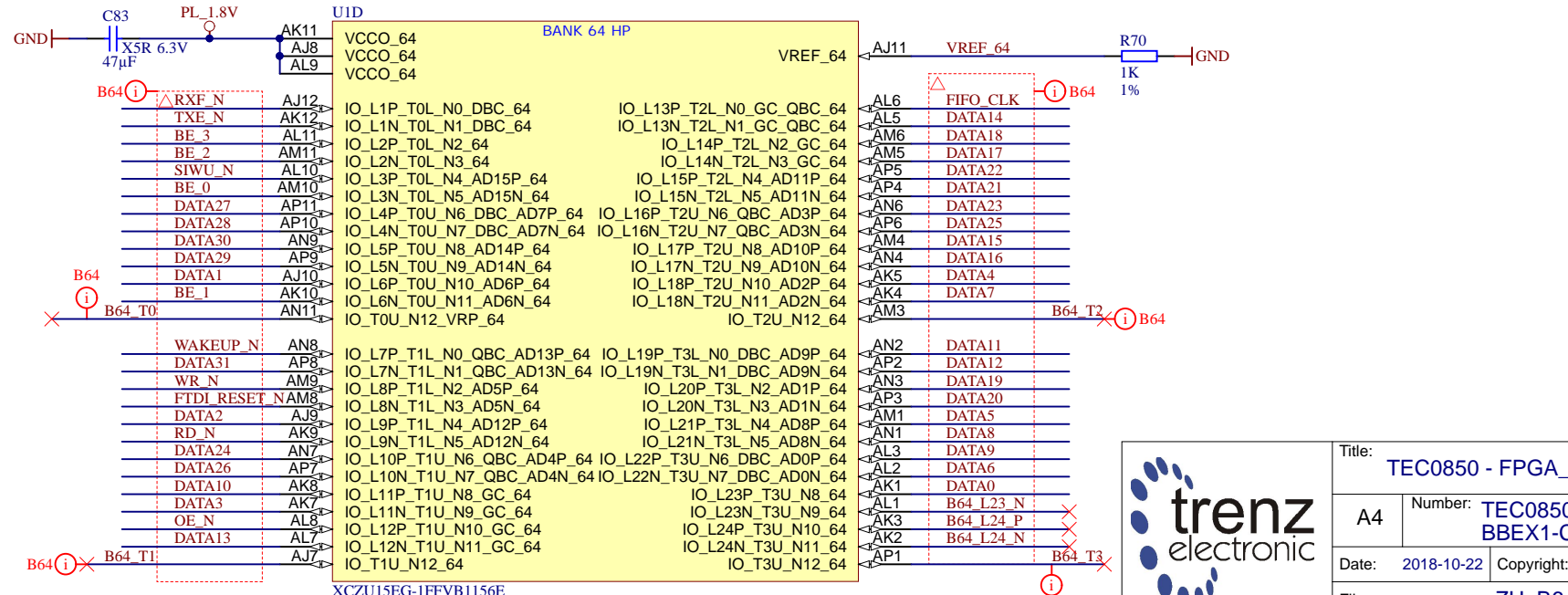
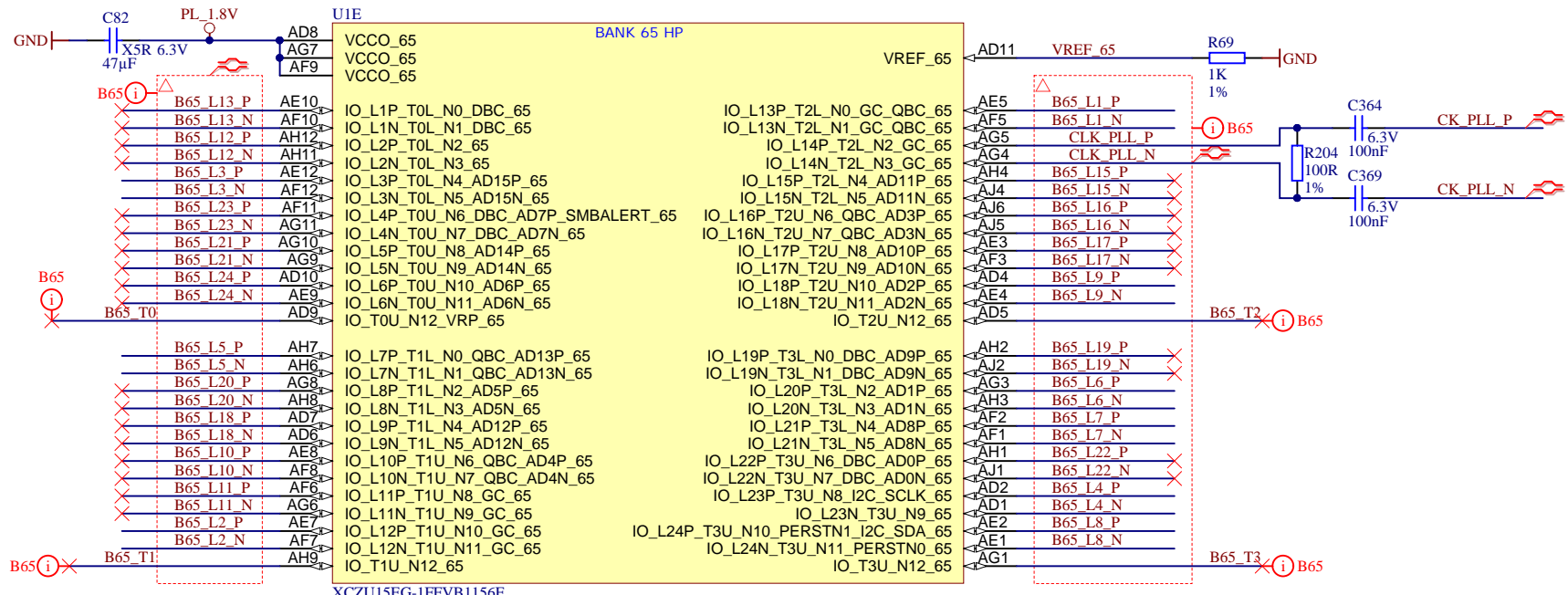




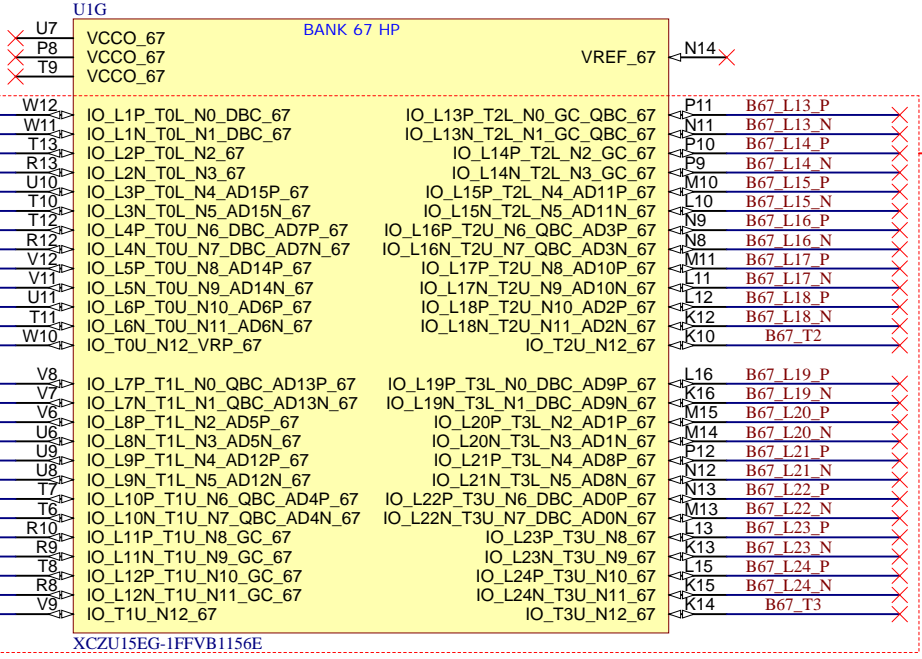
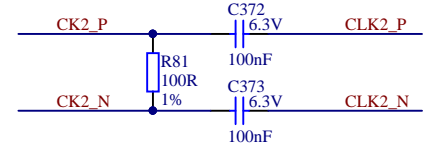
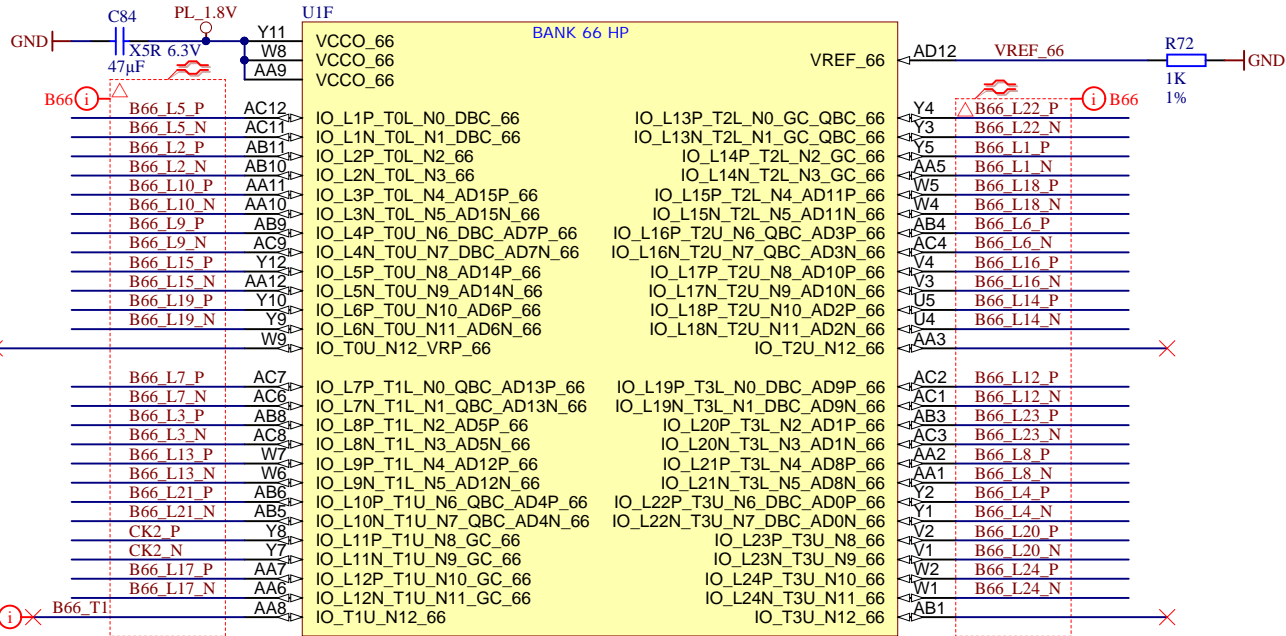
- B64\_B65  
ZU\_B64\_B65.SchDoc
- B66\_B67  
ZU\_B66\_B67.SchDoc
- HD  
ZU\_HD.SchDoc
- MGT\_L  
ZU\_MGT\_L.SchDoc
- MGT\_R  
ZU\_MGT\_R.SchDoc
- MIO  
ZU\_MIO.SchDoc
- PSDDR  
ZU\_PSDDR.SchDoc
- ZU\_PWR  
ZU\_PWR.SchDoc



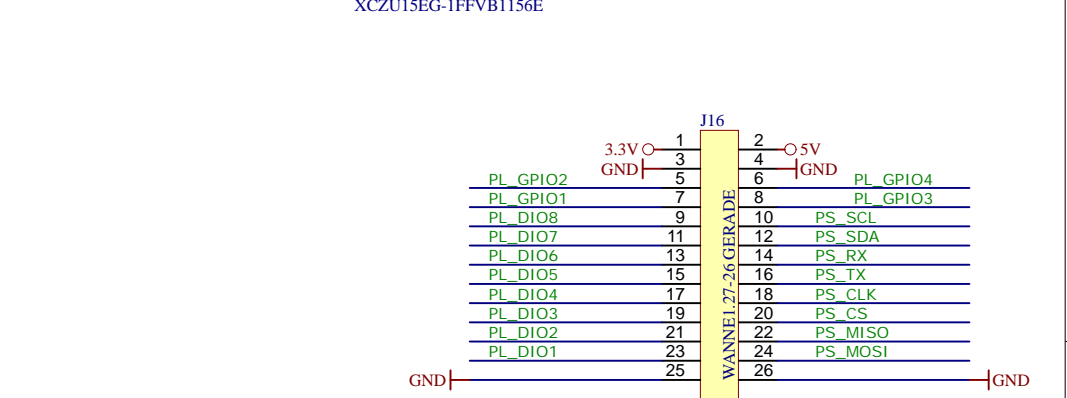
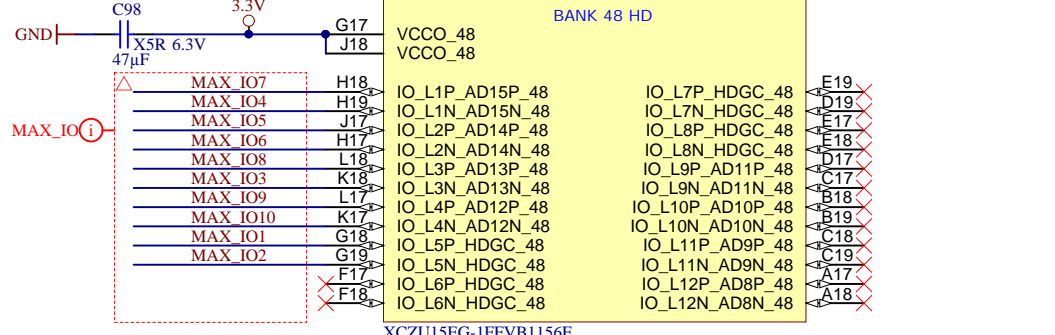
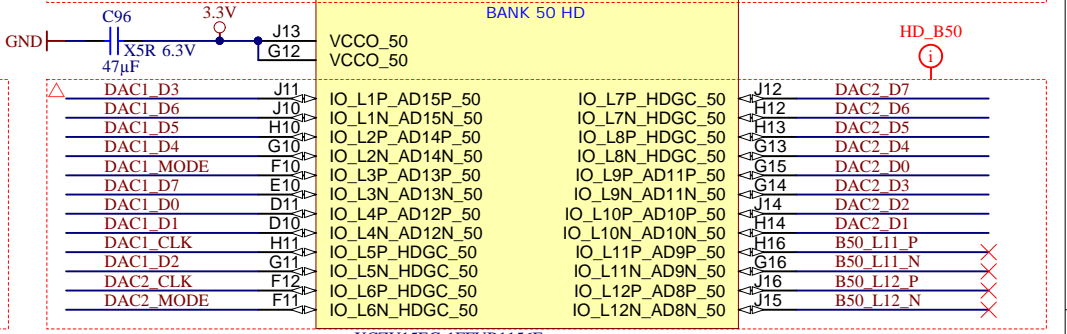
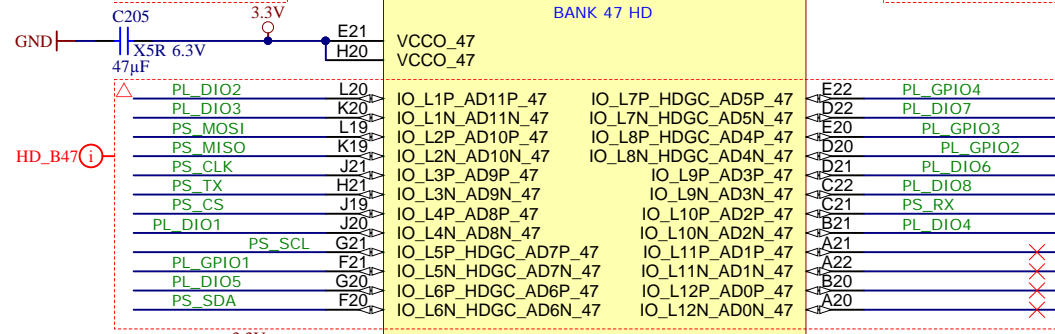
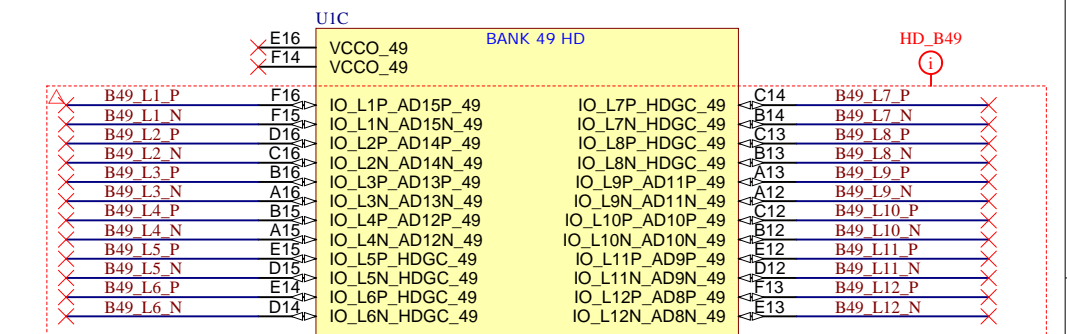
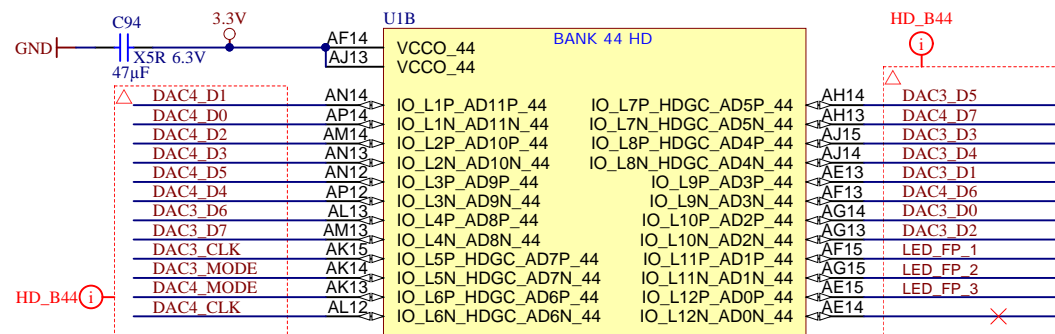
Title: TEC0850 - FPGA_CONFIG		
A4	Number: TEC0850 BBEX1-C	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page9 of 33
Filename: ZU.SchDoc		



Title: <b>TEC0850 - FPGA_B64_B65</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>10</b> of <b>33</b>
Filename: <b>ZU_B64_B65.SchDoc</b>		



Title: <b>TEC0850 - FPGA_B66_B67</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>11</b> of <b>33</b>
Filename: <b>ZU_B66_B67.SchDoc</b>		



XCZU15EG-1FFVB1156E

Title: **TEC0850 - FPGA\_HD**

A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>12</b> of <b>33</b>
Filename: <b>ZU_HD.SchDoc</b>		



A

B

C

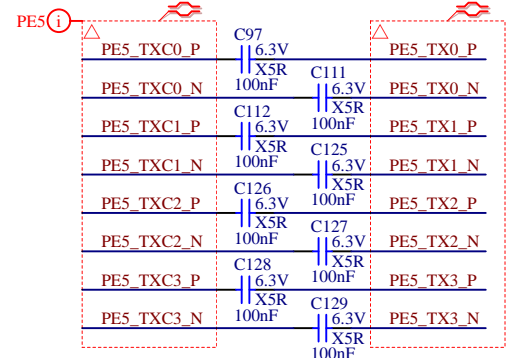
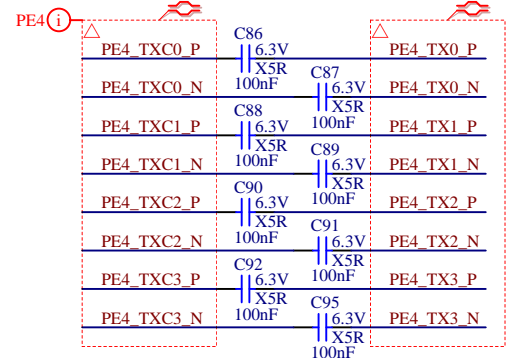
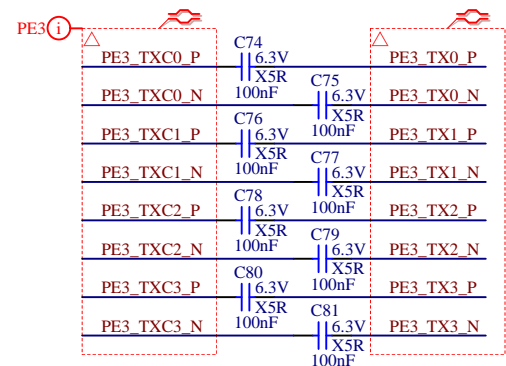
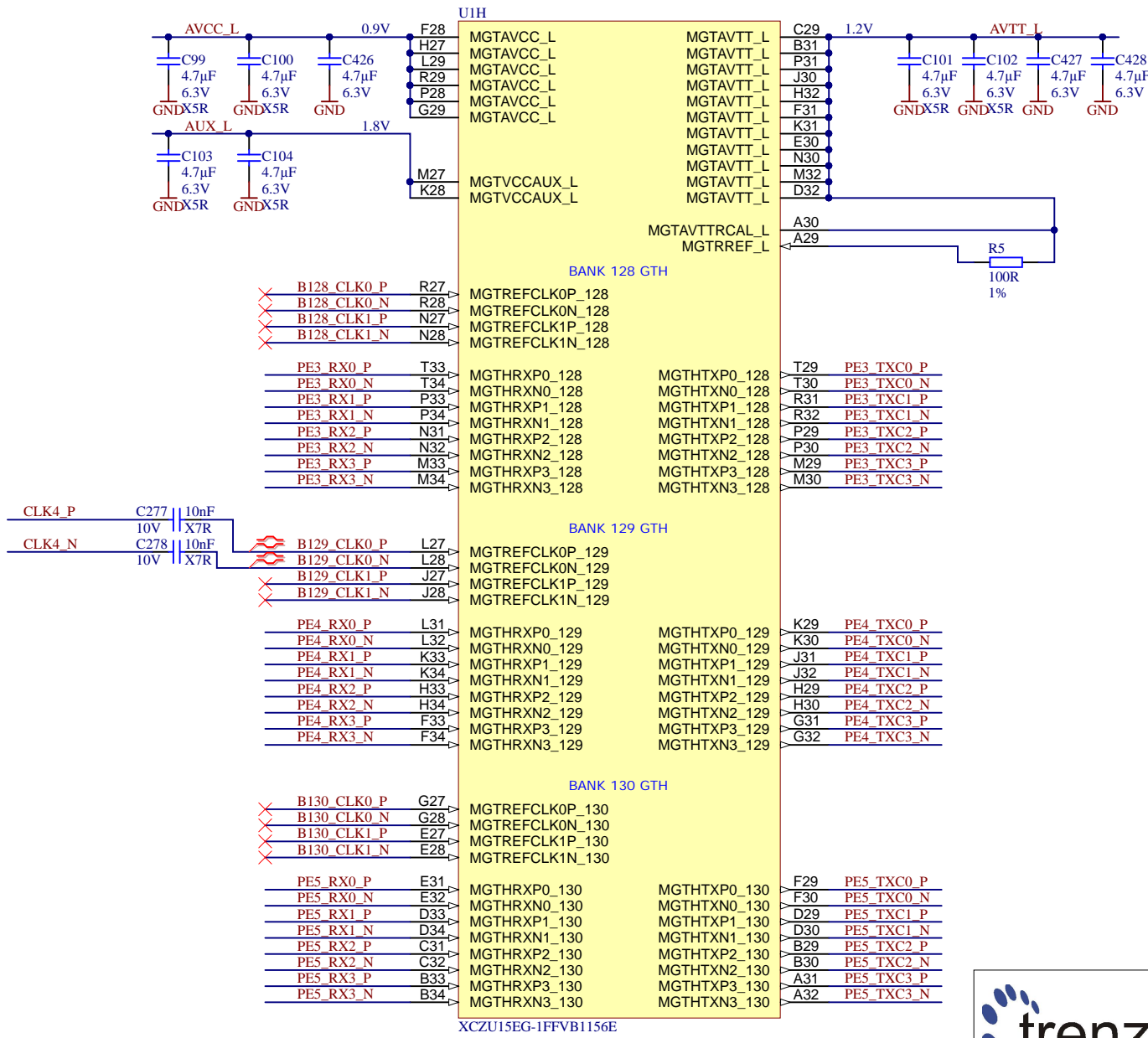
D

A

B

C

D



Title: <b>TEC0850 - FPGA_MGT_L</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>13</b> of <b>33</b>
Filename: <b>ZU_MGT_L.SchDoc</b>		

A

B

C

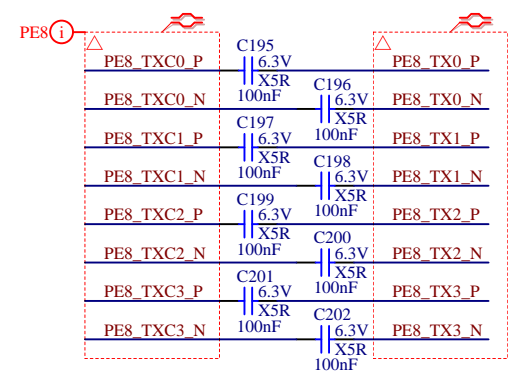
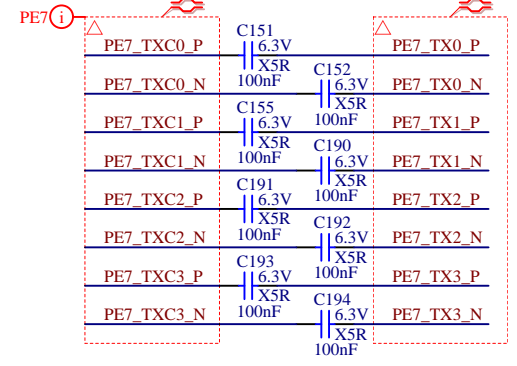
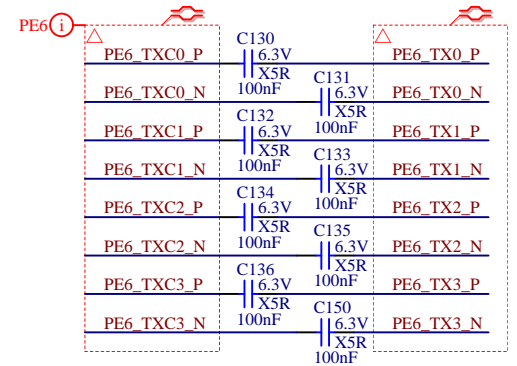
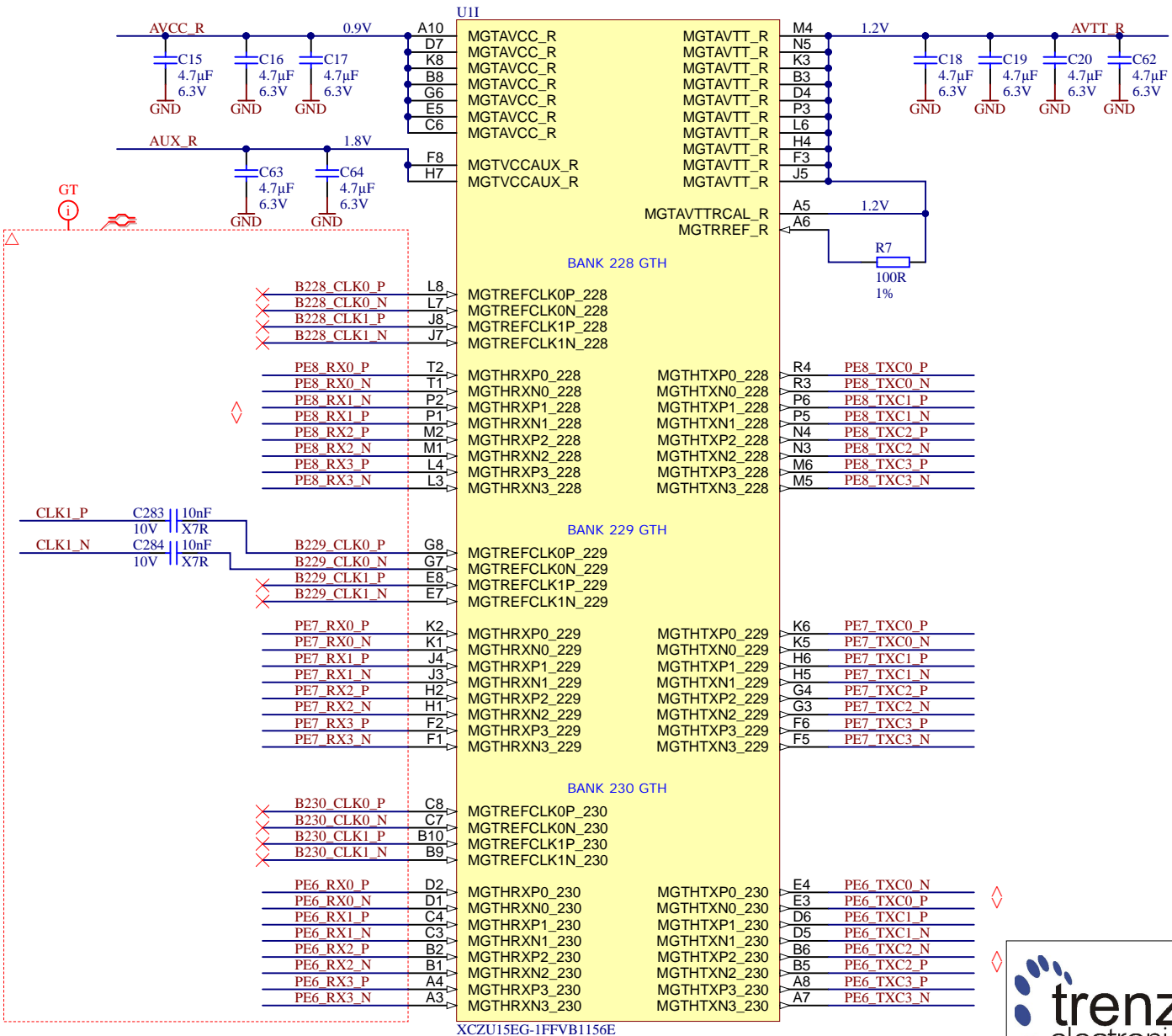
D

A

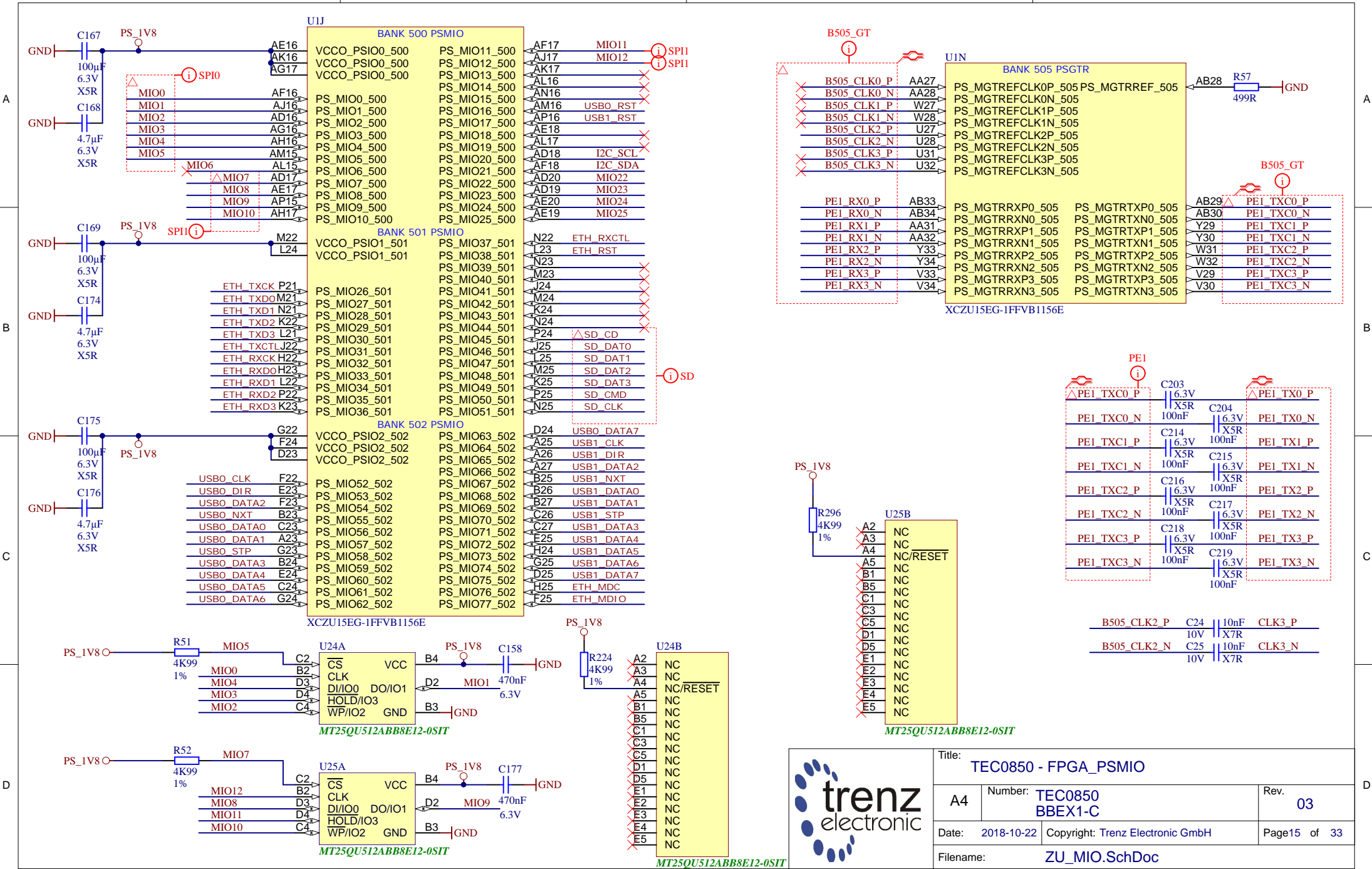
B

C

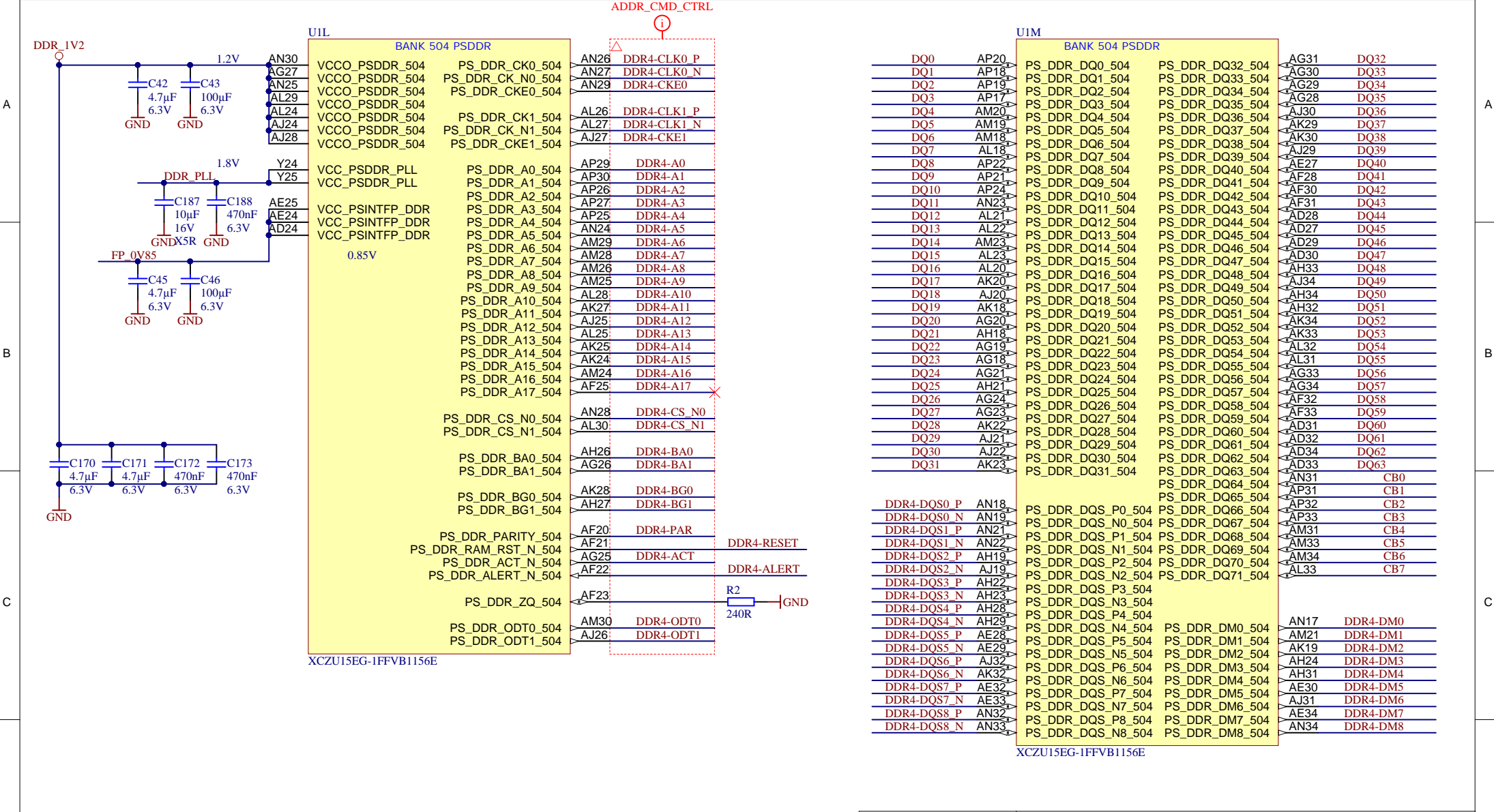
D



Title: <b>TEC0850 - FPGA_MGT_R</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>14</b> of <b>33</b>
Filename: <b>ZU_MGT_R.SchDoc</b>		



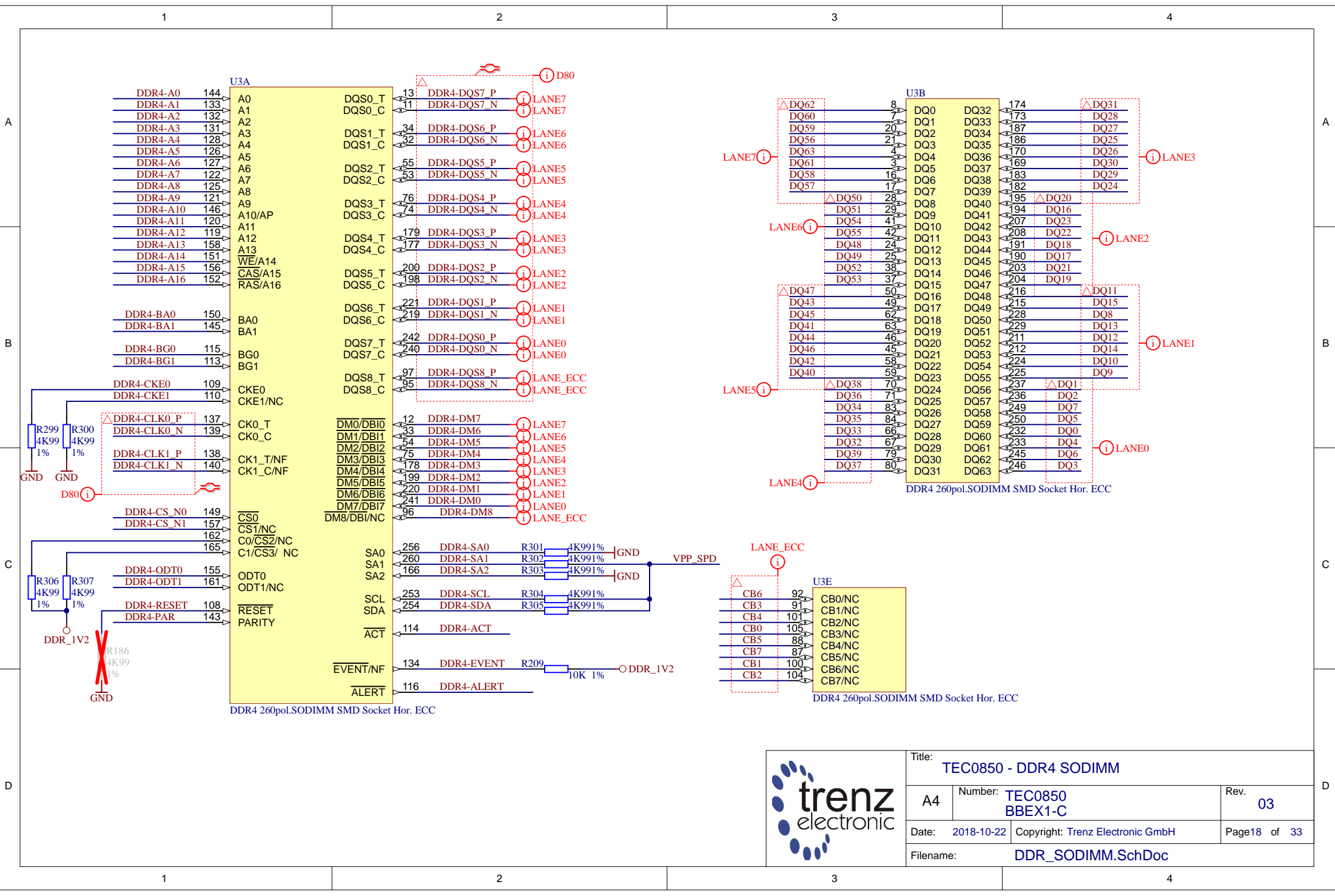
Title: <b>TEC0850 - FPGA_PSMIO</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>15</b> of <b>33</b>
Filename: <b>ZU_MIO.SchDoc</b>		




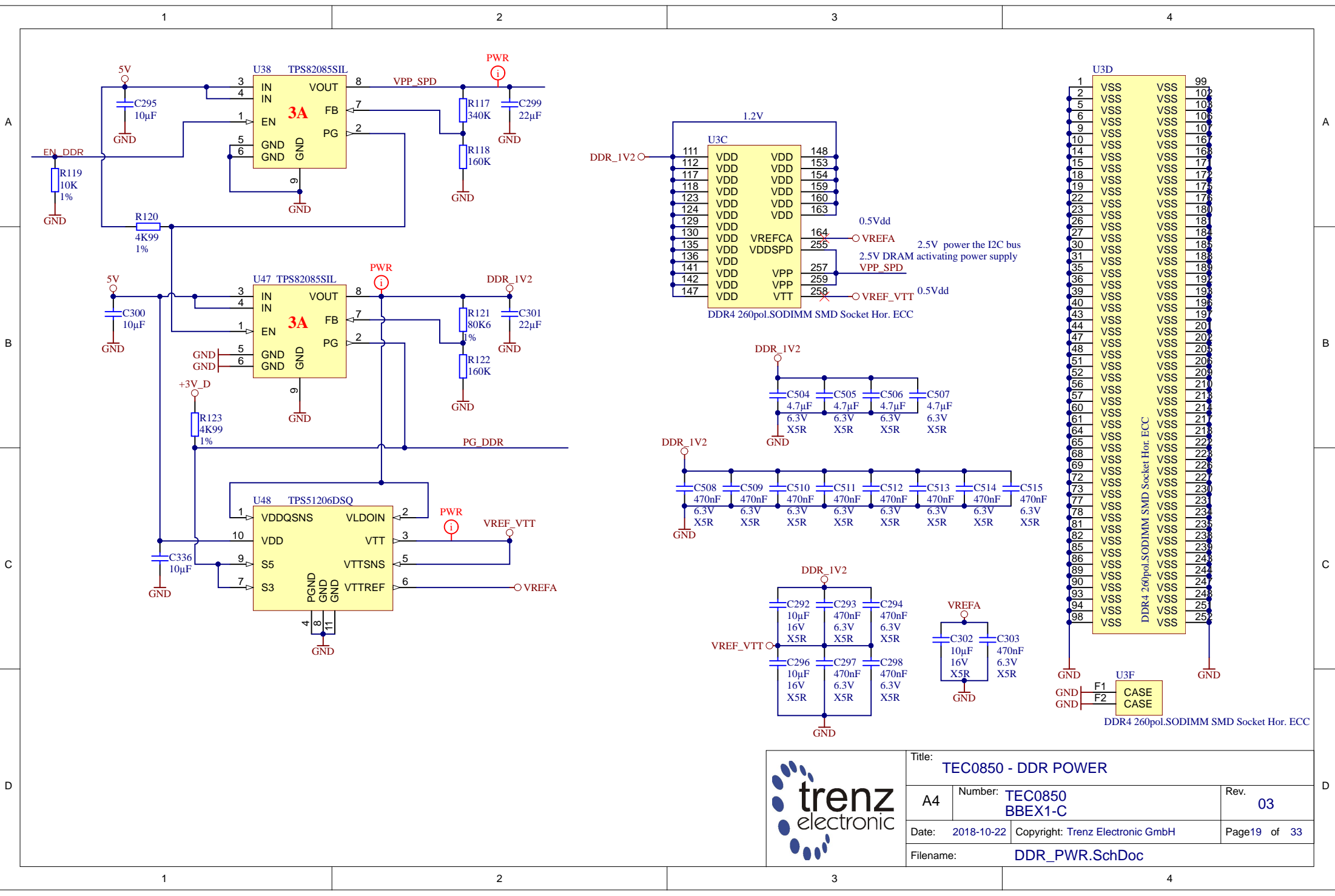
		Title: <b>TEC0850 - FPGA_PSDDR</b>	
		A4	Number: <b>TEC0850 BBEX1-C</b>
Date: <b>2018-10-22</b>		Copyright: <b>Trenz Electronic GmbH</b>	
Filename: <b>ZU_PSDDR.SchDoc</b>		Page <b>16</b> of <b>33</b>	



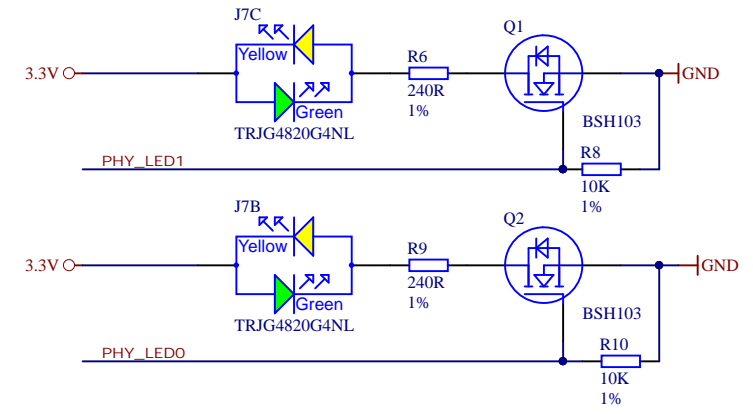
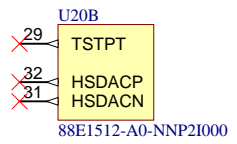
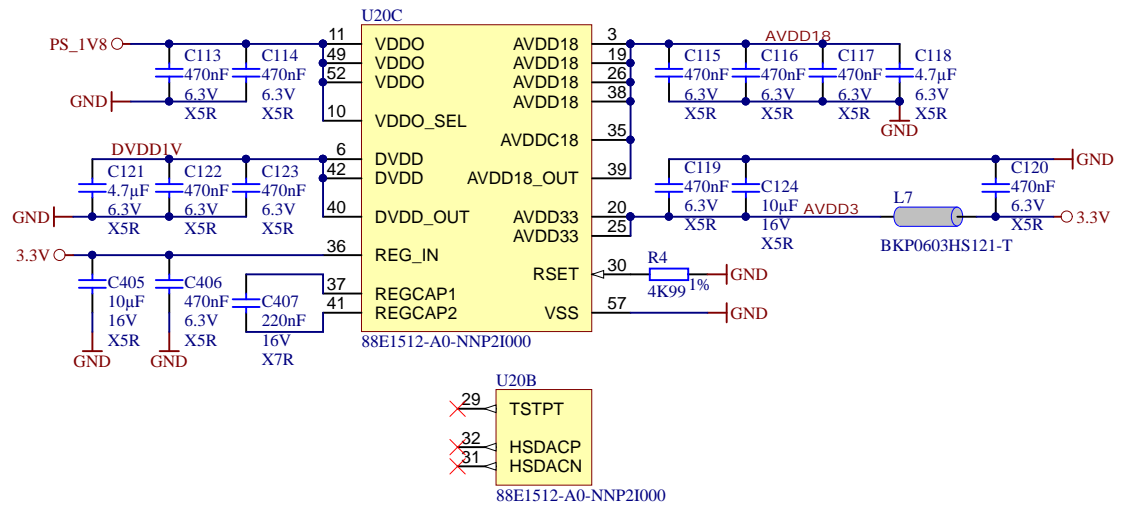
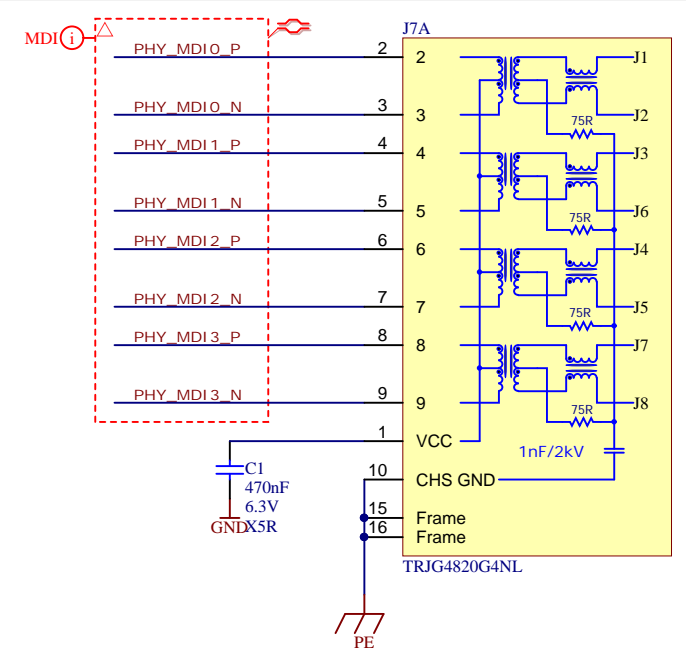
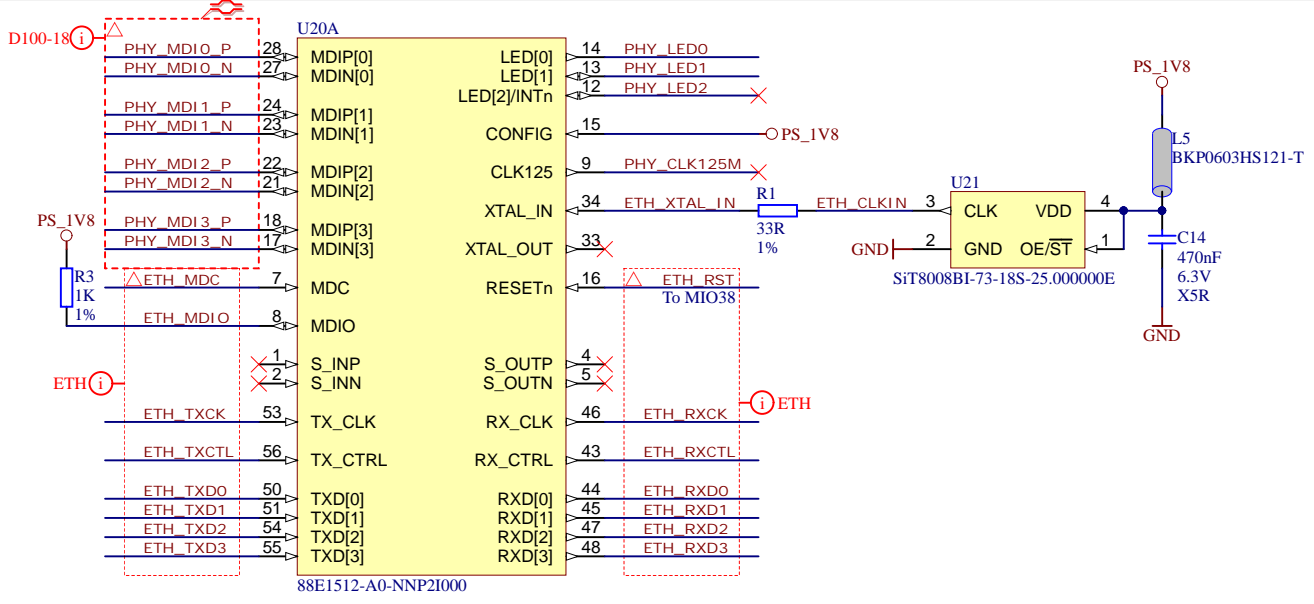




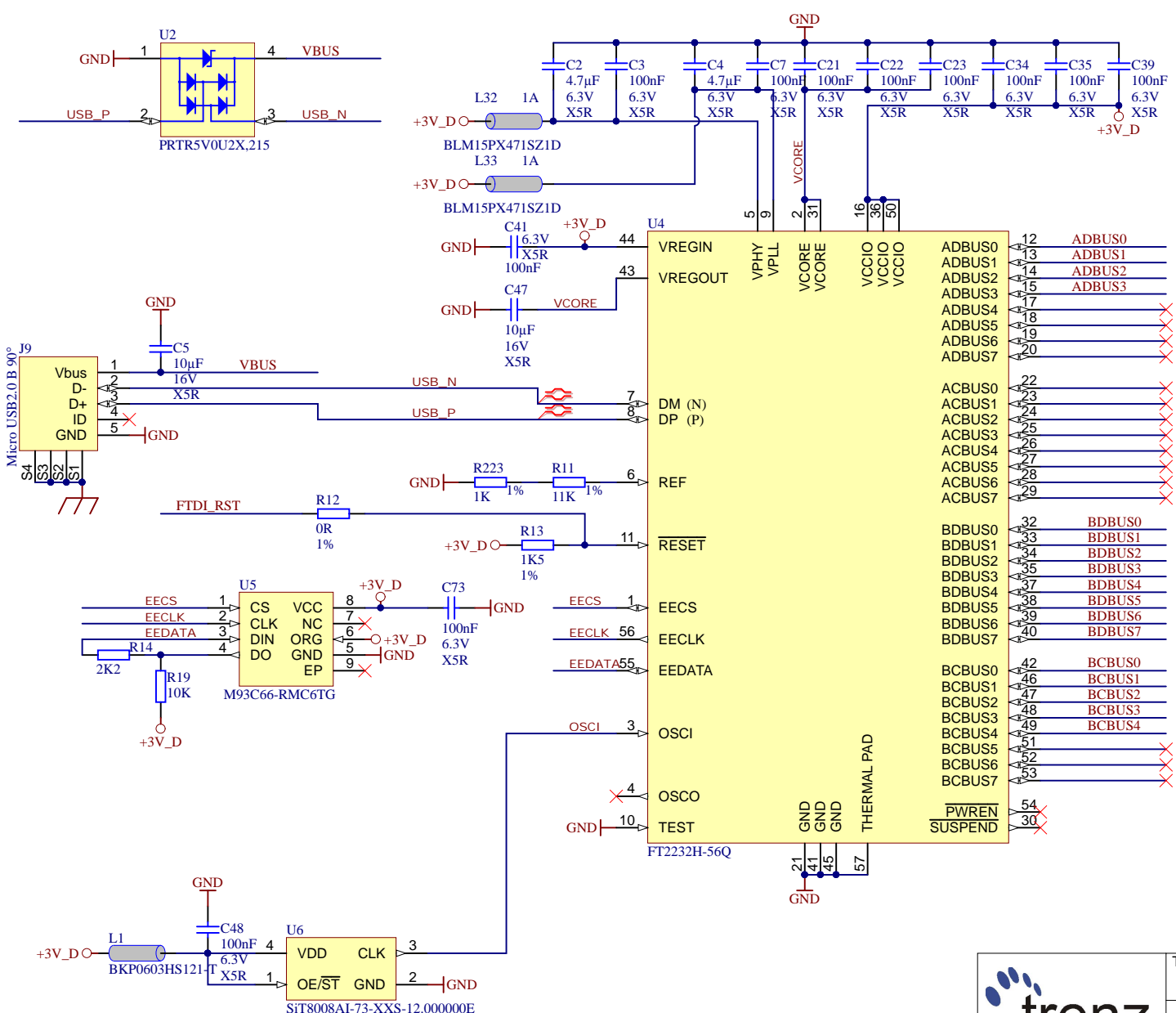
			Title: <b>TEC0850 - DDR4 SODIMM</b>	
			A4	Number: <b>TEC0850 BBEX1-C</b>
Date: <b>2018-10-22</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>18</b> of <b>33</b>
Filename: <b>DDR_SODIMM.SchDoc</b>				



Title: <b>TEC0850 - DDR POWER</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>19</b> of <b>33</b>
Filename: <b>DDR_PWR.SchDoc</b>		

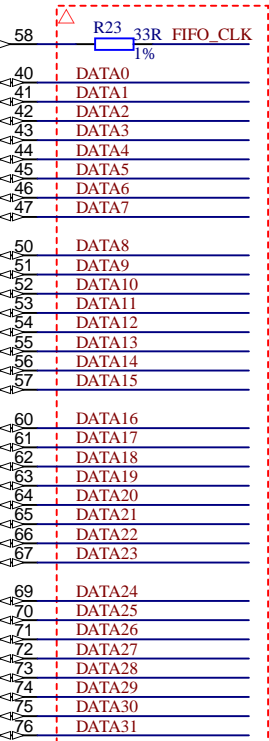
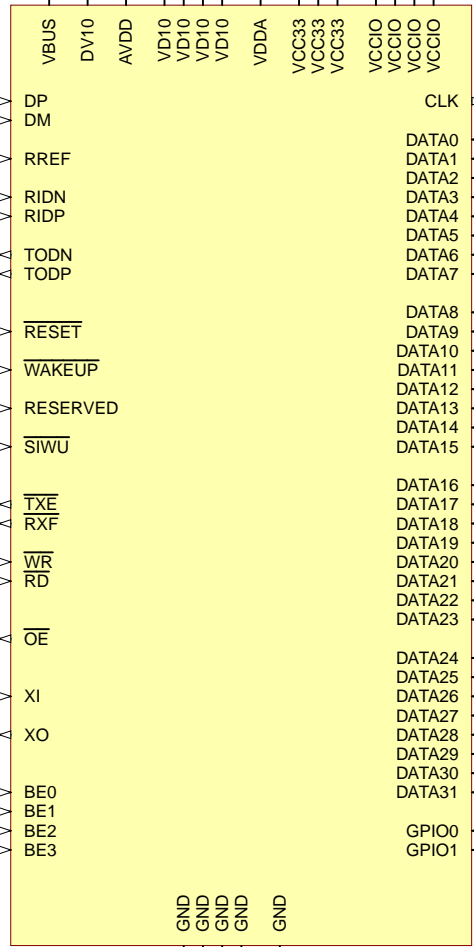
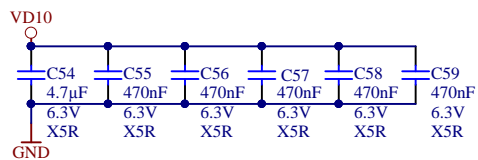
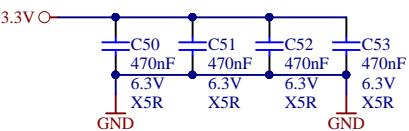
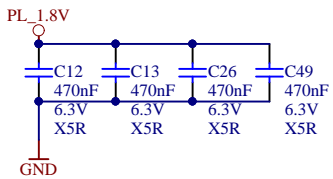
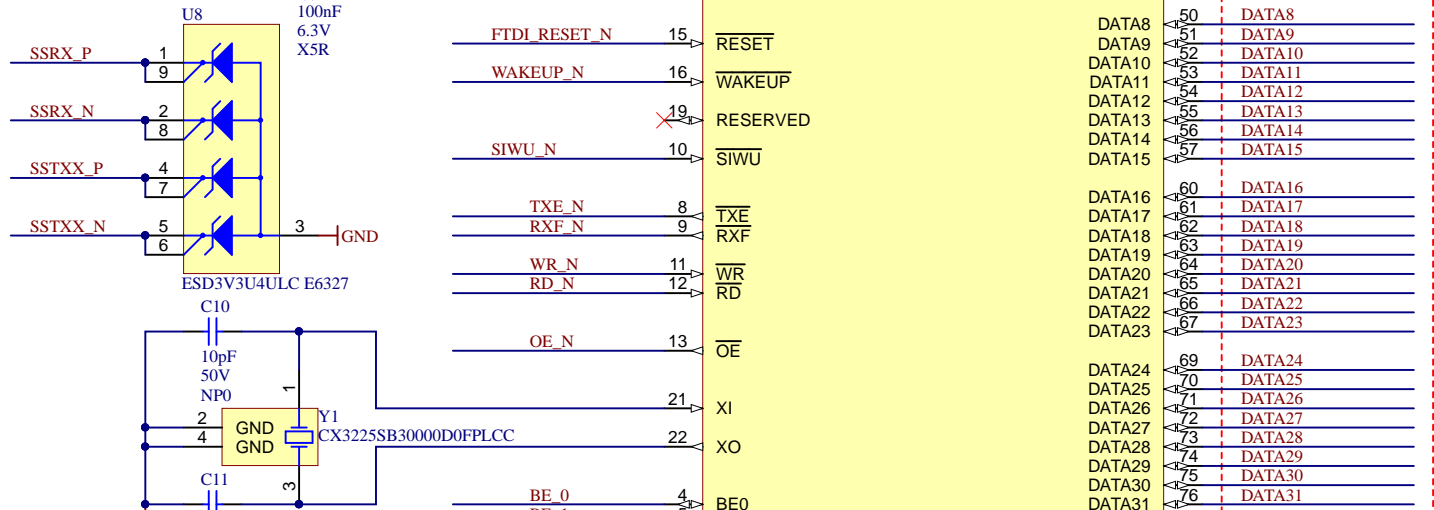
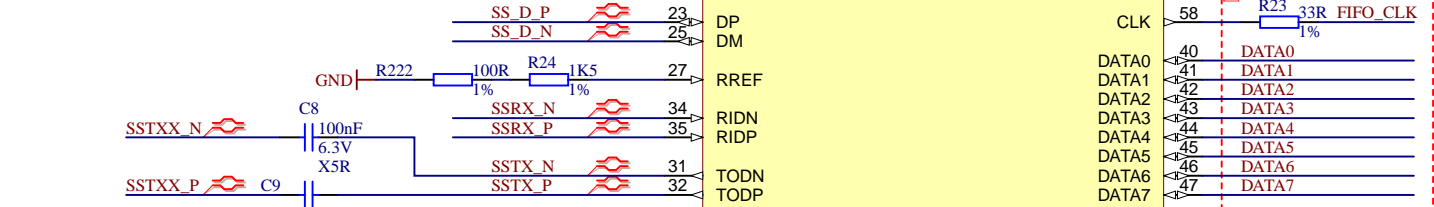
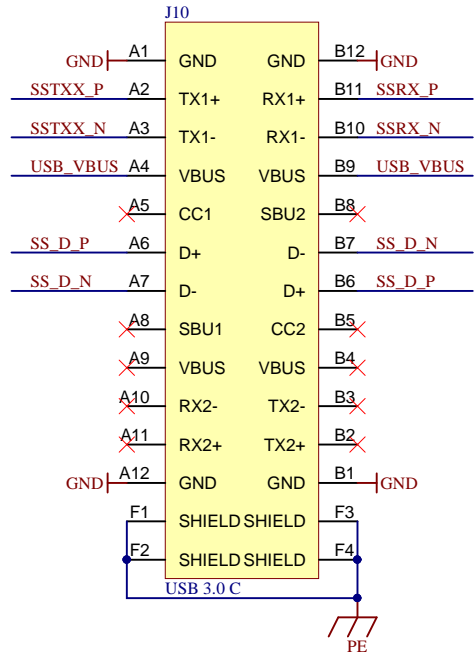
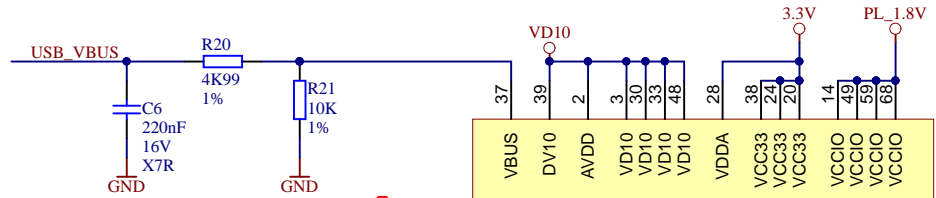
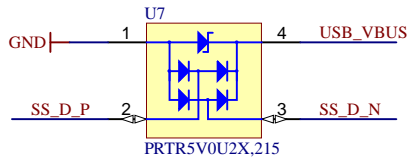


Title: TEC0850 - ETH		
A4	Number: TEC0850 BBEX1-C	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page20 of 33
Filename: Ethernet.SchDoc		



Title: <b>TEC0850 - FTDI</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>21</b> of <b>33</b>
Filename: <b>FTDI.SchDoc</b>		

A



C

D



Title: TEC0850 - USB3.0		
A4	Number: TEC0850 BBEX1-C	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page 22 of 33
Filename: USB30.SchDoc		

1

2

3

4

A

A

B

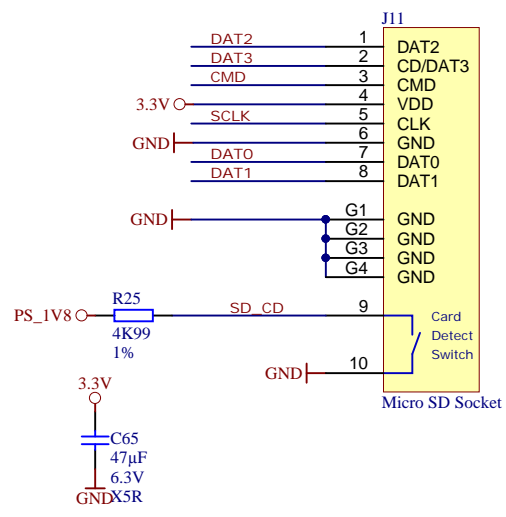
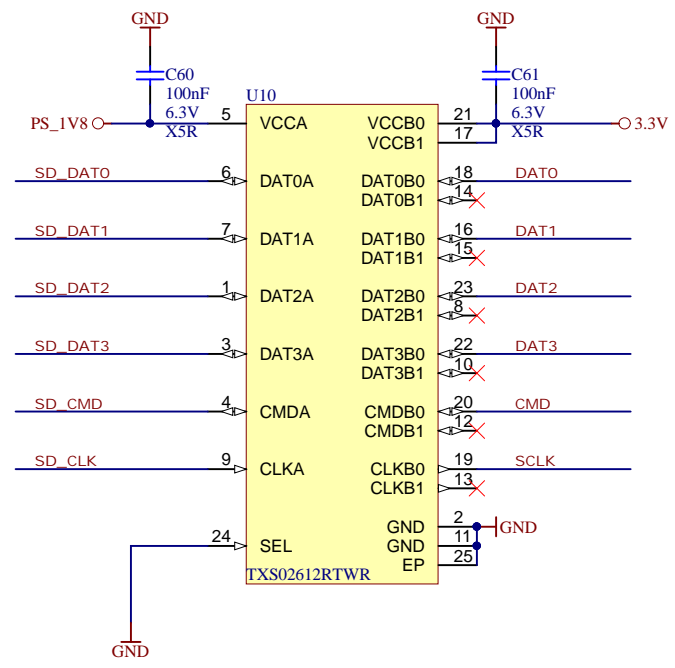
B

C

C

D

D



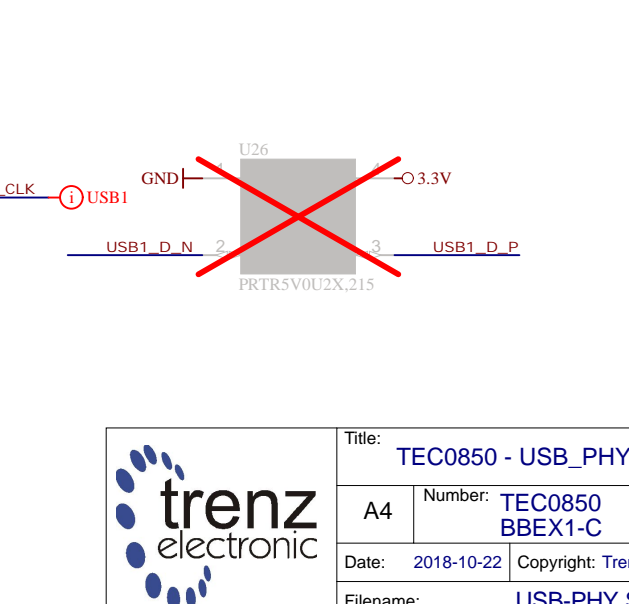
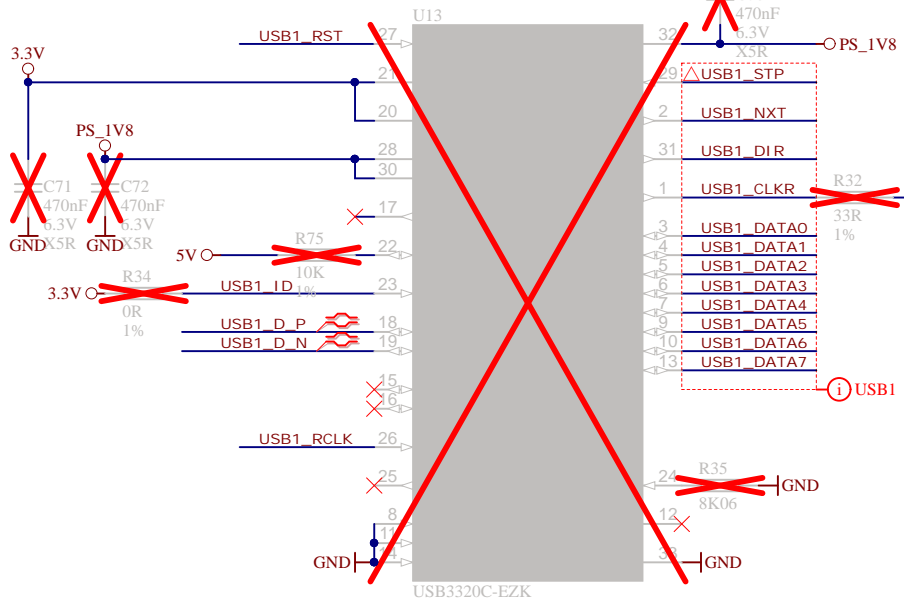
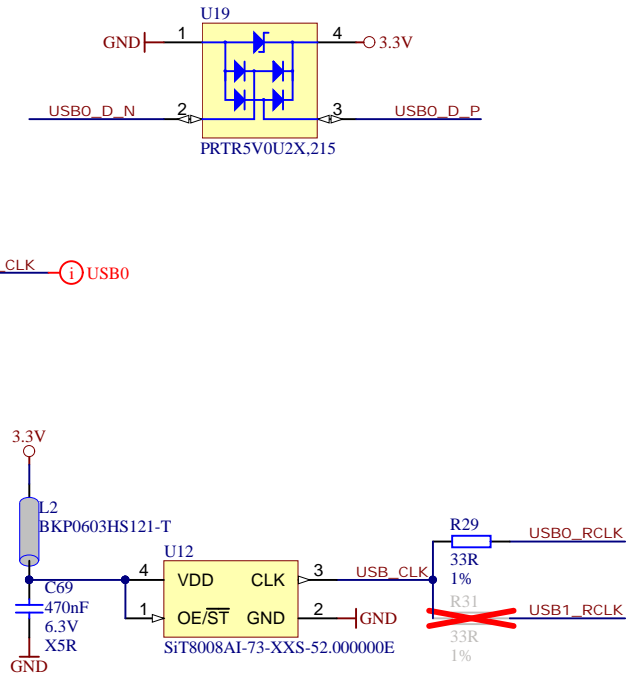
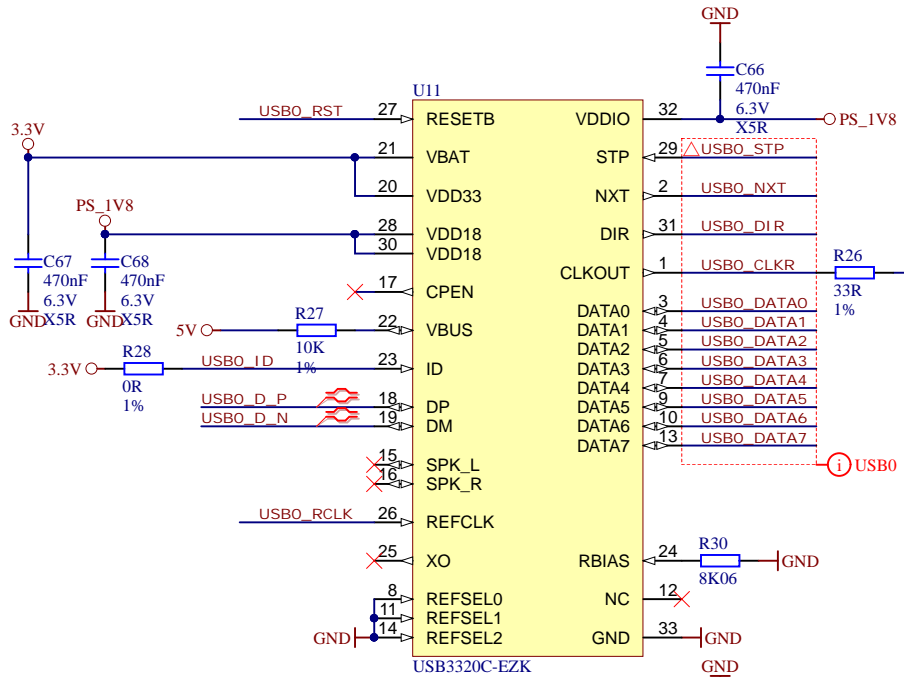
	Title: <b>TEC0850 - SDCard</b>	
	A4	Number: <b>TEC0850 BBEX1-C</b>
	Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>
	Rev. <b>03</b>	Page <b>23</b> of <b>33</b>
Filename: <b>SDCard.SchDoc</b>		

1

2

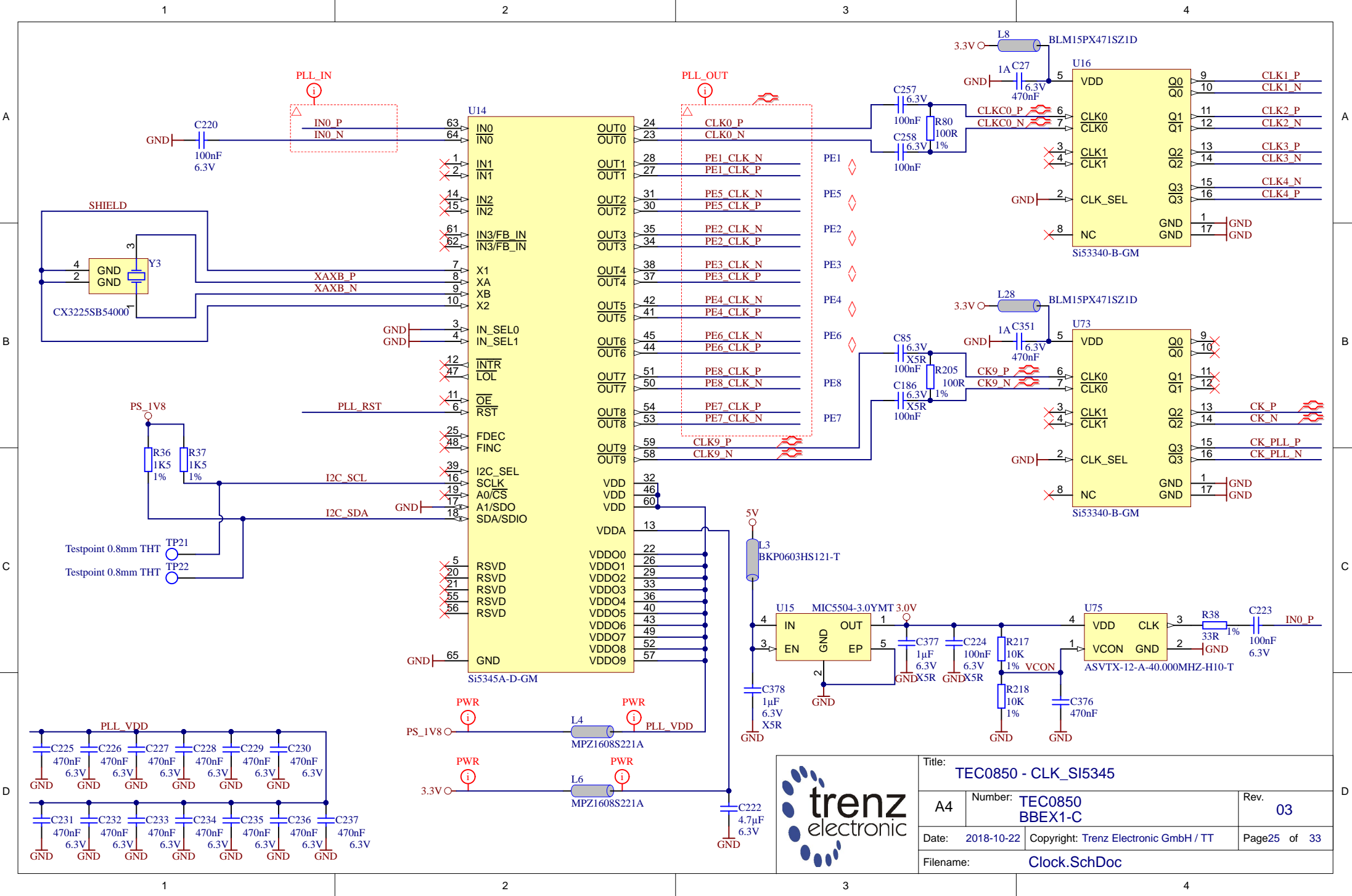
3

4

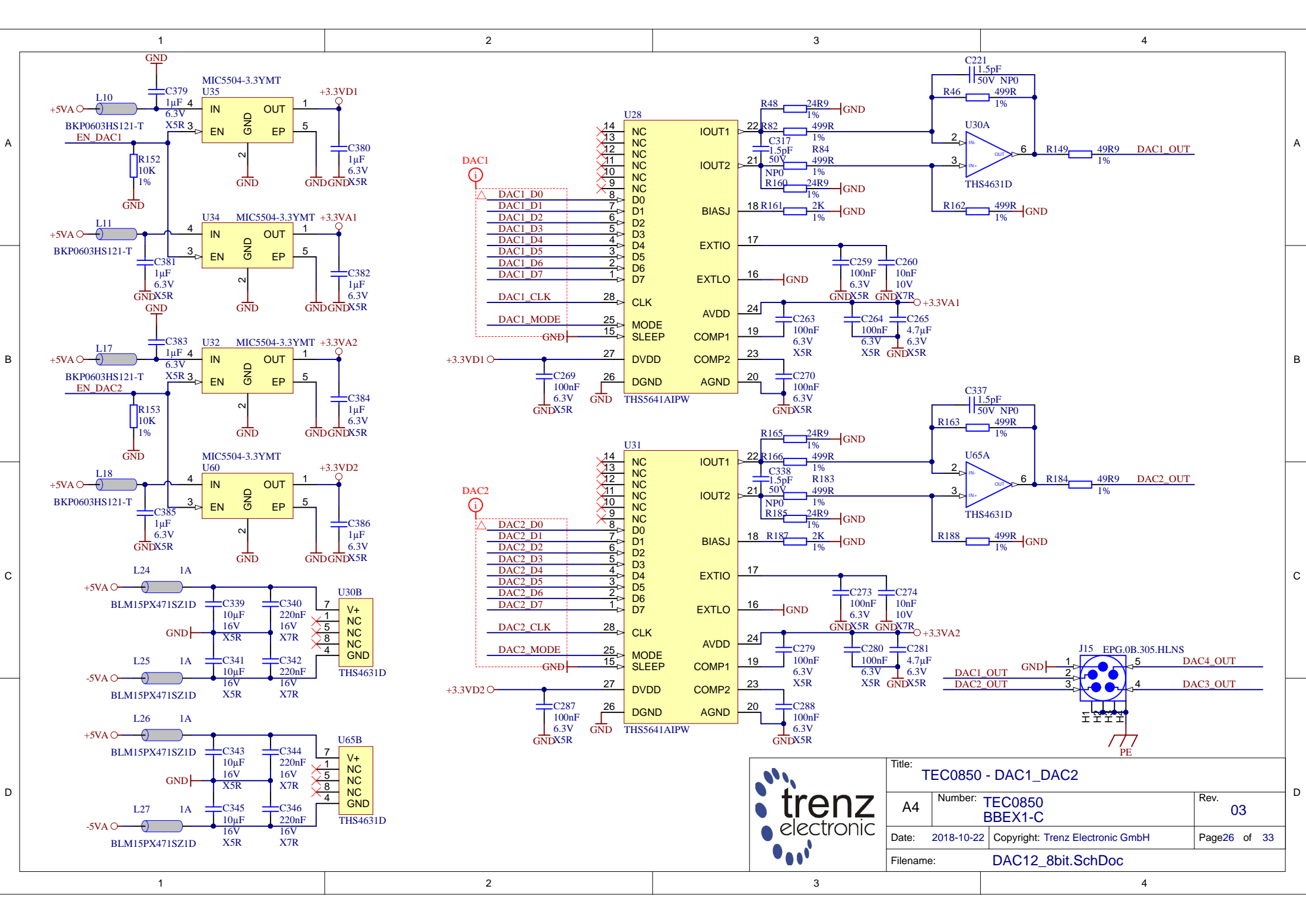


Title: <b>TEC0850 - USB_PHY</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	
Page <b>24</b> of <b>33</b>		Filename: <b>USB-PHY.SchDoc</b>

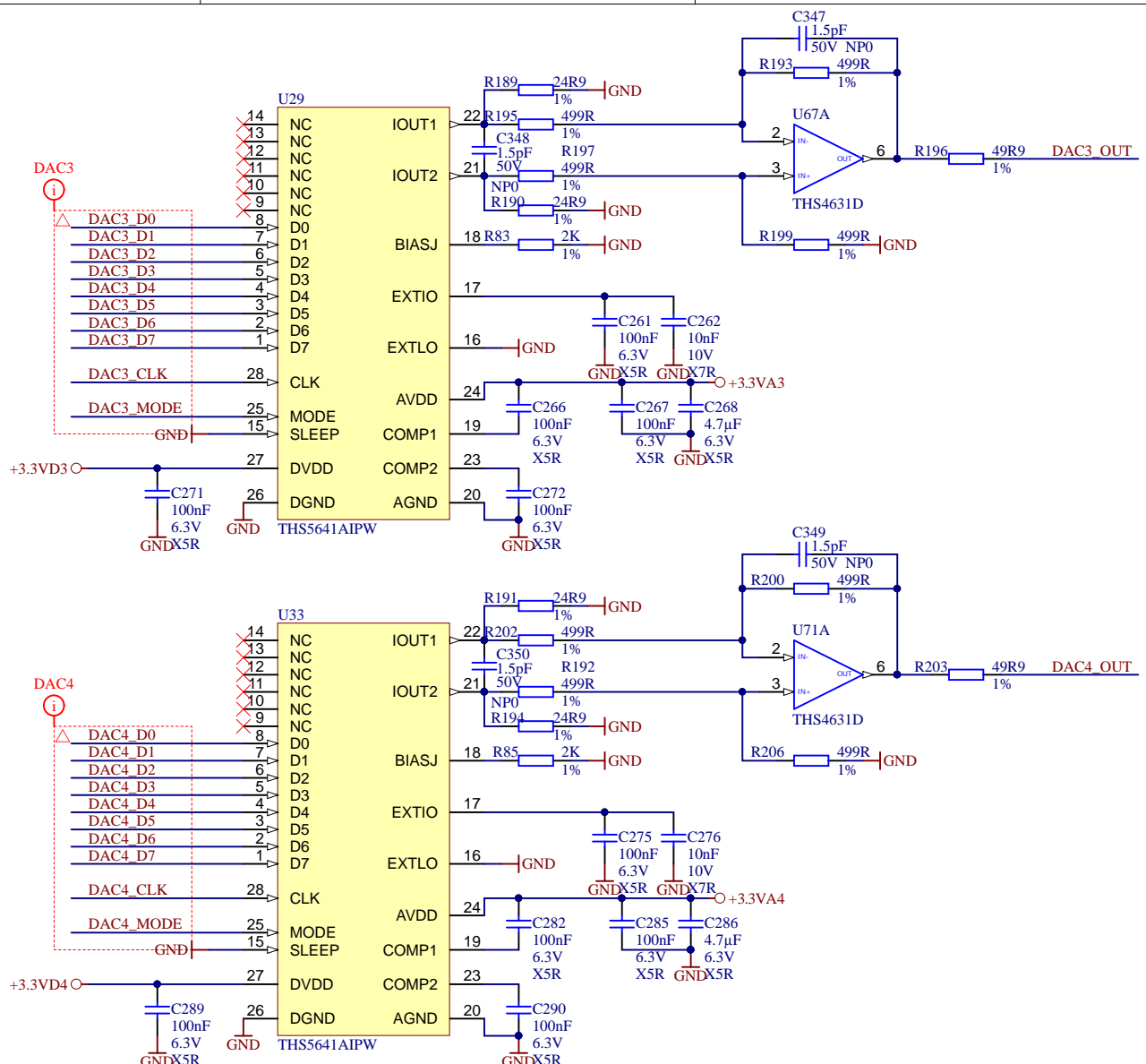
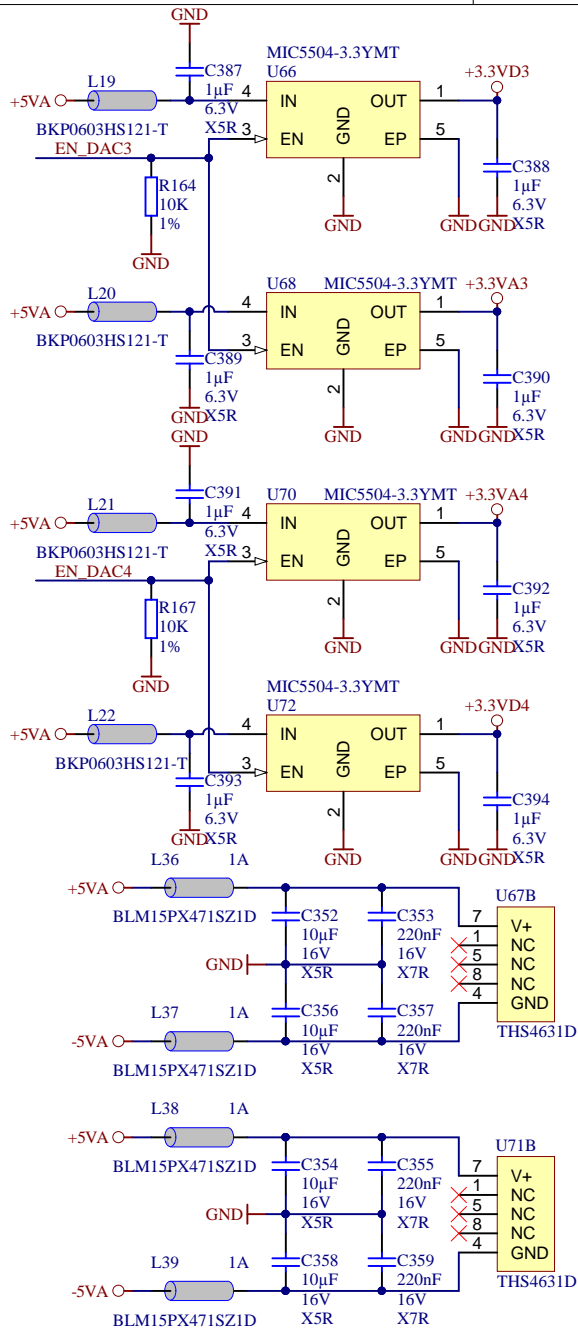




Title: TEC0850 - CLK_SI5345		
A4	Number: TEC0850 BBEX1-C	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH / TT	Page 25 of 33
Filename: Clock.SchDoc		

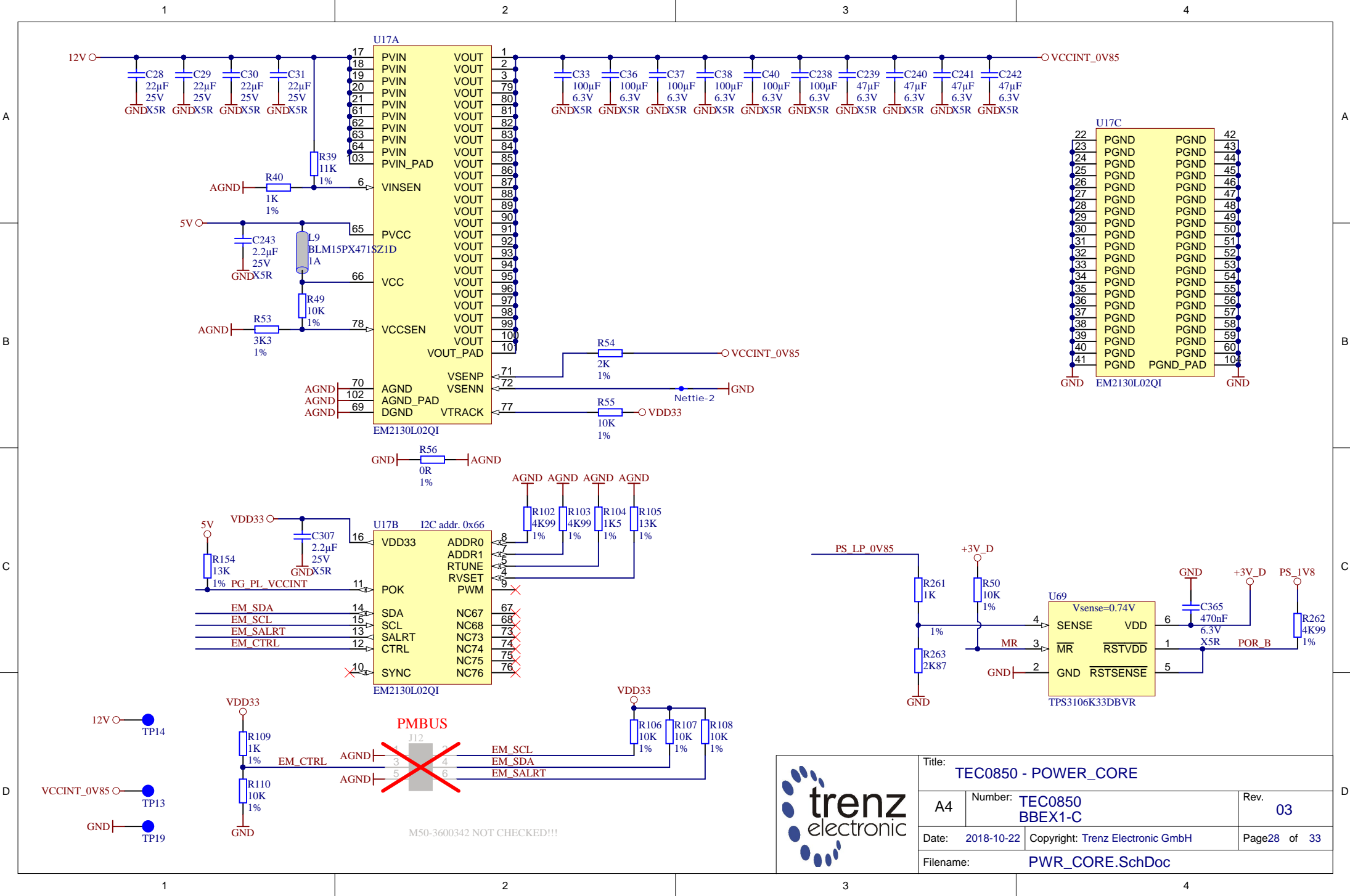


Title: <b>TEC0850 - DAC1_DAC2</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	
Page 26		of 33
Filename: <b>DAC12_8bit.SchDoc</b>		



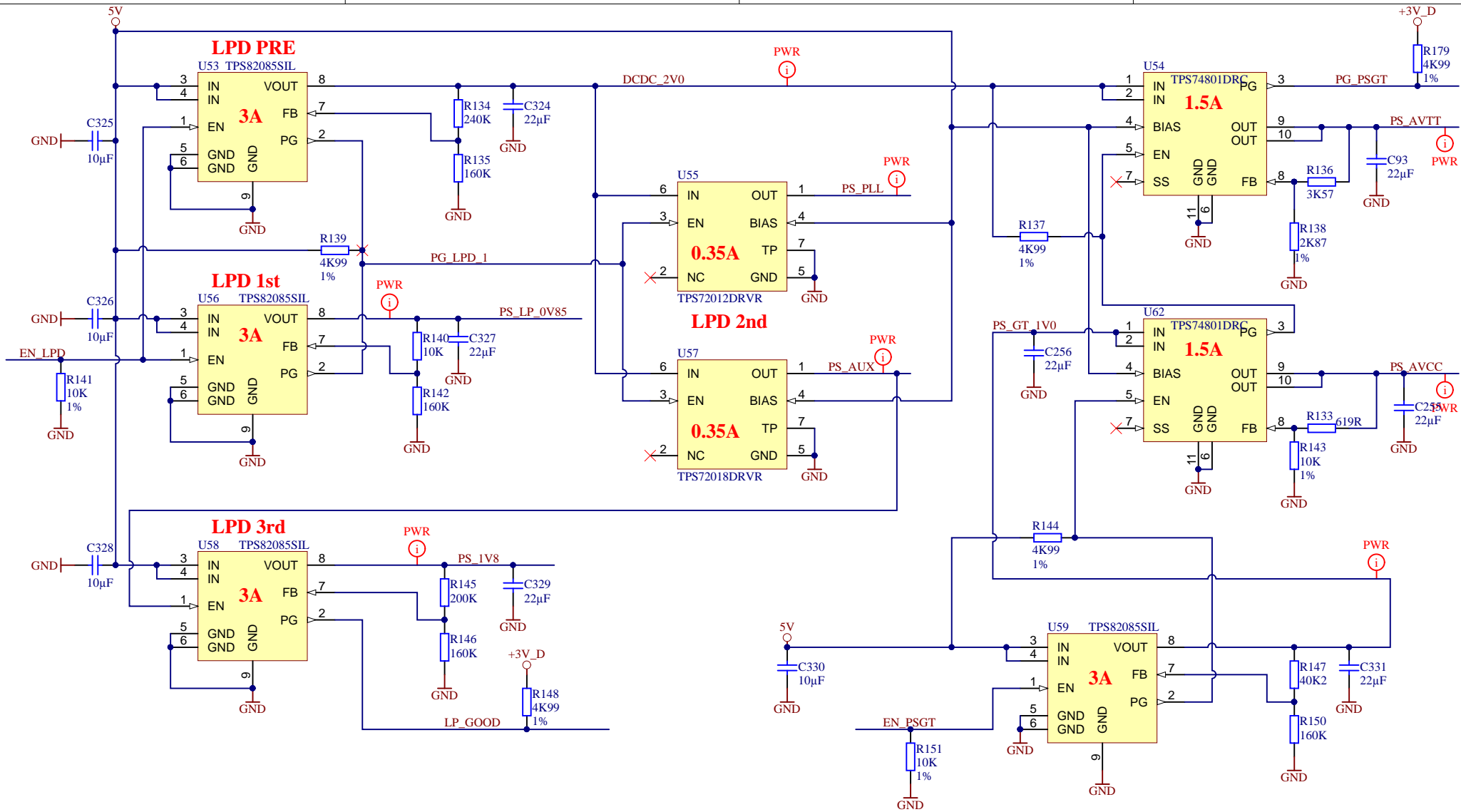
**trenz electronic**


Title: <b>TEC0850 - DAC3_DAC4</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page 27 of 33
Filename: <b>DAC34_8bit.SchDoc</b>		

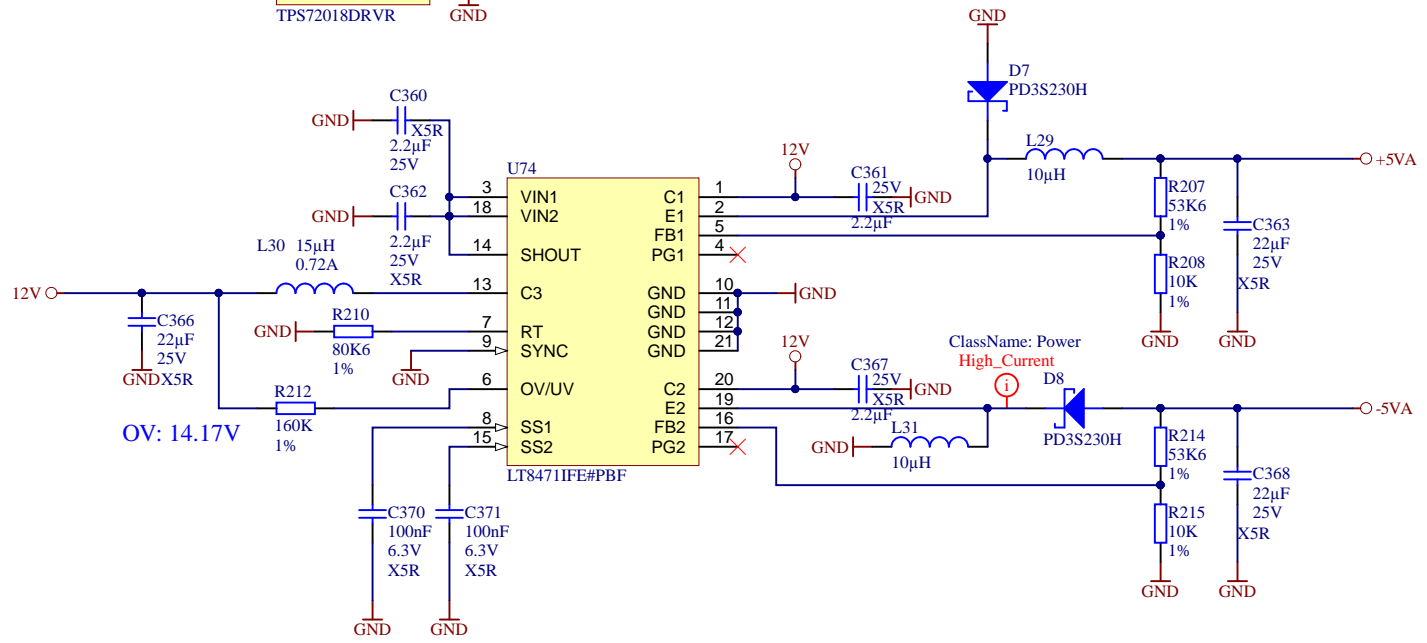
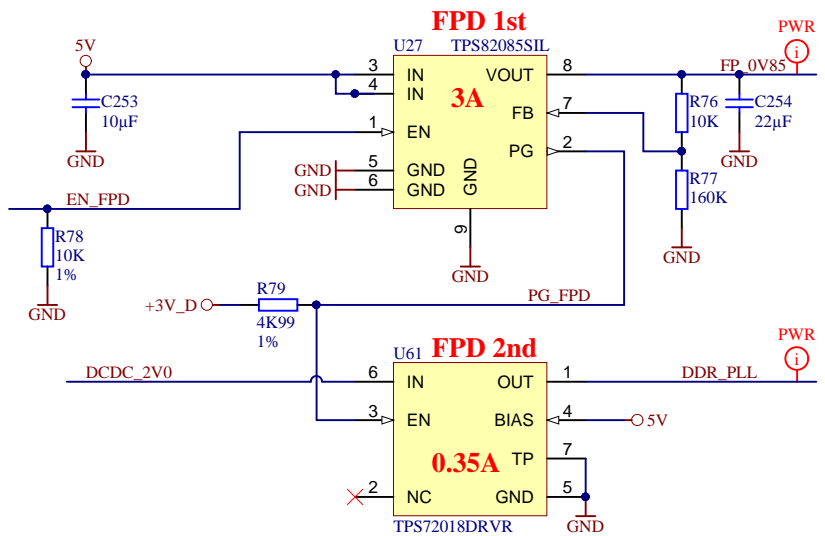


Title: TEC0850 - POWER_CORE		
A4	Number: TEC0850 BBEX1-C	Rev. 03
Date: 2018-10-22	Copyright: Trenz Electronic GmbH	Page 28 of 33
Filename: PWR_CORE.SchDoc		

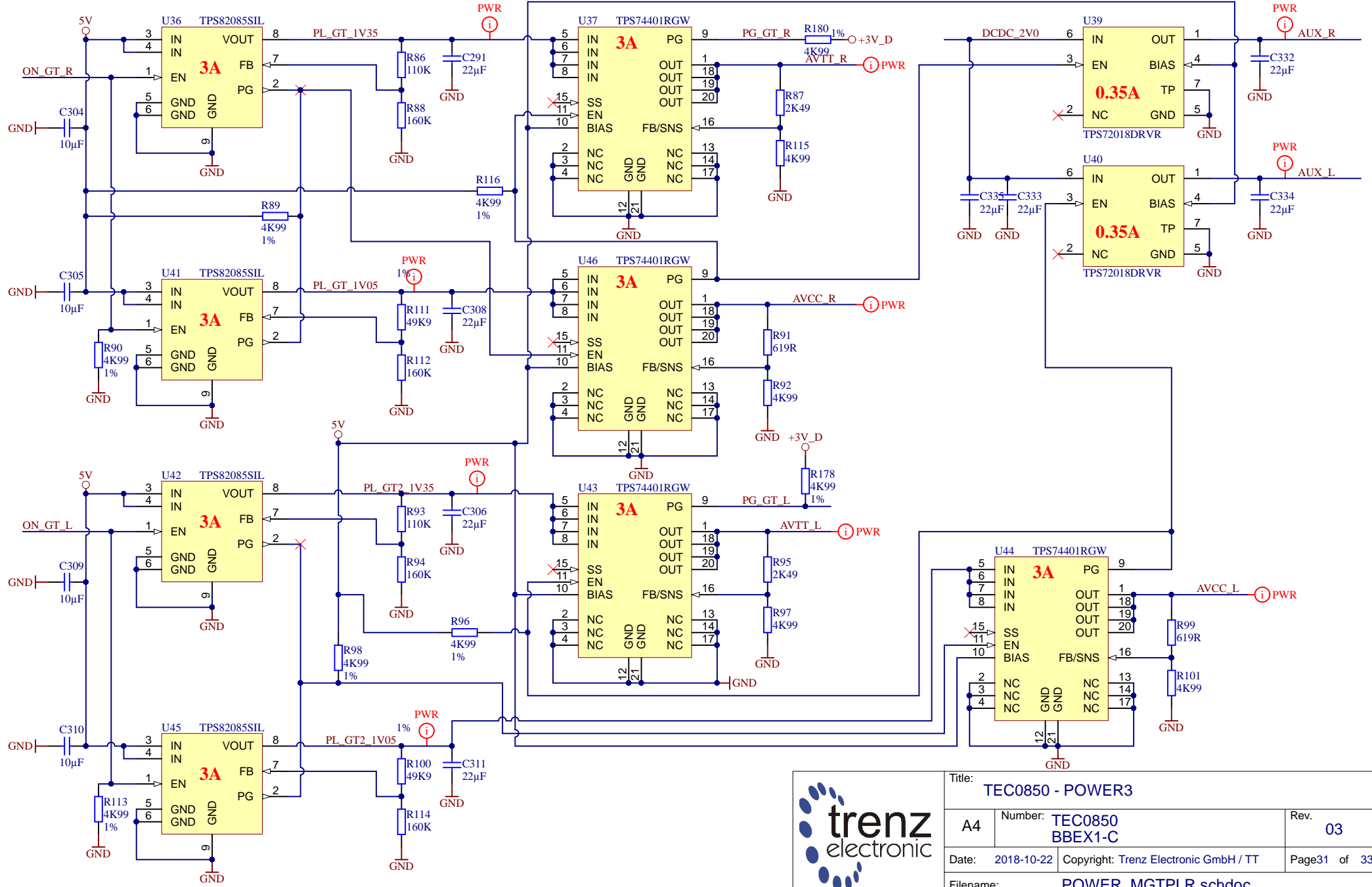
M50-3600342 NOT CHECKED!!!



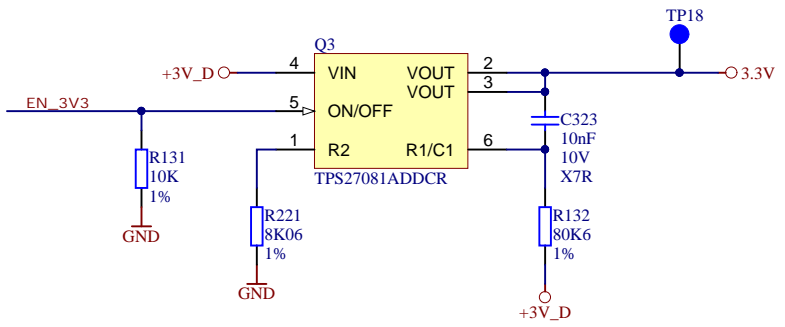
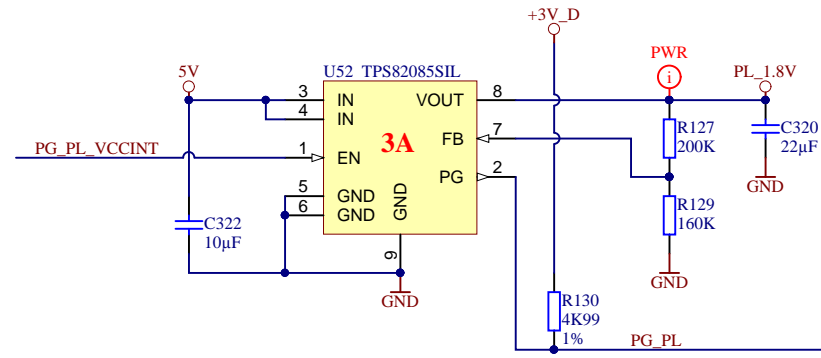
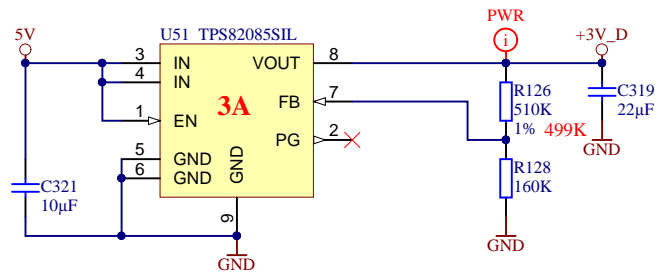
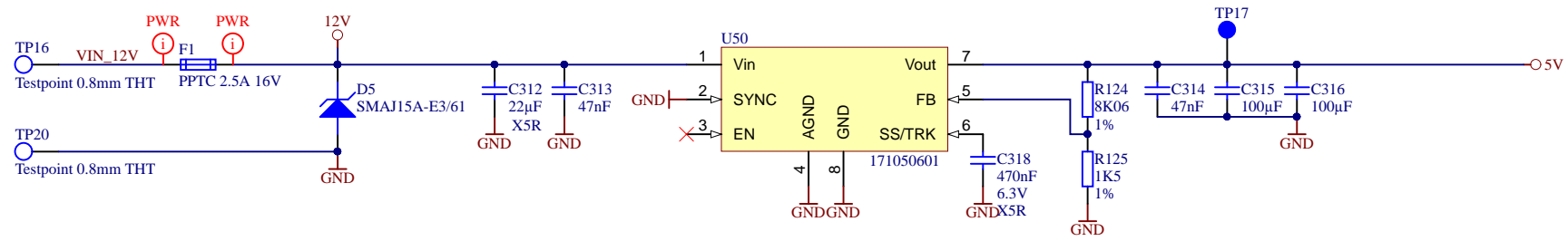
			Title: TEC0850 - POWER1	
			A4	Number: TEC0850 BBEX1-C
Date: 2018-10-22		Copyright: Trenz Electronic GmbH / TT		Page 29 of 33
Filename: POWER_PSLP.schdoc				



Title: <b>TEC0850 - POWER2</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>30</b> of <b>33</b>
Filename: <b>POWER_PSFP.schdoc</b>		



Title: <b>TEC0850 - POWER3</b>		
A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>31</b> of <b>33</b>
Filename: <b>POWER_MGTPLR.schdoc</b>		



	Title: <b>TEC0850 - POWER4</b>		
	A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
	Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>32</b> of <b>33</b>
	Filename: <b>POWER_MGTPLL.schdoc</b>		



1

2

3

4

CHANGES REV01 to REV02


- 1) Fixed connection for U16 (Si53340-B-GM)
- 2) Added THT-testpoints for I2C-bus
- 3) Changed MEMS osc to TCXO osc , added LDO for TCXO osc
- 4) Use out9 from PLL, added dual output buffer ("1" -> MPSOC, B65; "2" -> J1, cPCI-serial)
- 5) Changed connector J12 (do not populated)
- 6) Added capacitors C372, C373 on the clock line (AC-coupling)
- 7) Changed OPs for DACs (LT6200IS6 -> THS4631D)
- 8) Added additional DCDC (+/-5V) for THS4631D
- 9) Added THT-testpoints for VIN/GND
- 10) full update lib

CHANGES REV02 to REV03

- 1) Fixed connection for U74 (LT8471IFE#PBF)
- 2) Added additional resistors R219/R220
- 3) Fixed connection for Y2 (CM2012-2pad)
- 4) Changed U69 (TPS3106E09DBVR -> TPS3106K33DBVR)
- 5) Changed U73 (LTC6957IDD-2#PBF -> Si53340-B-GM)
- 6) Optimized BOM
- 7) full update lib

CHANGES REV03a

- 1) VY: replaced DDR4 SODIMM socket (b030-2604-6021-zhf -> 2309407-1)

	Title: <b>TEC0850 - Changes list</b>		
	A4	Number: <b>TEC0850 BBEX1-C</b>	Rev. <b>03</b>
	Date: <b>2018-10-22</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>33</b> of <b>33</b>
	Filename: <b>Revision_Changes.SchDoc</b>		

1

2

3

4