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U_FPGA
FPGA.SchDoc

U_FPGA_MISC
FPGA_MISC.SchDoc

U_PowerSupply
PowerSupply.SchDoc

U_FTDI
FTDI.SchDoc

U_Connectors
Connectors.SchDoc

U_Revision Changes
Revision Changes.SchDoc

Total I/O High Range/High Performance

CRUVI LS - 8 x HR
 CRUVI HS - 28 x HP, 9 x HR
 Pin Headers(bottom) - 44 HR
 TOTAL: 61 HR 28 HP

LEDS - 2
 Buttons - 1

Adjustable bank voltage 1.2 or 1.8V

LOGO1

TE Logo PRINT Layer

LOGO PRINT

MECH5

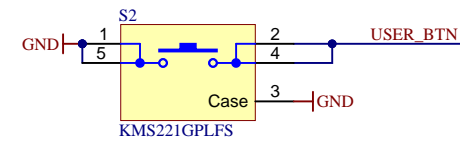
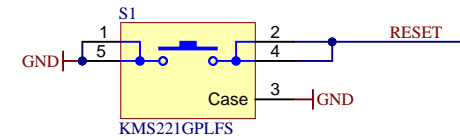
TE Address Overlay

LOGO ADDRESS

B

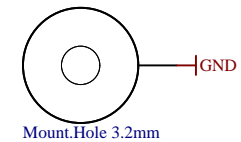
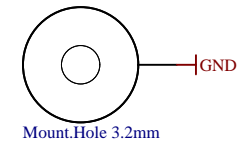
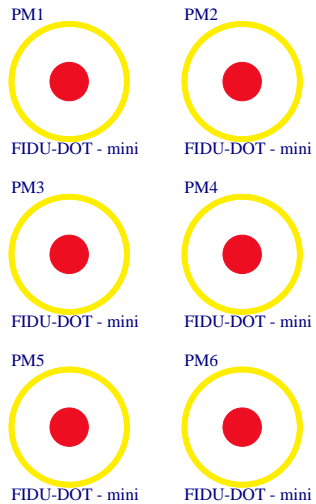
B

Serial
 Serialnumber 6,3 x 6.3mm



C

C



Assembly variant	A
Created by	VT
Modified by	VT
Modified at	2021-06-10
SVN Revision	1081 [Locally Modified]

D

D

Title: CR00103		
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Date: 17.03.2022	Copyright: MicroFPGA UG	Page 1 of 7
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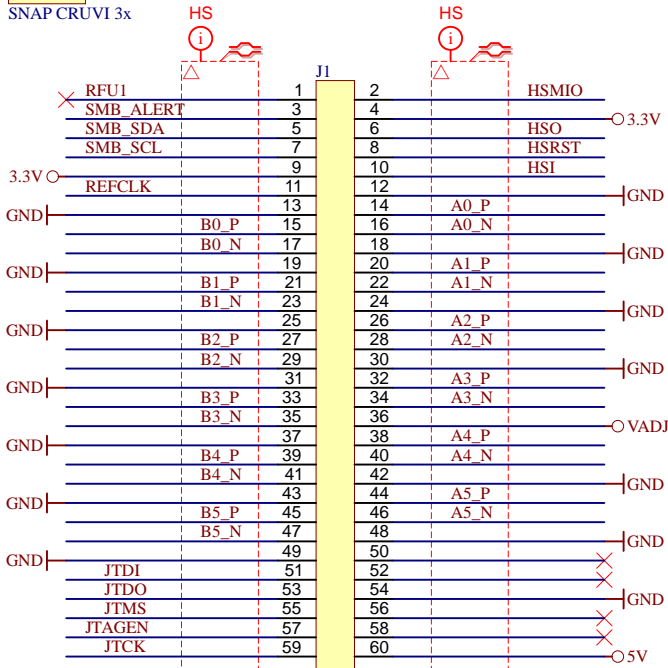
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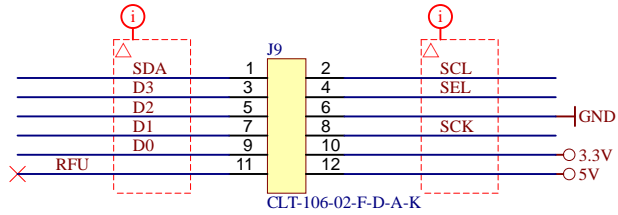
SNAP3

SNAP CRUV1 3x



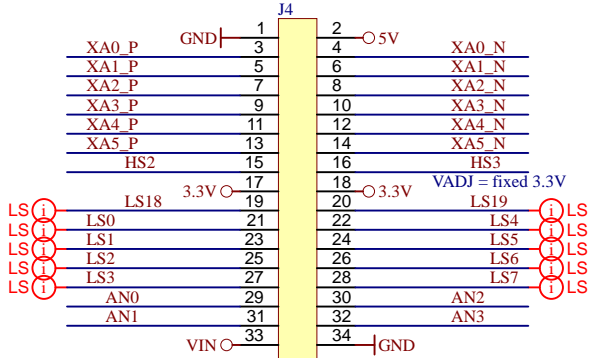
SS4-30-3.50-L-D-K-TR

LS_CRUV1

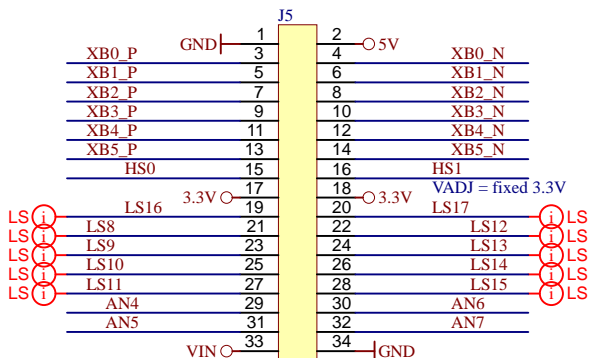


CLT-106-02-F-D-A-K

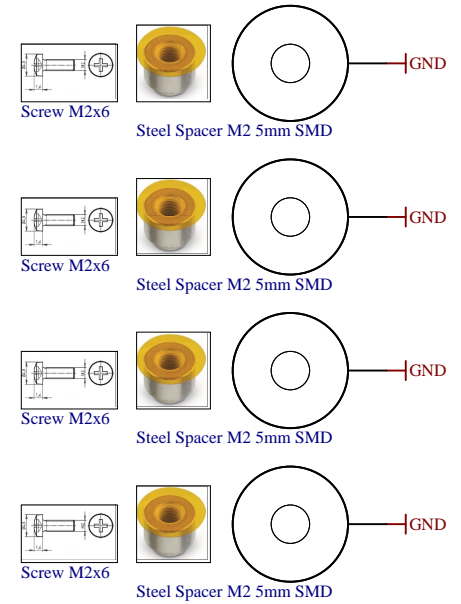
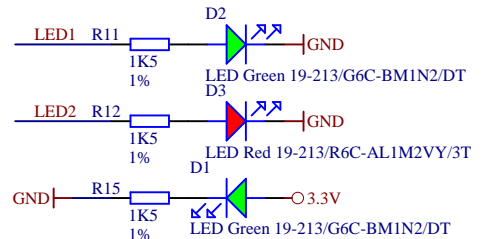
LS_CRUV1



SSM-117-F-DV-K

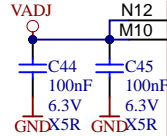


SSM-117-F-DV-K



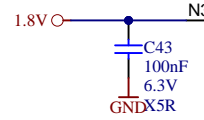
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High speed banks



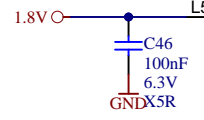
VCCIO3	PB54A/PCLKT3_0/VREF3_1/ADC_CP5	P8	B5_P
VCCIO3	PB54B/PCLKC3_0/ADC_CN5	N8	B5_N
	PB56A/ADC_CP7	K7	HS0
	PB56B/ADC_CN7	K8	HS1
	PB58A/PCLKT3_1/ADC_CP6	P9	B4_P
	PB58B/PCLKC3_1/ADC_CN6	N9	B4_N
	PB60A/ADC_CP9	P10	B3_P
	PB60B/ADC_CN9	N10	B3_N
	PB62A/ADC_CP10	L8	HSMIO
	PB62B/ADC_CN10	M8	HSI
	PB64A/ADC_CP4	M9	HS2
	PB64B/ADC_CN4	L9	HS3
	PB66A/COMP1P	K9	HSRST
	PB66B/COMP1N	K10	HSO
	PB68A/ADC_CP8	M11	A3_P
	PB68B/ADC_CN8	L12	A3_N
	PB70A/COMP2P	K11	A0_P
	PB70B/COMP2N	K12	A0_N
	PB72A/PCLKT3_2/ADC_CP13	P11	B2_P
	PB72B/PCLKC3_2/ADC_CN13	N11	B2_N
	PB74A/PCLKT3_3/ADC_CP14	P12	A5_P
	PB74B/PCLKC3_3/ADC_CN14	P13	A5_N
	PB76A/COMP3P	N13	A4_P
	PB76B/COMP3N	N14	A4_N
	PB78A/ADC_CP11	M14	B1_P
	PB78B/ADC_CN11	M13	B1_N
	PB80A/ADC_CP12	L13	A2_P
	PB80B/ADC_CN12	L14	A2_N
	PB82A/ADC_CP15	K13	A1_P
	PB82B/ADC_CN15	K14	A1_N
	PB84A/LRC_GPLL0T_IN	J14	B0_P
	PB84B/LRC_GPLL0C_INVREF3_2	J13	B0_N

UID LFD2NX-40-7BG196I



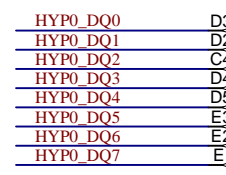
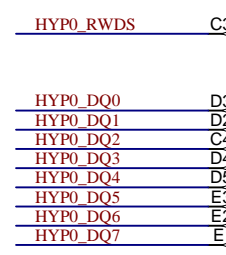
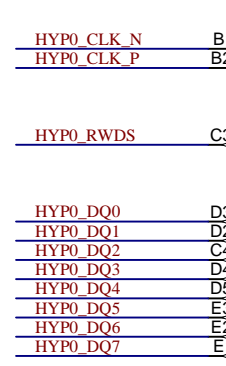
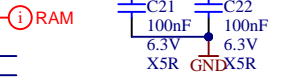
VCCIO5	PB4A/VREF5_1/ADC_CP0/COMP1P	K1	AN4
	PB4B/CDR_RXN0/ADC_CN0/COMP1N	L1	AN5
	PB6A/PCLKT5_0/CDR_RXP1/ADC_CP1/COMP2P	L3	AN6
	PB6B/PCLKC5_0/CDR_RXN1/ADC_CN1/COMP2N	M1	AN7
	PB8A/PCLKT5_1/LLC_GPLL0T_IN/ADC_CP3	N1	
	PB8B/PCLKC5_1/LLC_GPLL0C_INVREF3_2	L2	
	PB10A/PCLKT5_2/ADC_CP2/COMP3P	M2	
	PB10B/PCLKC5_2/ADC_CN2/COMP3N	P2	
	PB12A/PCLKT5_3	P3	
	PB12B/PCLKC5_3/VREF5_2		

UIF LFD2NX-40-7BG196I



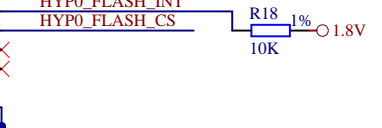
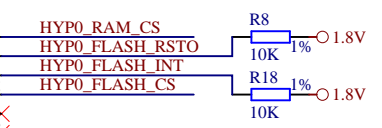
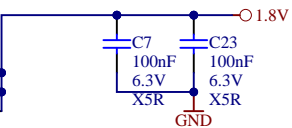
VCCIO4	PB16A/VREF4_1	L4	HYP0_DQ5
	PB16B	M4	HYP0_DQ3
	PB18A/PCLKT4_3	N4	HYP0_DQ6
	PB18B/PCLKC4_3	P4	HYP0_DQ7
	PB20A	K4	HYP0_DQ0
	PB20B	K5	HYP0_DQ4
	PB22A	N5	HYP0_DQ1
	PB22B	P5	HYP0_RWDS
	PB24A/PCLKT4_2	N6	HYP0_FLASH_CS
	PB24B/PCLKC4_2	P6	HYP0_RESET
	PB26A	K6	HYP0_FLASH_INT
	PB26B	L6	HYP0_DQ2
	PB28A	L7	HYP0_FLASH_RSTO
	PB28B	M7	HYP0_RAM_CS
	PB30A	N7	HYP0_CLK_P
	PB30B	P7	HYP0_CLK_N

UIE LFD2NX-40-7BG196I

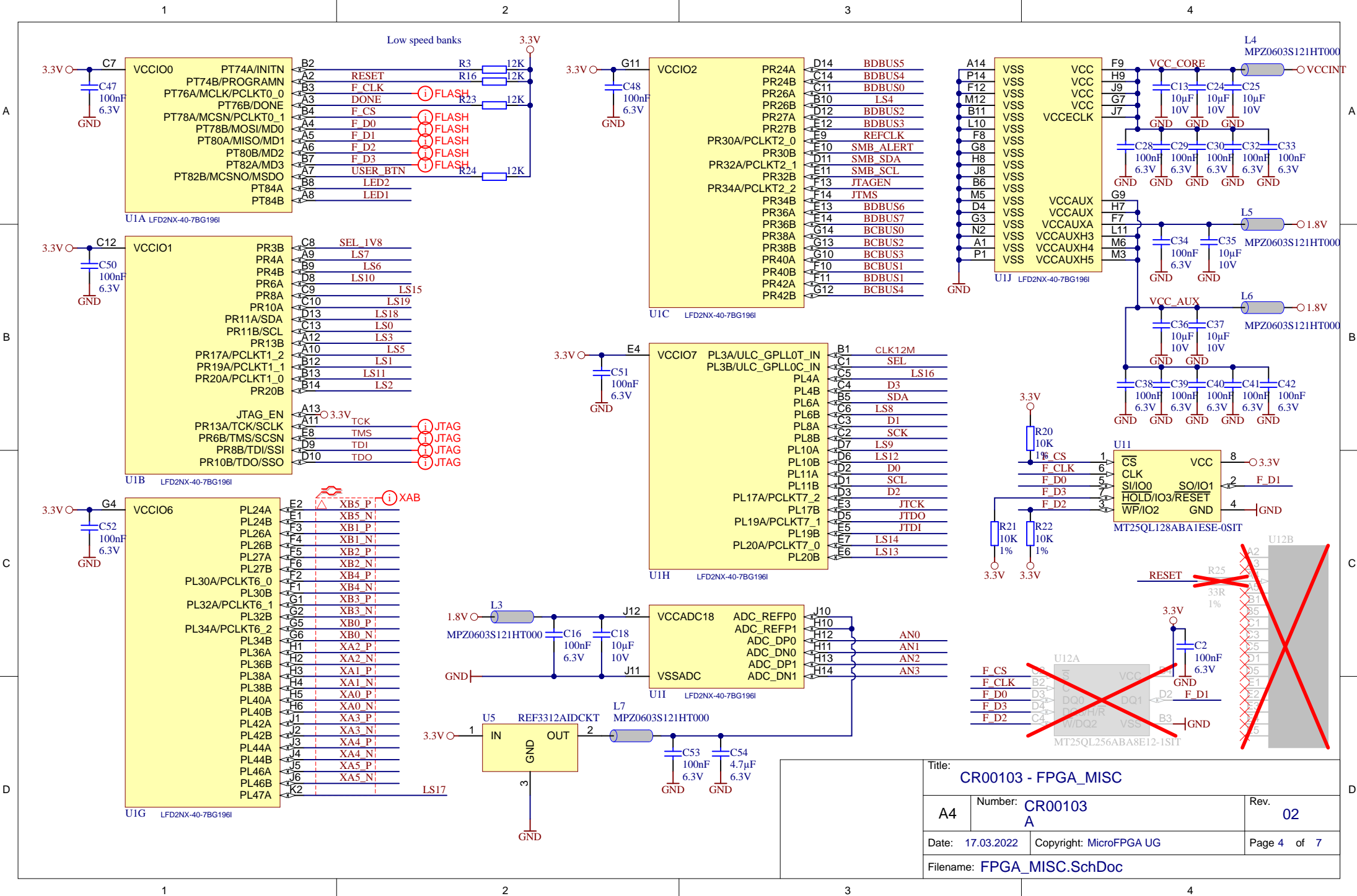


HYP0_CLK_N	B1	CK/RFU	B4	VCC
HYP0_CLK_P	B2	CK	D1	VCCQ
			E4	VCCQ
HYP0_RWDS	C3	RWDS	A4	RESET
HYP0_DQ0	D3	DQ0	A3	HYP0_RAM_CS
HYP0_DQ1	D2	DQ1	A2	HYP0_FLASH_RSTO
HYP0_DQ2	C4	DQ2	A5	HYP0_FLASH_INT
HYP0_DQ3	D4	DQ3	C2	HYP0_FLASH_CS
HYP0_DQ4	D5	DQ4	B5	
HYP0_DQ5	E3	DQ5	C5	
HYP0_DQ6	E2	DQ6	B3	VSS
HYP0_DQ7	E1	DQ7	A1	VSS
			C1	VSSQ
			E5	VSSQ

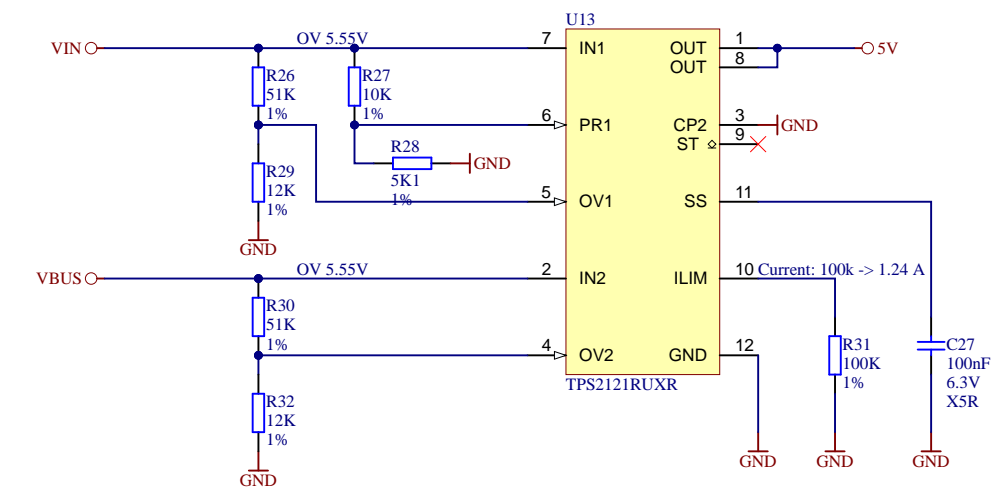
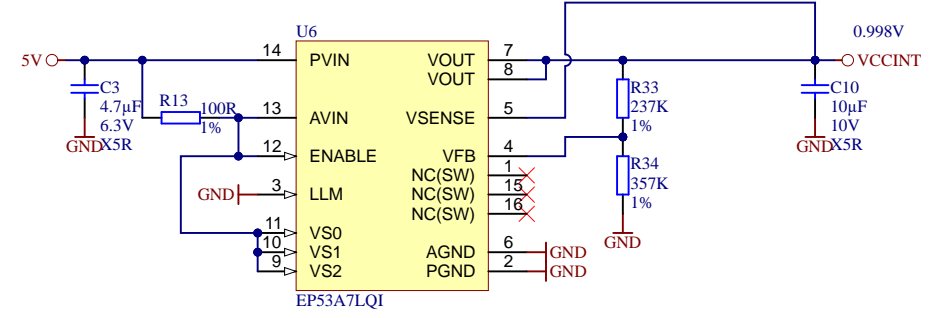
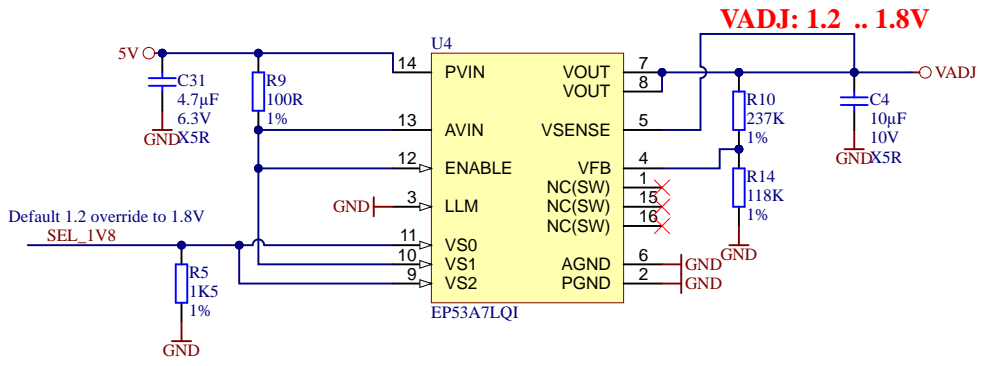
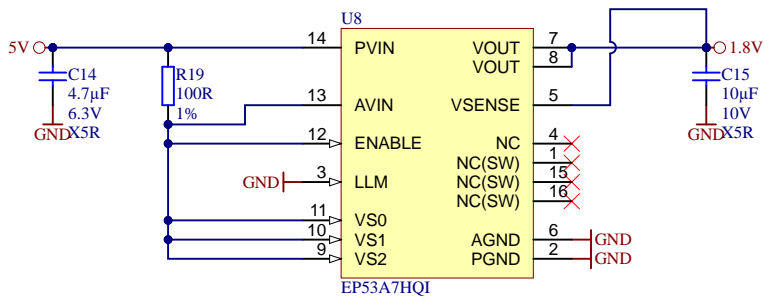
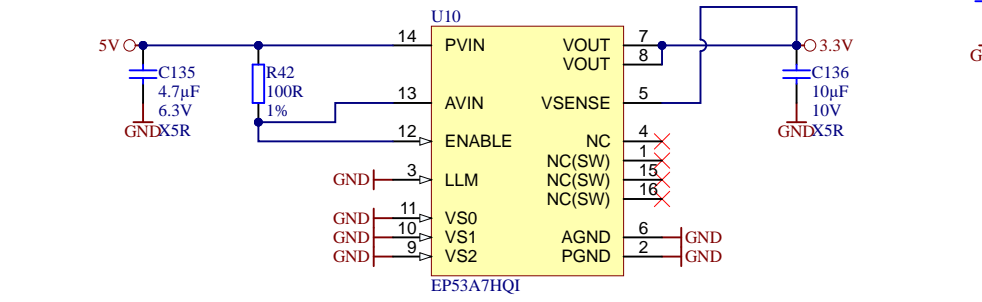
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Title: CR00103 - FPGA_MISC		
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Title: CR00103 - PWR		
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REV	Description	
-01	Initial revision	AL/VT
-02	1. Button S2 disconnected from U1.B2 and connected to U1.A7. Resistor R24 populated 2. Fixed U6 output voltage. Voltage divider R33-R34 connected to U6.4, updated VID control (U6.9-11)	AL/VY

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Title: CR00103 - Revision History		
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