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U_FPGA FPGA.SchDoc	U_FTDI FTDI.SchDoc
U_FPGA_MISC FPGA_MISC.SchDoc	U_Connectors Connectors.SchDoc
U_PowerSupply PowerSupply.SchDoc	U_Revision Changes Revision Changes.SchDoc

Total I/O High Range/High Performance

CRUVI LS - 8 x HR
CRUVI HS - 28 x HP, 9 x HR
TOTAL: 17 HR 28 HP

LEDS - 2
Buttons - 1

Adjustable bank voltage 1.8 or 3.3V

LOGO1

TE Logo PRINT Layer

LOGO PRINT

MECH5

TE Address Overlay

LOGO ADDRESS

UKCA

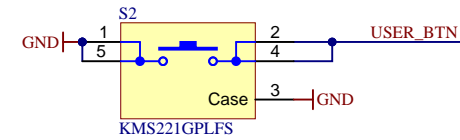
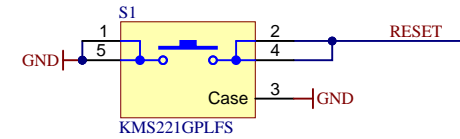
UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

B

B

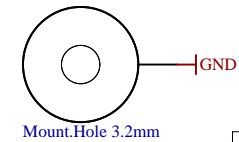
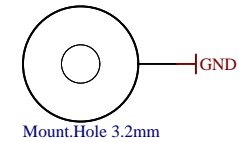
Serial
Serialnumber 6,3 x 6.3mm



C

C

PM1 FIDU-DOT - mini	PM2 FIDU-DOT - mini
PM3 FIDU-DOT - mini	PM4 FIDU-DOT - mini
PM5 FIDU-DOT - mini	PM6 FIDU-DOT - mini



Assembly variant	default
Created by	VT
Modified by	VT
Modified at	2022-05-23
SVN Revision	1220

D

D

Title: CR00107		
A4	Number: CR00107 default	Rev. 01
Date: 10.06.2022	Copyright: Trenz Electronic GmbH	Page 1 of 7
Filename: CR00107.SchDoc		

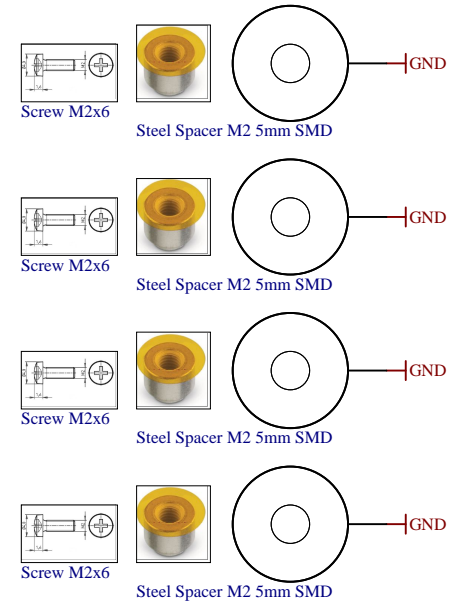
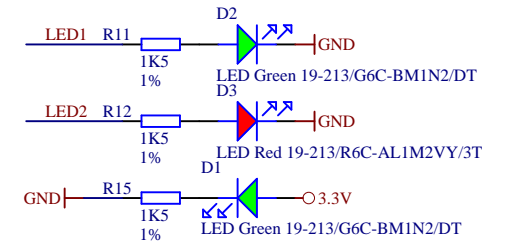
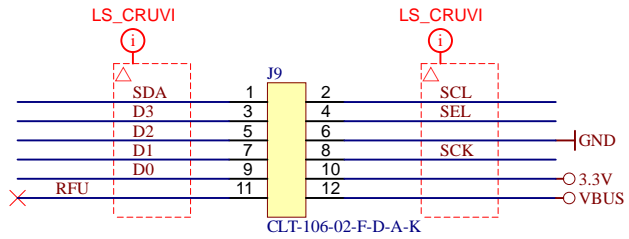
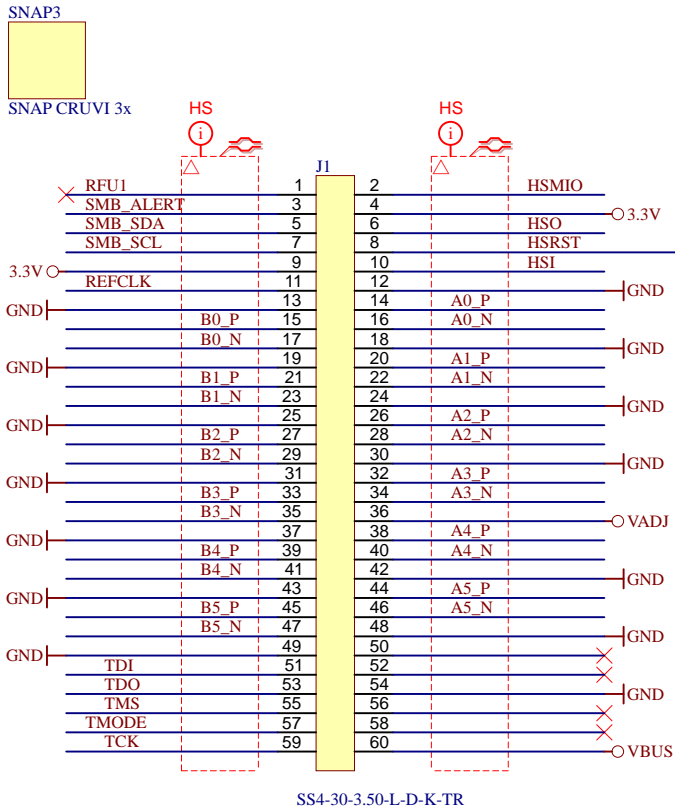
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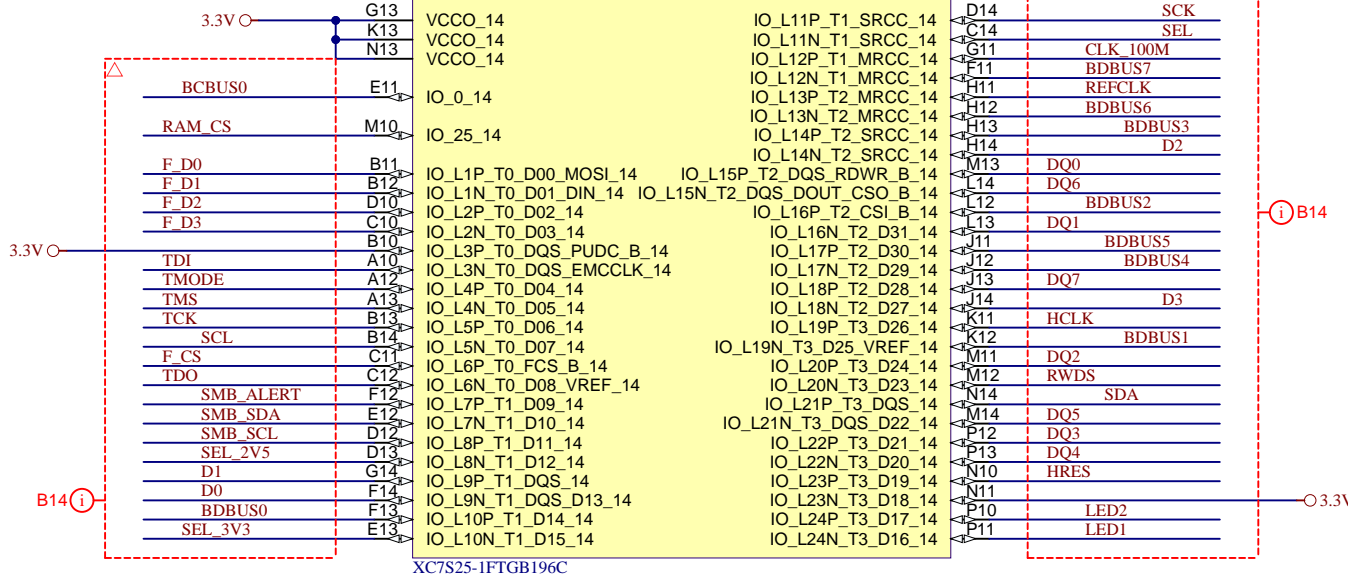
C

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UIA

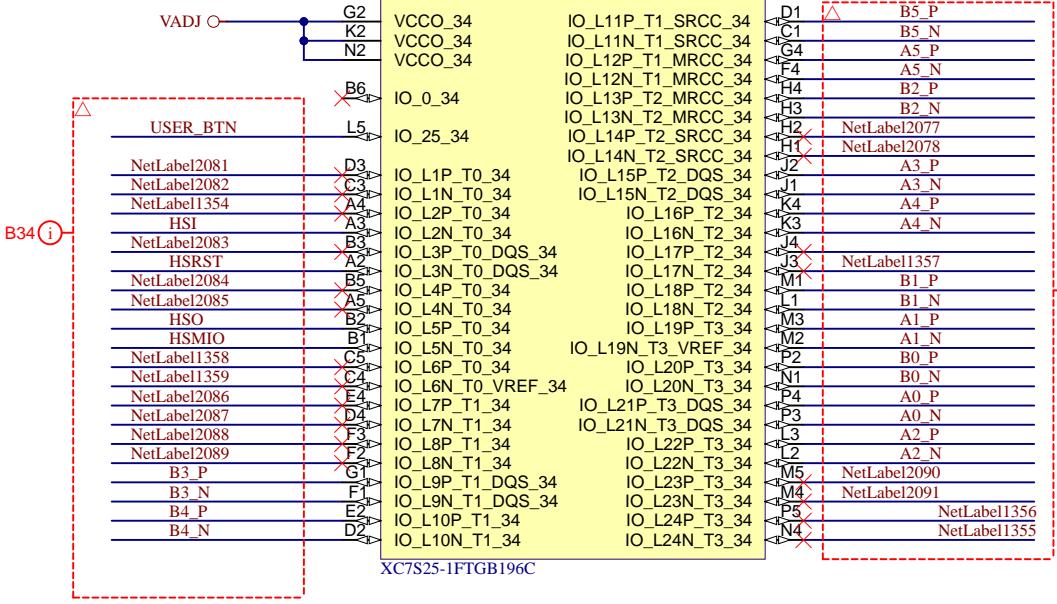
BANK14



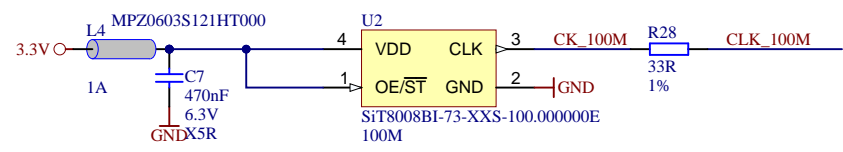
XC7S25-1FTGB196C

UIB

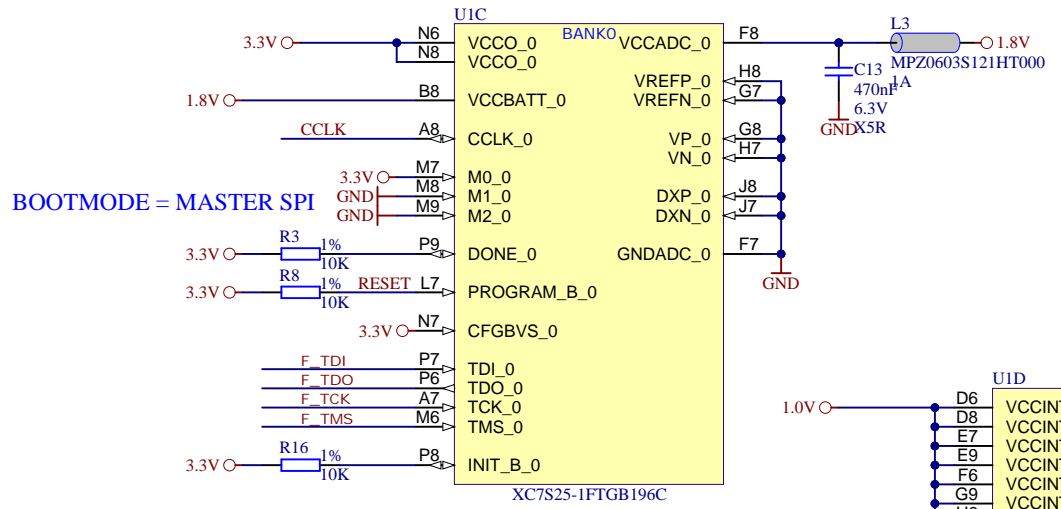
BANK34



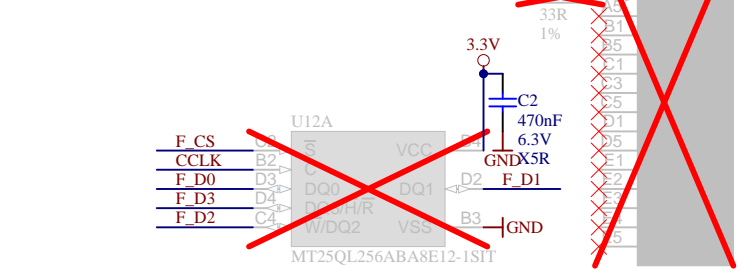
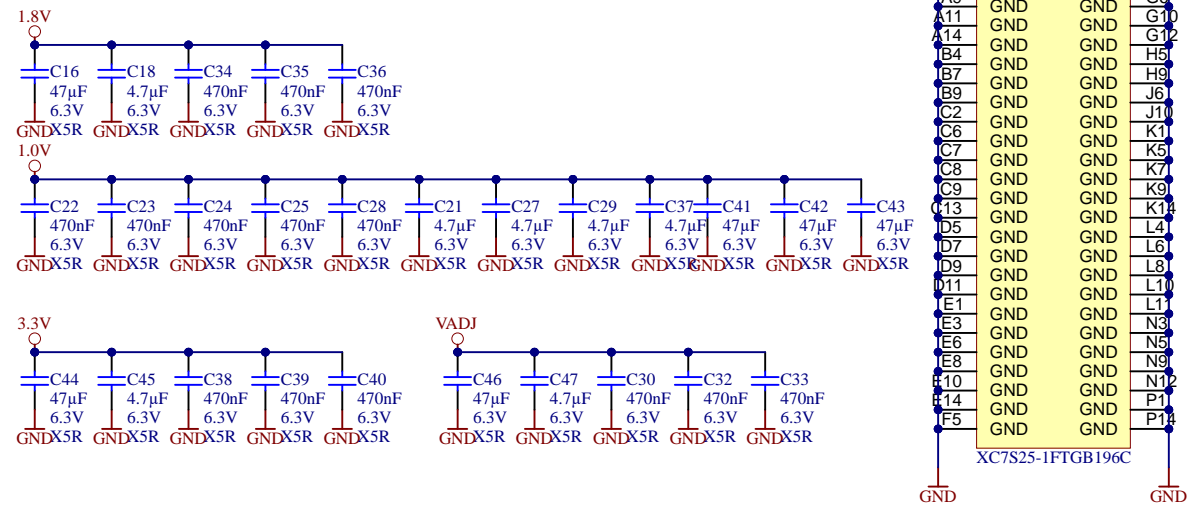
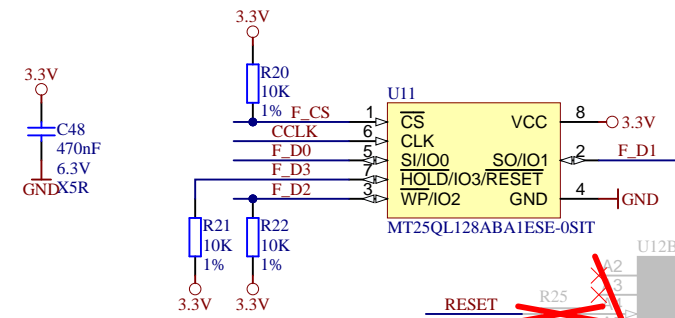
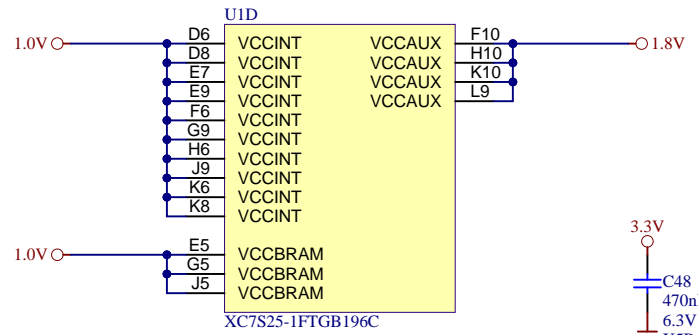
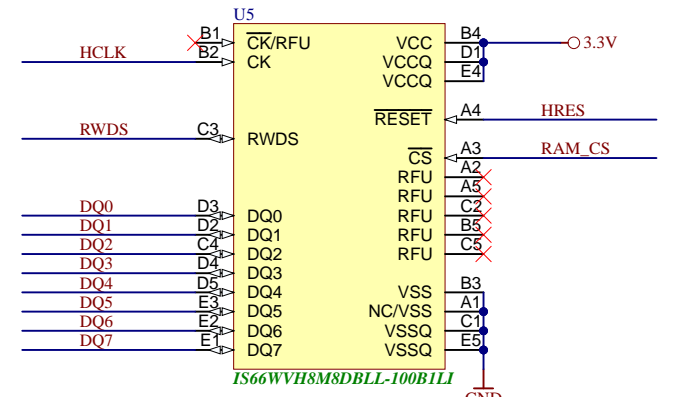
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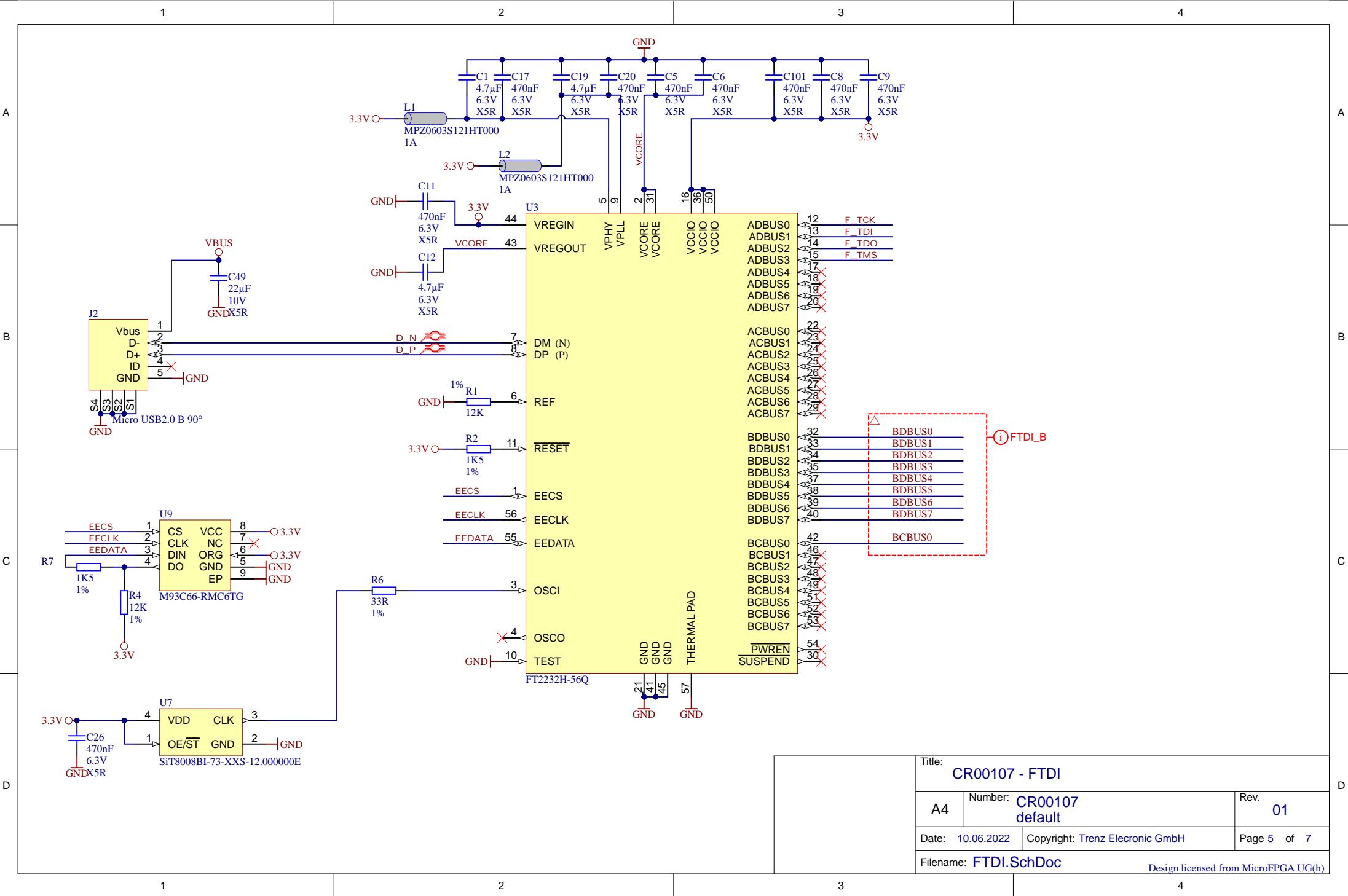
Title: CR00107 - FPGA		
A4	Number: CR00107 default	Rev. 01
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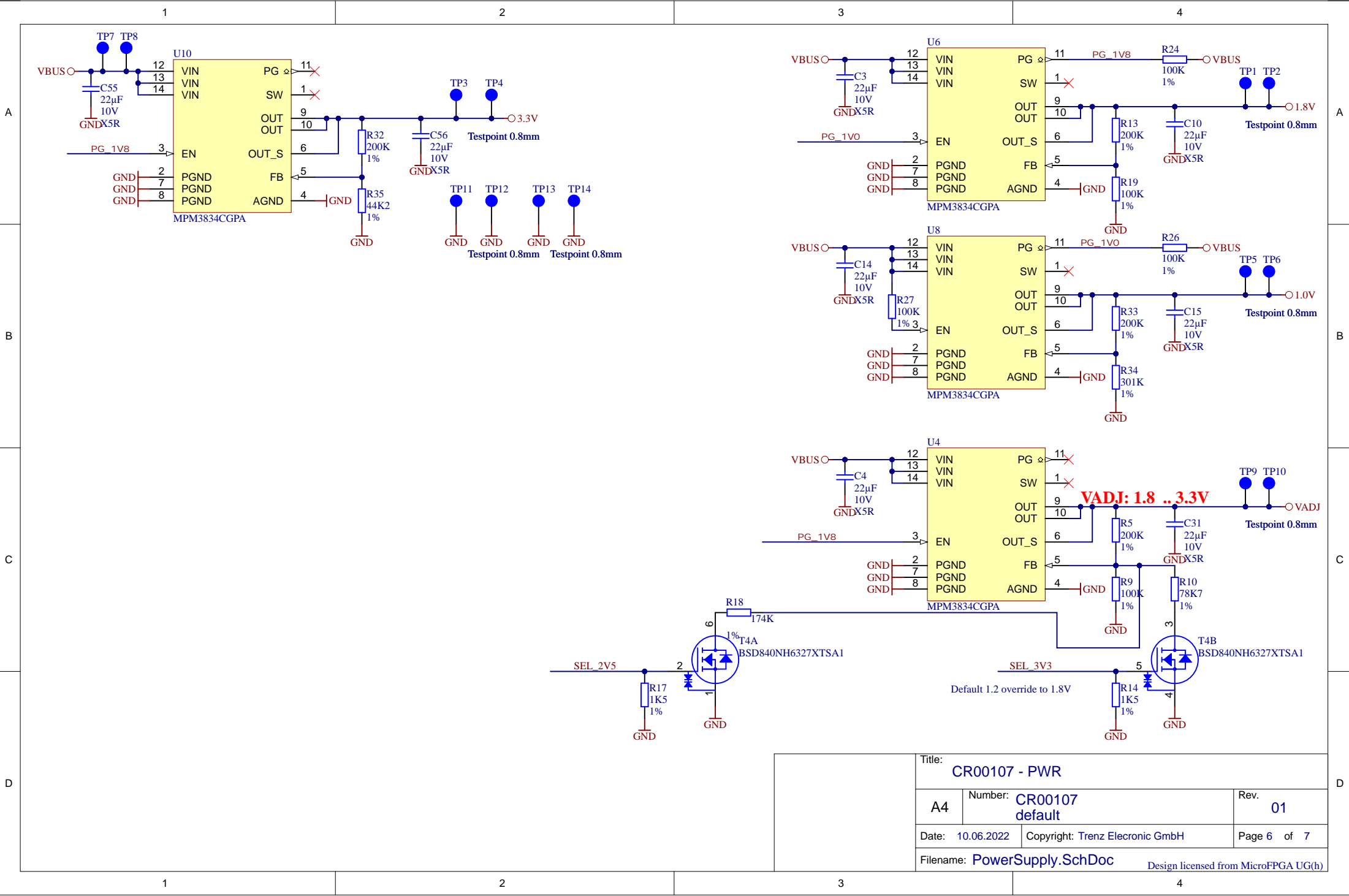
BOOTMODE = MASTER SPI



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REV	Description	
-01	Initial revision	AL/VT

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