


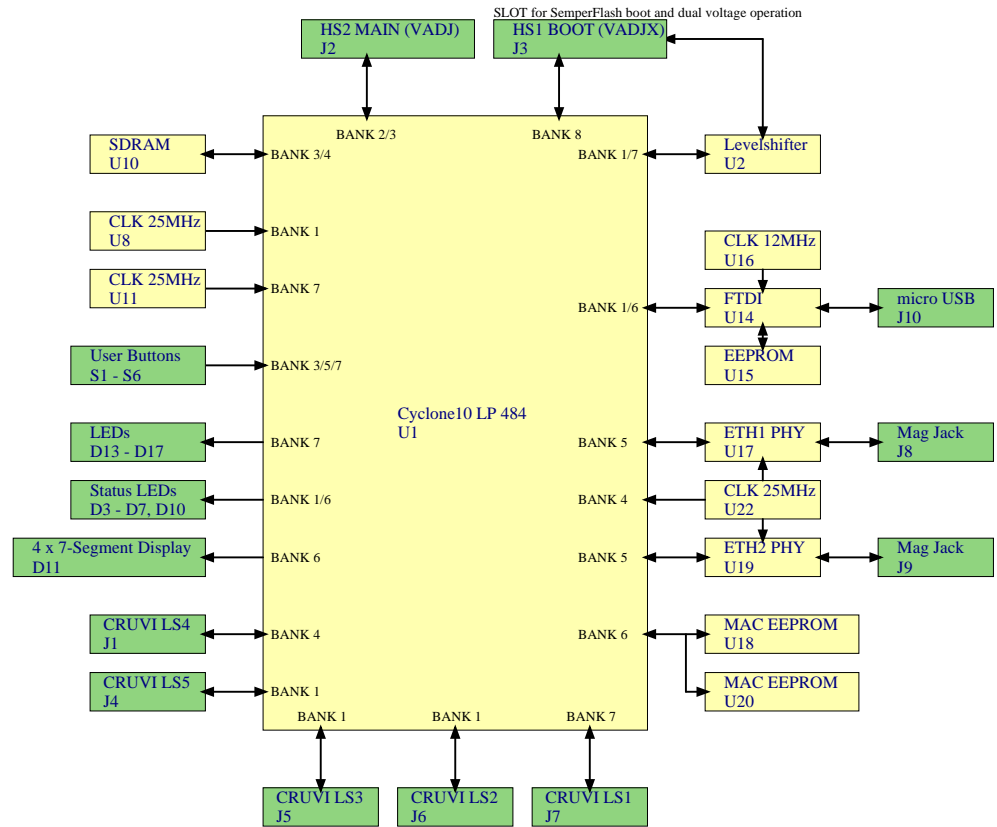
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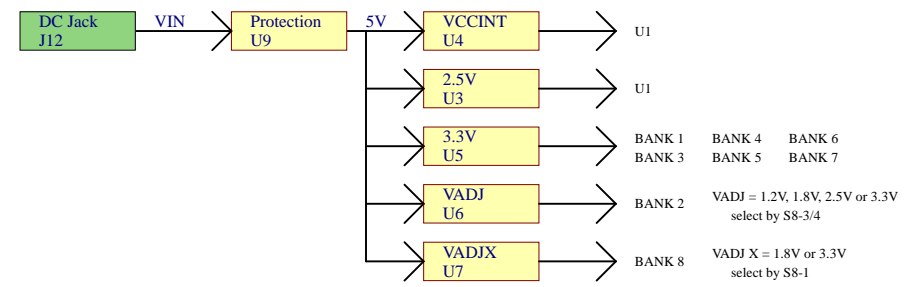
Schematics and other handouts serve for informational purposes only!

Design drawn by: * Checked by: *	Title: CR00109		
	Assembly variant: QHCN-A	Number: CR00109 QHCN-A	Rev. 01
Created by: MR Modified by: MR Modified at: 2022-02-08	Date: 22.04.2022 Copyright: Trenz Electronic GmbH / TT		Page 1 of 18
		Filename: Legal Notices.SchDoc	

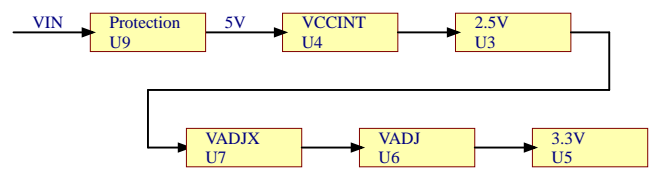
Block Diagramm



Power Supply Structure



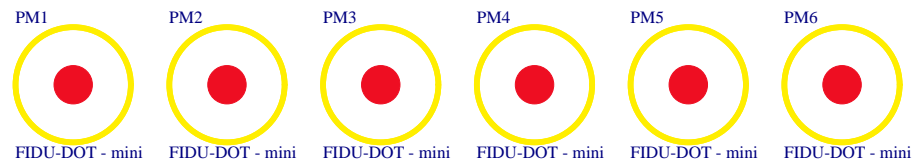
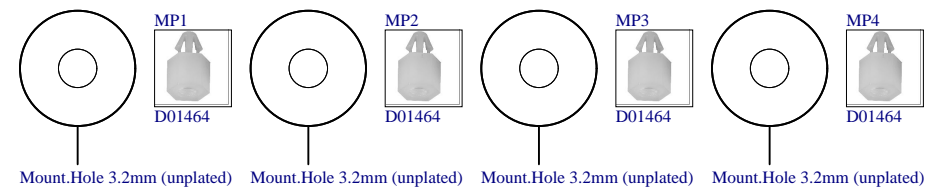
Power Supply Sequencing



UKCA
UKCA Logo on Top Overlay
UKCA-TOPOVERLAY

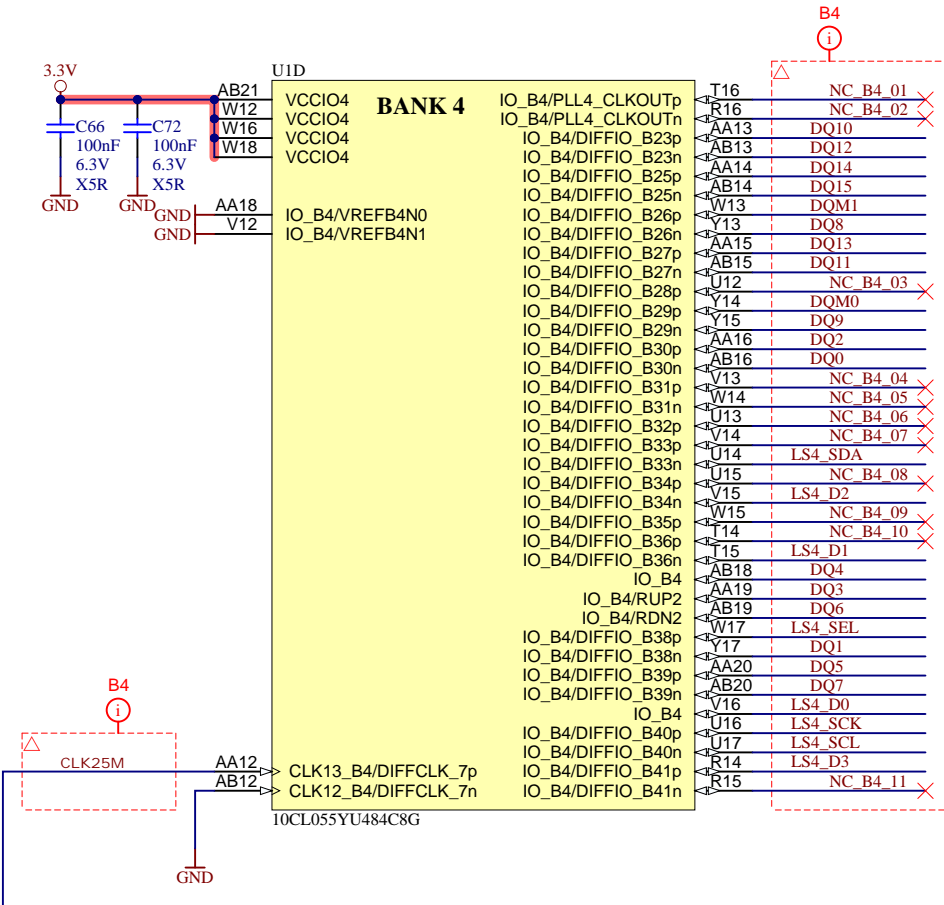
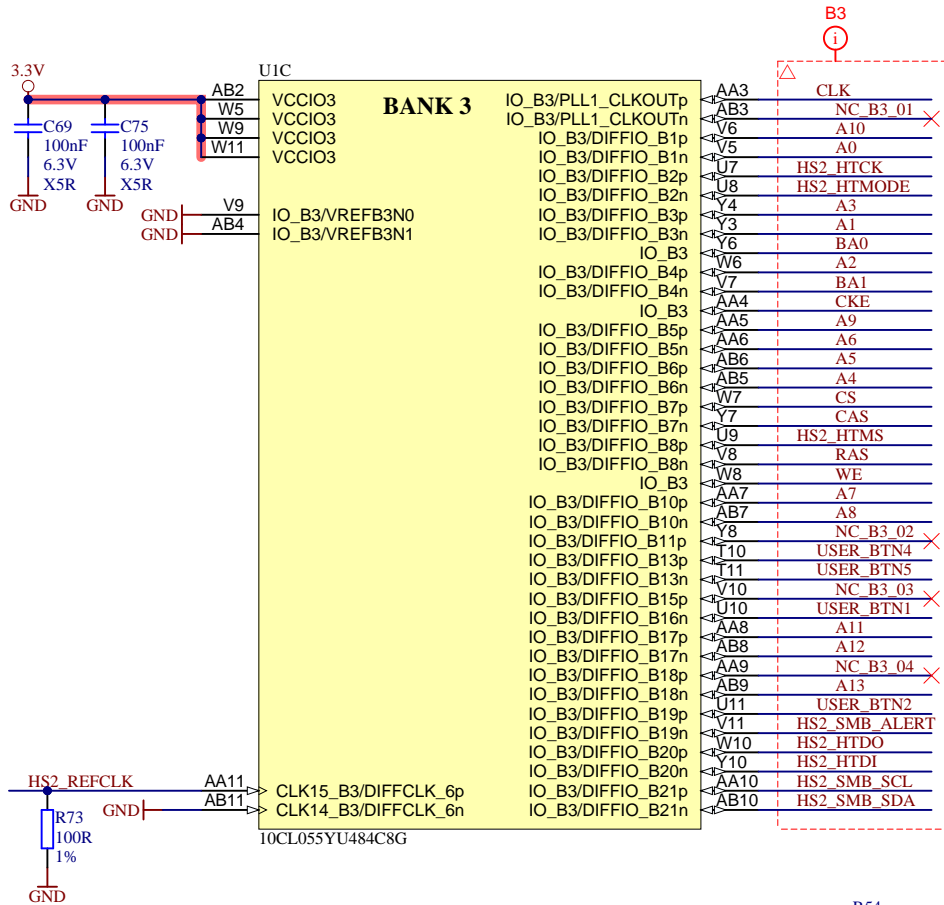

LOGO1
TE Logo PRINT Layer
LOGO PRINT

MECH14
TE Address Overlay
LOGO ADDRESS



Serial
Serialnumber 6,3 x 6,3mm

		Title: CR00109	
		A4	Number: CR00109 QHCN-A
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Title: CR00109		
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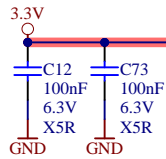
4

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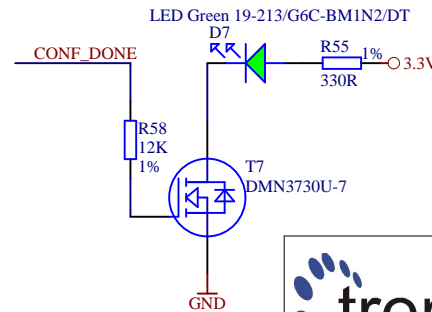
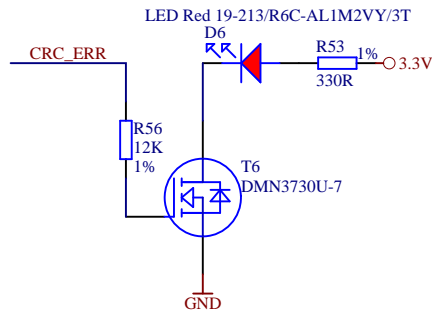
UIE

BANK 5

- VCCIO5
- VCCIO5
- VCCIO5
- IO_B5
- IO_B5/DIFFIO_R18p
- IO_B5/DIFFIO_R18n
- IO_B5/DIFFIO_R19p
- IO_B5/DIFFIO_R19n
- IO_B5/DEV_CLRn/DIFFIO_R20p
- IO_B5/DEV_OE/DIFFIO_R20n
- IO_B5/DIFFIO_R21p
- IO_B5/DIFFIO_R21n
- IO_B5/DIFFIO_R22p
- IO_B5/DIFFIO_R22n
- IO_B5/DIFFIO_R23p
- IO_B5/DIFFIO_R23n
- IO_B5/DIFFIO_R24p
- IO_B5/DIFFIO_R24n
- IO_B5/DIFFIO_R25p
- IO_B5/DIFFIO_R25n
- IO_B5/DIFFIO_R26p
- IO_B5/DIFFIO_R26n
- IO_B5/DIFFIO_R27p
- IO_B5/DIFFIO_R27n
- IO_B5/DIFFIO_R28p
- IO_B5/DIFFIO_R28n
- IO_B5/DIFFIO_R29p
- IO_B5/DIFFIO_R29n
- IO_B5/DIFFIO_R30p
- IO_B5/DIFFIO_R30n
- IO_B5/DIFFIO_R31p
- IO_B5/DIFFIO_R31n
- IO_B5/DIFFIO_R32p
- IO_B5/DIFFIO_R32n
- IO_B5/DIFFIO_R34p
- IO_B5/DIFFIO_R34n
- IO_B5/DIFFIO_R35p
- IO_B5/DIFFIO_R35n
- IO_B5
- IO_B5/RDN3
- IO_B5/RUP3
- IO_B5/DIFFIO_R36p
- IO_B5/DIFFIO_R36n

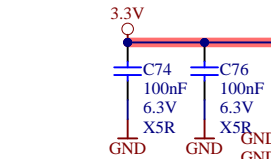
- M16 ETH2_RXD2
- M19 ETH2_RXD1
- M20 ETH2_RXD0
- M21 ETH2_RST
- M22 ETH2_TXD2
- N21 RST_GPIO
- N22 ETH2_TXD3
- N18 ETH2_MDC
- N17 ETH2_INTRP
- N19 ETH2_RXD3
- N20 ETH2_TXD1
- P21 ETH2_COL
- P22 ETH2_CRS
- R21 ETH2_TXD0
- R22 ETH2_TXEN
- N16 ETH2_TXC
- R19 ETH1_RST
- R18 ETH2_RXDV
- U21 ETH1_TXC
- U22 ETH1_INTRP
- R20 ETH1_CRS
- V21 ETH1_RXER
- V22 ETH1_RXC
- P17 ETH2_RXER
- R17 ETH2_RXC
- T19 ETH1_COL
- T20 ETH1_TXD3
- W21 ETH1_RXDV
- W22 ETH1_RXD0
- J19 ETH1_TXD2
- U20 ETH1_TXD1
- Y21 ETH1_RXD2
- Y22 ETH1_RXD3
- W20 ETH1_RXD1
- T18 ETH1_TXEN
- T17 ETH1_TXD0
- AA21 ETH1_MDIO
- AA22 ETH1_MDC

10CL055YU484C8G



- TP16 INIT_DONE Testpoint 0.8mm THT
- TP17 CRC_ERR Testpoint 0.8mm THT
- TP18 CONF_DONE Testpoint 0.8mm THT

VREF not used -> GND

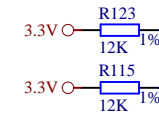
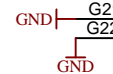
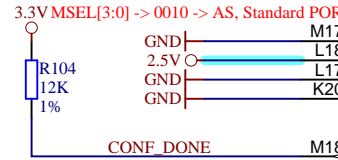


UIF

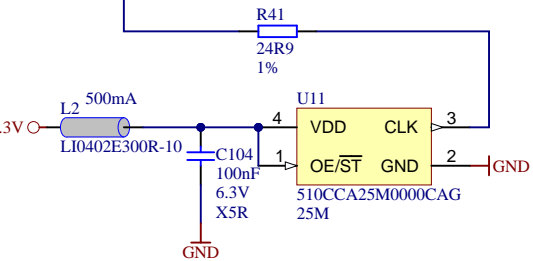
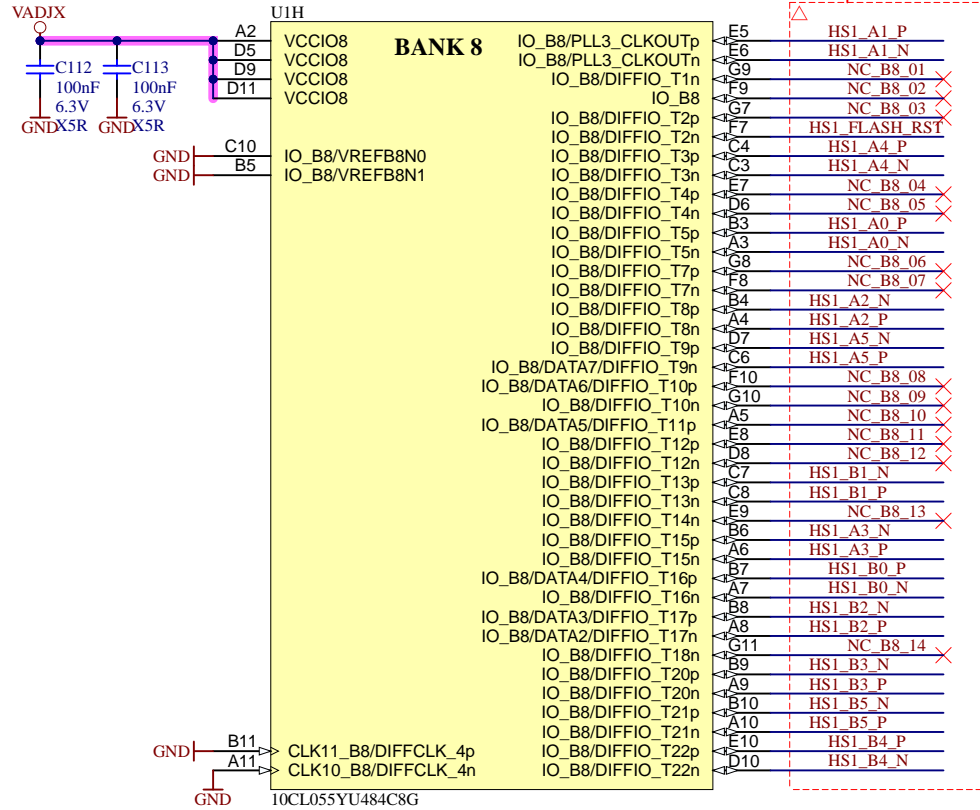
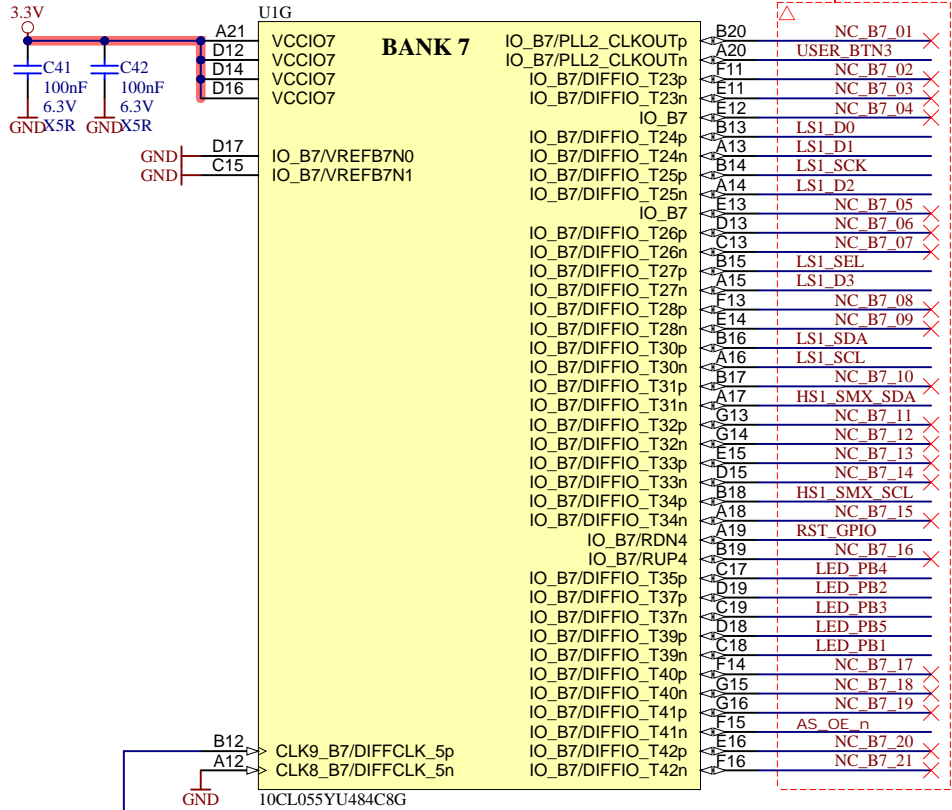
BANK 6

- VCCIO6
- VCCIO6
- VCCIO6
- IO_B6/DIFFIO_R1p
- IO_B6/DIFFIO_R1n
- IO_B6/DIFFIO_R2p
- IO_B6/DIFFIO_R2n
- IO_B6/DIFFIO_R3p
- IO_B6/DIFFIO_R3n
- IO_B6/DIFFIO_R4p
- IO_B6/DIFFIO_R4n
- IO_B6/DIFFIO_R5p
- IO_B6/DIFFIO_R5n
- IO_B6/DIFFIO_R6p
- IO_B6/DIFFIO_R6n
- IO_B6/DIFFIO_R7p
- IO_B6/DIFFIO_R7n
- IO_B6
- IO_B6/DIFFIO_R8p
- IO_B6/DIFFIO_R8n
- IO_B6/DIFFIO_R9p
- IO_B6/DIFFIO_R9n
- IO_B6
- IO_B6/DIFFIO_R10p
- IO_B6/DIFFIO_R10n
- IO_B6/DIFFIO_R11p
- IO_B6/DIFFIO_R11n
- IO_B6/DIFFIO_R12n
- IO_B6/DIFFIO_R13p
- IO_B6/DIFFIO_R13n
- IO_B6/DIFFIO_R14p
- IO_B6/DIFFIO_R14n
- IO_B6/DIFFIO_R15p
- IO_B6/DIFFIO_R15n
- IO_B6/CLKUSR/DIFFIO_R16p
- IO_B6/nCEO/DIFFIO_R16n
- IO_B6/CRC_ERROR/DIFFIO_R17p
- IO_B6/INIT_DONE/DIFFIO_R17n

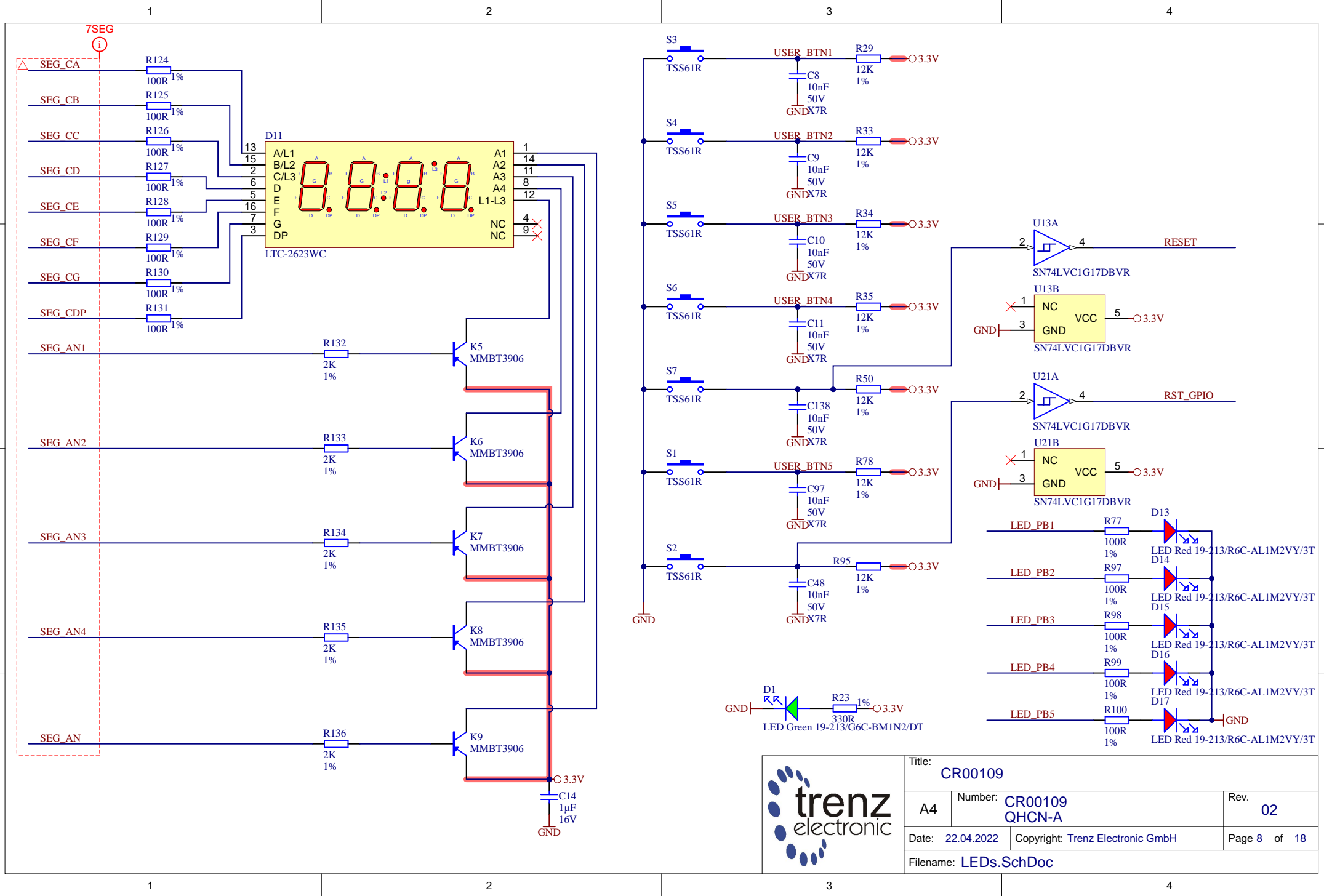
- G17 SEG_CC
- F17 I2C_SDA
- D20 I2C_SCL
- C20 BDBUS0
- B21 BDBUS1
- B22 BDBUS2
- C21 BDBUS3
- C22 BDBUS4
- H17 SEG_CB
- G18 SEG_CD
- F19 SEG_CF
- F20 SEG_AN
- D21 BDBUS5
- D22 BDBUS6
- H16 SEG_AN4
- E21 BDBUS7
- E22 BCBUS0
- H19 SEG_CDP
- H20 SEG_AN1
- J17 SEG_CA
- J19 BCBUS7
- J20 SEG_AN3
- F21 BCBUS1
- F22 BCBUS2
- J18 SEG_CG
- K18 SEG_CE
- K17 SEG_AN2
- H21 BCBUS3
- H22 BCBUS4
- J21 BCBUS5
- J22 BCBUS6
- K21 NC_B6[0]
- K22 CRC_ERR
- L21 INIT_DONE
- L22 INIT_DONE




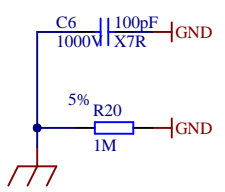
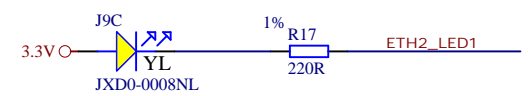
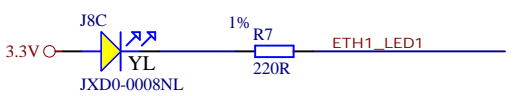
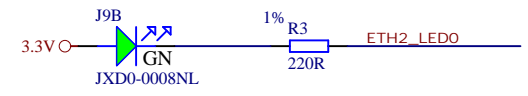
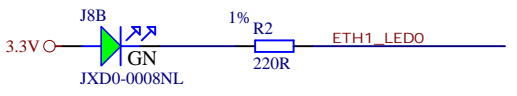
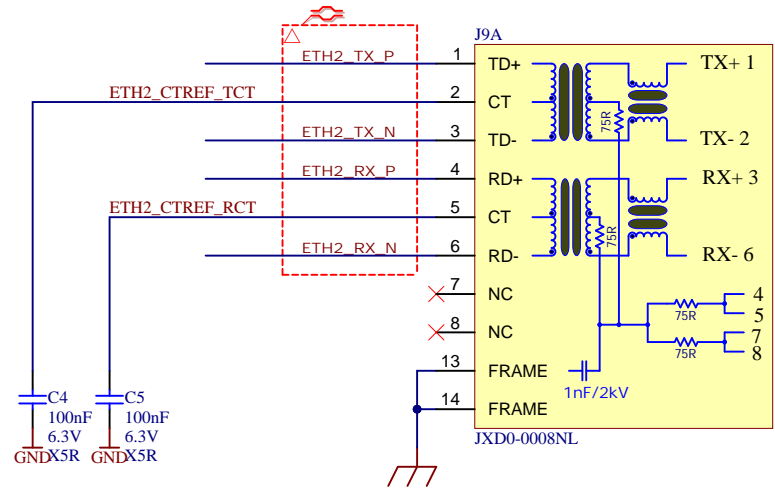
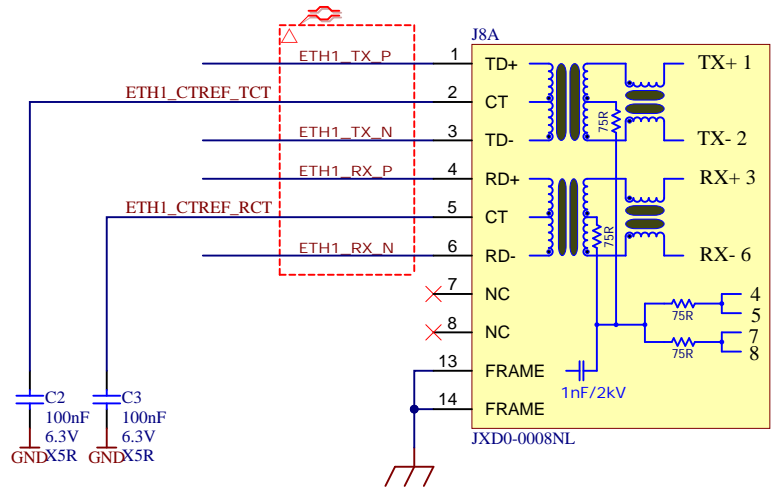
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Date: 22.04.2022	Copyright: Trenz Electronic GmbH	Page 5 of 18
Filename: FPGA3.SchDoc		



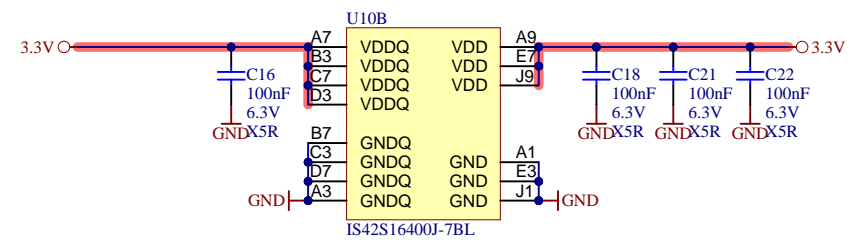
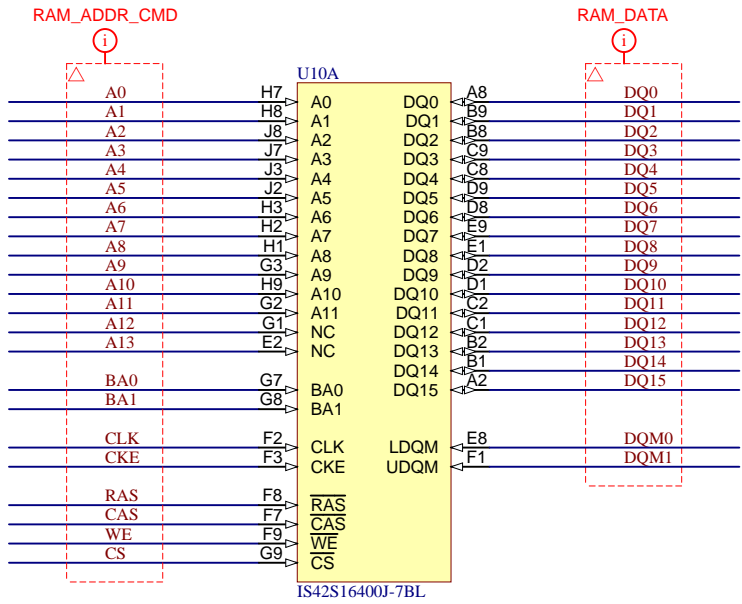
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Date: 22.04.2022	Copyright: Trenz Electronic GmbH	Page 6 of 18
Filename: FPGA4.SchDoc		




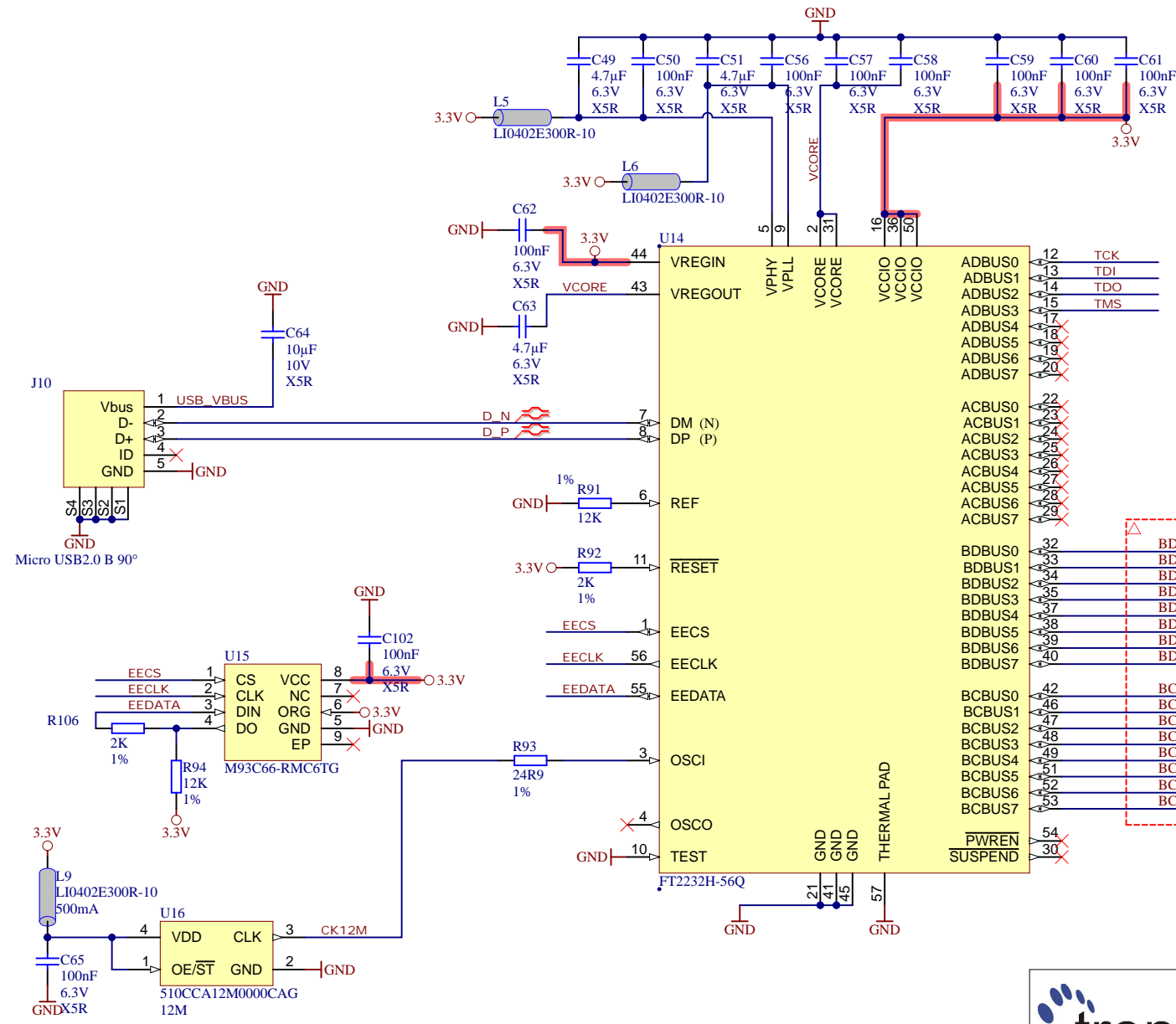
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Filename: Ethernet.SchDoc		



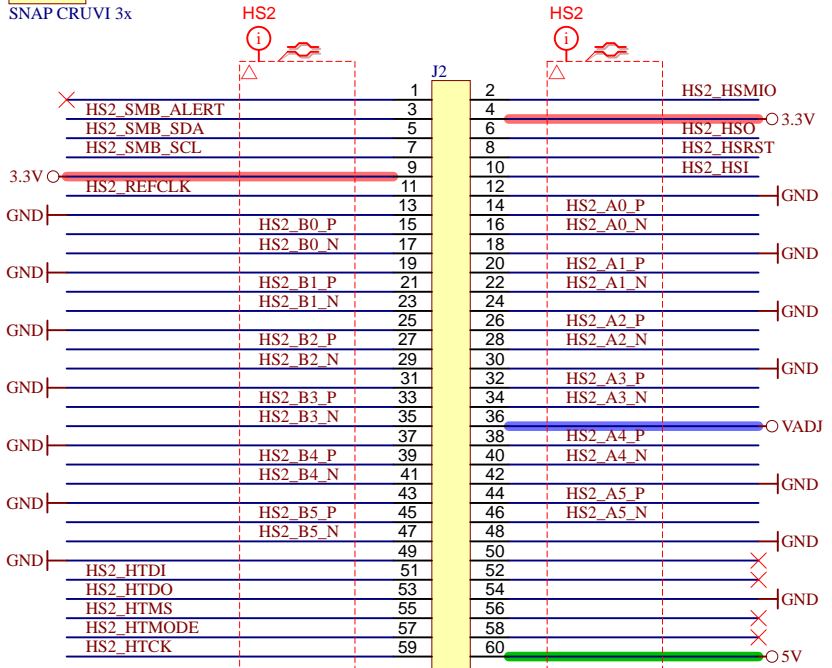
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Date: 22.04.2022		Copyright: Trenz Electronic GmbH	
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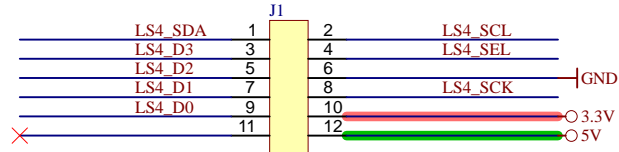
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Filename: FTDI.SchDoc		

SNAP1

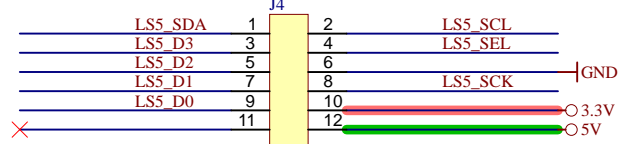
SNAP CRUVI 3x



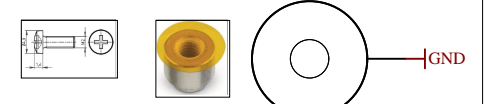
SS4-30-3.50-L-D-K-TR



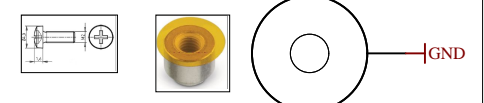
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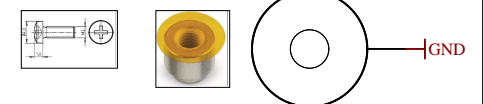
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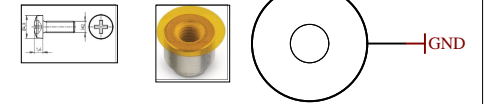
Screw M2x6 Steel Spacer M2 5mm SMD



Screw M2x6 Steel Spacer M2 5mm SMD



Screw M2x6 Steel Spacer M2 5mm SMD



Screw M2x6 Steel Spacer M2 5mm SMD



Screw M2x6 Steel Spacer M2 5mm SMD

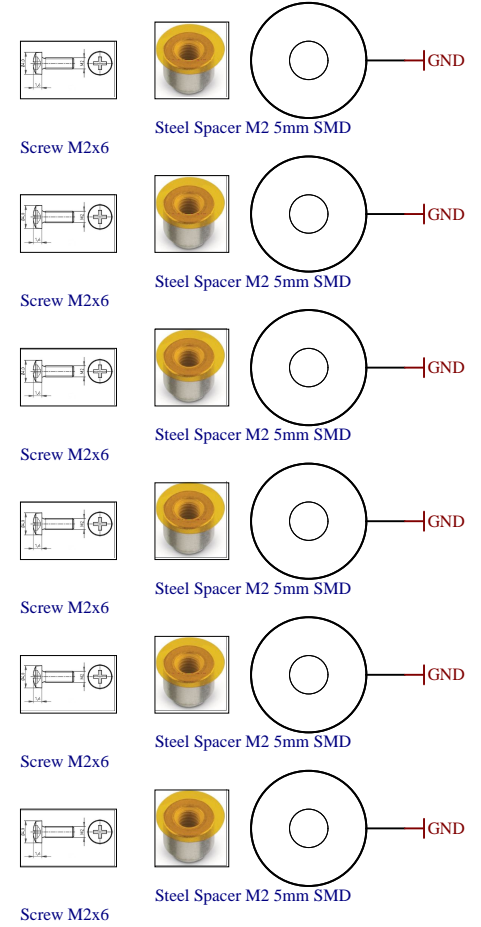
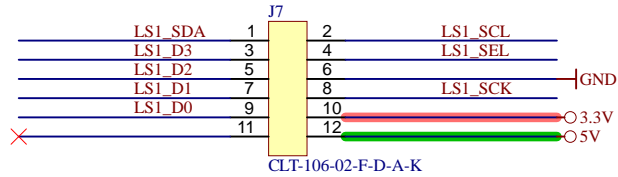
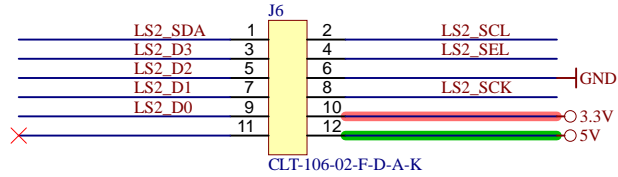
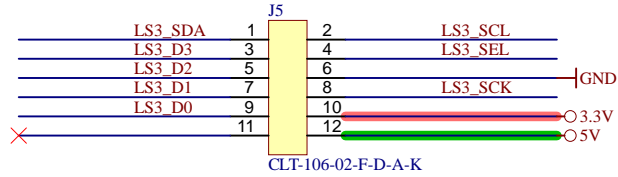



Screw M2x6 Steel Spacer M2 5mm SMD



Title: CR00109		
A4	Number: CR00109 QHCN-A	Rev. 02
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SNAP2
SNAP CRUVI 3x



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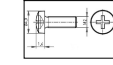
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SNAP3



SNAP CRUVI 3x

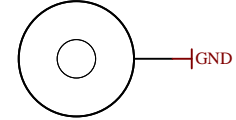
Special SLOT for SemperFlash boot and dual voltage operation



Screw M2x6



Steel Spacer M2 5mm SMD

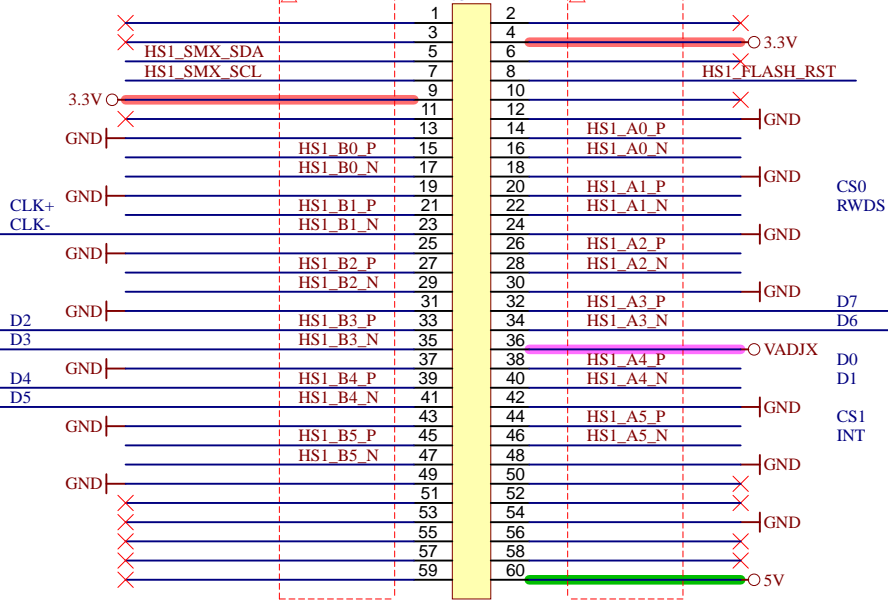


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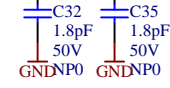
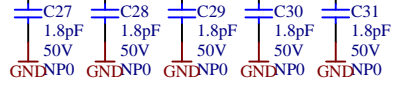
HS1

HS1

J3



SS4-30-3.50-L-D-K-TR



1

2

3

4

A

B

C

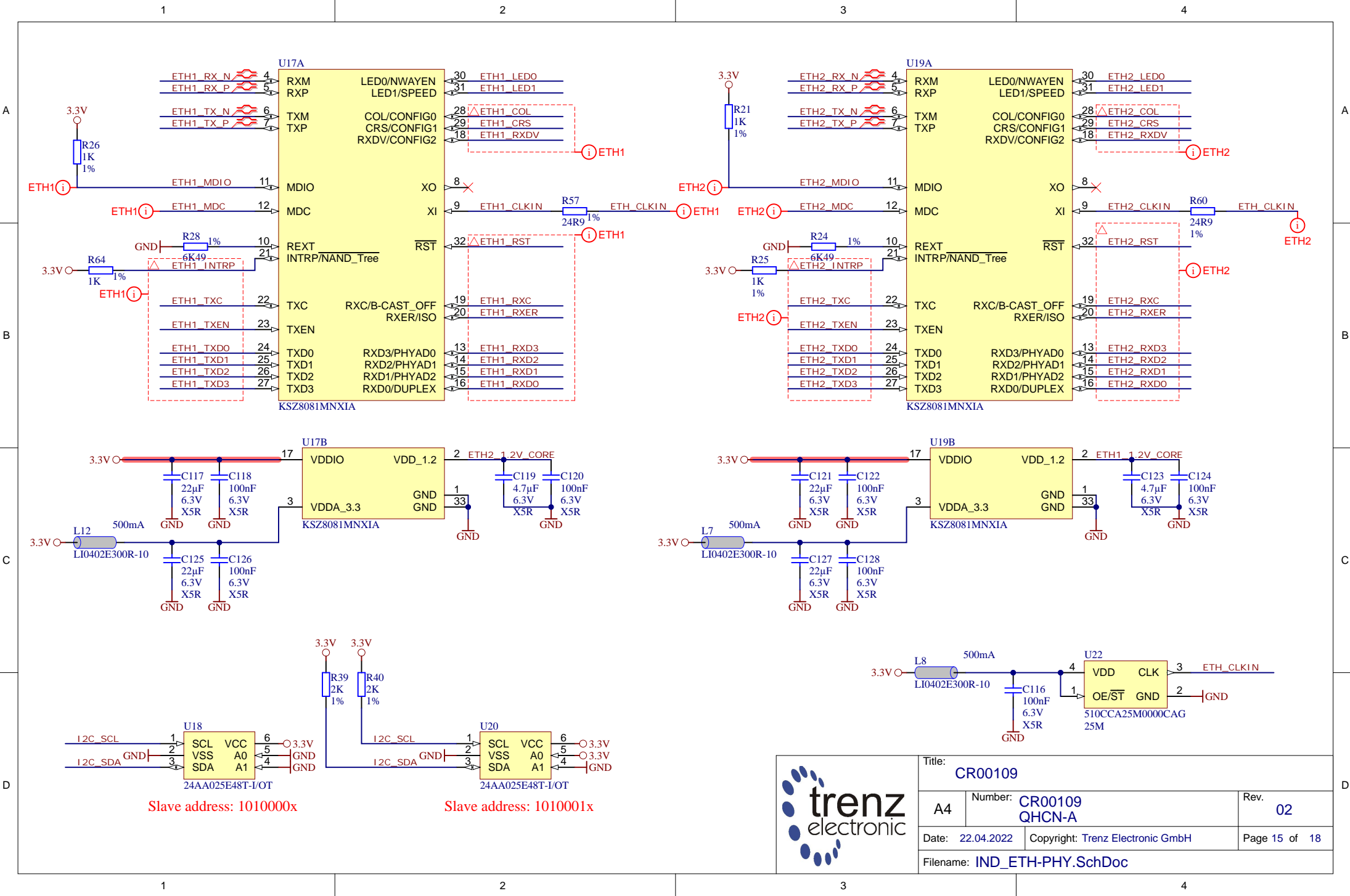
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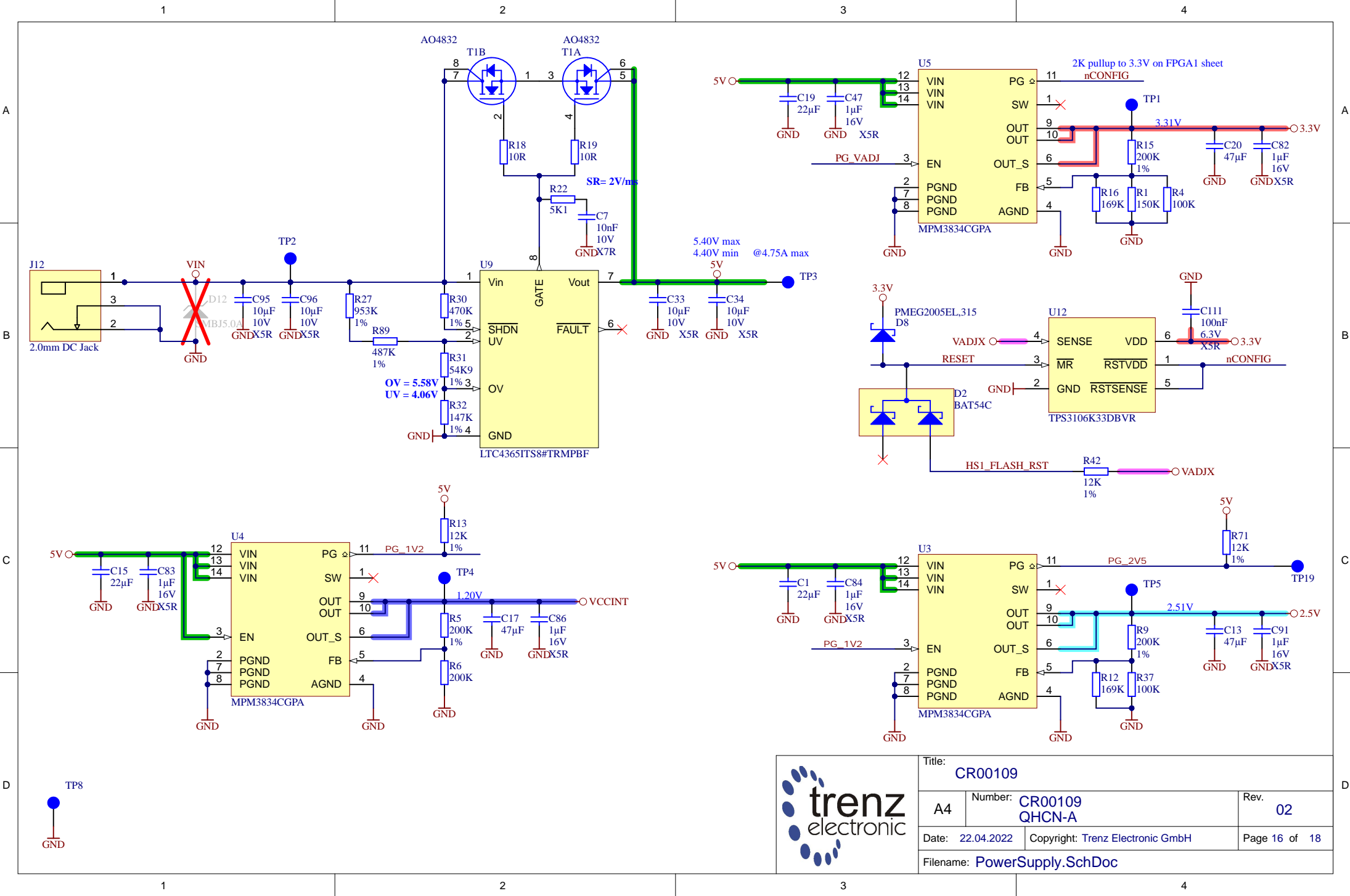
B


C

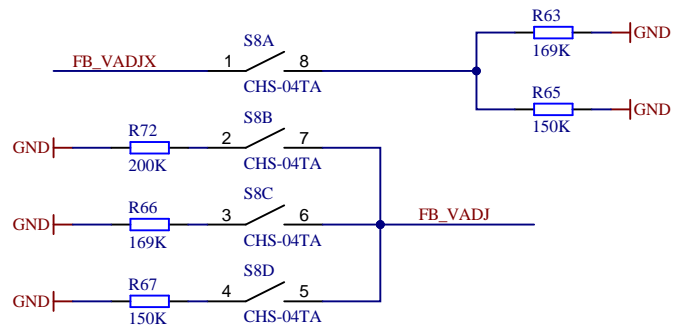
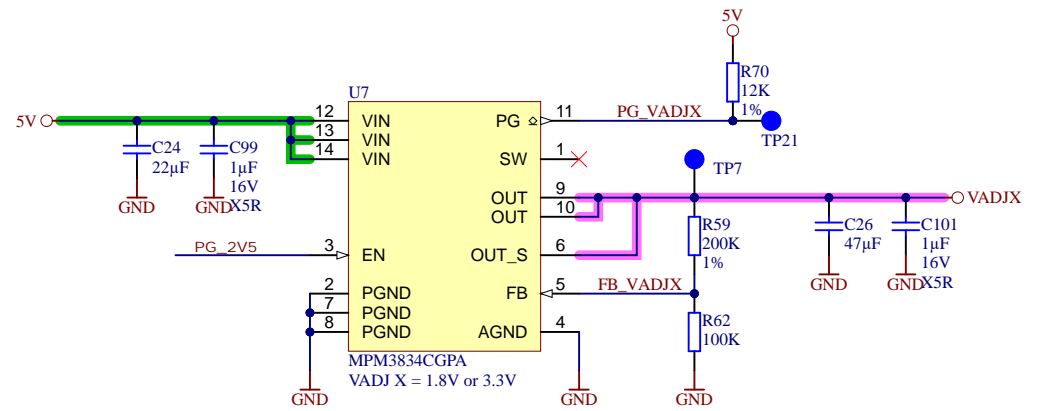
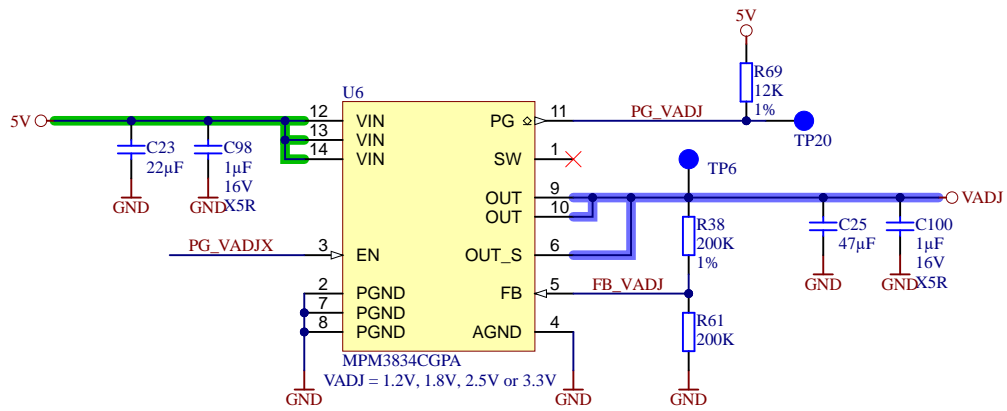

D

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	Filename: C-Headers-3.SchDoc	
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			Title: CR00109	
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Date: 22.04.2022		Copyright: Trenz Electronic GmbH		Page 16 of 18
Filename: PowerSupply.SchDoc				

Title: CR00109		
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Filename: PowerSupplyAdj.SchDoc		

REV	Description	
-01	Initial revision	IG
-02	<ol style="list-style-type: none"> 1. U4 (1.2V), U5(3.3V) changed to MPM3834C 2. R96 changed to 2K 3. U3 (2.5V) changed to MPM3834C 4. U6, U7 (VADJX, VADJ) changed to MPM3834C 5. Moved selection Dips for VADJ to S8-3&4 6. USB connector J10 changed to 629105150521 7. Transistor T2 changed to DMN3730U-7 8. R14 changed to 2K Ohm 9. Added series Resistor R44 12K Ohm on conf done 10. Added pullup R45 12K OHM on AS_NCS 11. Added FLASH_RST on bank 8 pin F7. 12. U2: Text note about possible option SN74AXC4T774RSVR added 13. Added C36 and C37 100nF decoupling for U2 14. Added decoupling capacitor C102 to EEPROM U15 15. Added decoupling capacitor and inductor to clocks U8 and U11 16. Added THT tespoints for AS_DATA0, AS_ASDO, AS_NCS, AS_DCLK, and AS_OE_N, CRC_ERR, INIT_DONE, NSTATUS, NCONFIG, CONF_DONE 17. Added LED indicator for CRC_ERR, INIT_DONE, NSTATUS, NCONFIG, CONF_DONE, AS_OE_N 18. Switched some parts (K5 - K9, R124- R136, C14) from bottom to top and moved away from THT pins to be compatible with selective soldering process 19. Update from library 20. Renamed unused Netlables for better readability 21. Added legal notices page sheet and content 22. Added block diagram on CR00109 sheet 23. Added power structure and sequencing on CR00109 sheet 24. Added revision changes sheet and content 25. Updated silkscreen with descriptions for better usability, including description for Dips (voltage selection) 26. Changed HS2_REFCLK signal pin at FPGA from AA9 to AA11 (clock capable) and added parallel termination R73 to GND. 	MR

	Title: CR00109		
	A4	Number: CR00109 QHCHN-A	Rev. 02
	Date: 22.04.2022	Copyright: Trenz Electronic GmbH	Page 18 of 18
	Filename: Revision Changes.SchDoc		