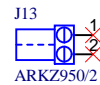
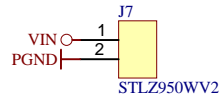
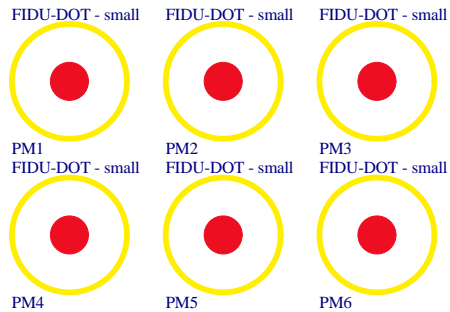
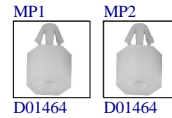
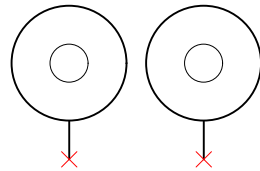


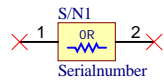
ACQCURR_A
ACQCURR_A.SchDoc
ACQCURR_B
ACQCURR_B.SchDoc
ACQVOLTAGE
ACQVOLTAGE.SchDoc
ENCODER
ENCODER.SchDoc
Comparator
Comparator.SchDoc
Power_Protection_1
Power_Protection_1.SchDoc
Power
Power.SchDoc
DRIVER
DRIVER.SchDoc

FPGA
FPGA.SchDoc
CRUVI
CRUVI.SchDoc

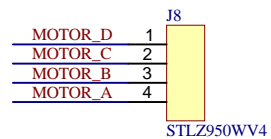
Mount.Hole 3.2mm Mount.Hole 3.2mm



MECHI
TE Address Overlay
LOGO ADDRESS



Serial1
Serial
Serialnumber 6,3 x 6.3mm

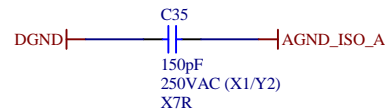
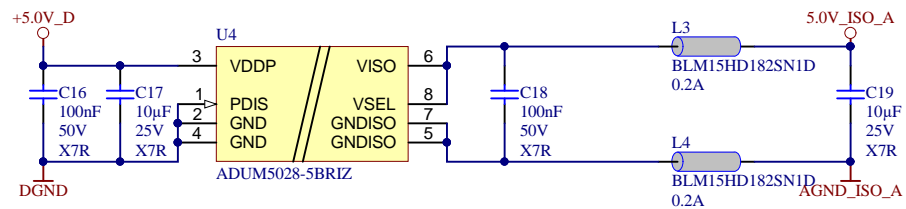
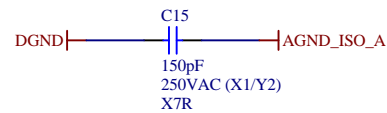
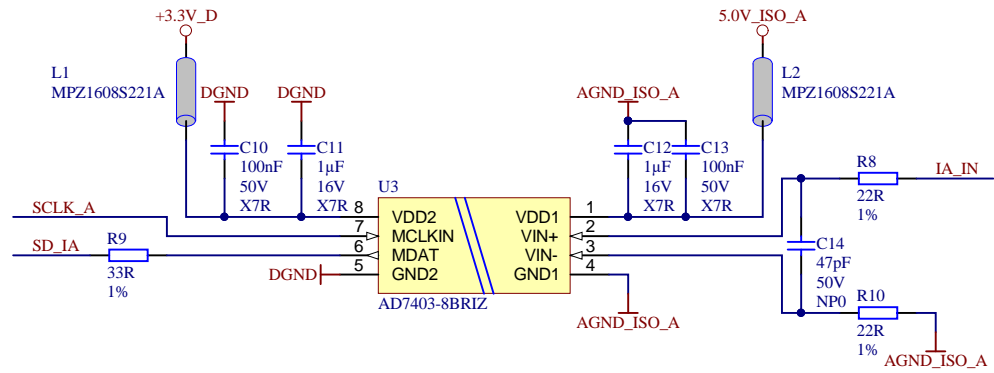



LOGO1
TE Logo PRINT Layer
LOGO PRINT

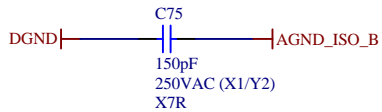
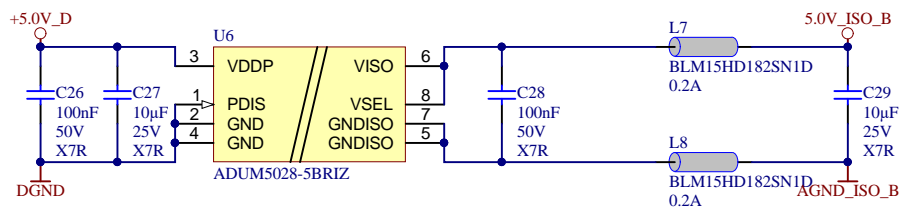
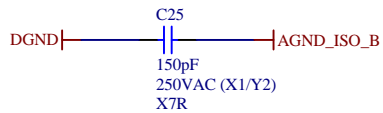
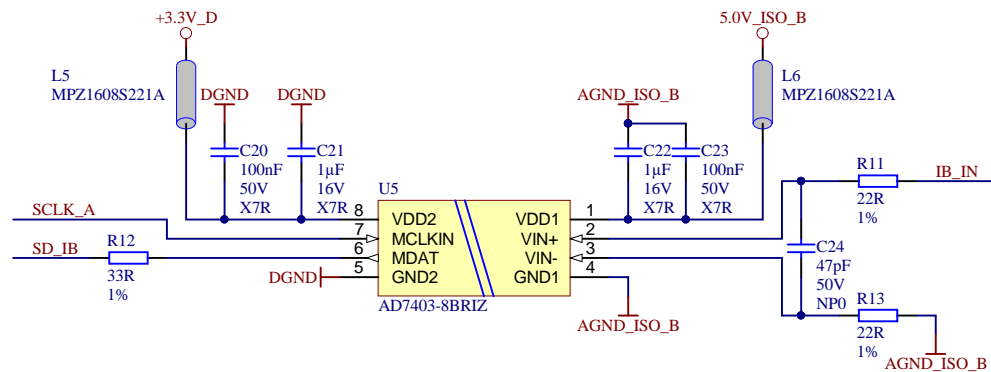
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Created by	MR
Modified by	MR
Modified at	2019-10-29
SVN Revision	



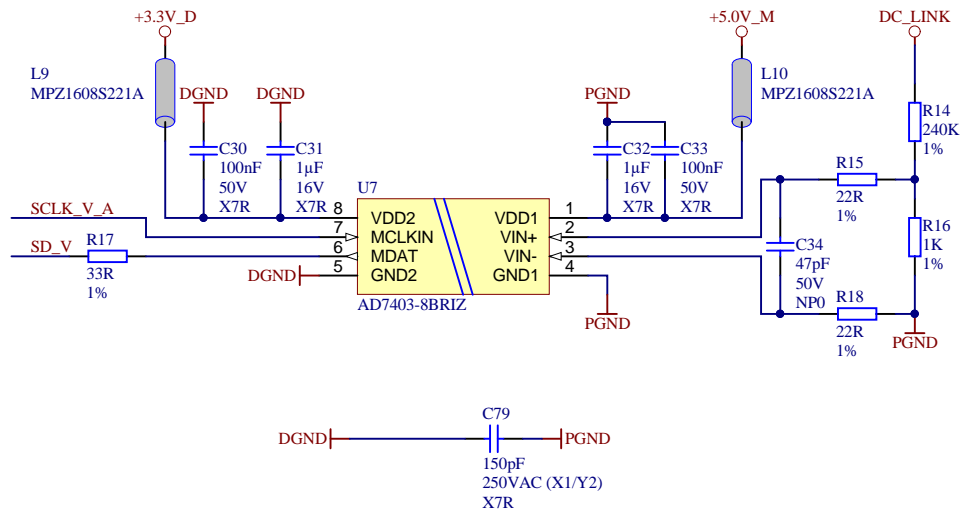
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A4	Number: CR00140 default	Rev. 02
Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 1 of 20
Drawn by:	Filename: CR00140.SchDoc	




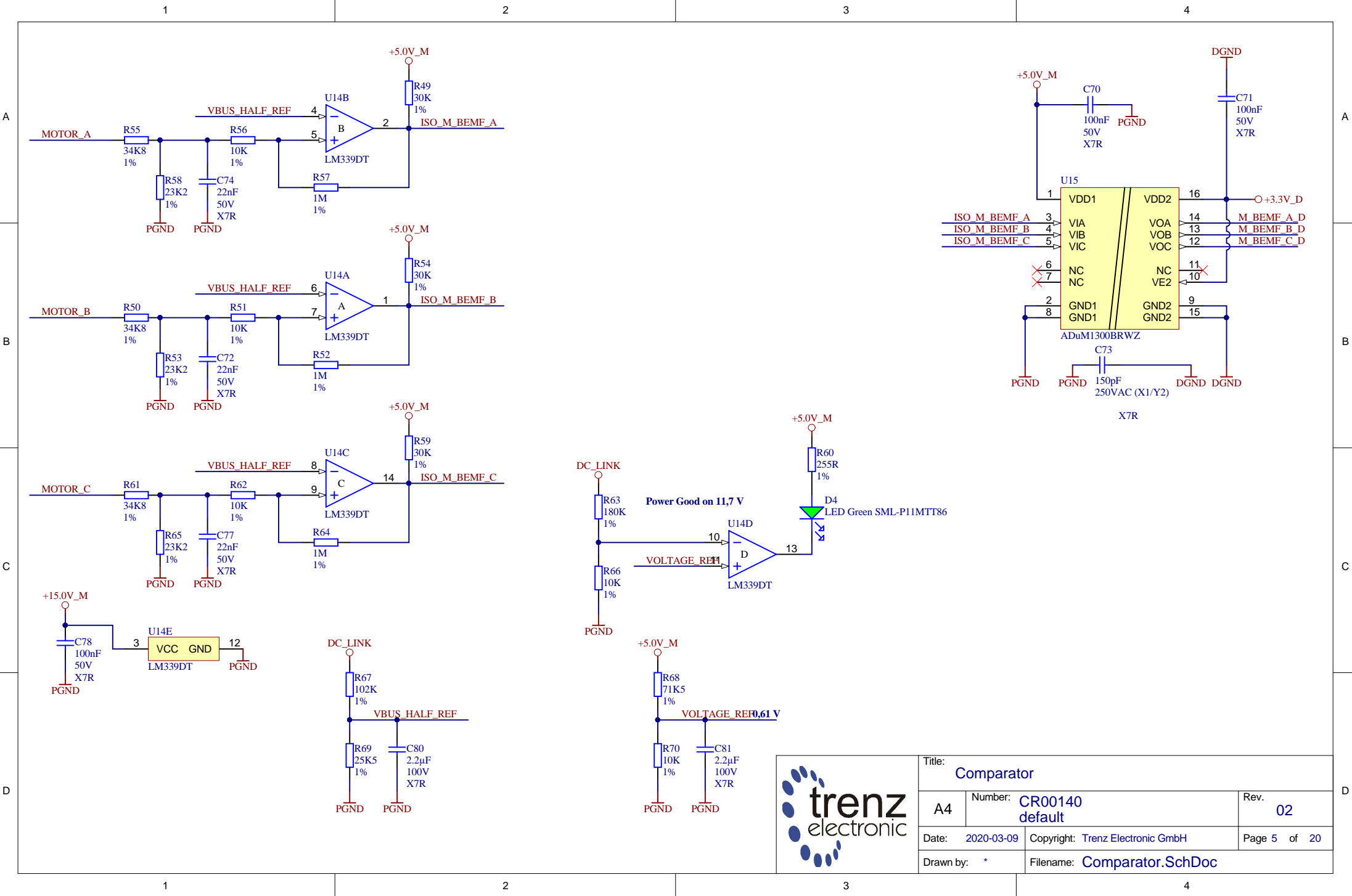
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	Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 2 of 20
	Drawn by: *	Filename: ACQCURR_A.SchDoc	



	Title: ACQCURR_B		
	A4	Number: CR00140 default	Rev. 02
	Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 3 of 20
	Drawn by: *	Filename: ACQCURR_B.SchDoc	



		Title: ACQVOLTAGE	
		A4	Number: CR00140 default
Date: 2020-03-09		Copyright: Trenz Electronic GmbH	
Page 4 of 20		Filename: ACQVOLTAGE.SchDoc	
Drawn by: *			



Title: Comparator		
A4	Number: CR00140 default	Rev. 02
Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 5 of 20
Drawn by: *	Filename: Comparator.SchDoc	

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4

DRIVER_A
DRIVER_A.SchDoc

DRIVER_B
DRIVER_B.SchDoc

DRIVER_C
DRIVER_C.SchDoc

DRIVER_D
DRIVER_D.SchDoc

A

A

B


B

C

C

D

D

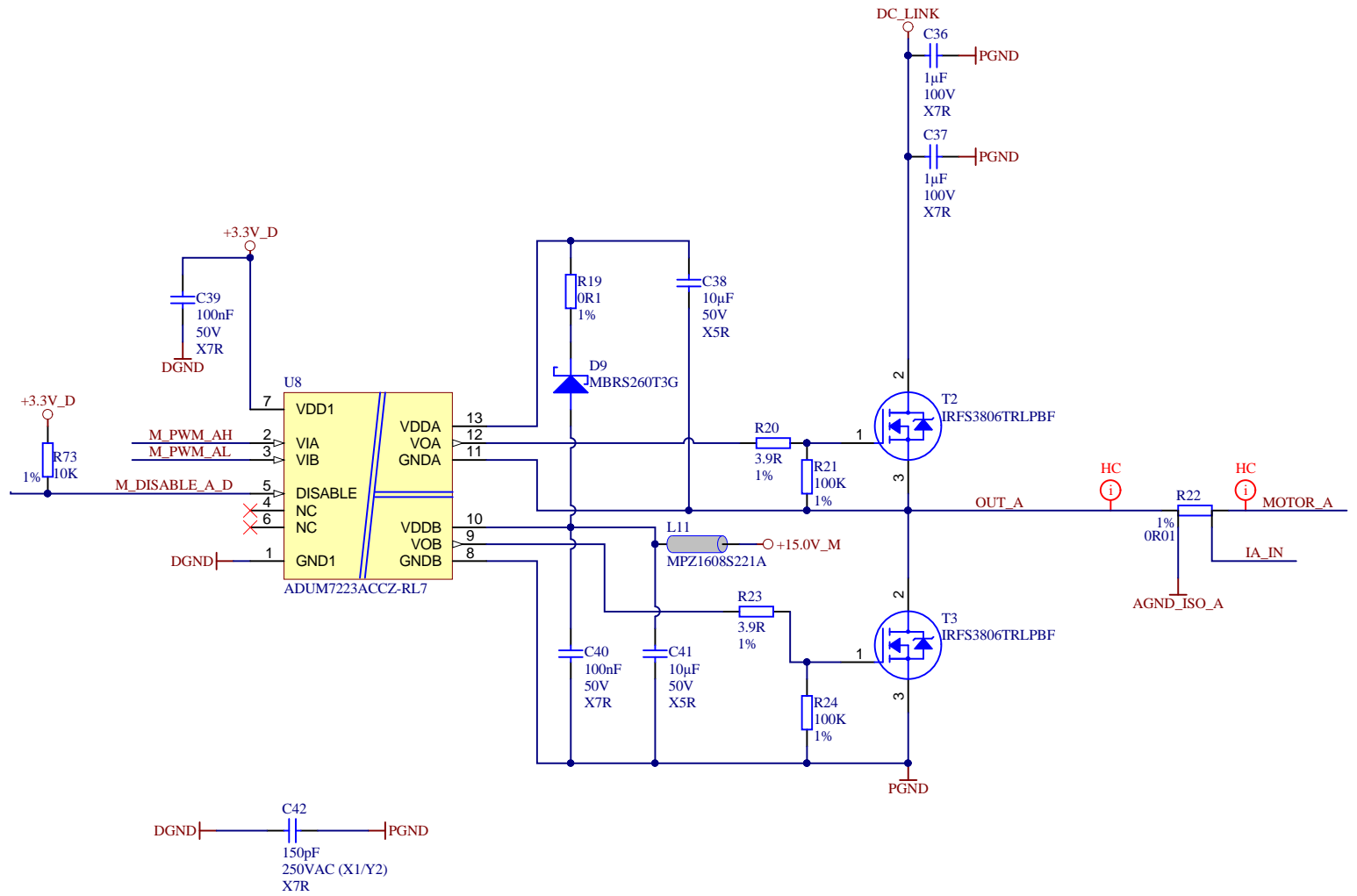
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	Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 6 of 20
	Drawn by: *	Filename: DRIVER.SchDoc	


1

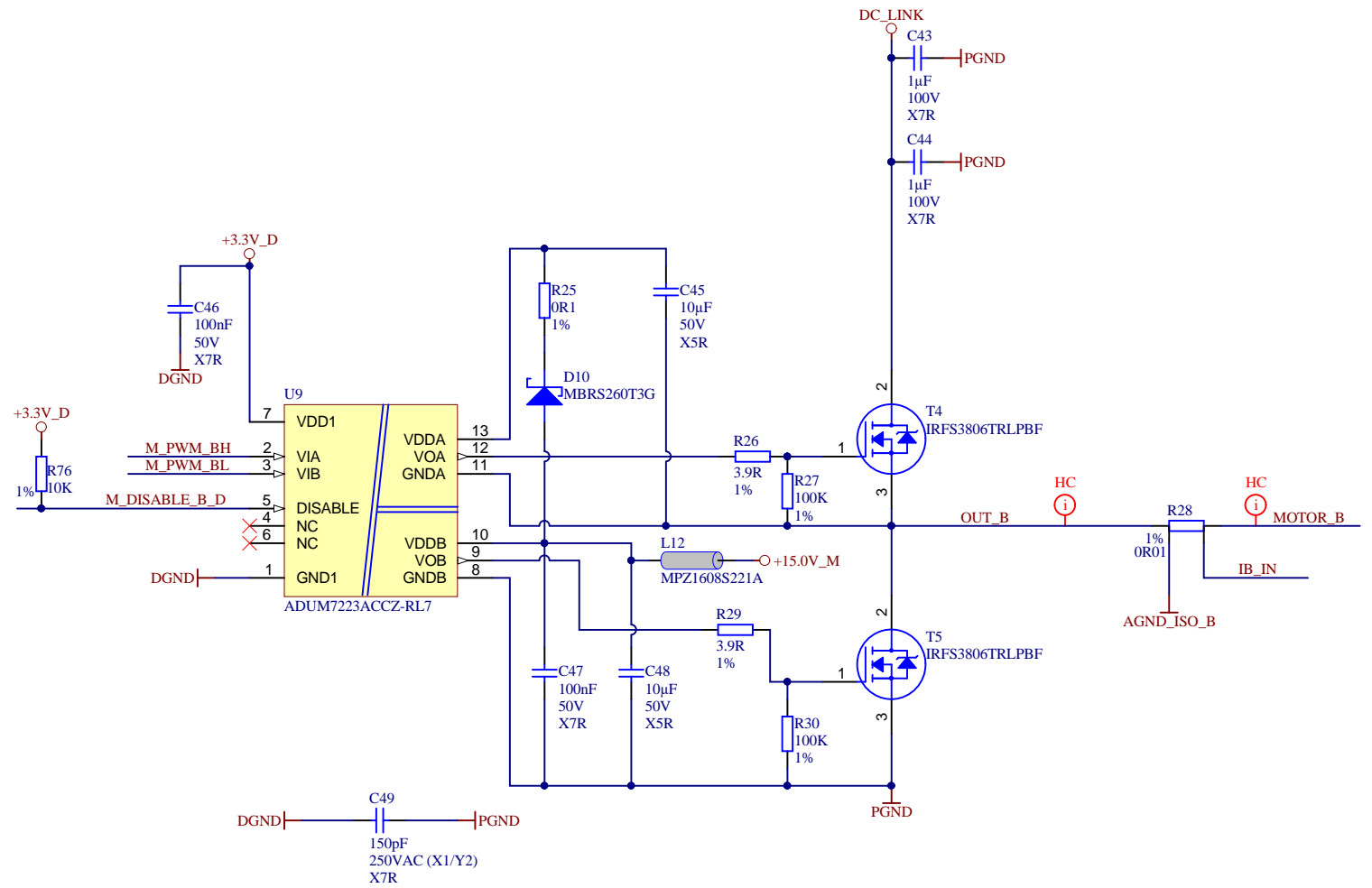
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3

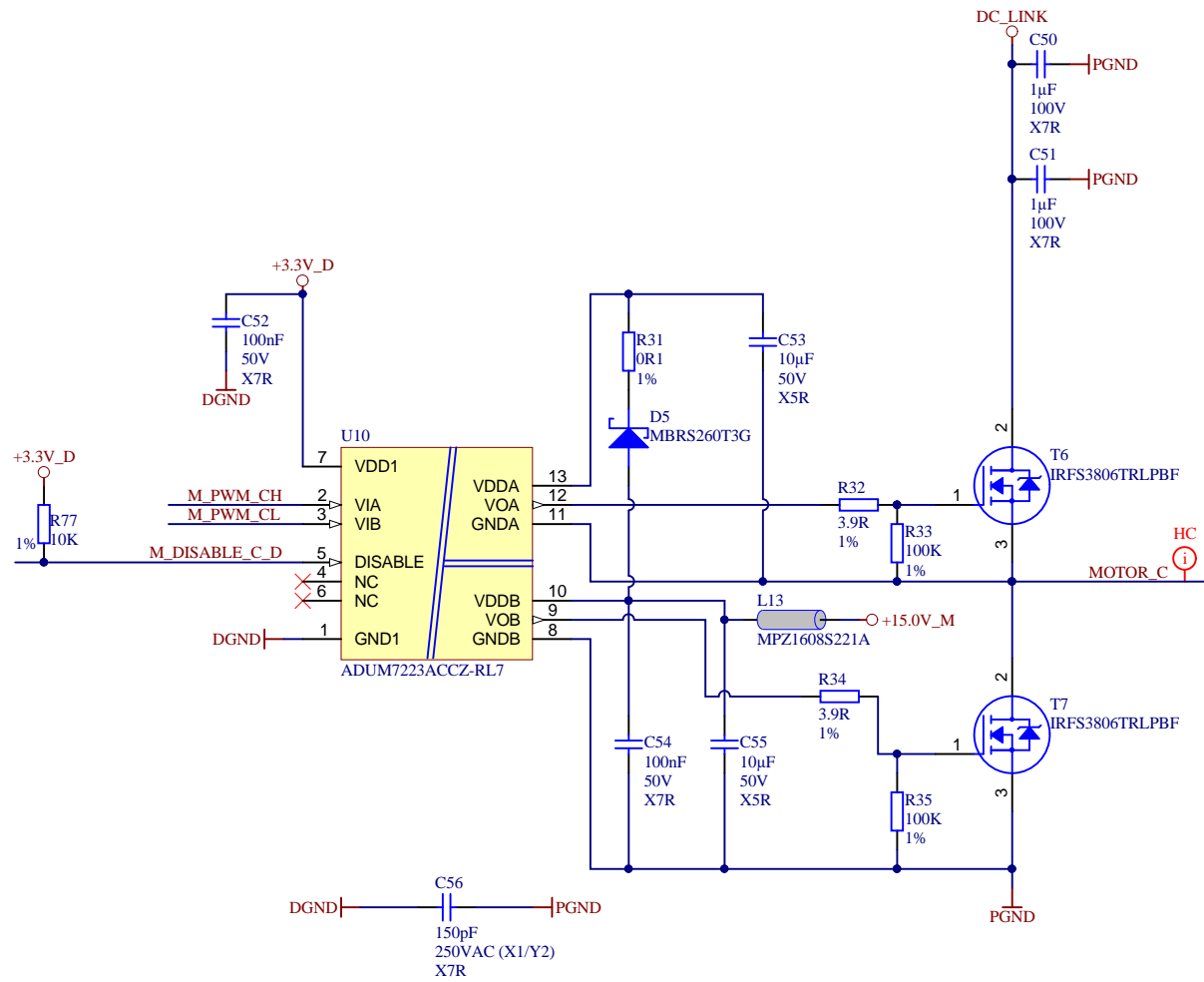
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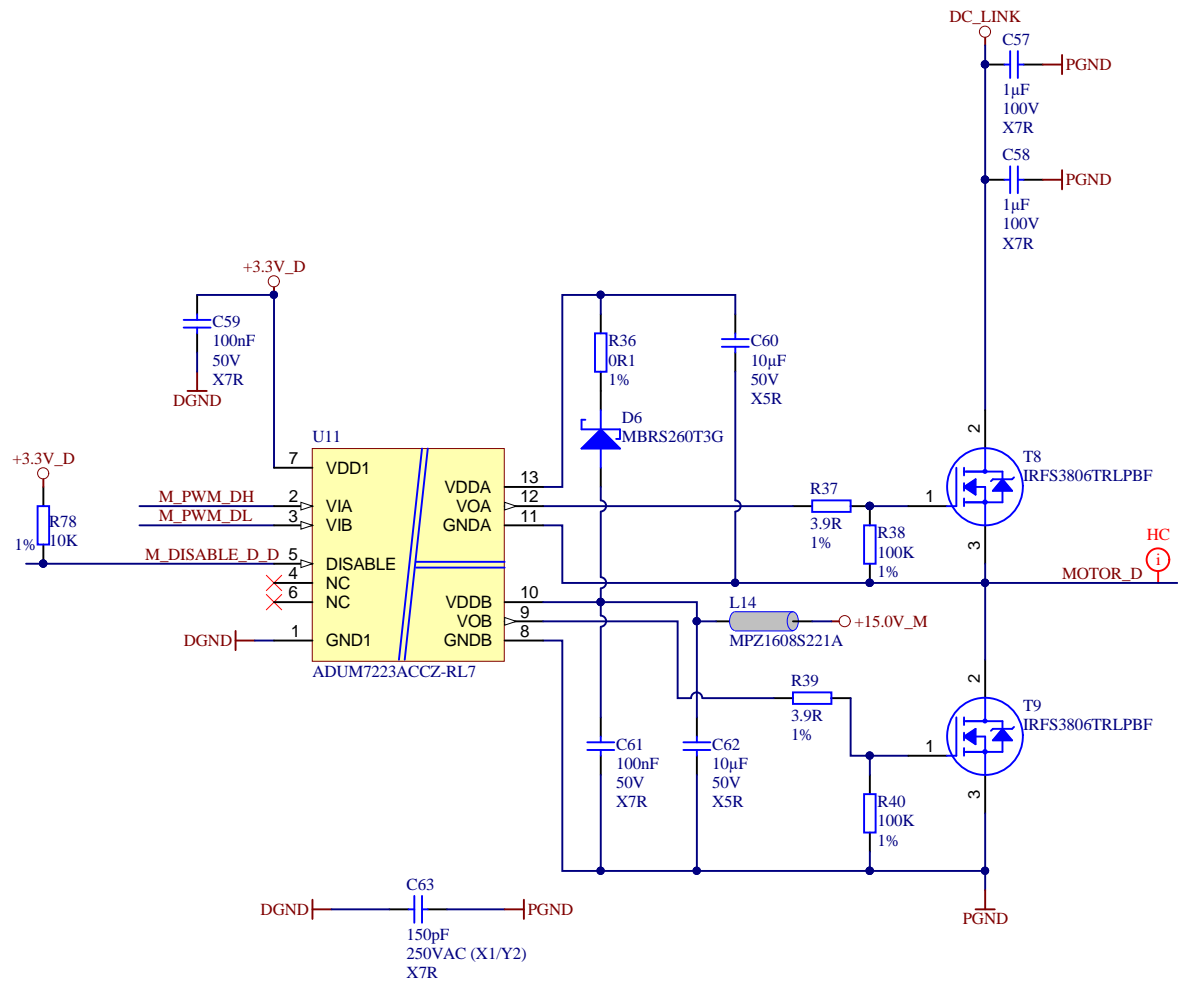
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	Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 7 of 20
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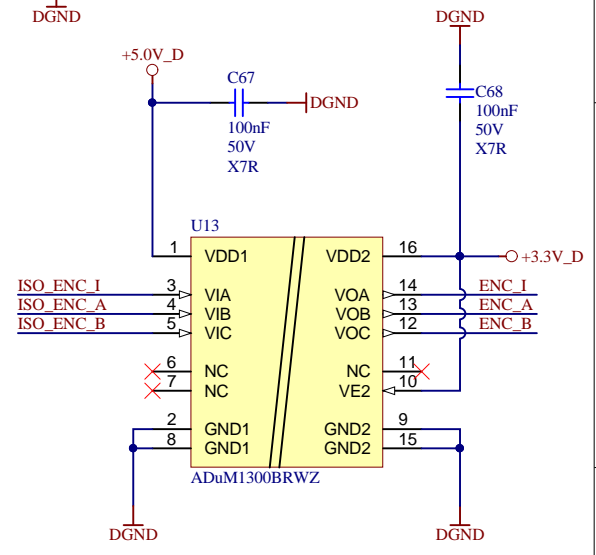
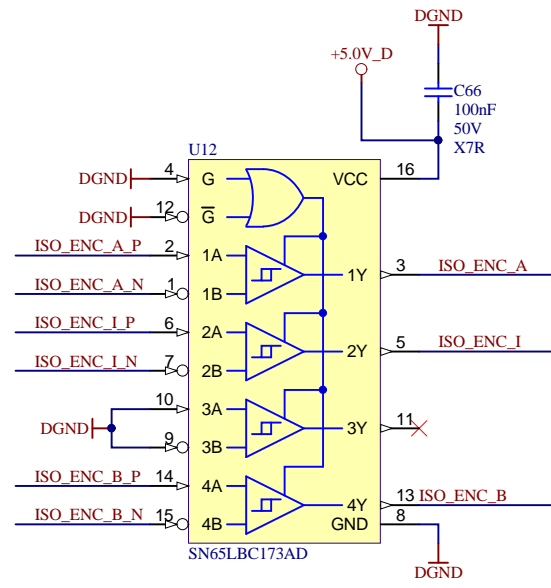
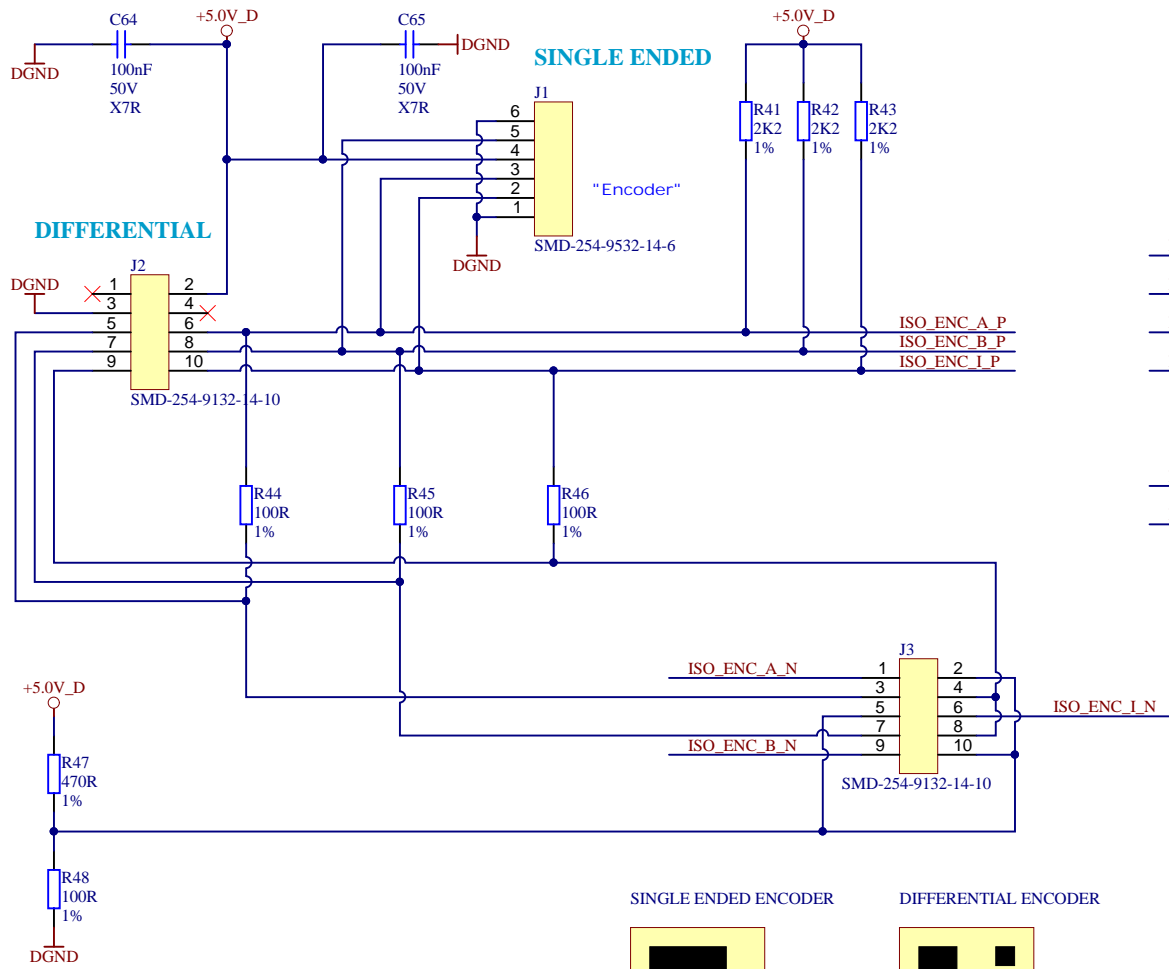
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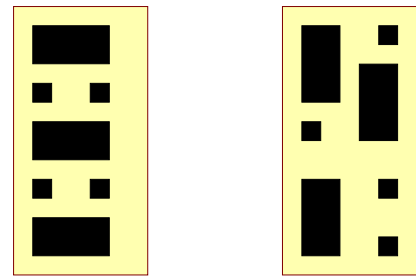
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Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 9 of 20
Drawn by: *	Filename: DRIVER_C.SchDoc	



Title: DRIVER_D		
A4	Number: CR00140 default	Rev. 02
Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 10 of 20
Drawn by: *	Filename: DRIVER_D.SchDoc	



SINGLE ENDED ENCODER DIFFERENTIAL ENCODER



			Title: ENCODER	
			A4	Number: CR00140 default
Date: 2020-03-09		Copyright: Trenz Electronic GmbH		Page 11 of 20
Drawn by: *		Filename: ENCODER.SchDoc		

1

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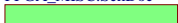
A

A

FPGA_Main
FPGA_Main.SchDoc



FPGA_MISC
FPGA_MISC.SchDoc



B


B

C

C

D

D

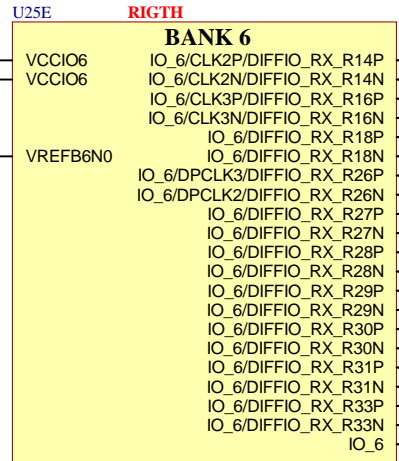
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	Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 12 of 20
	Drawn by: *	Filename: FPGA.SchDoc	

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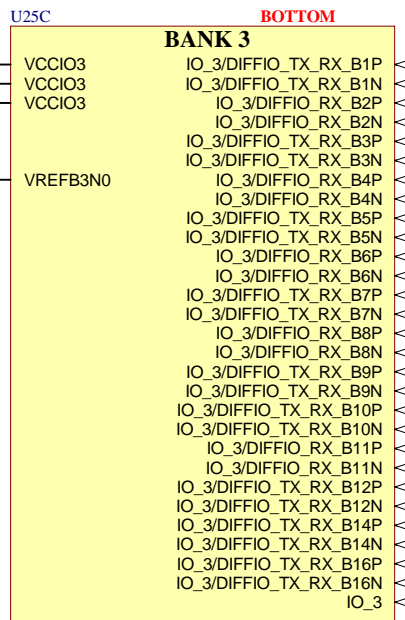
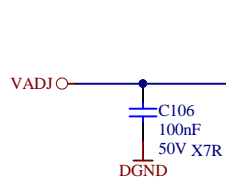
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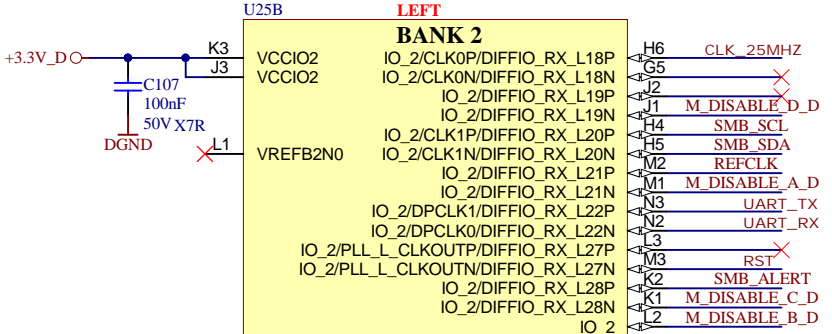
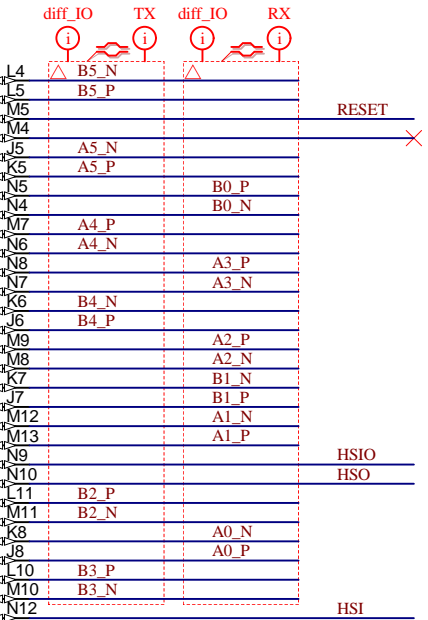


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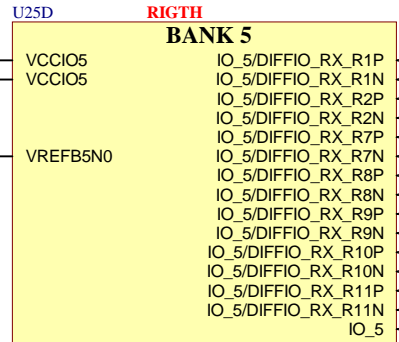
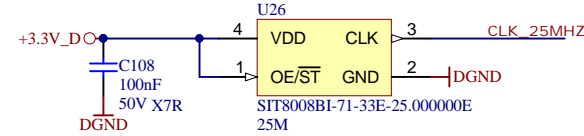
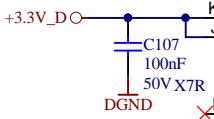


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Max10 View



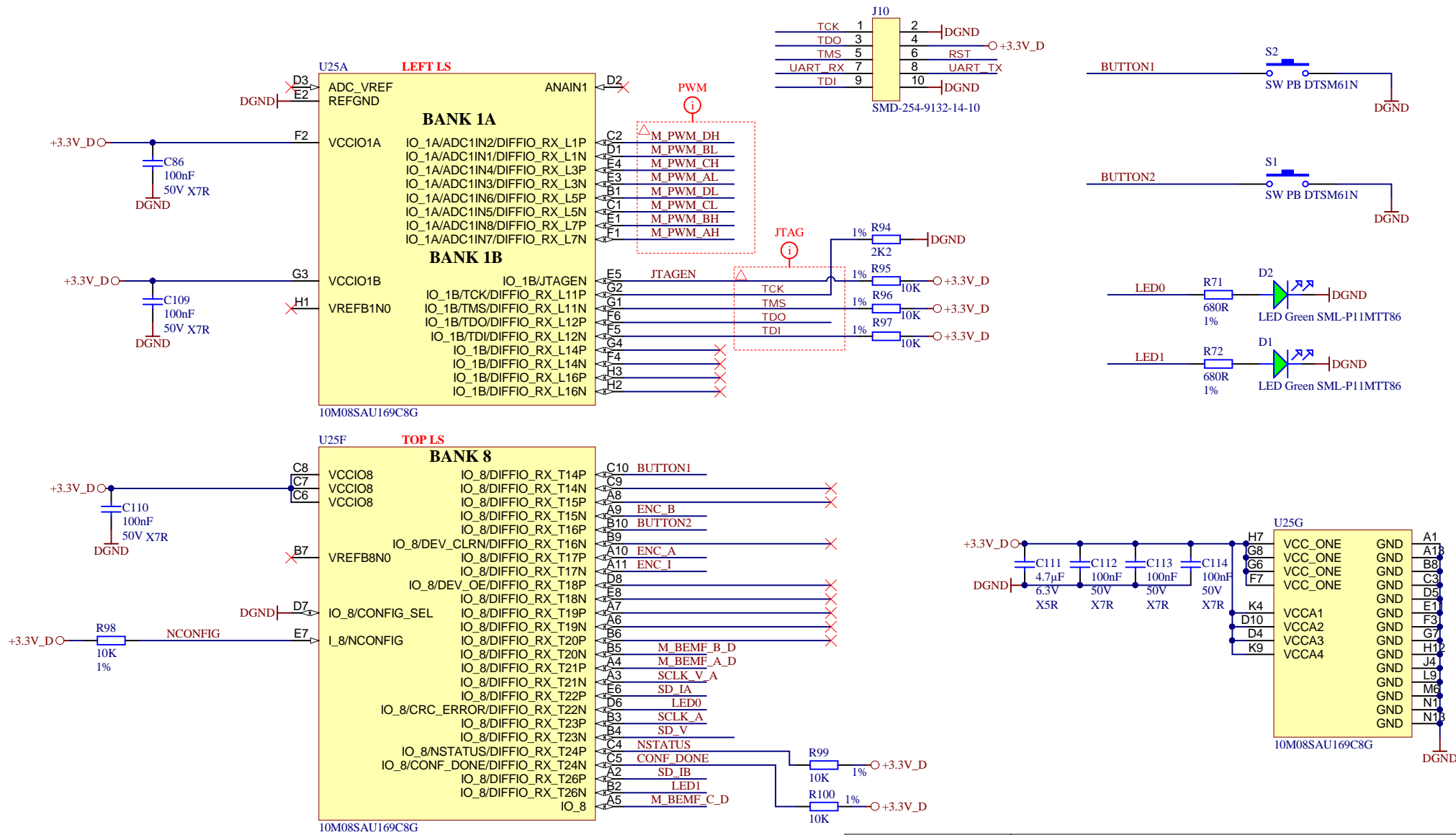
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10M08SAU169C8G



Title: FPGA_Main		
A4	Number: CR00140 default	Rev. 02
Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 13 of 20
Drawn by: *	Filename: FPGA_Main.SchDoc	



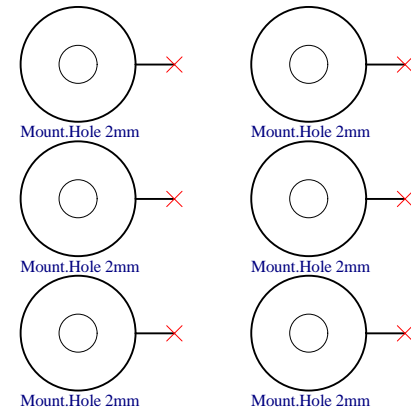
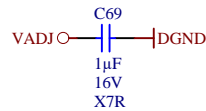
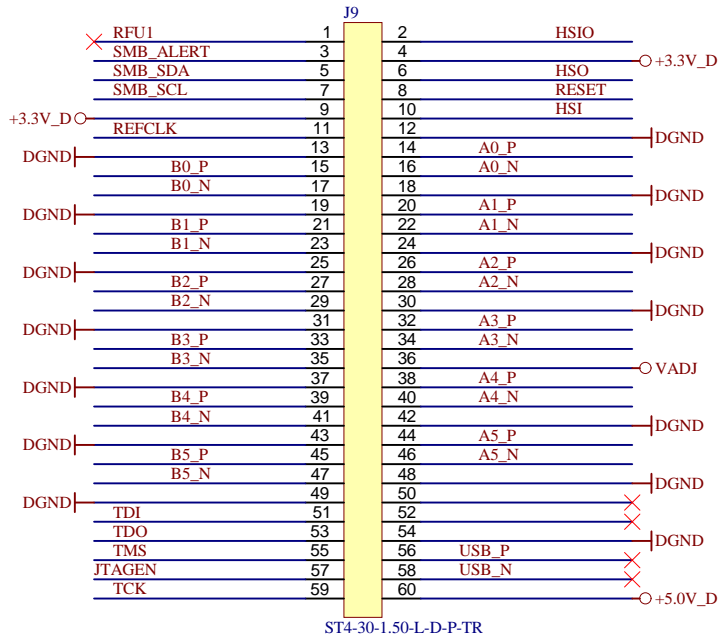
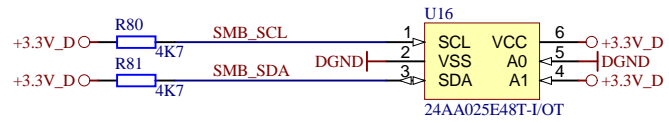
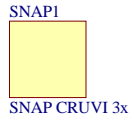
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A4	Number: CR00140 default	Rev. 02
Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 14 of 20
Drawn by: *	Filename: FPGA_MISC.SchDoc	


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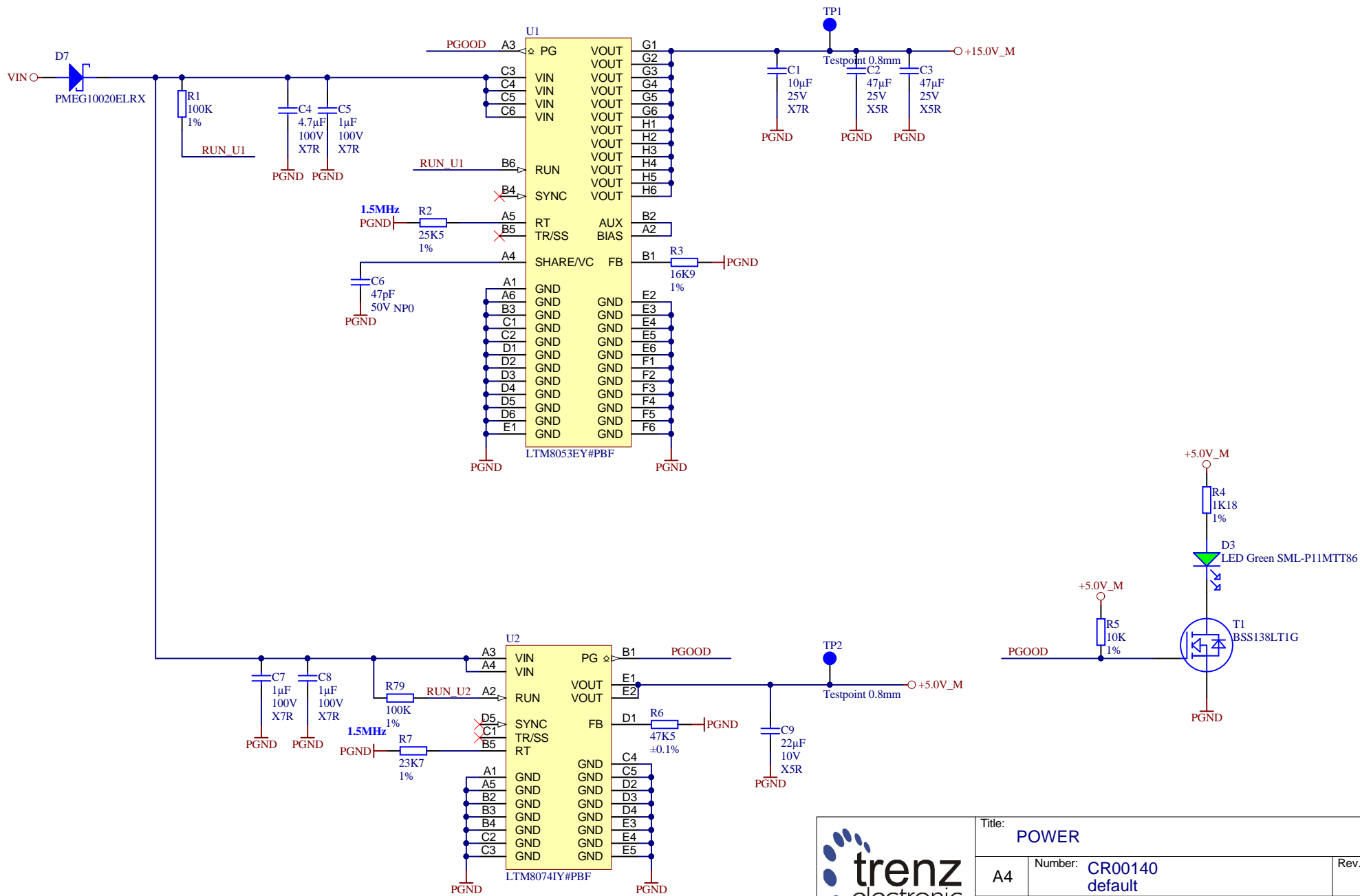
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Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 15 of 20		
Drawn by: *	Filename: CRUVI.SchDoc			

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Title: POWER		
A4	Number: CR00140 default	Rev. 02
Date: 2020-03-09	Copyright: Trenz Electronic GmbH	Page 16 of 20
Drawn by:	Filename: POWER.SchDoc	



		Title: Power_Protection_1	
		A4	Number: CR00140 default
Date: 2020-03-09		Copyright: Trenz Electronic GmbH	
Page 17 of 20		Filename: Power_Protection_1.SchDoc	
Drawn by: *			

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CHANGES REV01

initial Revision

REV01 - REV02

- 1) Removed LS connector J11
- 2) Added identification EEPROM
- 3) Updated to new TE Address
- 4) Moved J2
- 5) Rerouted AGND for current measurement

A

A

B


B

C

C

D

D

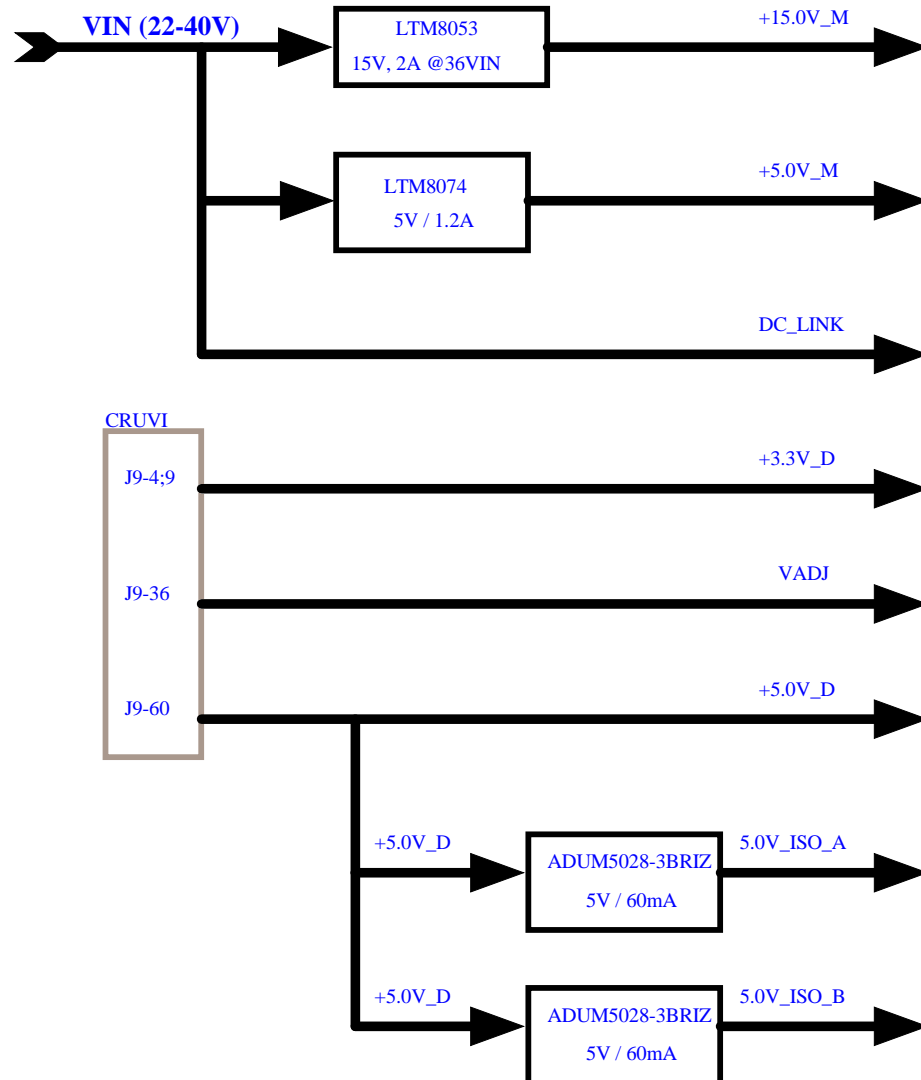
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		A4	Number: CR00140 default
Date: 2020-03-09		Copyright: Trenz Electronic GmbH	
Page 20 of 20		Drawn by: Filename: Power_Overview.SchDoc	