

1

2

3

4

A

A

REV	Description	
-01	Initial revision	AL/VG

B

B

C

C

D

D

Title: CR00240- Revision History			<small>Design licensed from MicroFPGA UG(h)</small>
A4	Number: CR00240 A	Rev. 01	
Date: 18-Sep-23	Copyright: Trenz Electronic GmbH	Page 1 of 4	
Filename: Revision Changes.SchDoc			

1

2

3

4

CRUVI
CRUVI.SchDoc



LOGO1

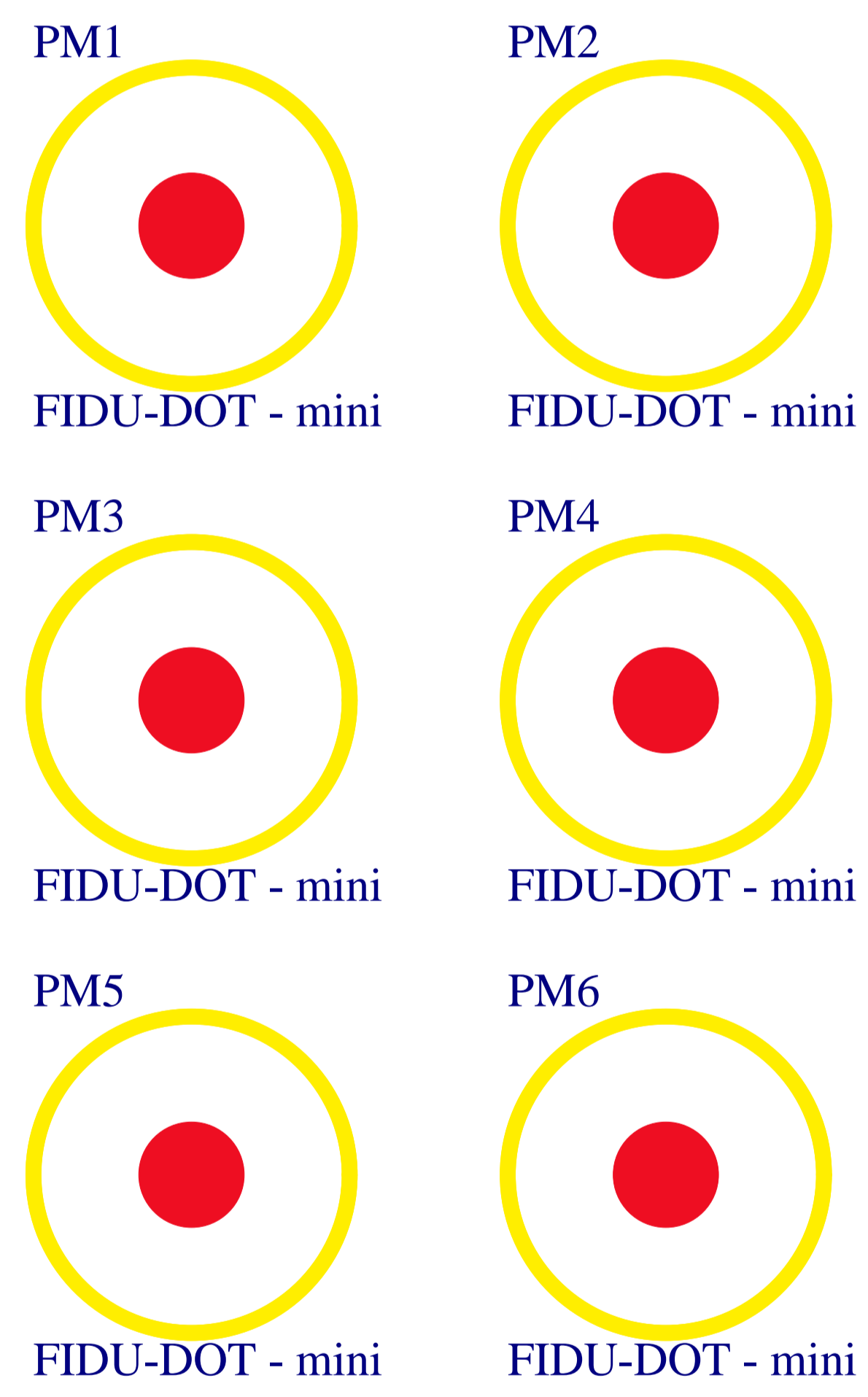
TE Logo PRINT Layer

LOGO PRINT

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

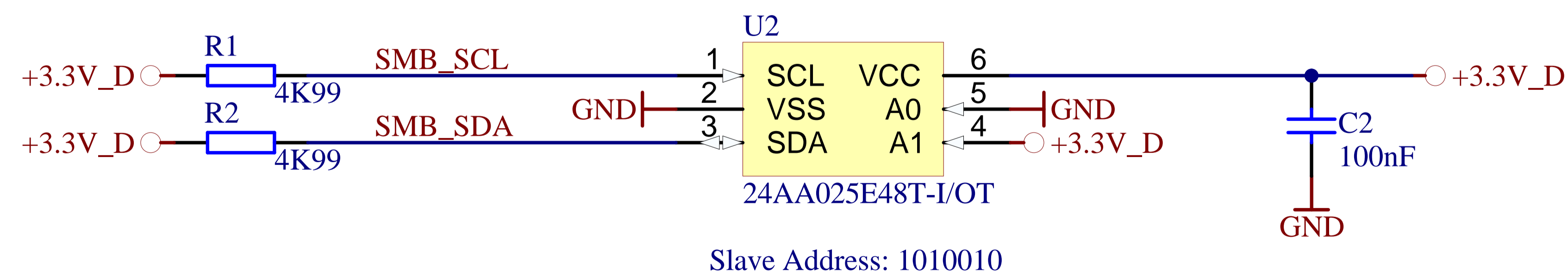
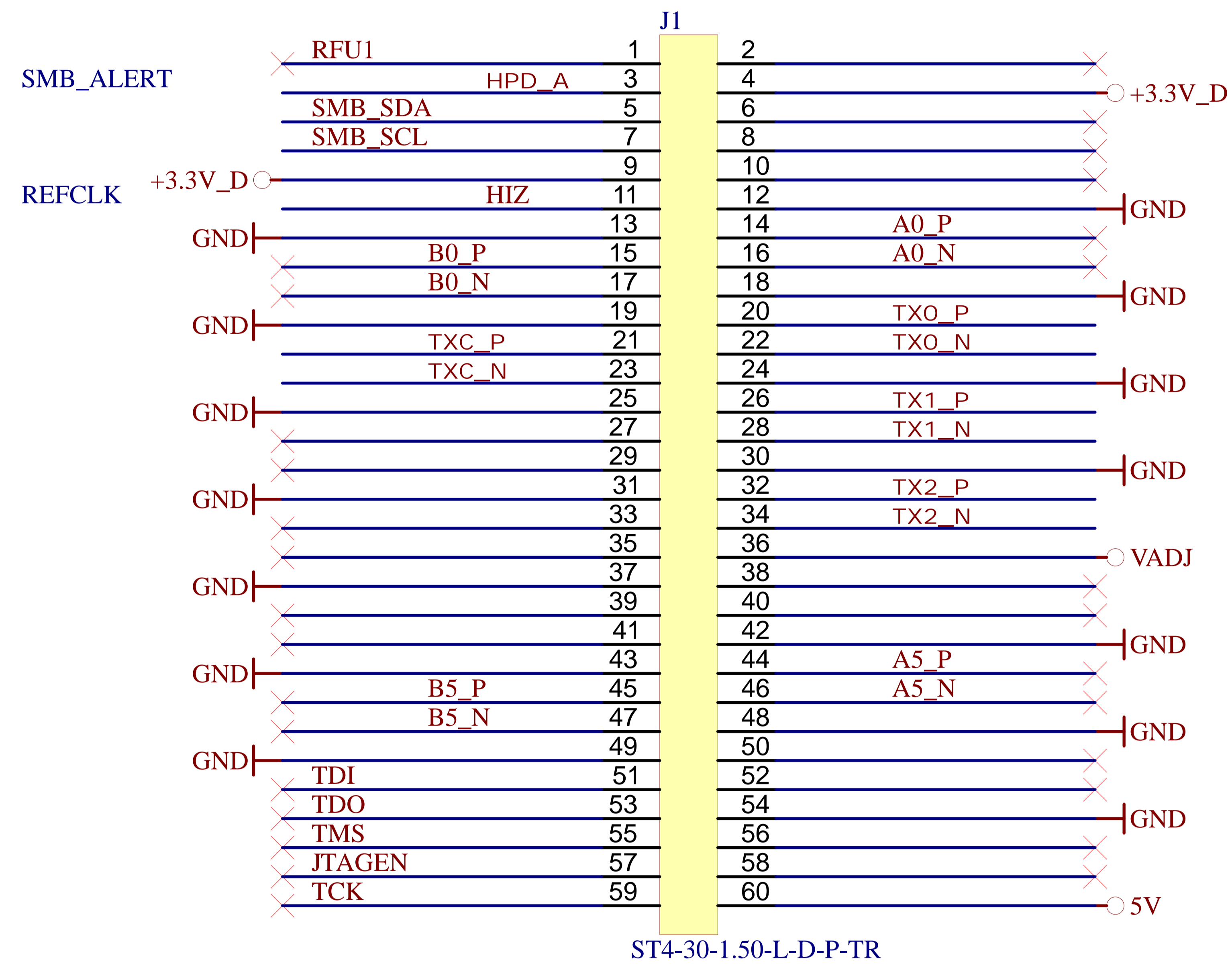
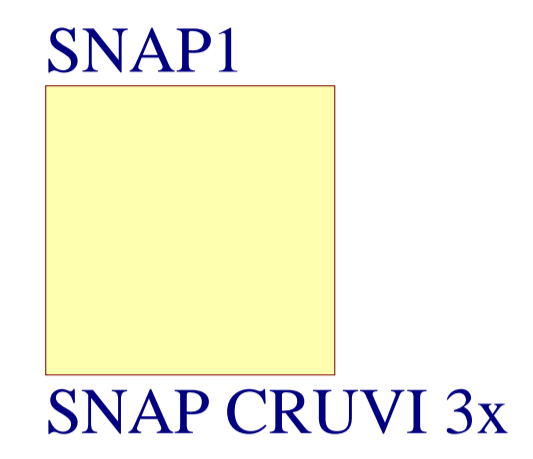
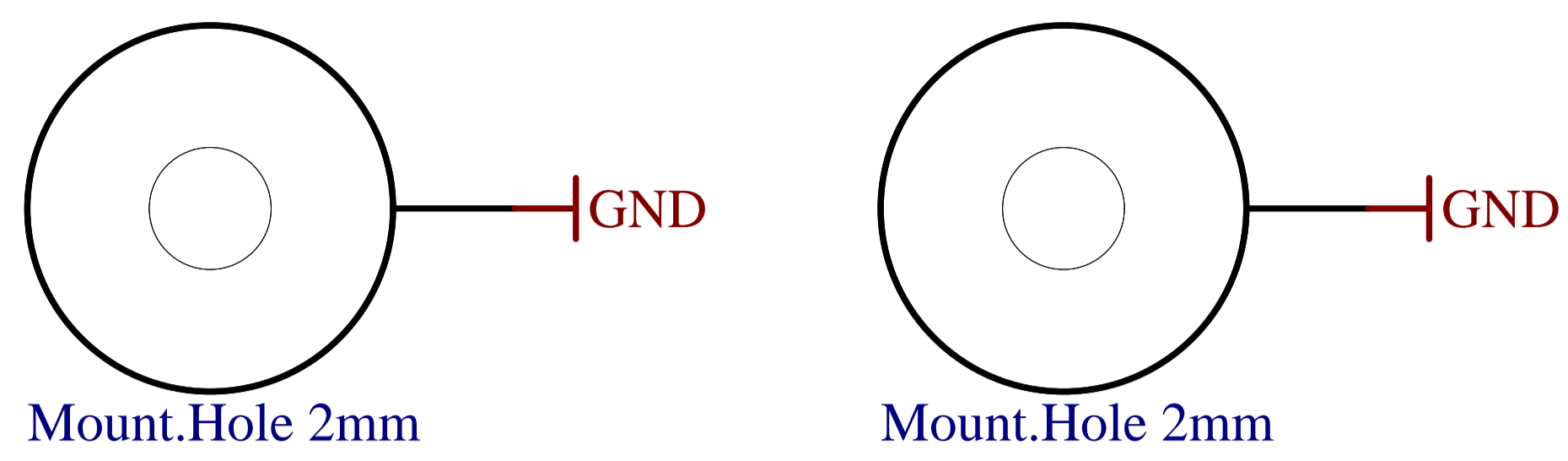


Assembly variant	A
Created by	MT
Modified by	-
Modified at	-
SVN Revision	1402 [Locally Modified]

Serial1
Serial
Serialnumber 6,3 x 6.3mm

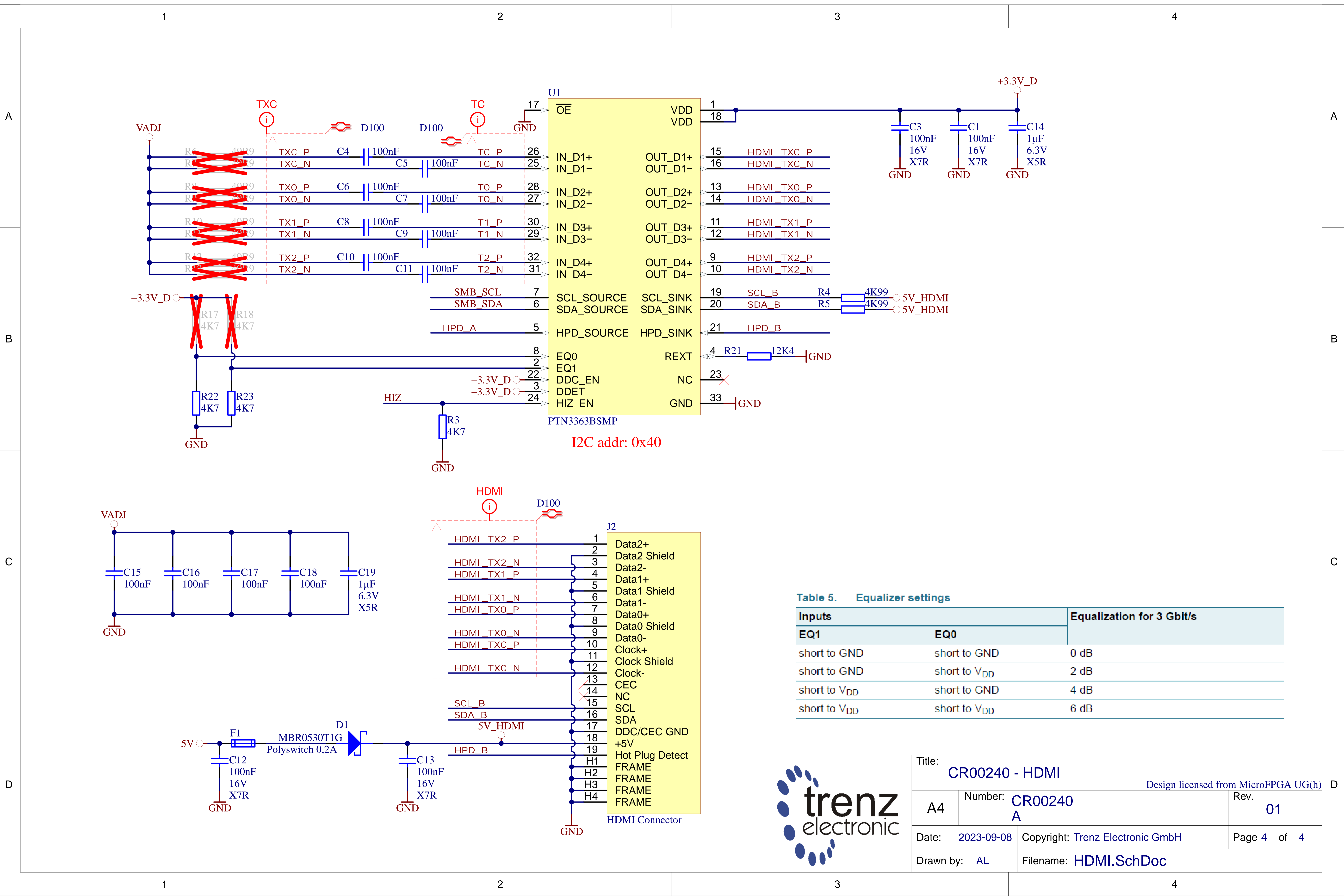
Based on P001

Title: CR00240		Design licensed from MicroFPGA UG(h)	
A4	Number: CR00240 A	Rev. 01	
Date: 11-Apr-25	Copyright: Trenz Electronic GmbH	Page 2 of 4	
Drawn by: AL	Filename: CR00240.SchDoc		



Assembly variant	A
Created by	MT
Modified by	-
Modified at	-
SVN Revision	1402

Title: CR00240 - Connectors		Design licensed from MicroFPGA UG(h)	
A4	Number: CR00240	Rev. 01	
Date: 18-Sep-23	Copyright: Trenz Electronic GmbH	Page 3 of 4	
Drawn by: AL	Filename: CRUVI.SchDoc		



I2C addr: 0x40

Table 5. Equalizer settings

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V _{DD}	2 dB
short to V _{DD}	short to GND	4 dB
short to V _{DD}	short to V _{DD}	6 dB



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A4	Number: CR00240 A		Rev. 01		
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Drawn by: AL		Filename: HDMI.SchDoc			