

1

2

3

4

A

A

REV	Description	
-01	Initial revision	AL/VG

B

B

C

C

D

D

Title: CR00240- Revision History		<small>Design licensed from MicroFPGA UG(h)</small>	
A4	Number: CR00240 P001	Rev.	01
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Filename: Revision Changes.SchDoc			

1

2

3

4

CRUVI
CRUVI.SchDoc



LOGO1

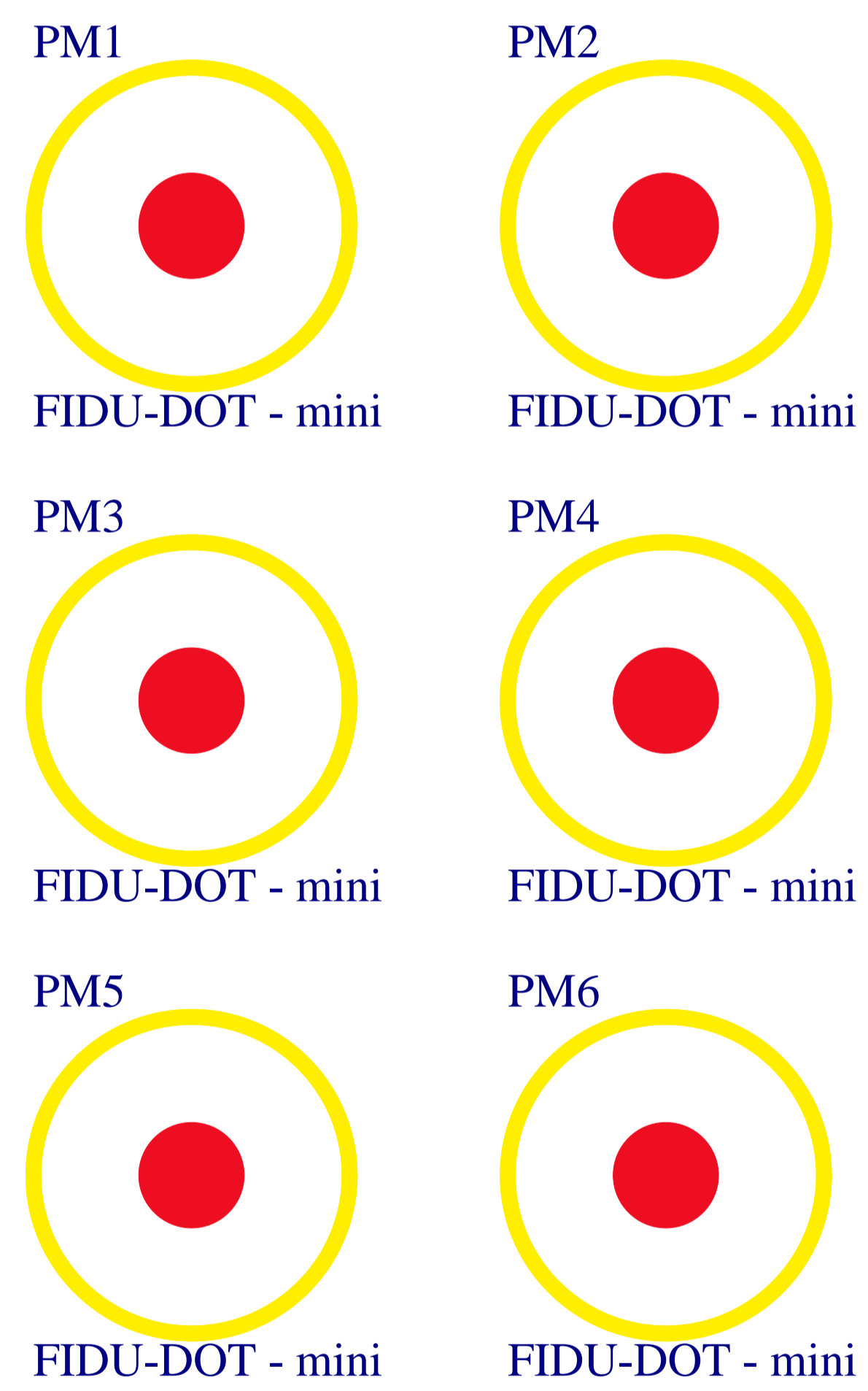
TE Logo PRINT Layer

LOGO PRINT

CE

CE Logo on Top Overlay

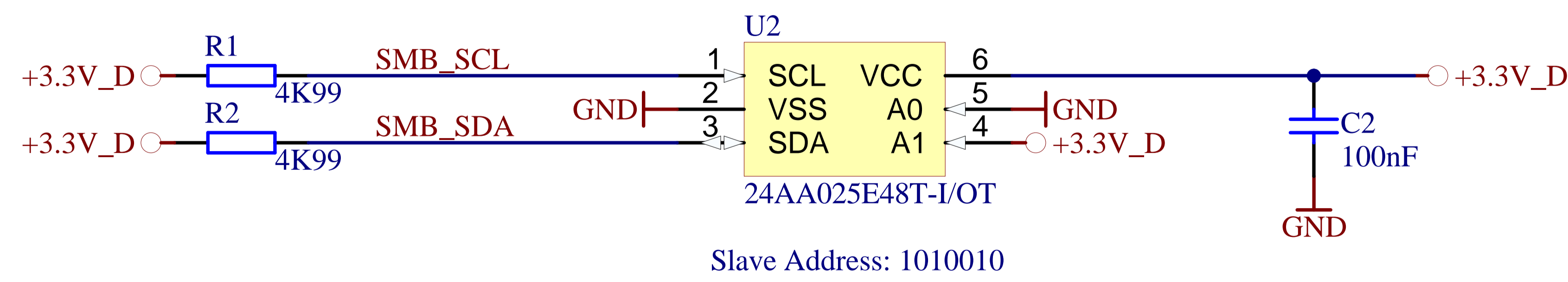
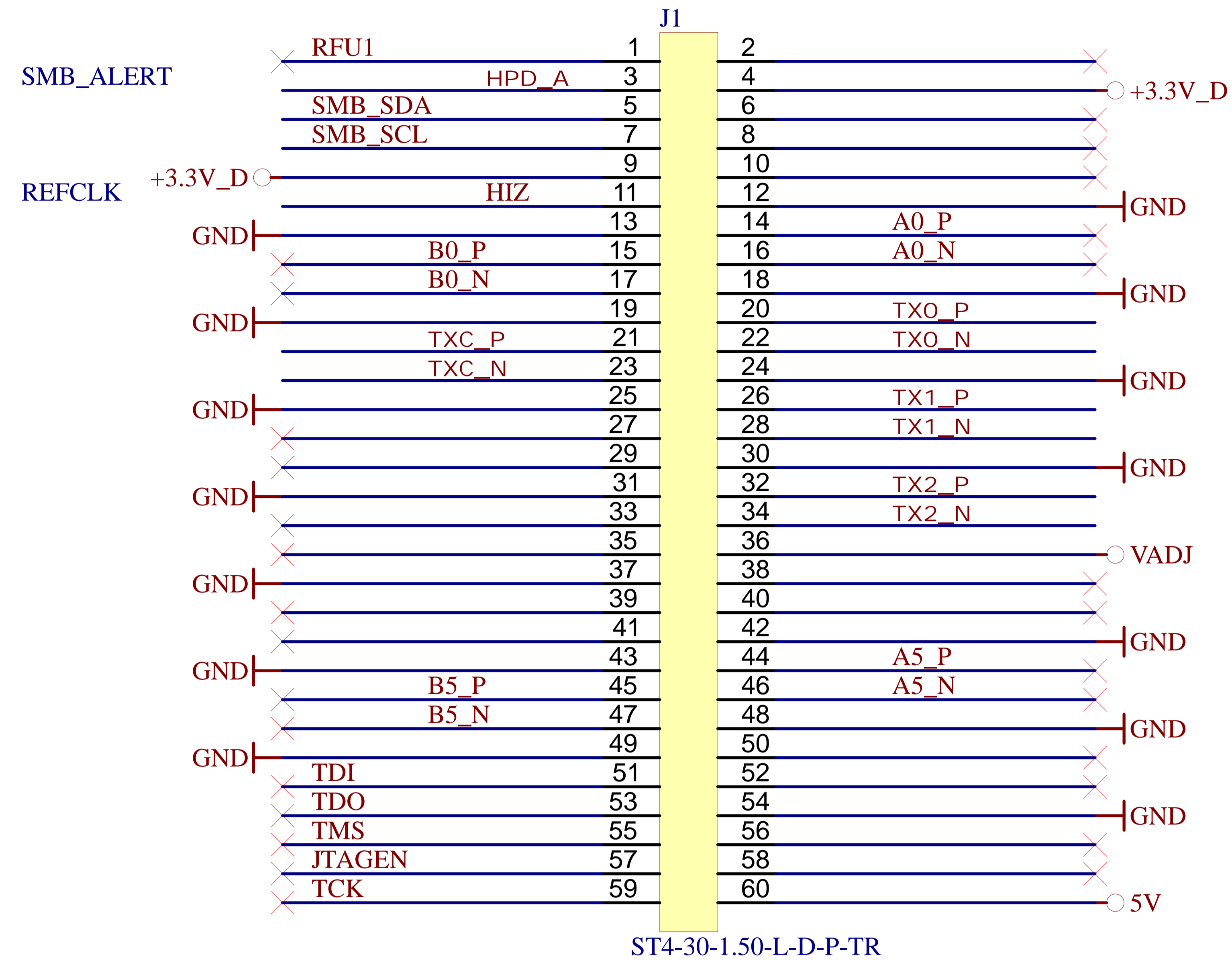
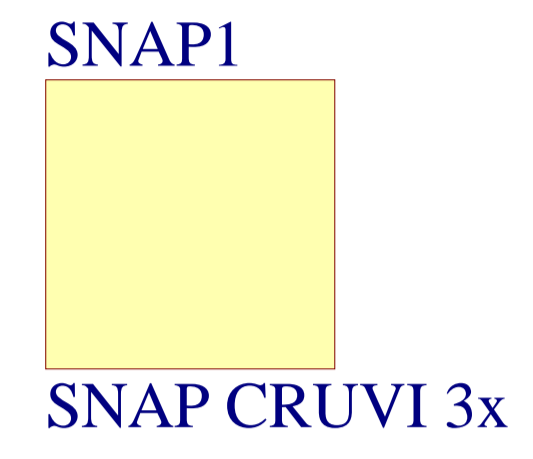
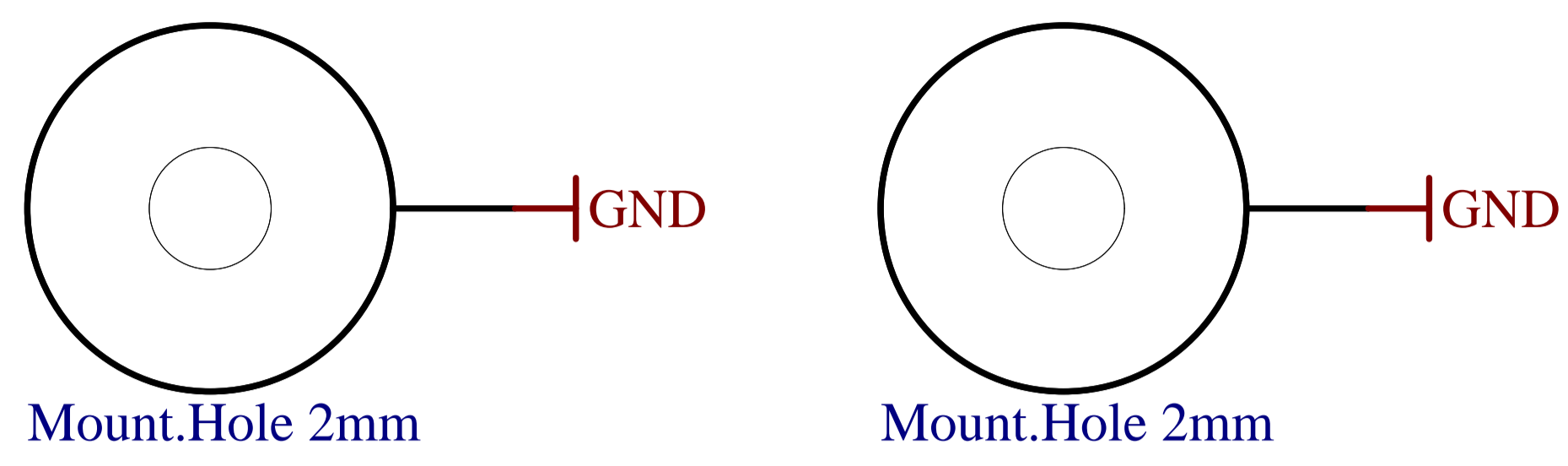
CE-TOPOVERLAY



Assembly variant	P001
Created by	VG
Modified by	-
Modified at	-
SVN Revision	

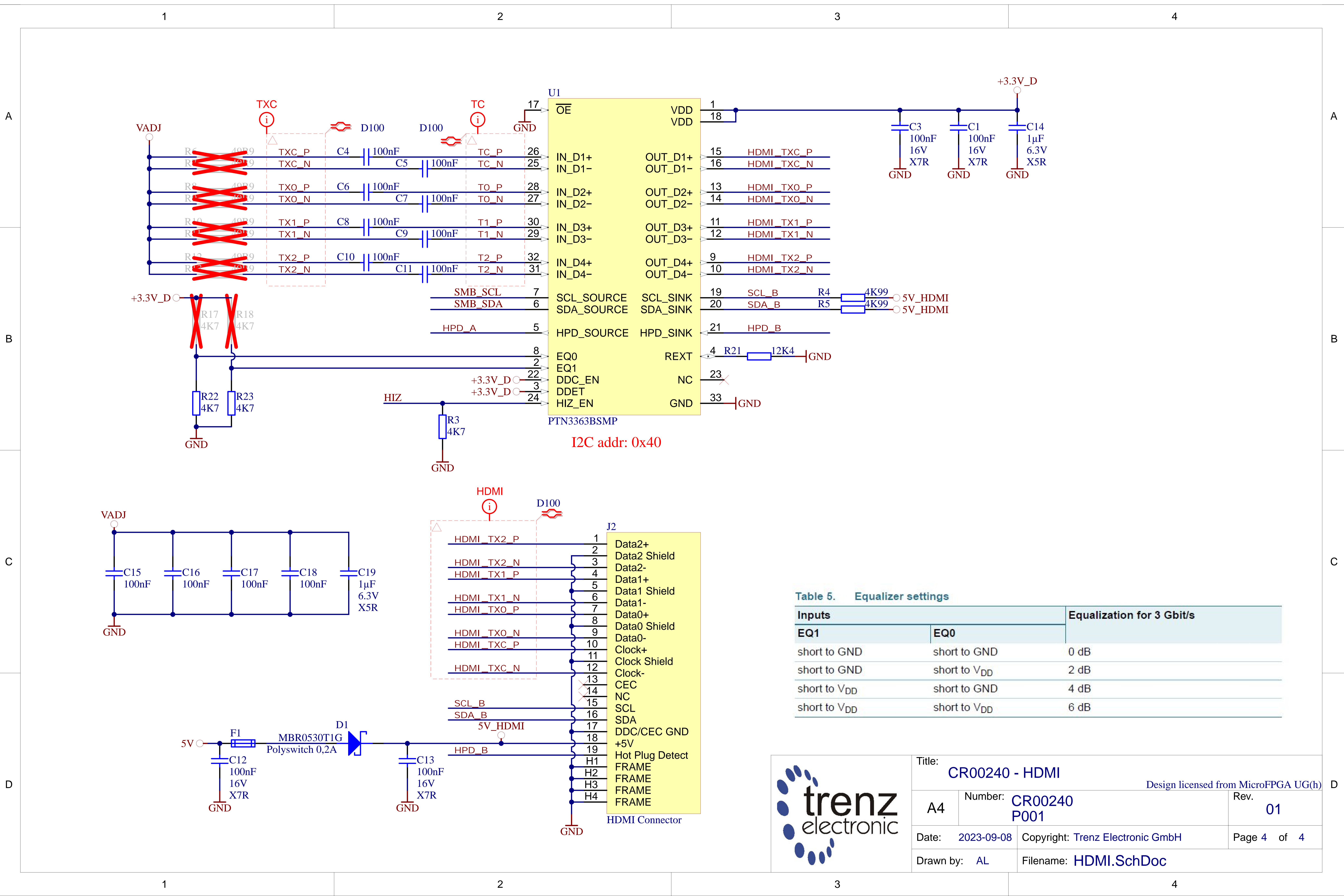
Serial1
Serial
Serialnumber 6,3 x 6.3mm

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Assembly variant	P001
Created by	VG
Modified by	-
Modified at	-
SVN Revision	

Title: CR00240 - Connectors		Design licensed from MicroFPGA UG(h)	
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I2C addr: 0x40

Table 5. Equalizer settings

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V _{DD}	2 dB
short to V _{DD}	short to GND	4 dB
short to V _{DD}	short to V _{DD}	6 dB



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Drawn by: AL		Filename: HDMI.SchDoc			