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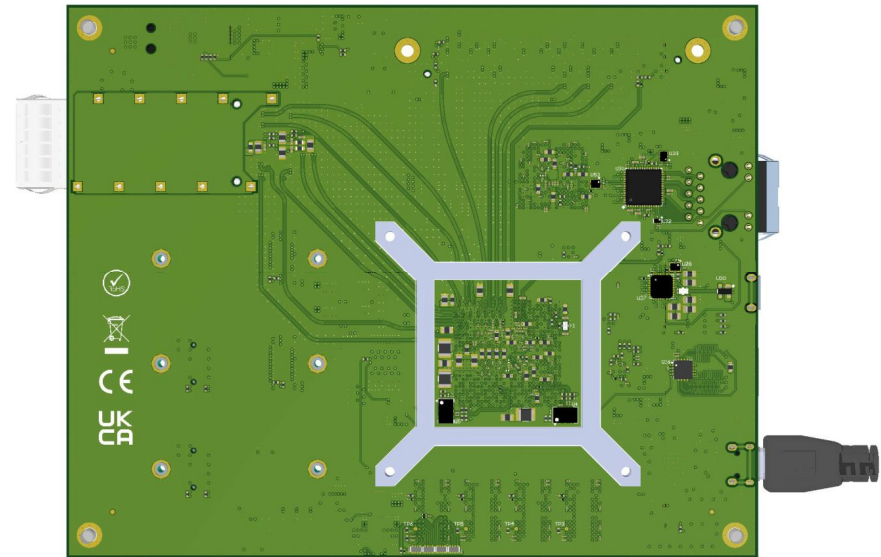
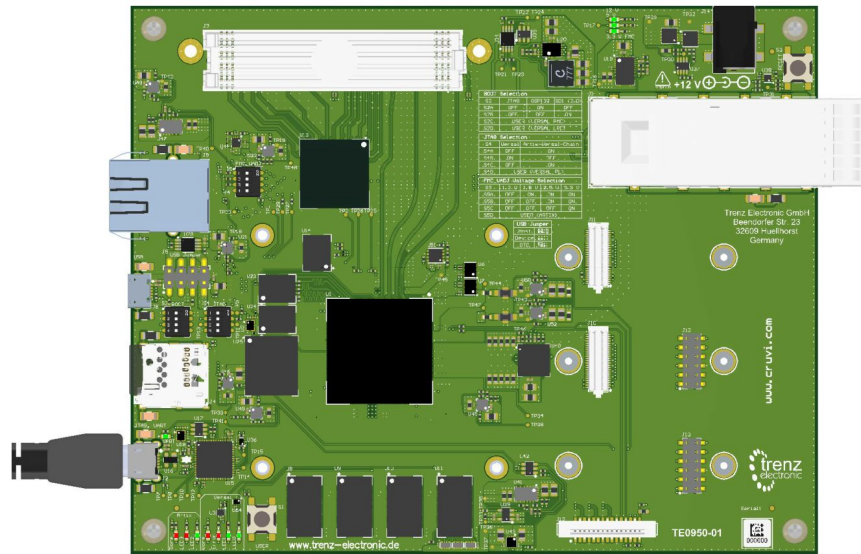
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Regarding the usage of our schematics and alike documentation for Trenz module TE0950.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0950 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

Drawn by	MR
Checked by	*
Assembly variant	EGBE11A
Created by	MR
Modified by	MR
Modified at	2023-01-31



Title: <b>Legal Notices</b>		
A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
Date: <b>24.02.2023</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>1</b> of <b>38</b>
Filename: <b>Legal Notices TE0950.SchDoc</b>		

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REV	Description	
-01	Initial revision	MR

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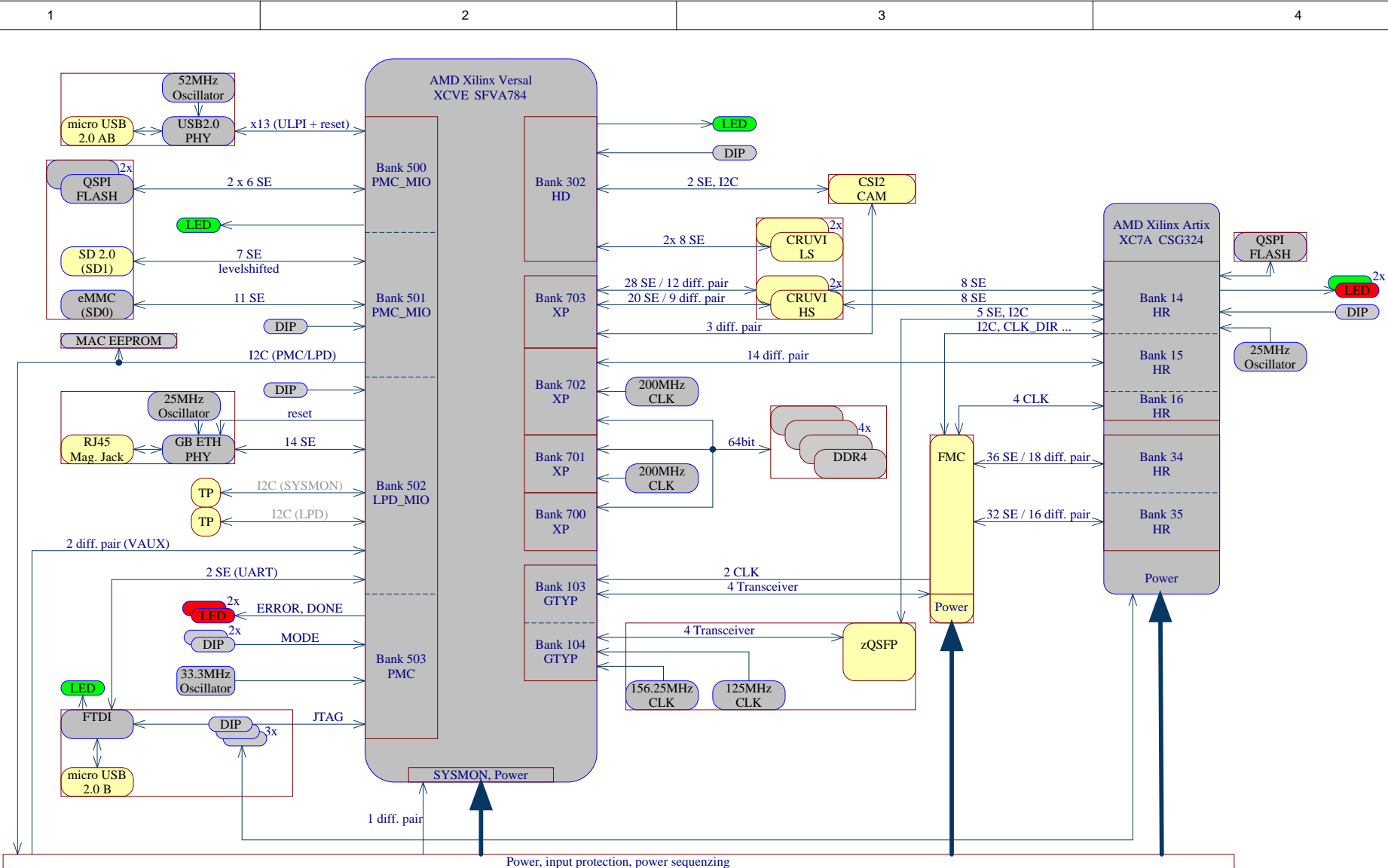
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			A4	Number: <b>TE0950</b> <b>EGBE11A</b>	Rev. <b>01</b>
Date: <b>24.02.2023</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>2</b> of <b>38</b>	
Filename: <b>Revision Changes.SchDoc</b>					

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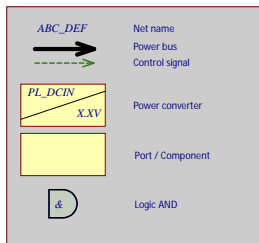
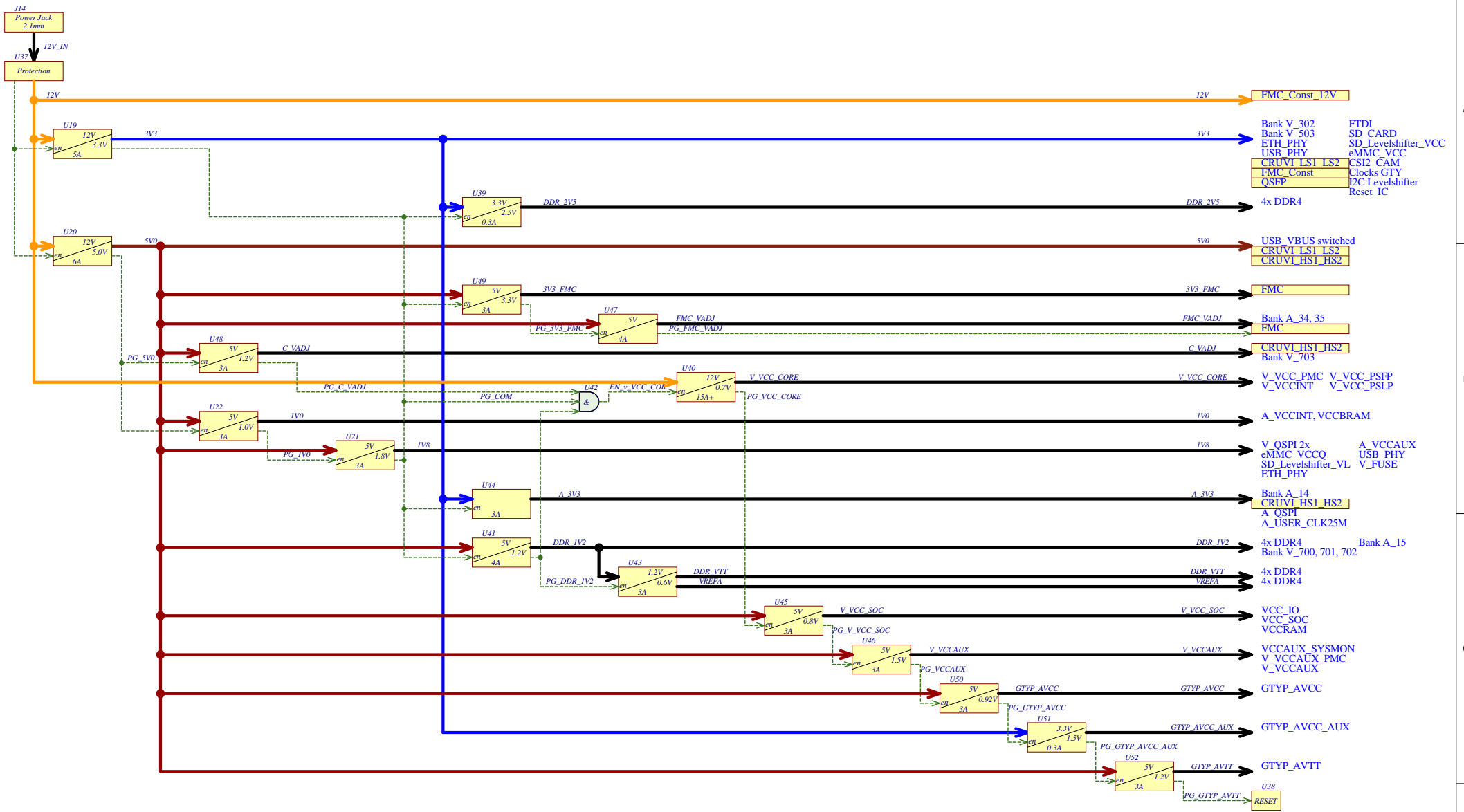
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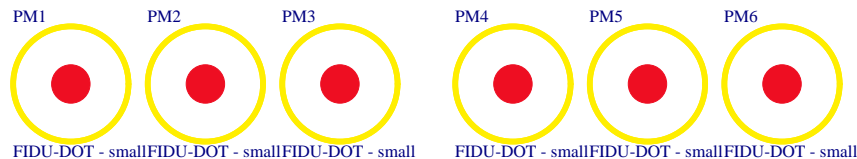
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Special notes:

	Title: <b>System Overview</b>		
	A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
	Date: 27.02.2023	Copyright: Trenz Electronic GmbH	Page 3 of 38
	Filename: <b>Overview.SchDoc</b>		





### I2C Addresses:

Device	Bus	Address	Note
24AA025E48	PMC_I2C	1010000 50H	EEPROM for MAC with user area
MP8869SGL-Z	PMC_I2C	1100001 61H	5V DCDC

MECH1

TE Address Overlay

LOGO ADDRESS

LOGO1

TE Logo PRINT Layer

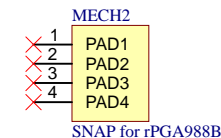
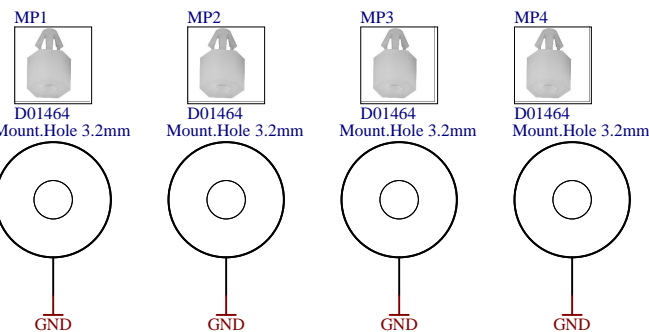
LOGO PRINT

Serial1

Serial  
Serialnumber 6,3 x 6.3mm

### Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
12V_IN	IN	12V	+/-5%	Board Power	-
5V0	OUT	5.0V	+/-3%	CRUVI LS and HS 5V	Shared with onboard 5V supplies and with further switch (U29) for rail USB_VBUS_SUP via jumper (J5) connectable to USB (J8).
3V3	OUT	3.3V	+/-3%	QSFP, CRUVI LS 3.3V, CSI-2 CAM	Shared with VERSAL VCCO Bank 302 and onboard peripherals.
C_VADJ	OUT	1.2V	+/-3%	CRUVI HS IO	Shared with VERSAL VCCIO XPIO Bank 703.
A_3V3	OUT	3.3V	+/-3%	CRUVI HS 3.3V	Shared with ARTIX VCCIO Bank 14 and onboard peripherals.
12V	OUT	12V	+/-5%	FMC	Derived from 12V_IN after input protection. Shared with onboard peripherals.
3V3_FMC	OUT	3.3V	+/-3%	FMC	-
FMC_VADJ	OUT	1.2V - 3.3V	+/-3%	FMC	Selectable by dip settings.



CE1  
CE Logo on Top Overlay

CE-TOPOVERLAY

UKCA1  
UKCA Logo on Top Overlay

UKCA-TOPOVERLAY



Title: <b>TEB0850</b>		
A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
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Filename: <b>TE0950.SchDoc</b>		

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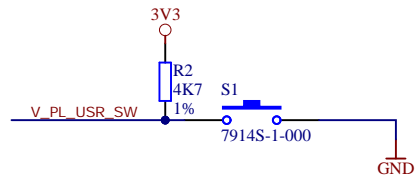
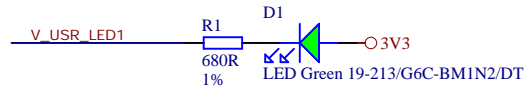
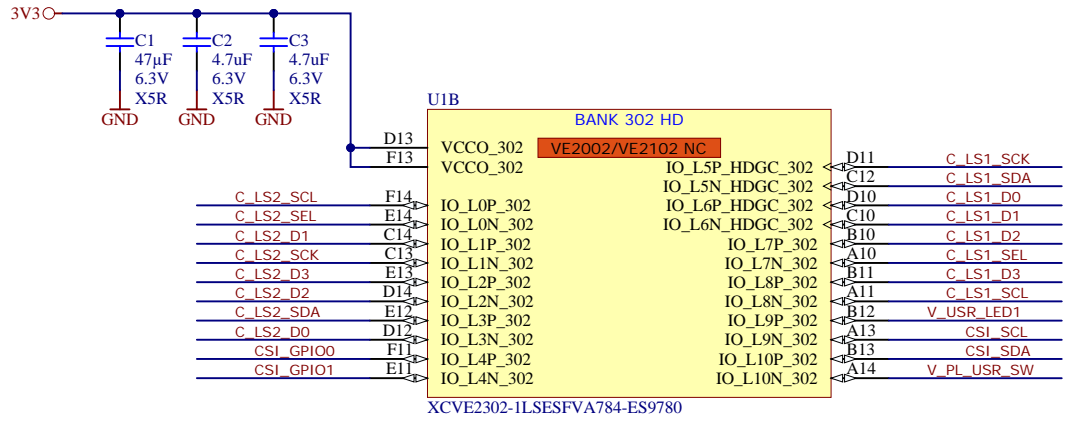
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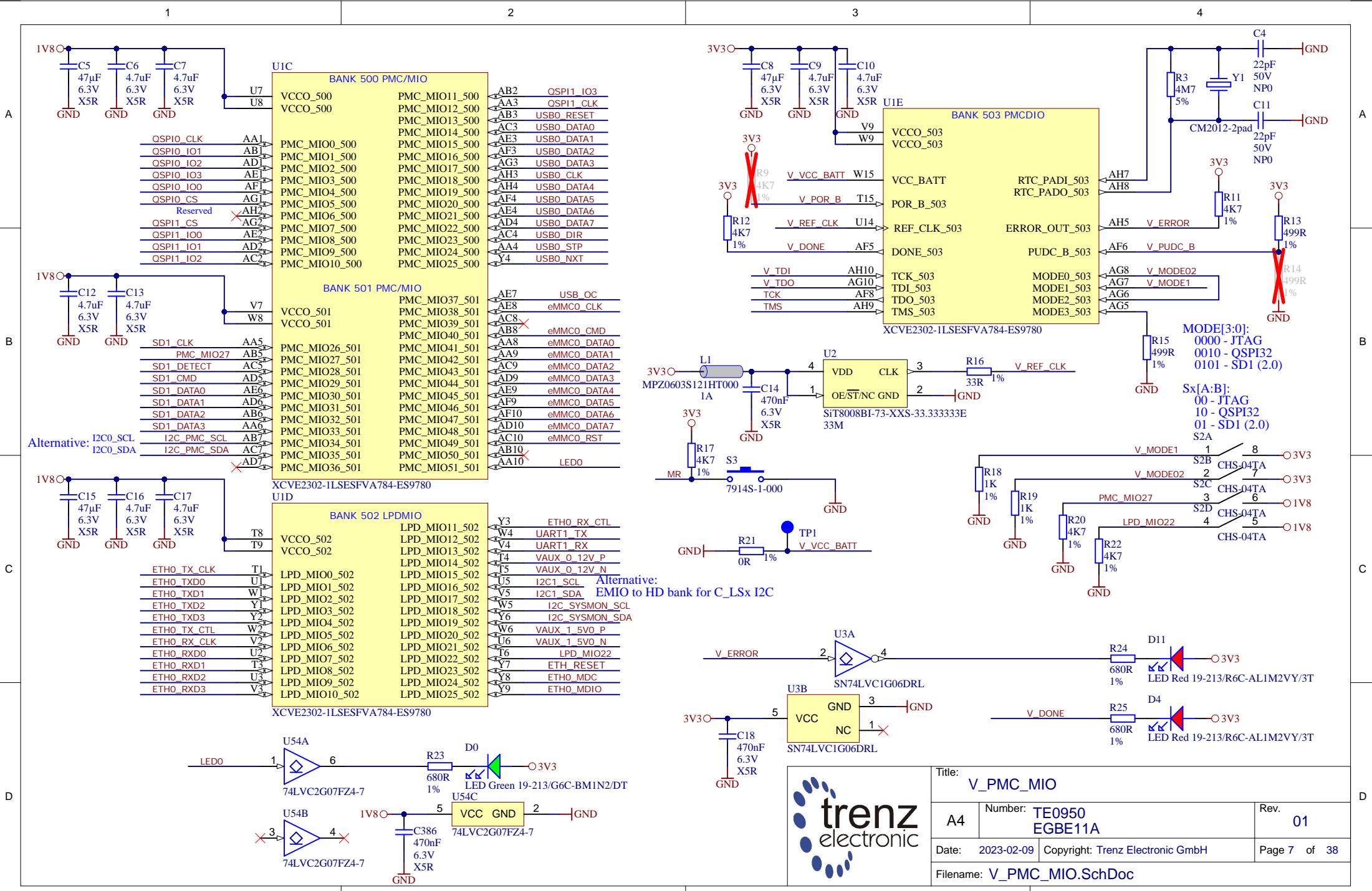
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A4	Number: TE0950 EGBE11A	Rev. 01
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Filename: V_HD.SchDoc		

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Title: V_PMC_MIO		
A4	Number: TE0950 EGBE11A	Rev. 01
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Filename: V_PMC_MIO.SchDoc		Page 7 of 38

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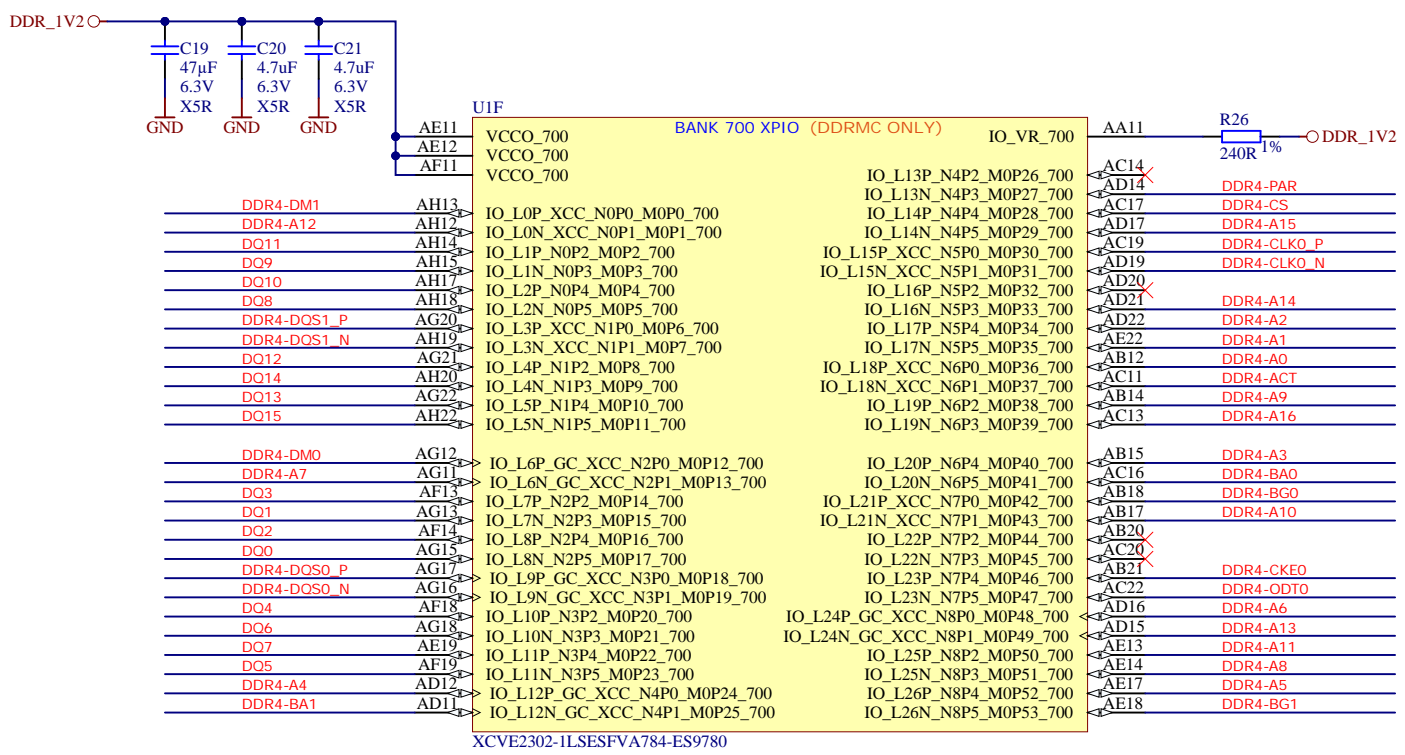
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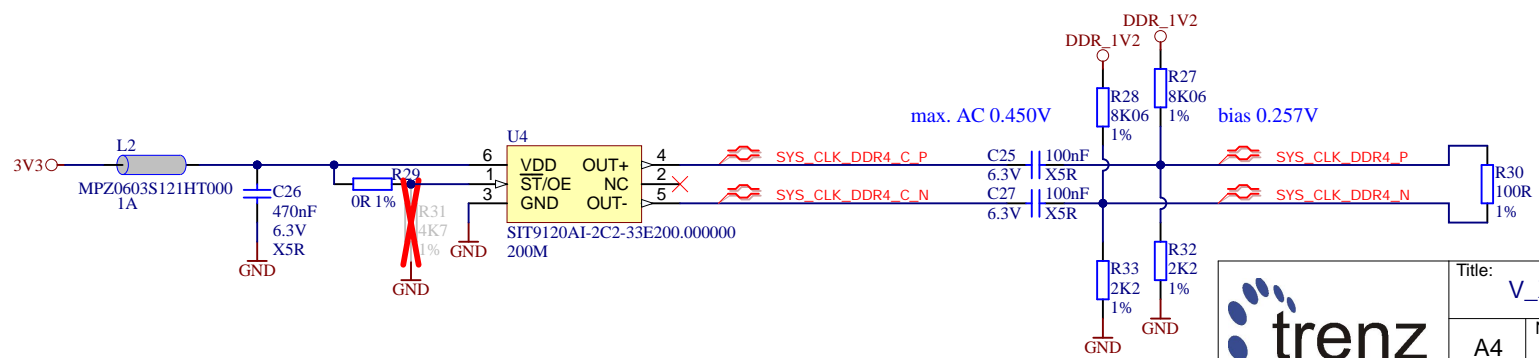
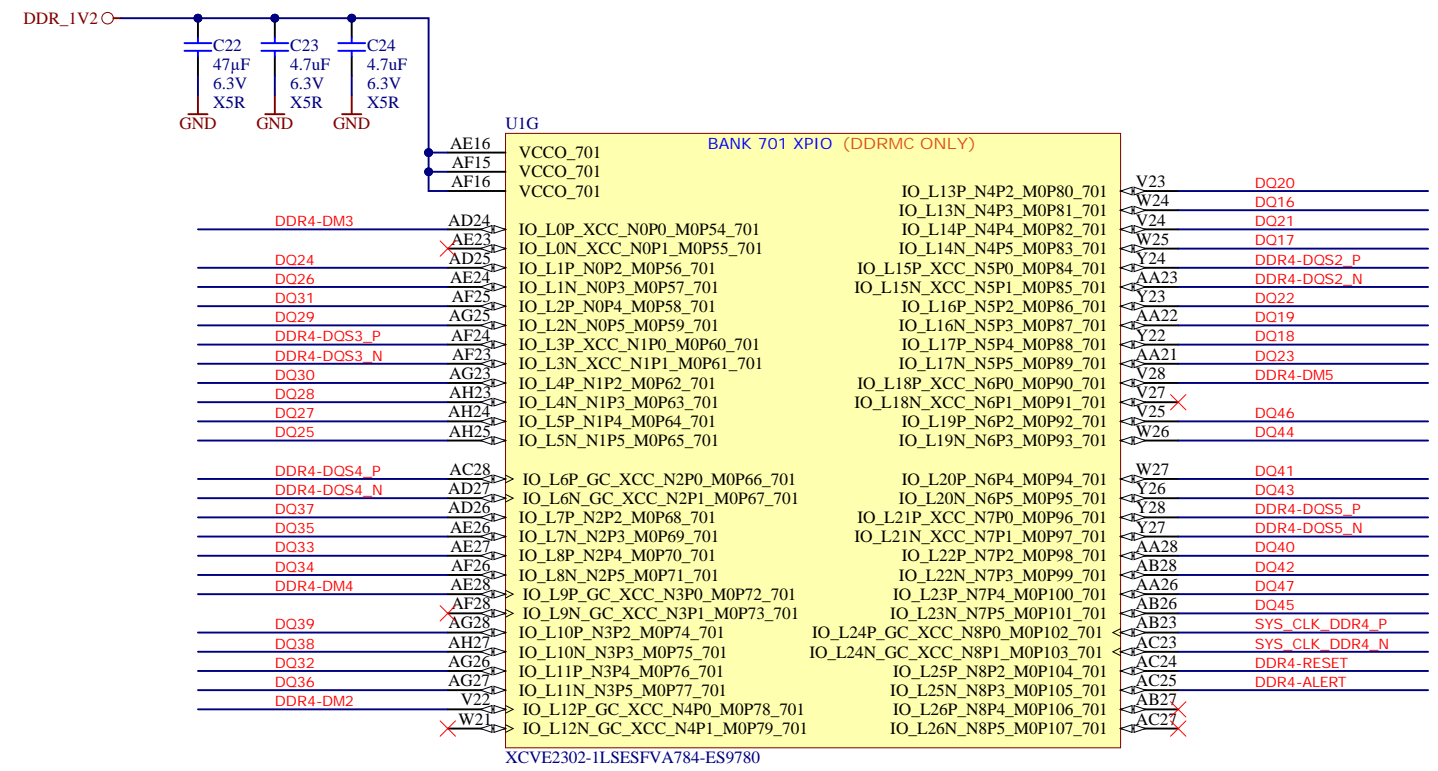
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Date: 2023-02-09	Copyright: Trenz Electronic GmbH	Page 8 of 38
Filename: V_XPIO_700.SchDoc		





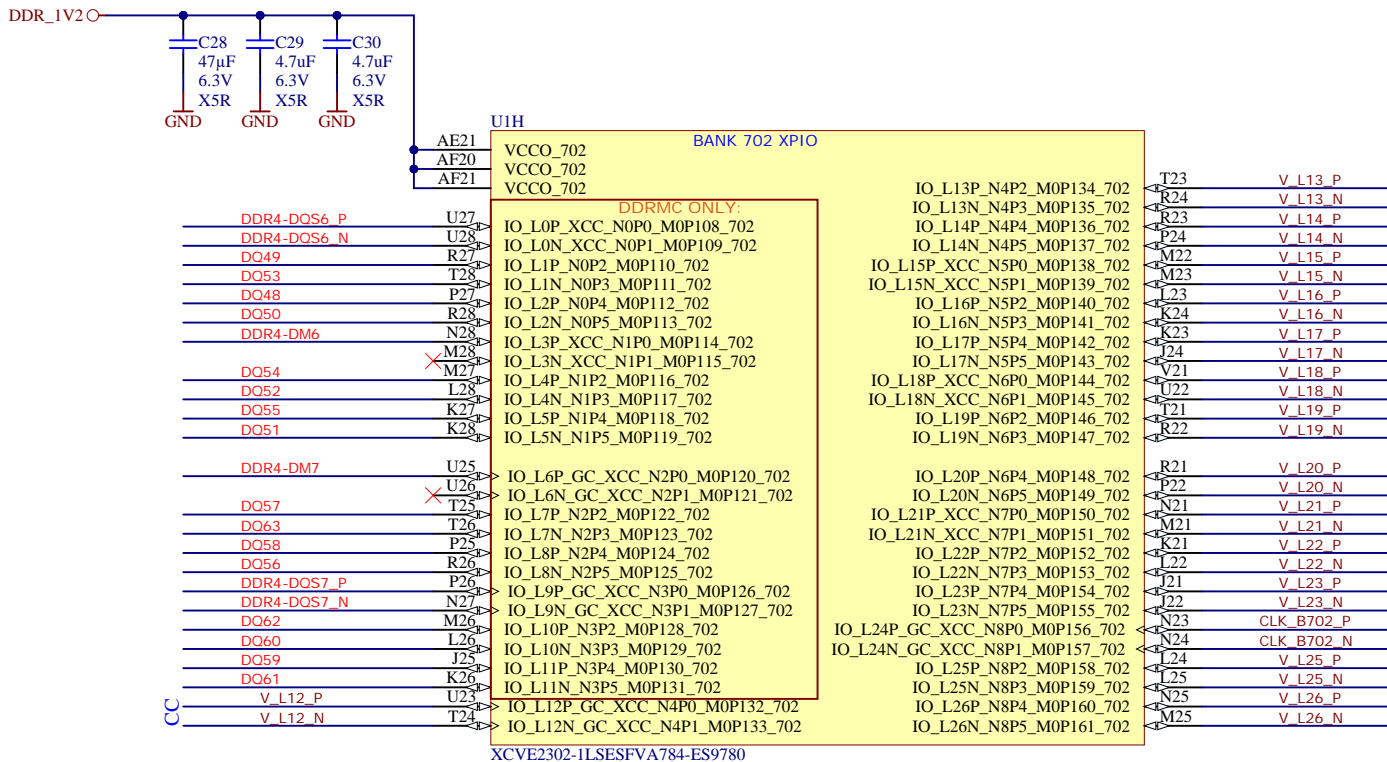
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Date: 2023-02-09	Copyright: Trenz Electronic GmbH	Page 9 of 38
Filename: V_XPIO_701.SchDoc		

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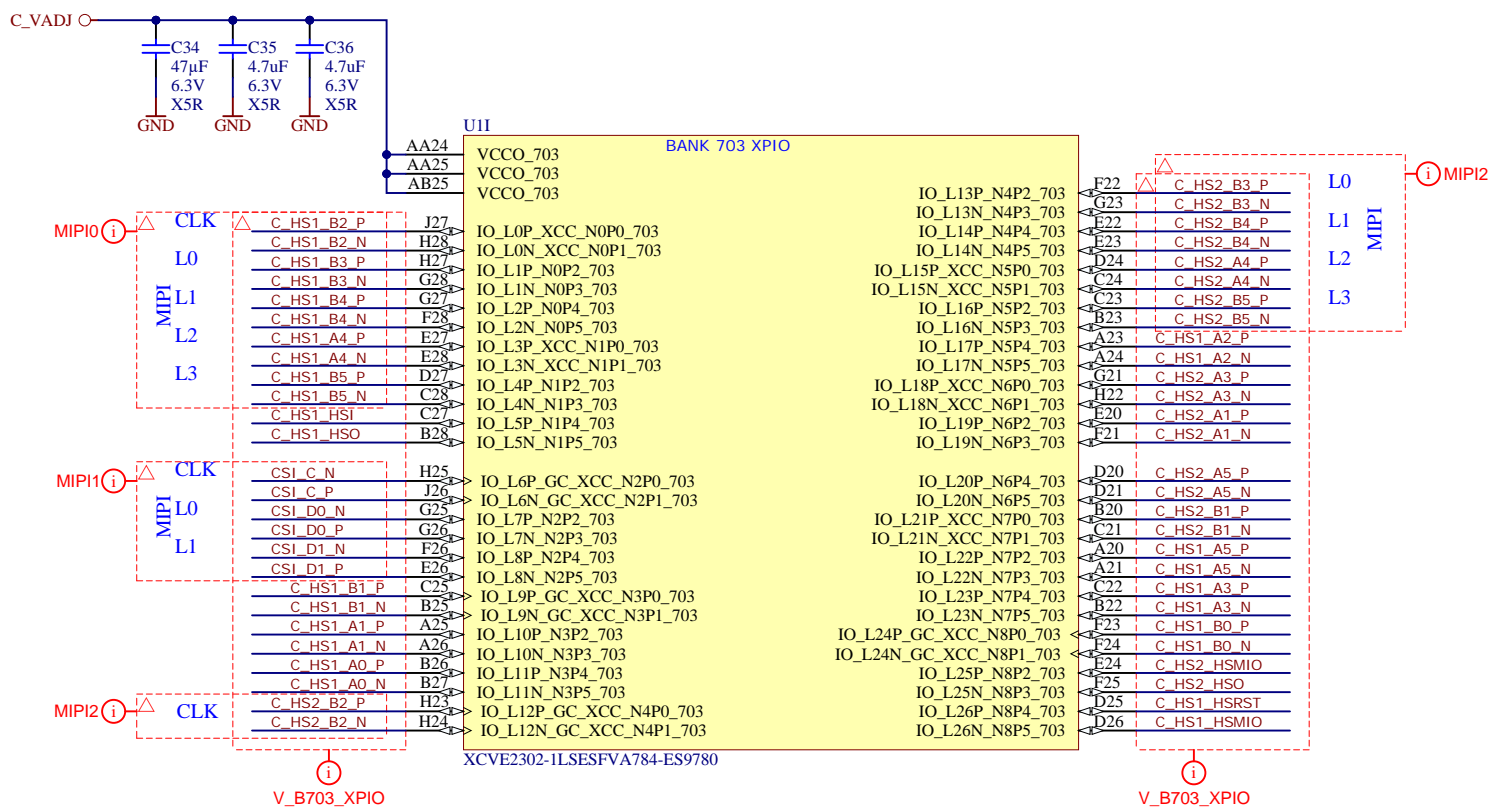
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Date: 2023-02-09	Copyright: Trenz Electronic GmbH	Page 10 of 38
Filename: V_XPIO_702.SchDoc		


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		Title: V_XPIO_703	
		A4	Number: TE0950 EGBE11A
Date: 2023-02-09		Copyright: Trenz Electronic GmbH	
Filename: V_XPIO_703.SchDoc		Rev. 01	
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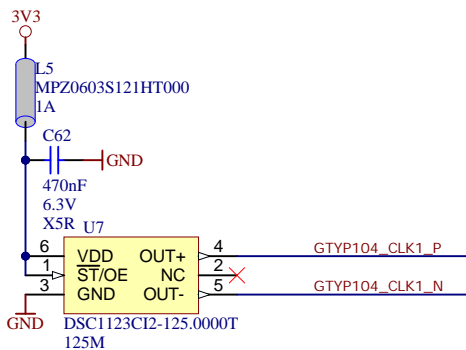
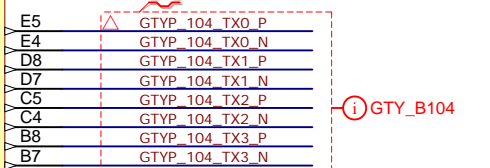
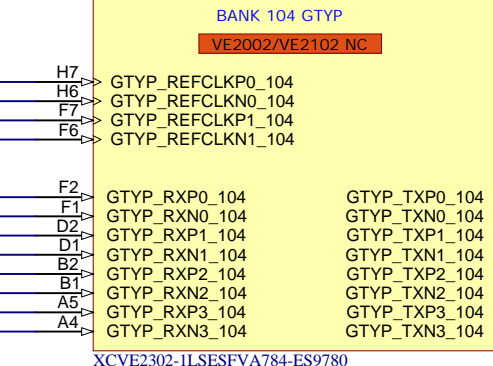
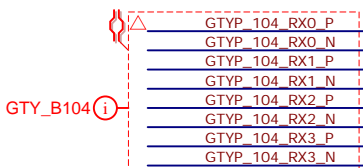
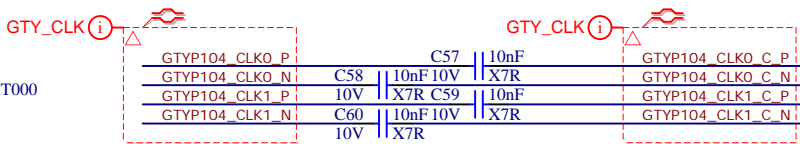
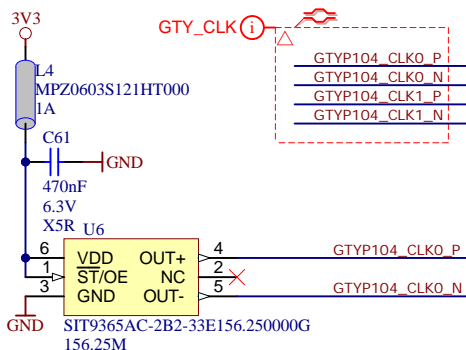
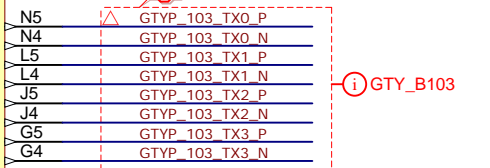
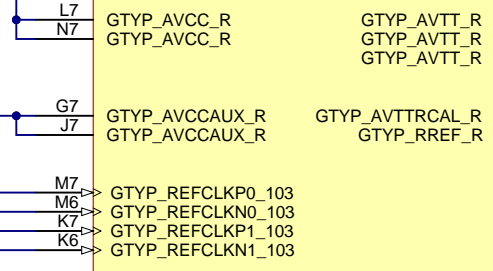
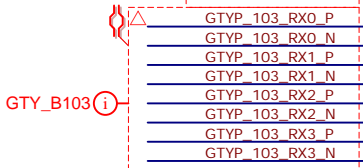
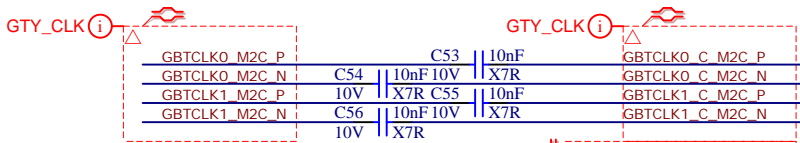
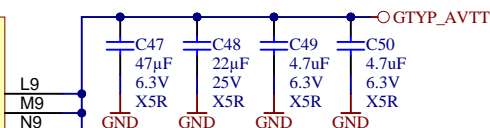
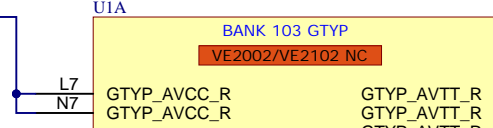
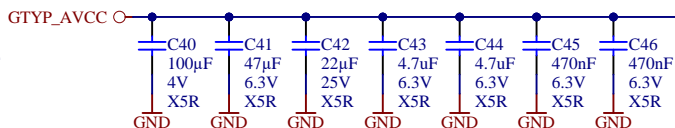
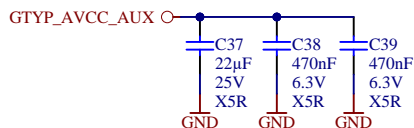
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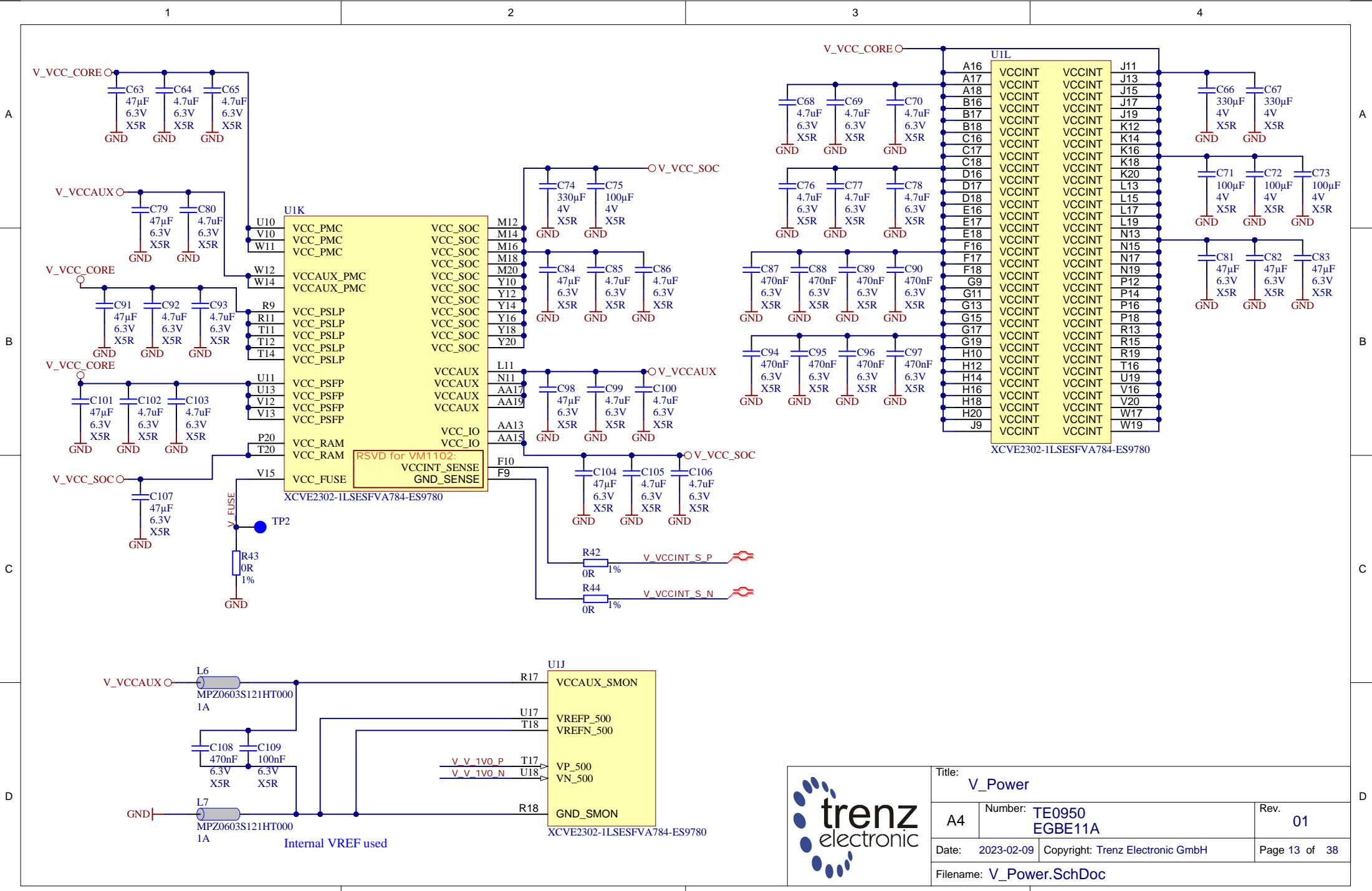
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Date: 2023-02-09	Copyright: Trenz Electronic GmbH	Page 12 of 38
Filename: V_GTYP.SchDoc		

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Title: <b>V_Power</b>		
A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
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Filename: <b>V_Power.SchDoc</b>		

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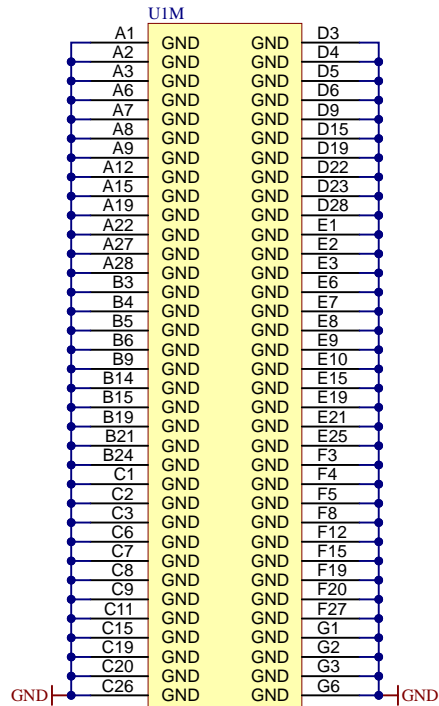
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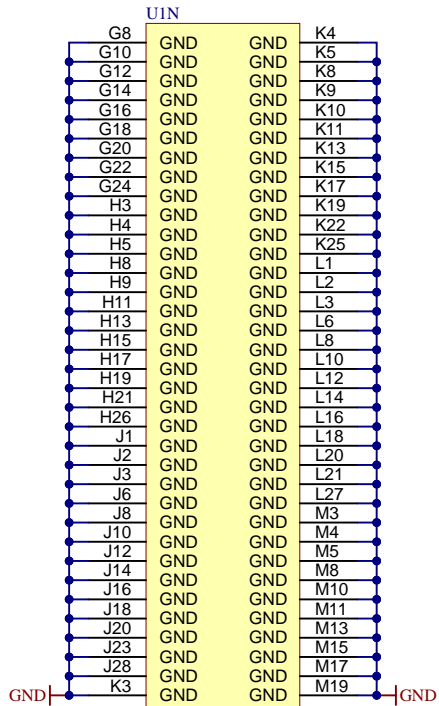
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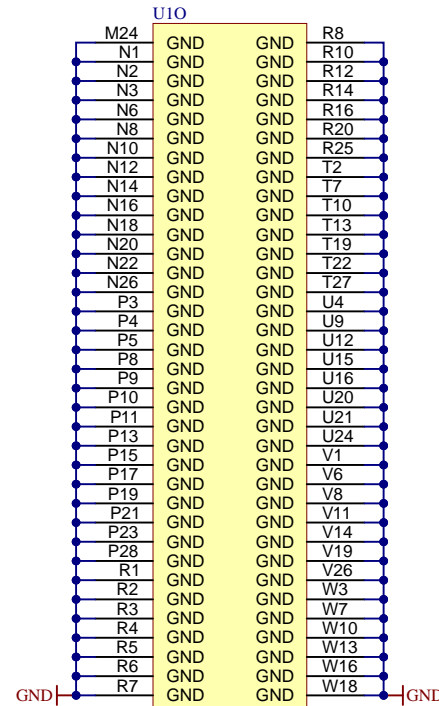
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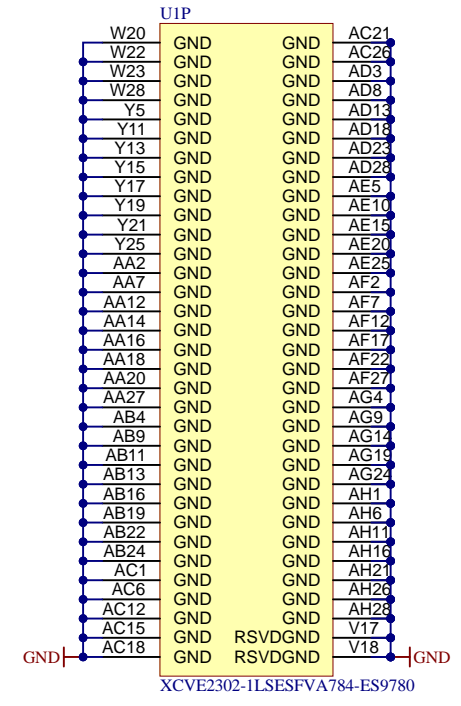
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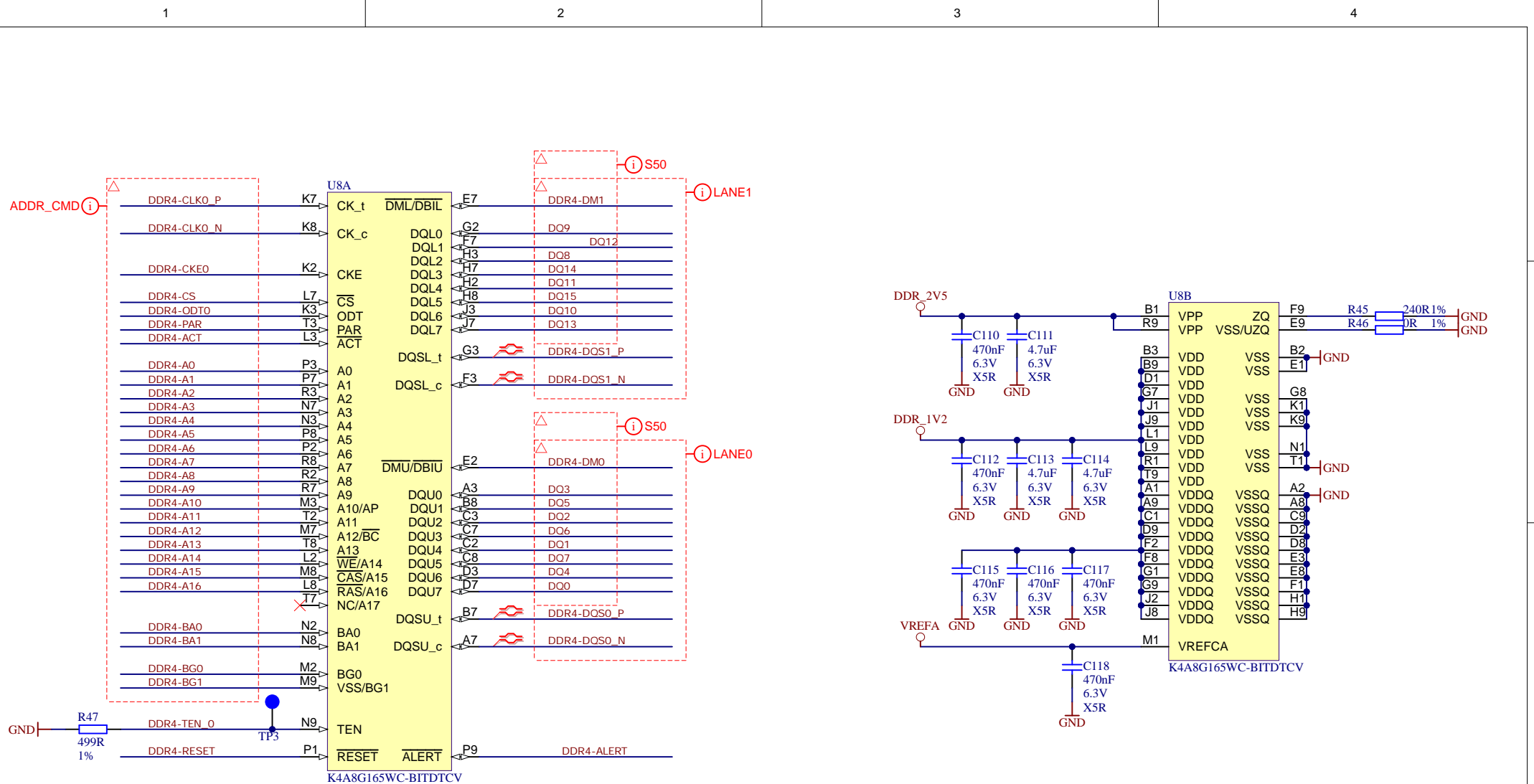
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Date: <b>2023-02-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>14</b> of <b>38</b>
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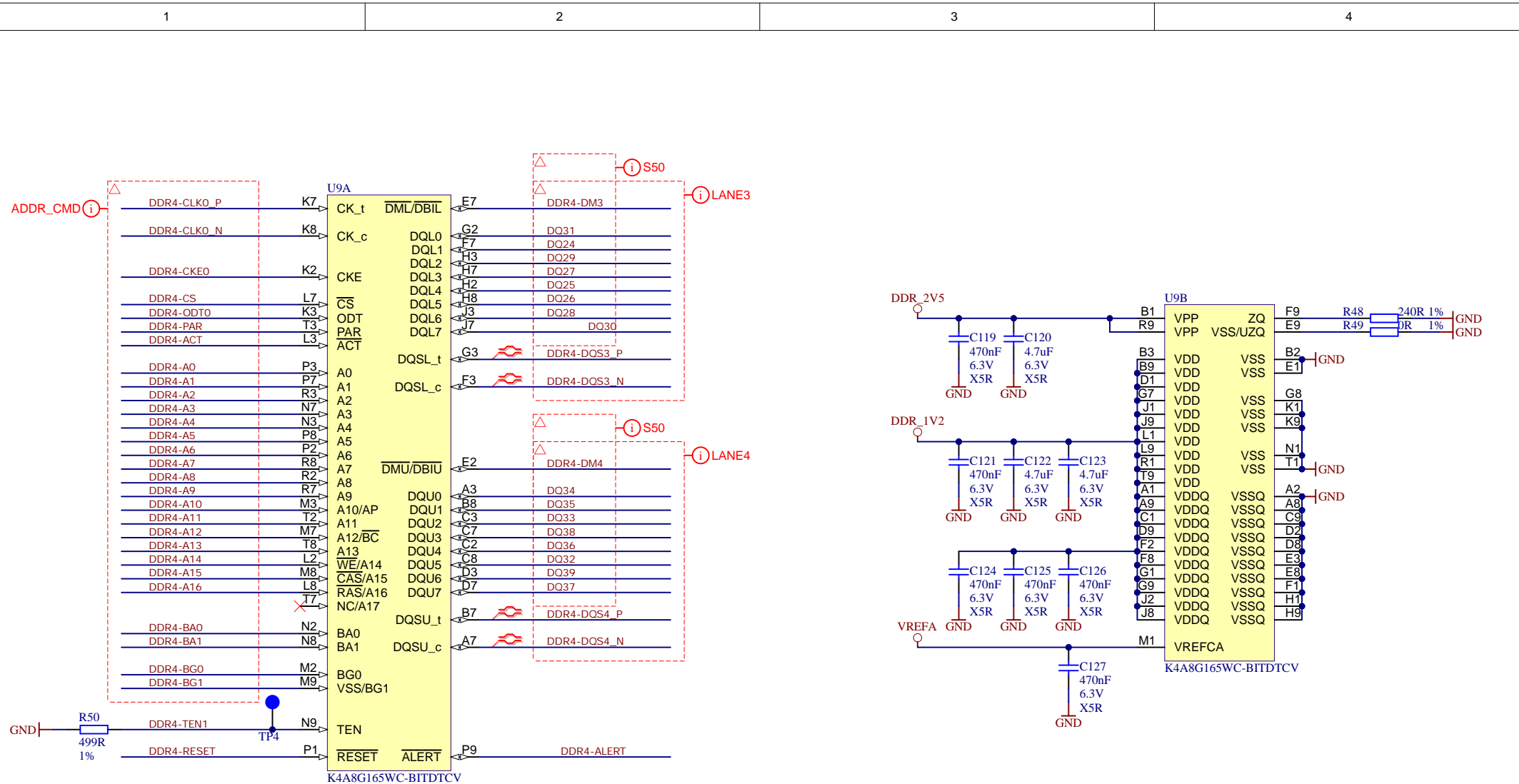
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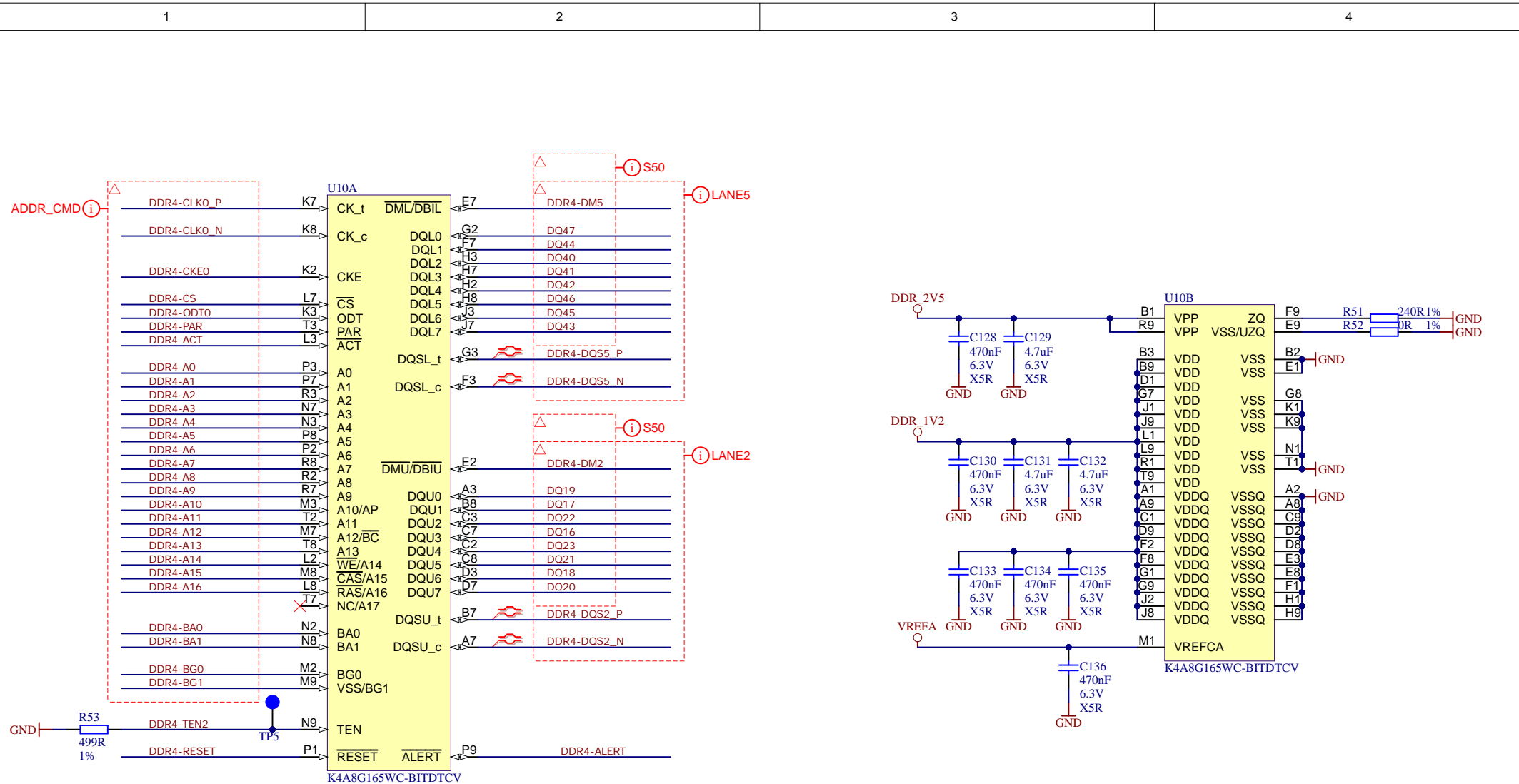
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- DDR4\_3.SchDoc
- DDR4\_4.SchDoc
- DDR4\_TERM.SchDoc


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Date: 2023-02-09		Copyright: Trenz Electronic GmbH	
Page 15 of 38		Page 15 of 38	
Filename: <b>DDR4_1.SchDoc</b>			

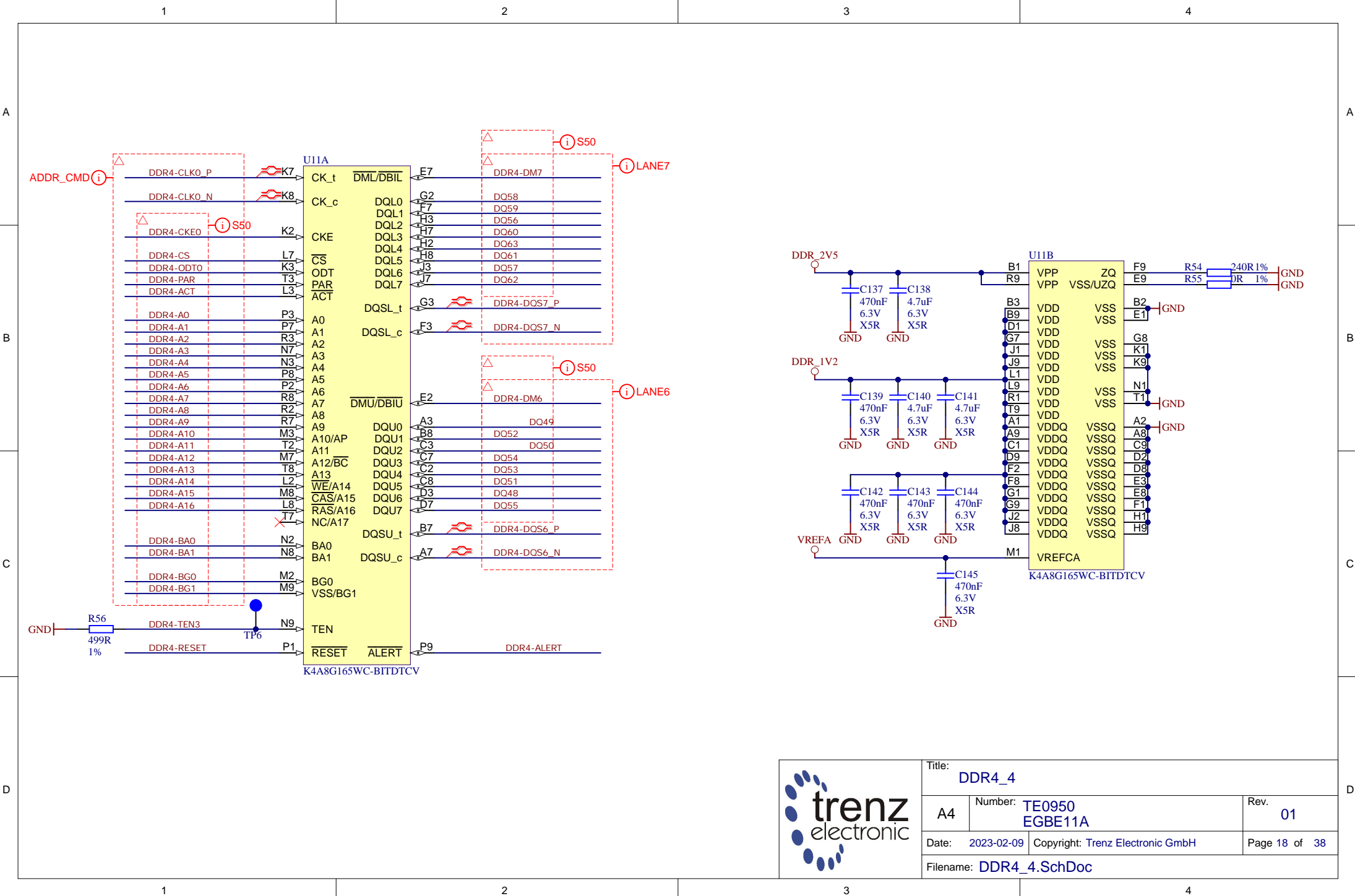



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Date: <b>2023-02-09</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>16</b> of <b>38</b>
Filename: <b>DDR4_2.SchDoc</b>				





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			A4	Number: <b>TE0950 EGBE11A</b>
Date: <b>2023-02-09</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>17</b> of <b>38</b>
Filename: <b>DDR4_3.SchDoc</b>				



		Title: <b>DDR4_4</b>	
		A4	Number: <b>TE0950</b> <b>EGBE11A</b>
Date: 2023-02-09		Copyright: Trenz Electronic GmbH	
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Filename: <b>DDR4_4.SchDoc</b>			

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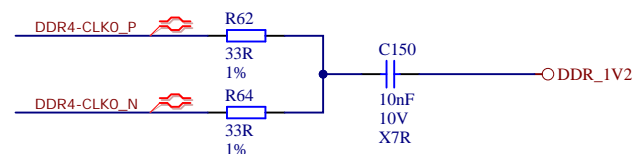
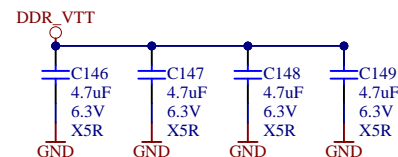
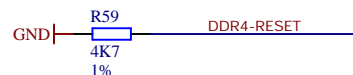
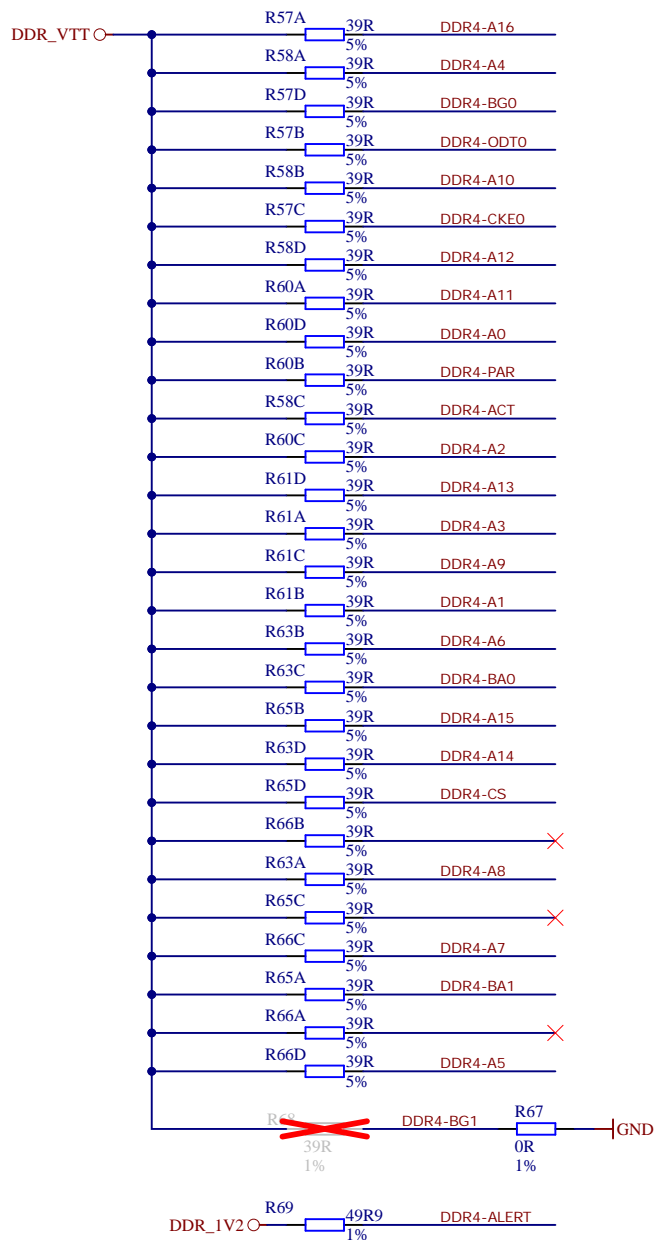
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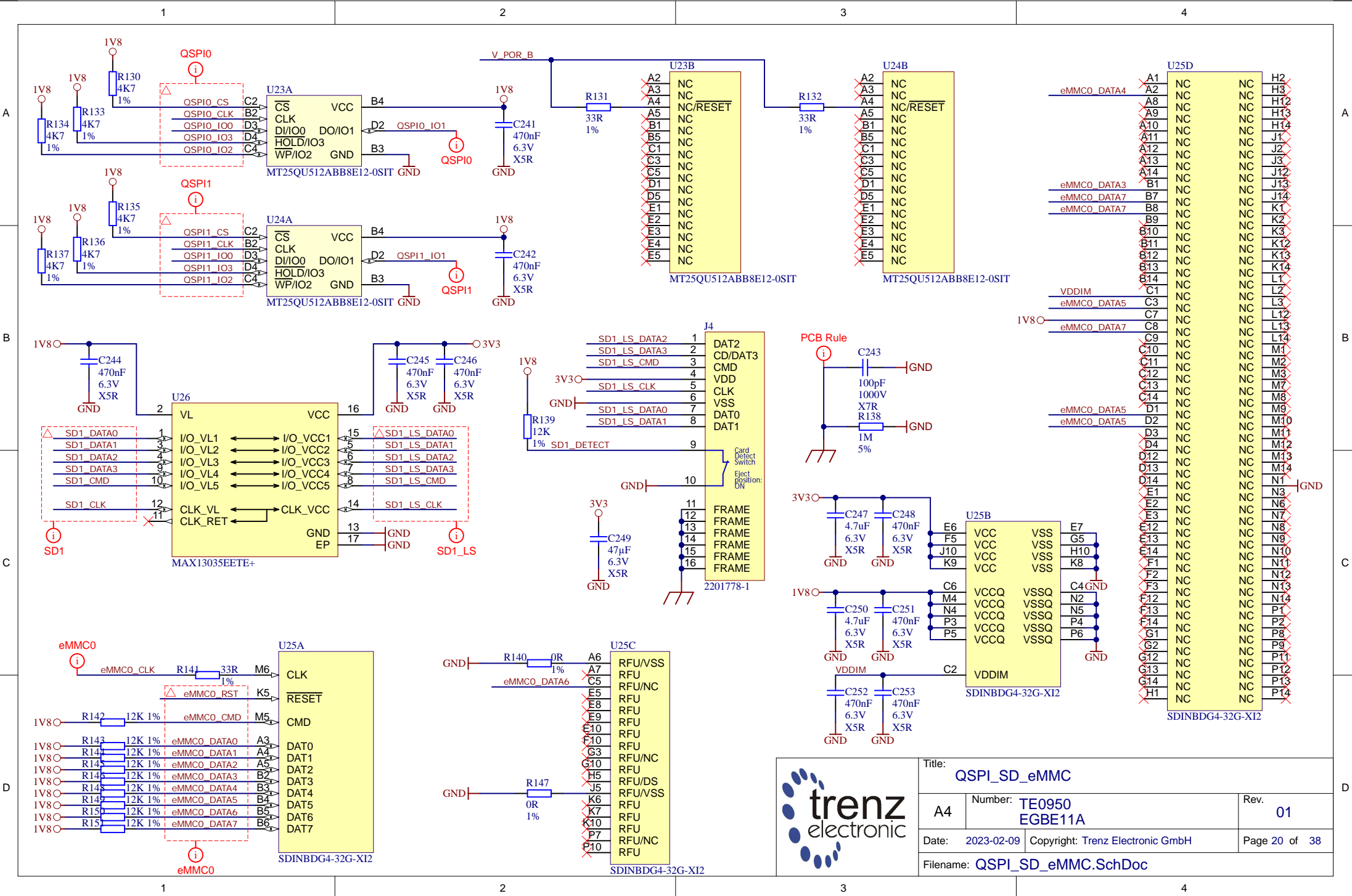
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Date: <b>2023-02-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>19</b> of <b>38</b>
Filename: <b>DDR4_TERM.SchDoc</b>		

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**trenz electronic**

Title: **QSPI\_SD\_eMMC**

A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
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Filename: <b>QSPI_SD_eMMC.SchDoc</b>		

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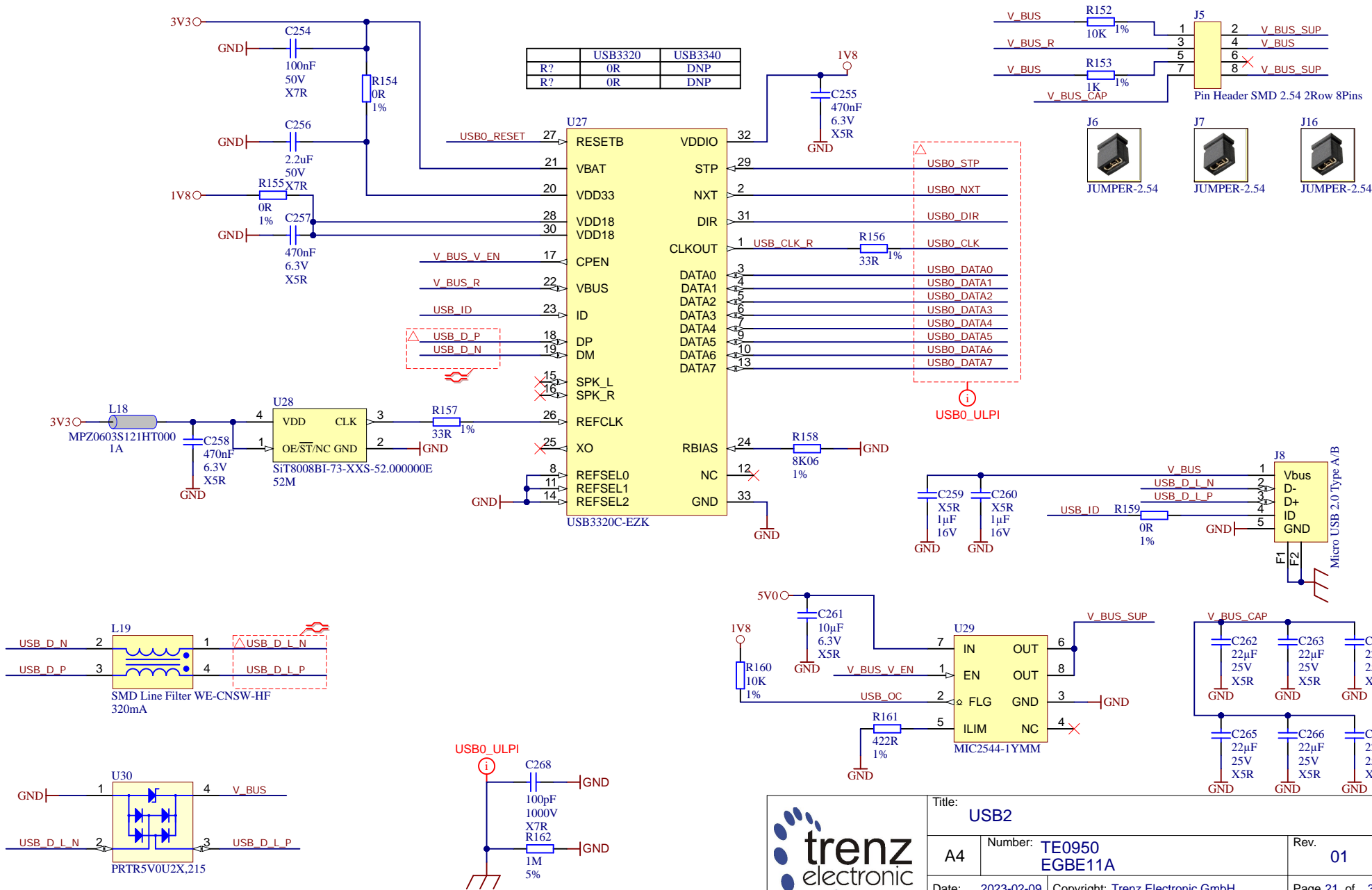
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Title: <b>USB2</b>		
A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
Date: 2023-02-09	Copyright: Trenz Electronic GmbH	Page 21 of 38
Filename: <b>USB2.SchDoc</b>		

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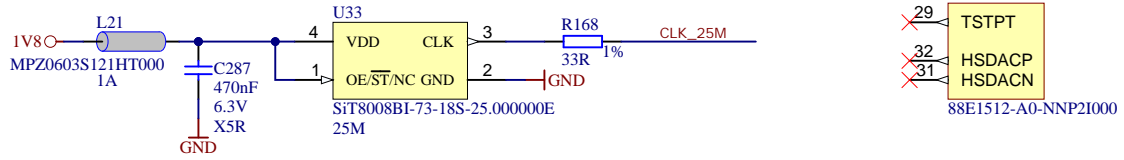
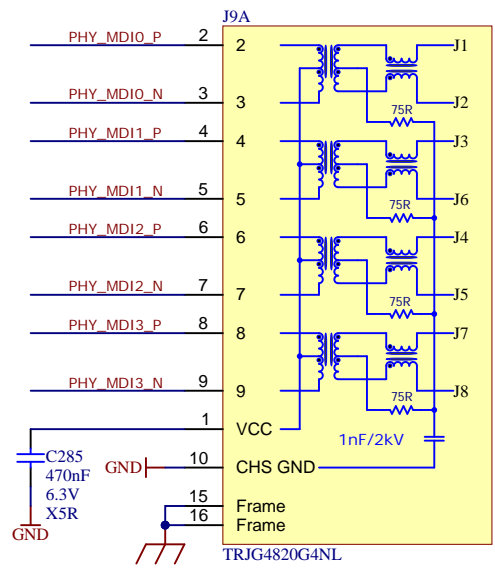
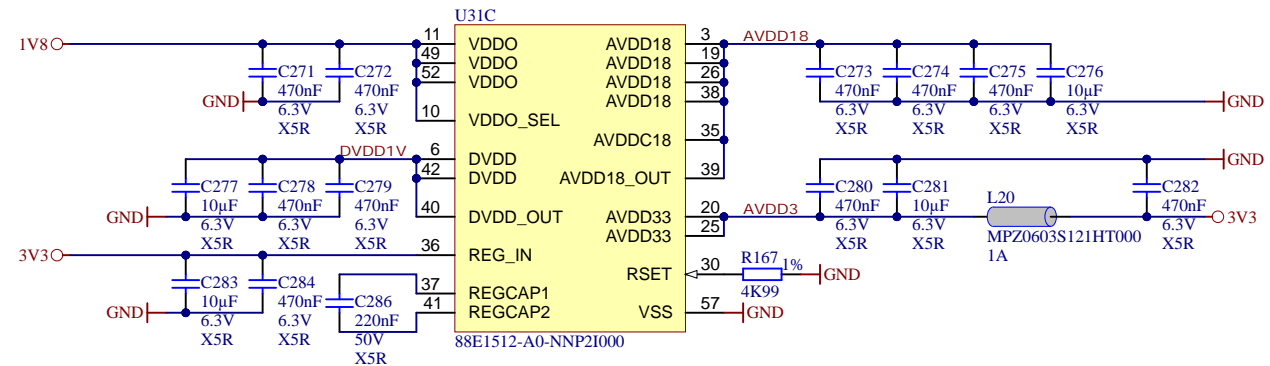
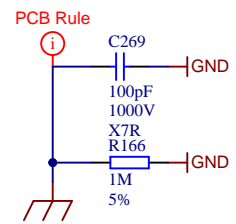
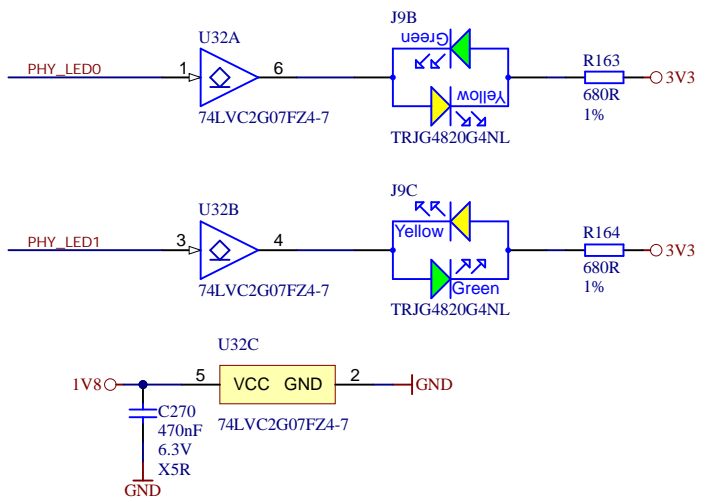
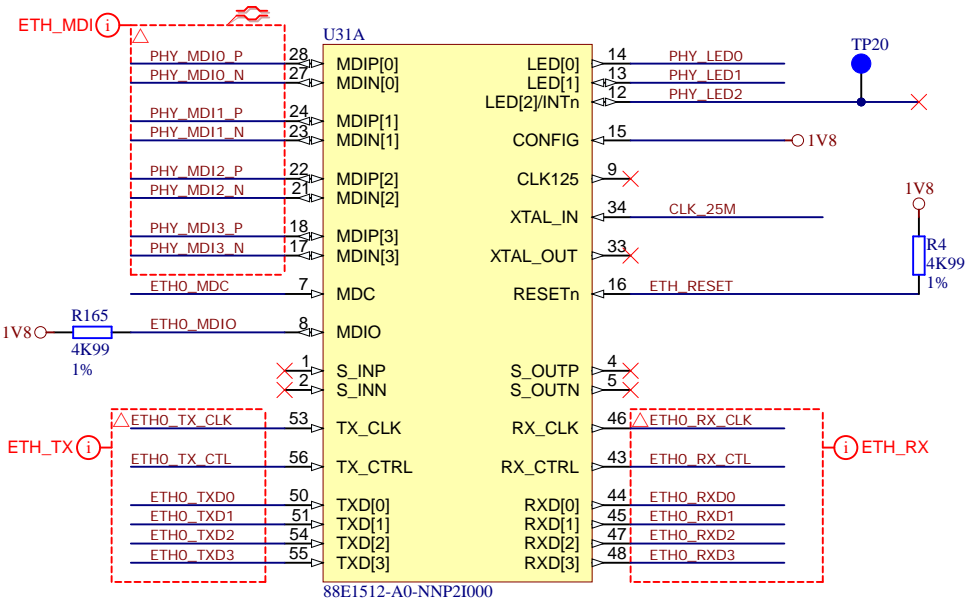
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Title: <b>GB_ETH</b>		
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Date: <b>2023-02-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>22</b> of <b>38</b>
Filename: <b>GB_ETH.SchDoc</b>		

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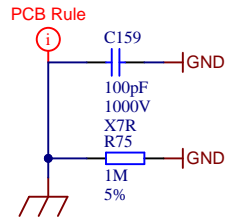
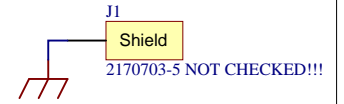
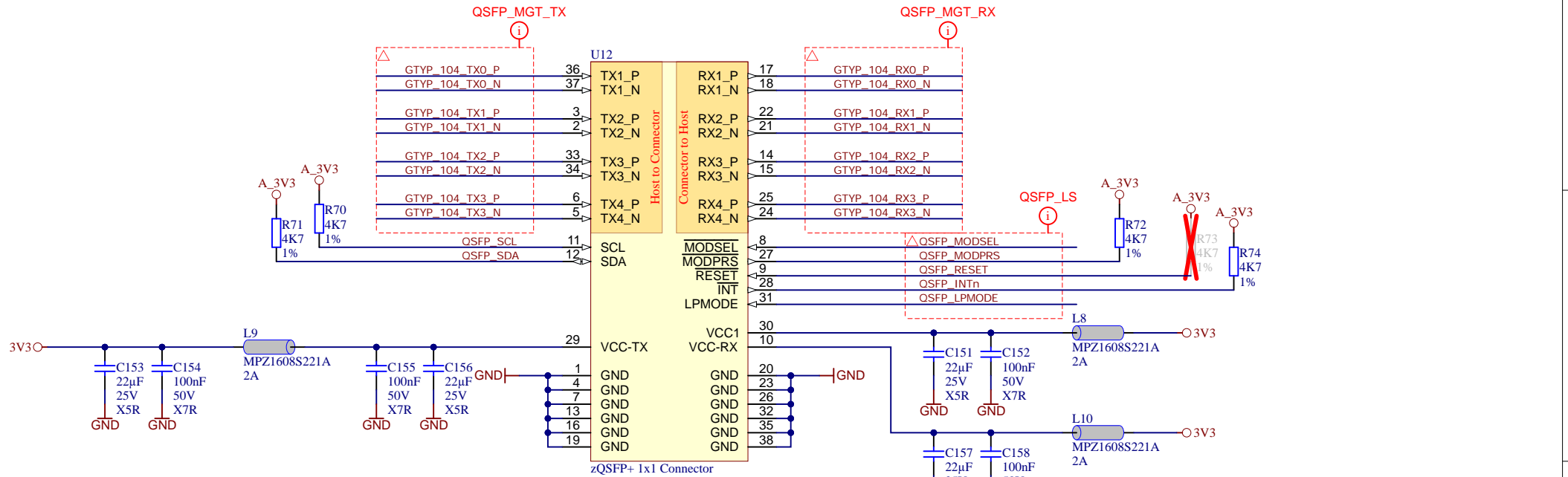
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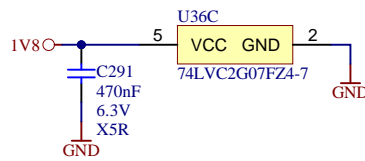
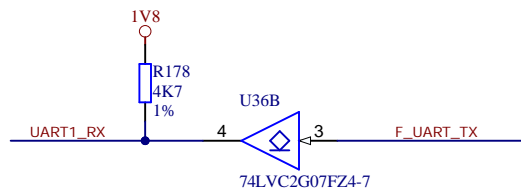
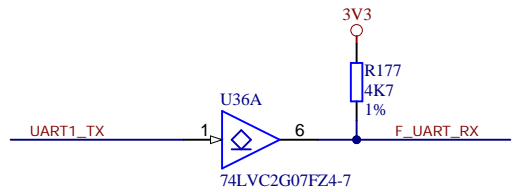
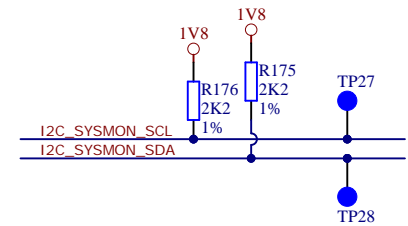
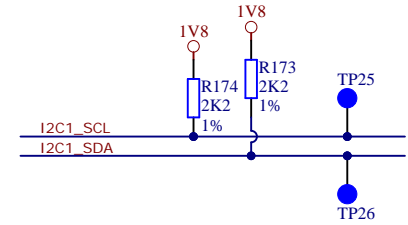
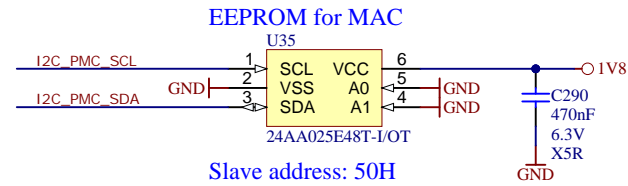
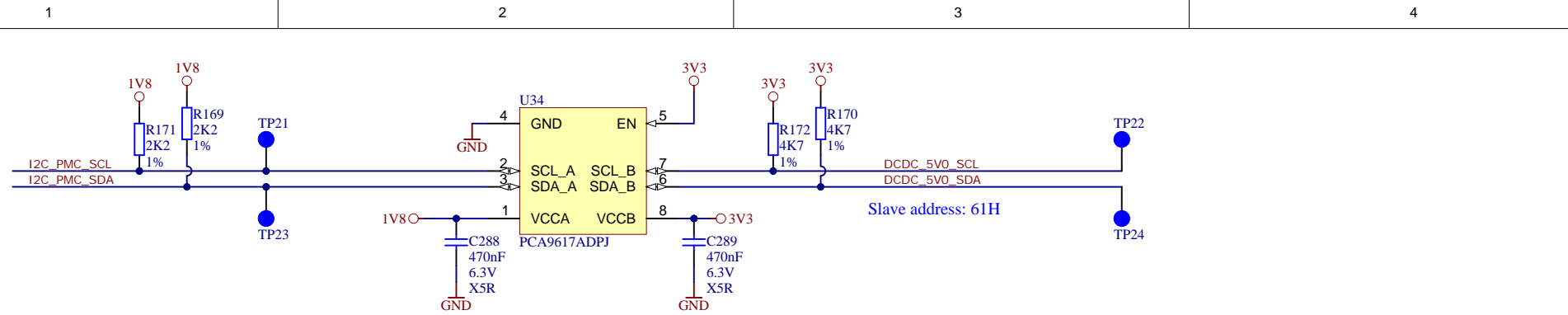
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	A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
	Date: <b>2023-02-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	
	Filename: <b>QSFP.SchDoc</b>		Page <b>23</b> of <b>37</b>

1

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4



Title: I2C		
A4	Number: TE0950 EGBE11A	Rev. 01
Date: 2023-02-09	Copyright: Trenz Electronic GmbH	Page 23 of 38
Filename: I2C.SchDoc		



1

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A

A

B

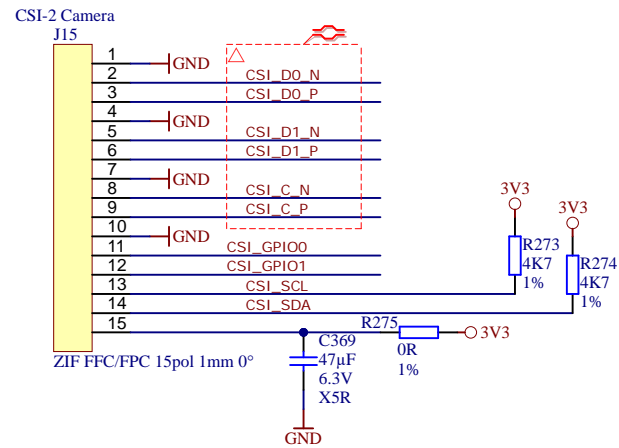
B


C

C

D

D



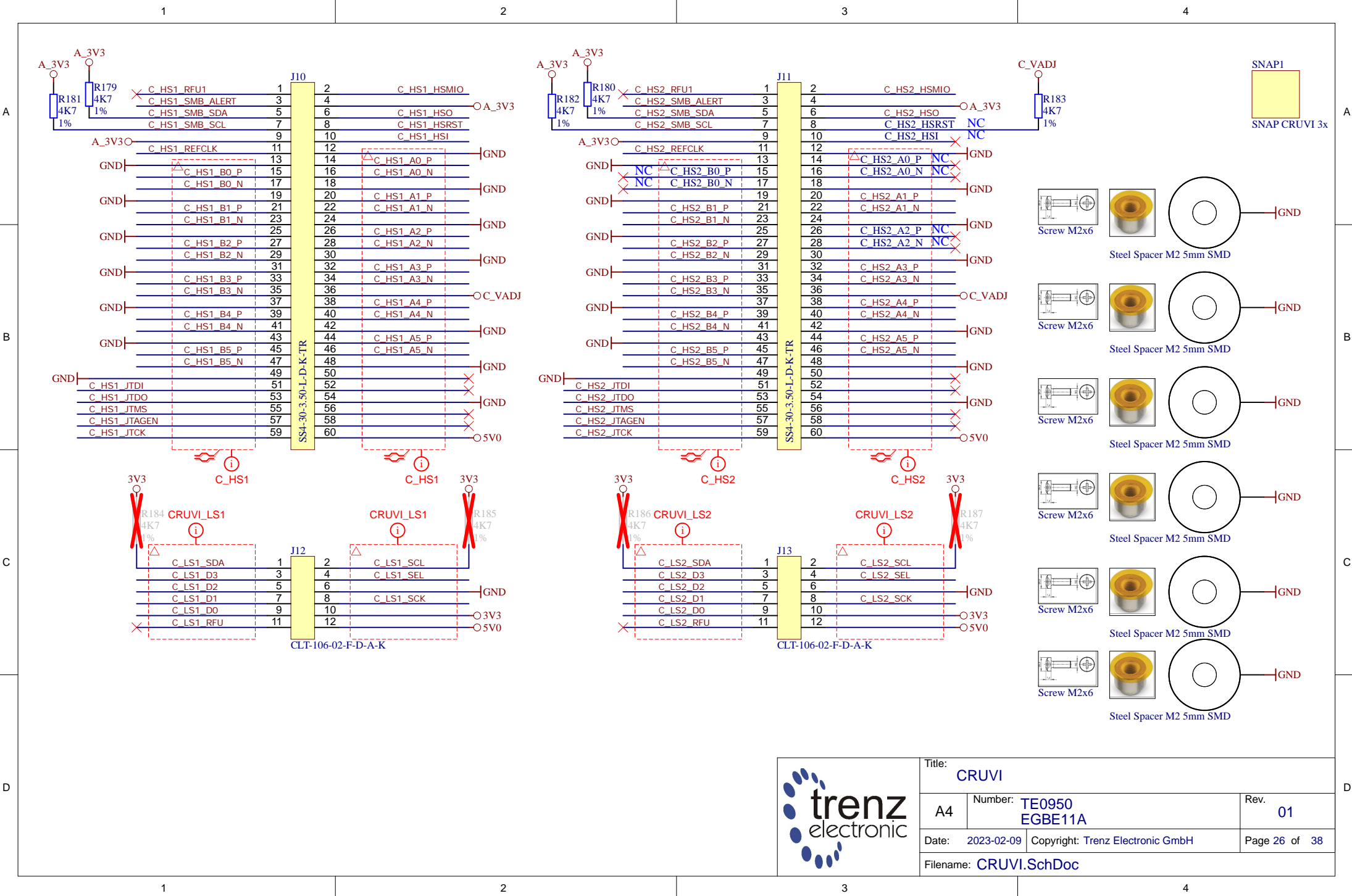
	Title: CSI2_CAM		
	A4	Number: TE0950 EGBE11A	Rev. 01
	Date: 2023-02-09	Copyright: Trenz Electronic GmbH	Page 25 of 38
	Filename: CSI2_CAM.SchDoc		

1

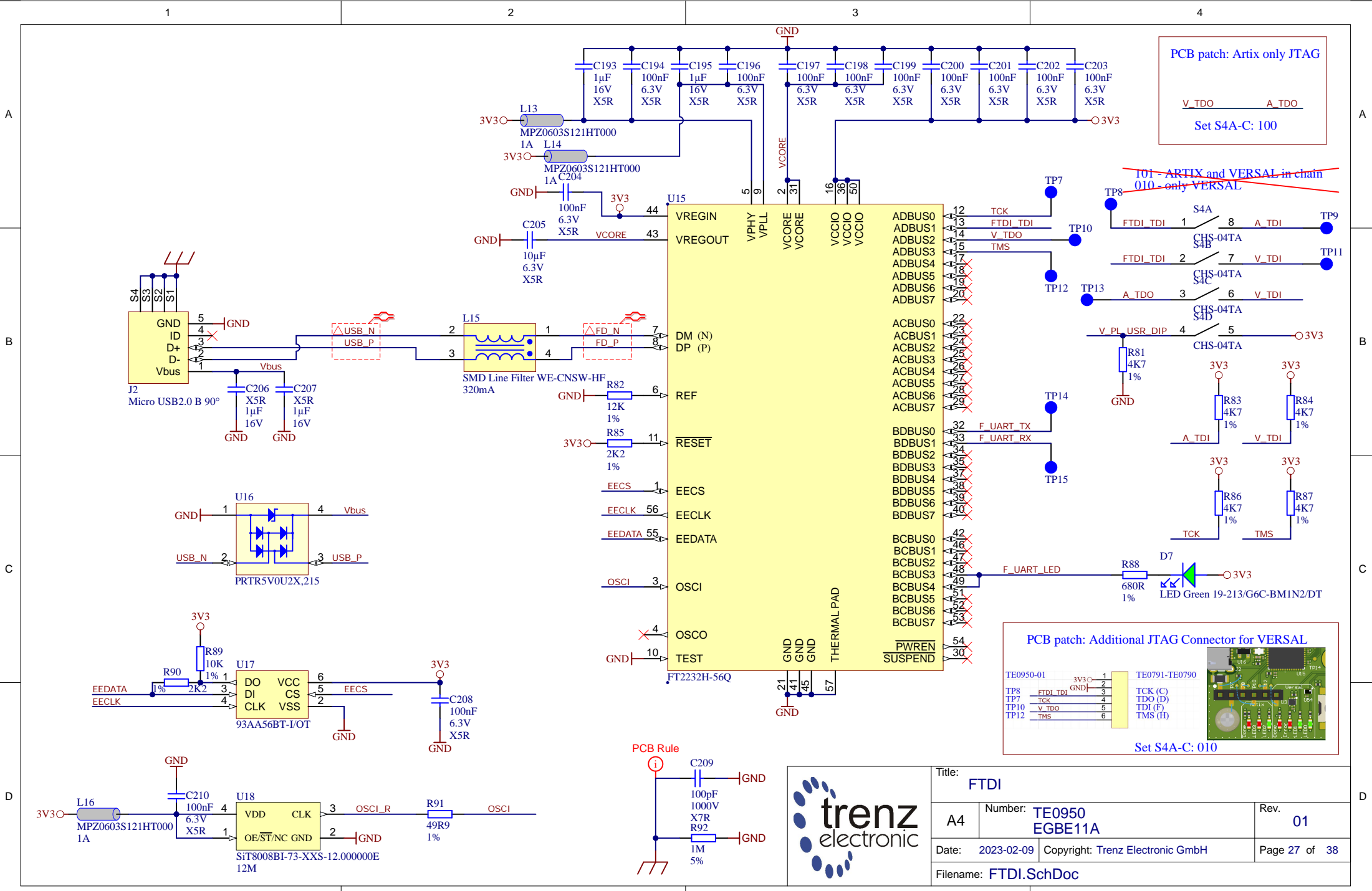
2

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4



Title: <b>CRUVI</b>		
A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
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Filename: <b>CRUVI.SchDoc</b>		Page <b>26</b> of <b>38</b>



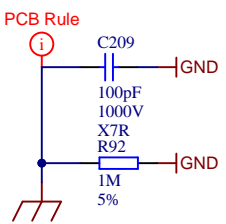
PCB patch: Artix only JTAG  
 V\_TDO \_\_\_\_\_ A\_TDO  
 Set S4A-C: 100

~~101 - ARTIX and VERSAL in chain  
 010 - only VERSAL~~

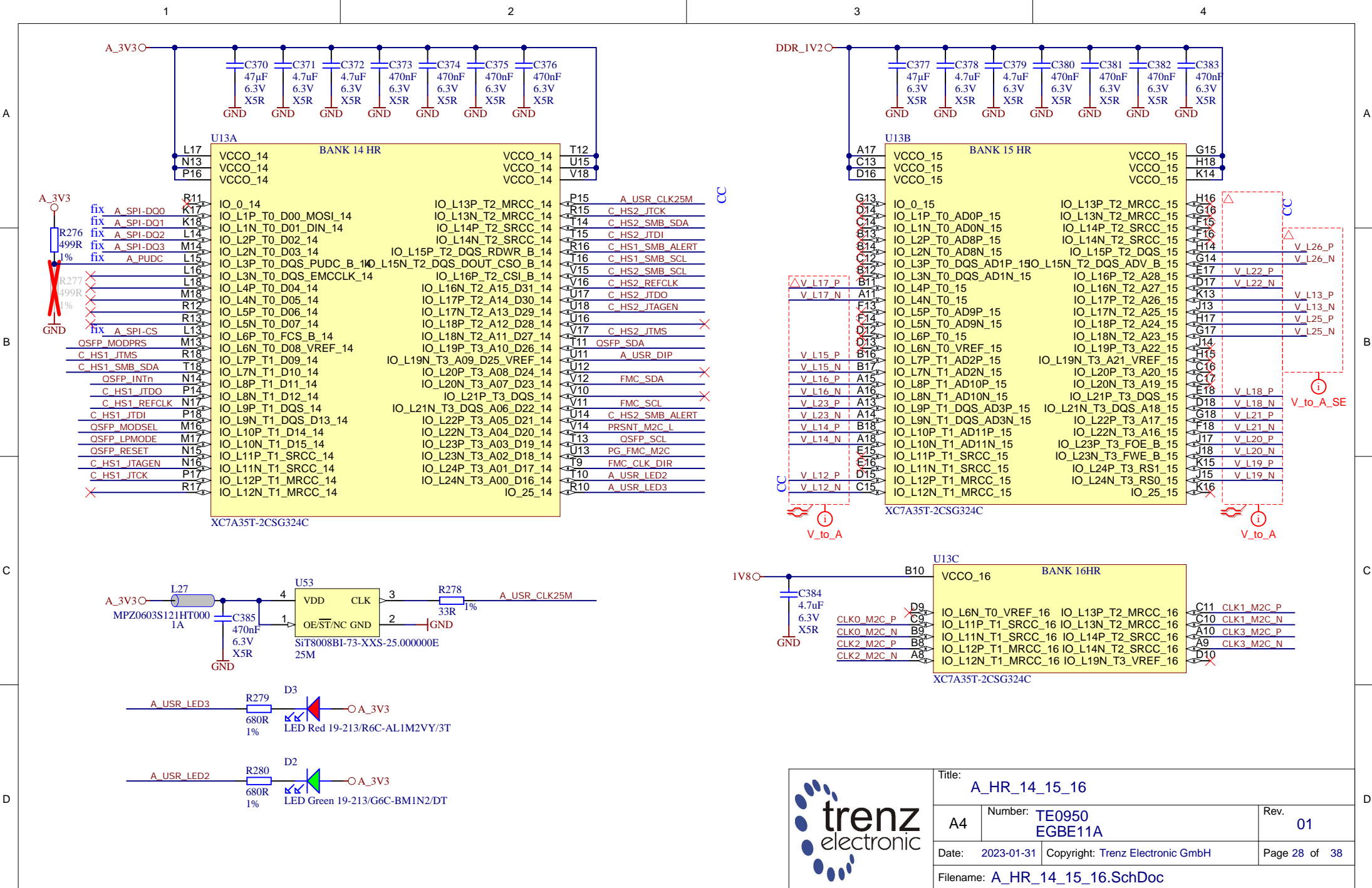
PCB patch: Additional JTAG Connector for VERSAL

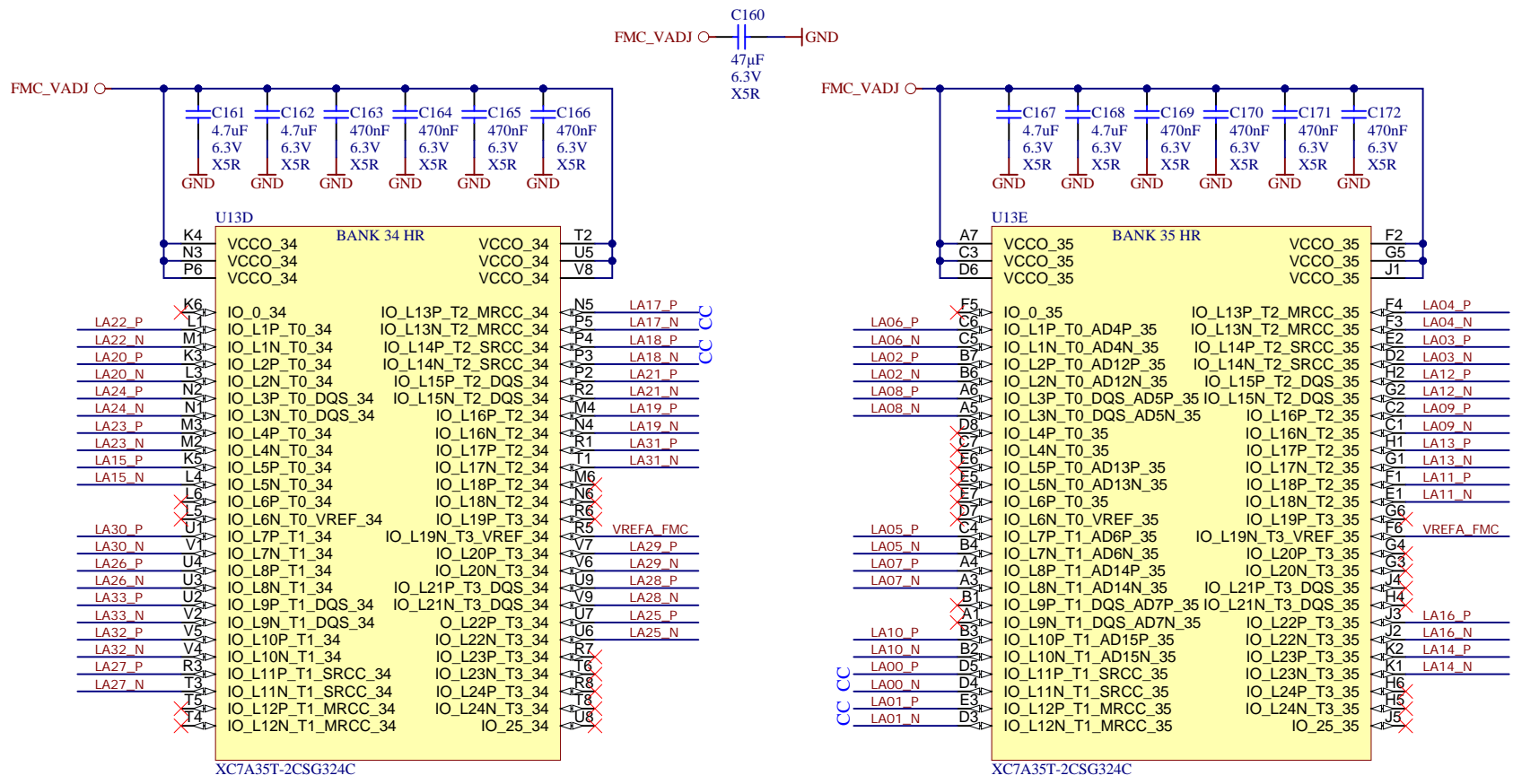
TE0950-01	3V3	1	TE0791-TE0790
TP8	FTDI_TDI	2	TCK (C)
TP7	TCK	3	TDO (D)
TP10	V_TDO	4	TDI (F)
TP12	TMS	6	TMS (H)


Set S4A-C: 010

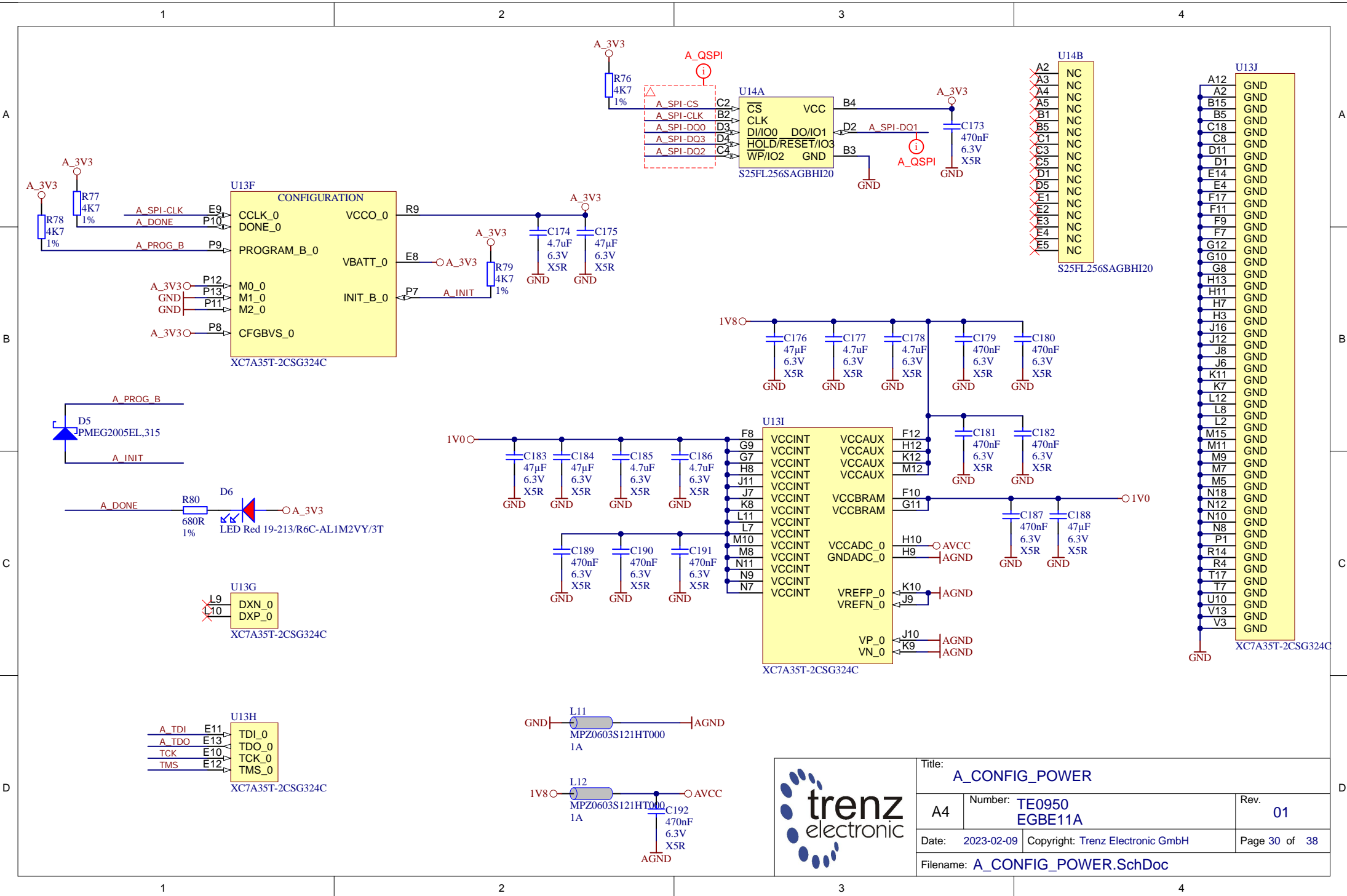



Title: <b>FTDI</b>		
A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
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Filename: <b>FTDI.SchDoc</b>		





		Title: A_HR_34_35	
		A4	Number: TE0950 EGBE11A
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		Title: <b>A_CONFIG_POWER</b>	
		A4	Number: <b>TE0950 EGBE11A</b>
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Filename: <b>A_CONFIG_POWER.SchDoc</b>		Page 30 of 38	

1

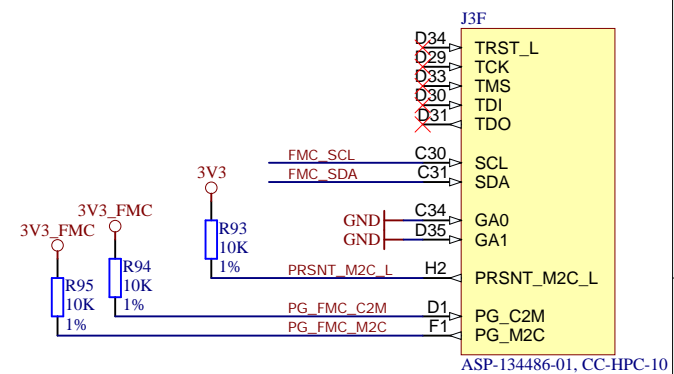
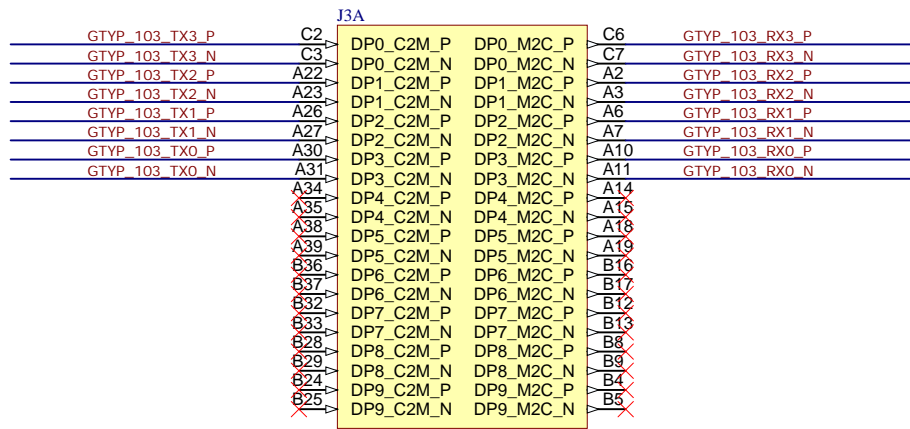
2

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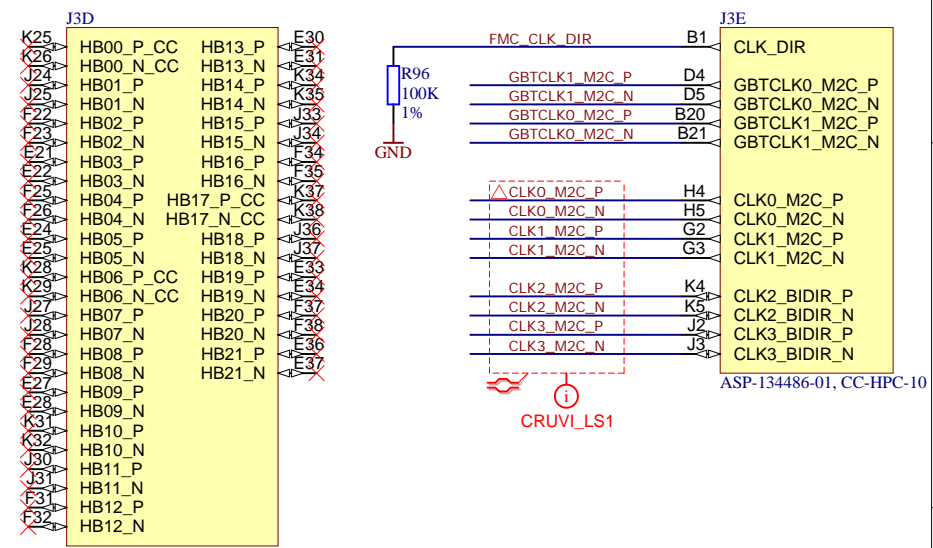
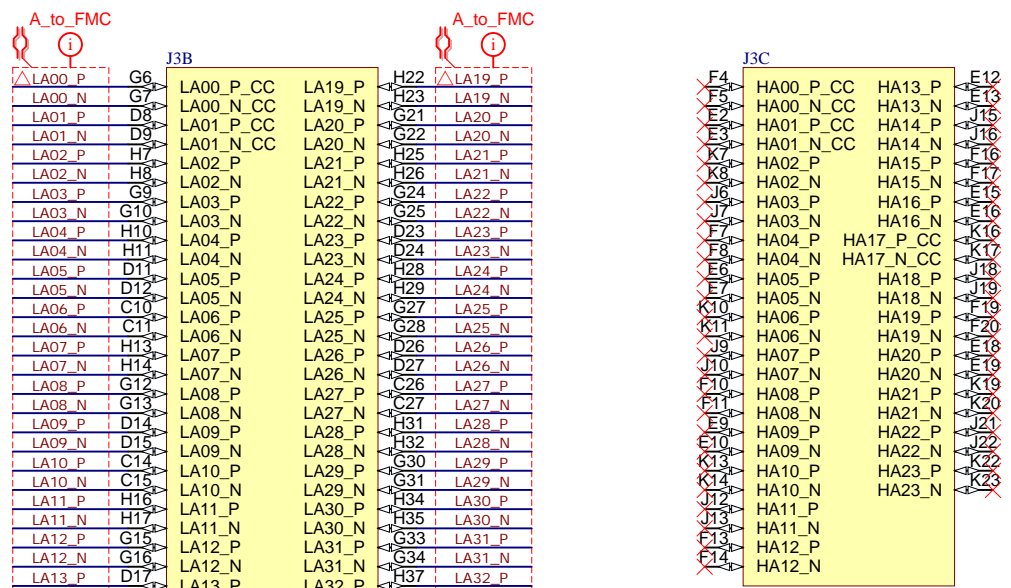
A

A



B

B



C

C

D

D

**trenz electronic**

Title: <b>FMC</b>		
A4	Number: <b>TE0950 EGBE11A</b>	Rev: <b>01</b>
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Filename: <b>FMC.SchDoc</b>		

1

2

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1

2

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A

A

B

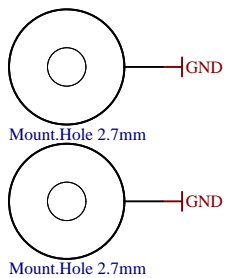
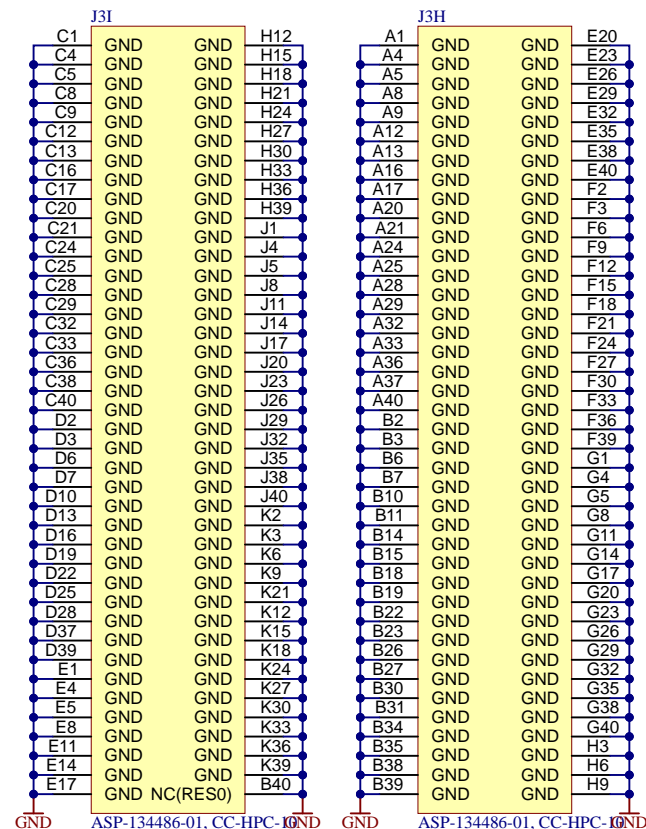
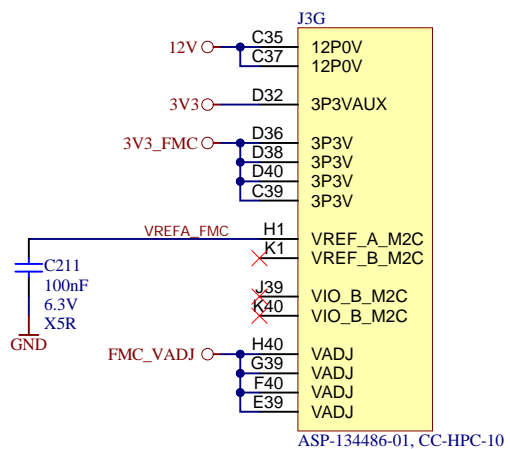
B

C

C

D

D



Title: <b>FMC_Power</b>		
A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
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Filename: <b>FMC_Power.SchDoc</b>		

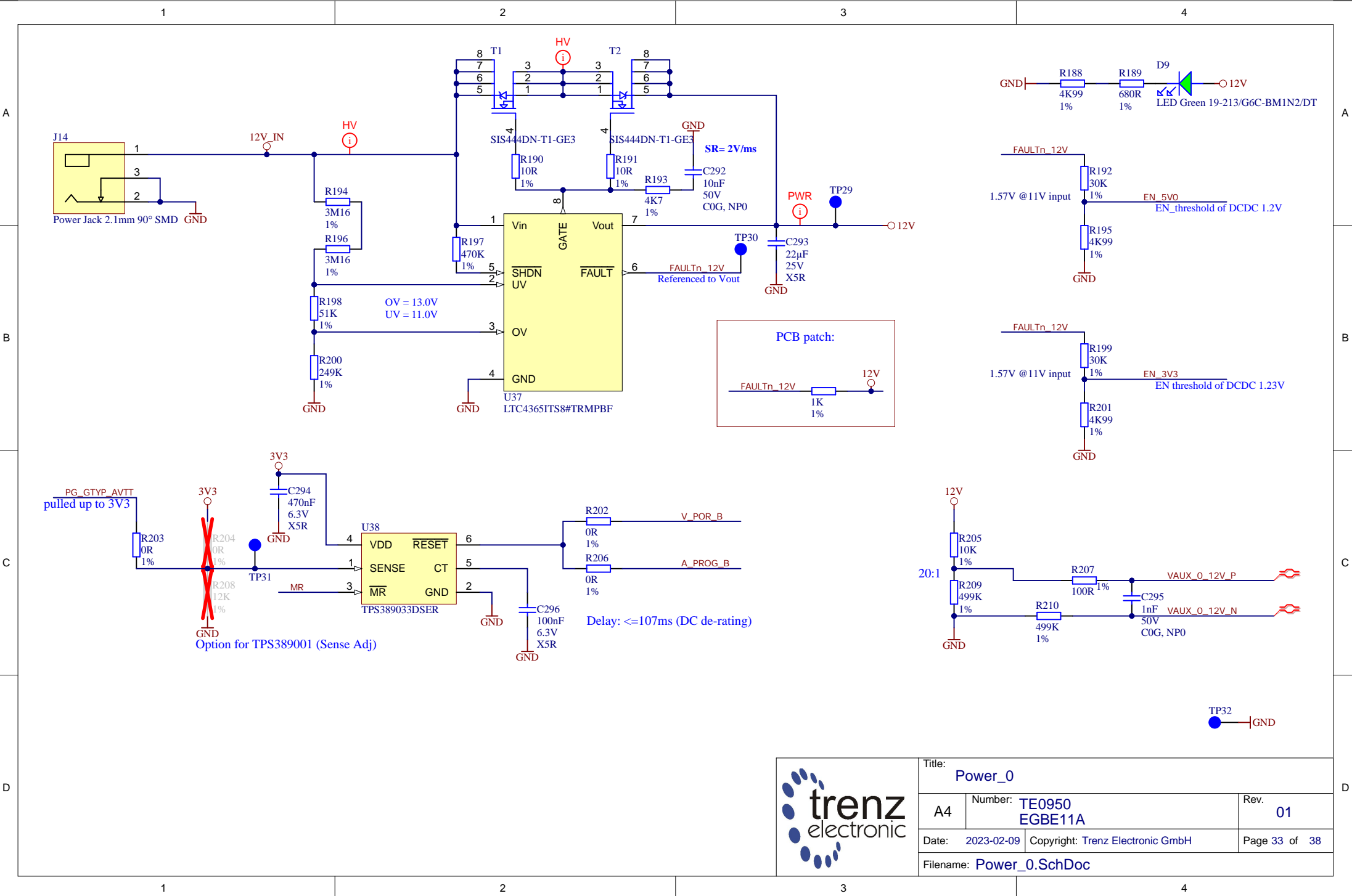
1

2

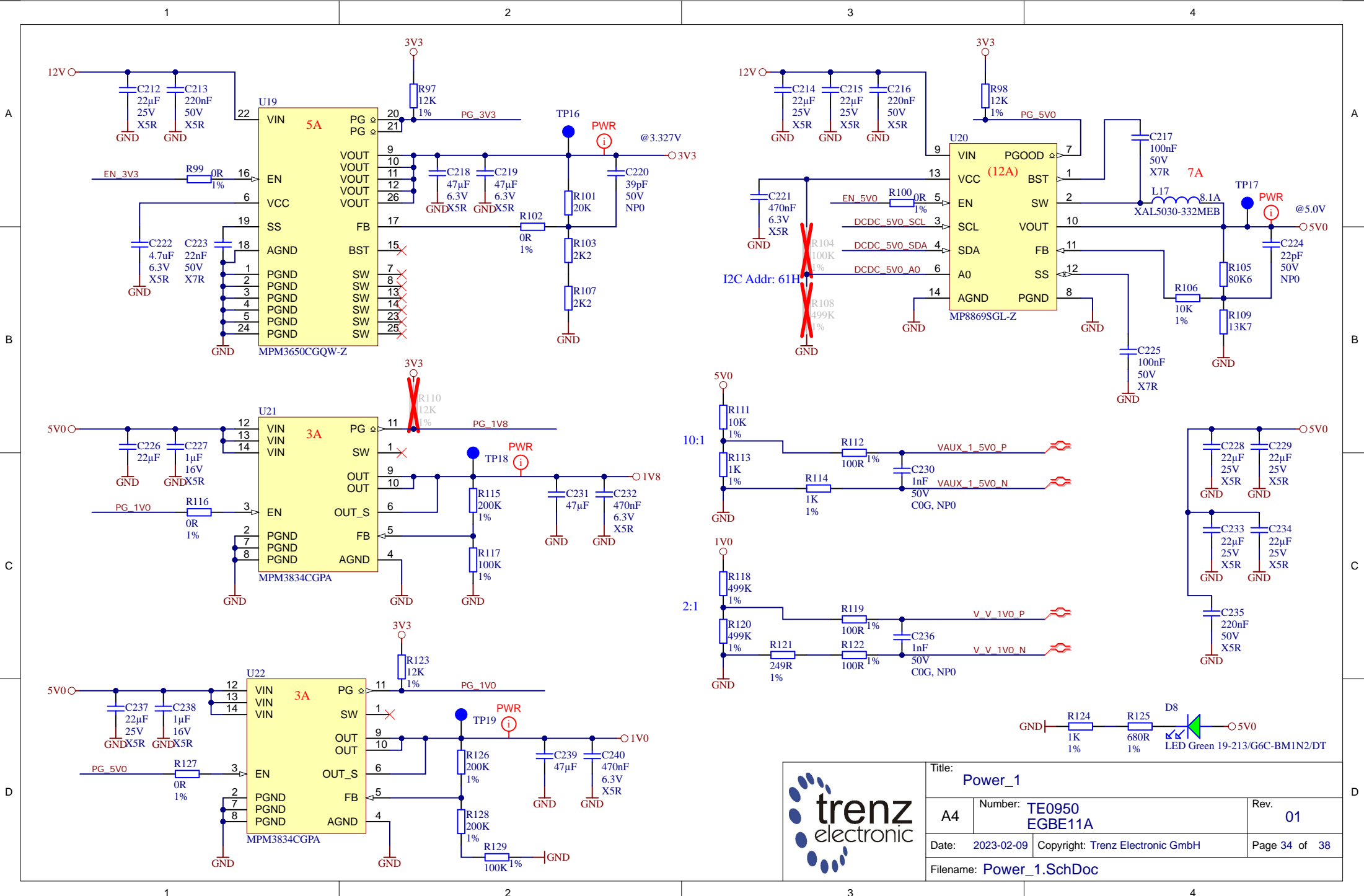
3

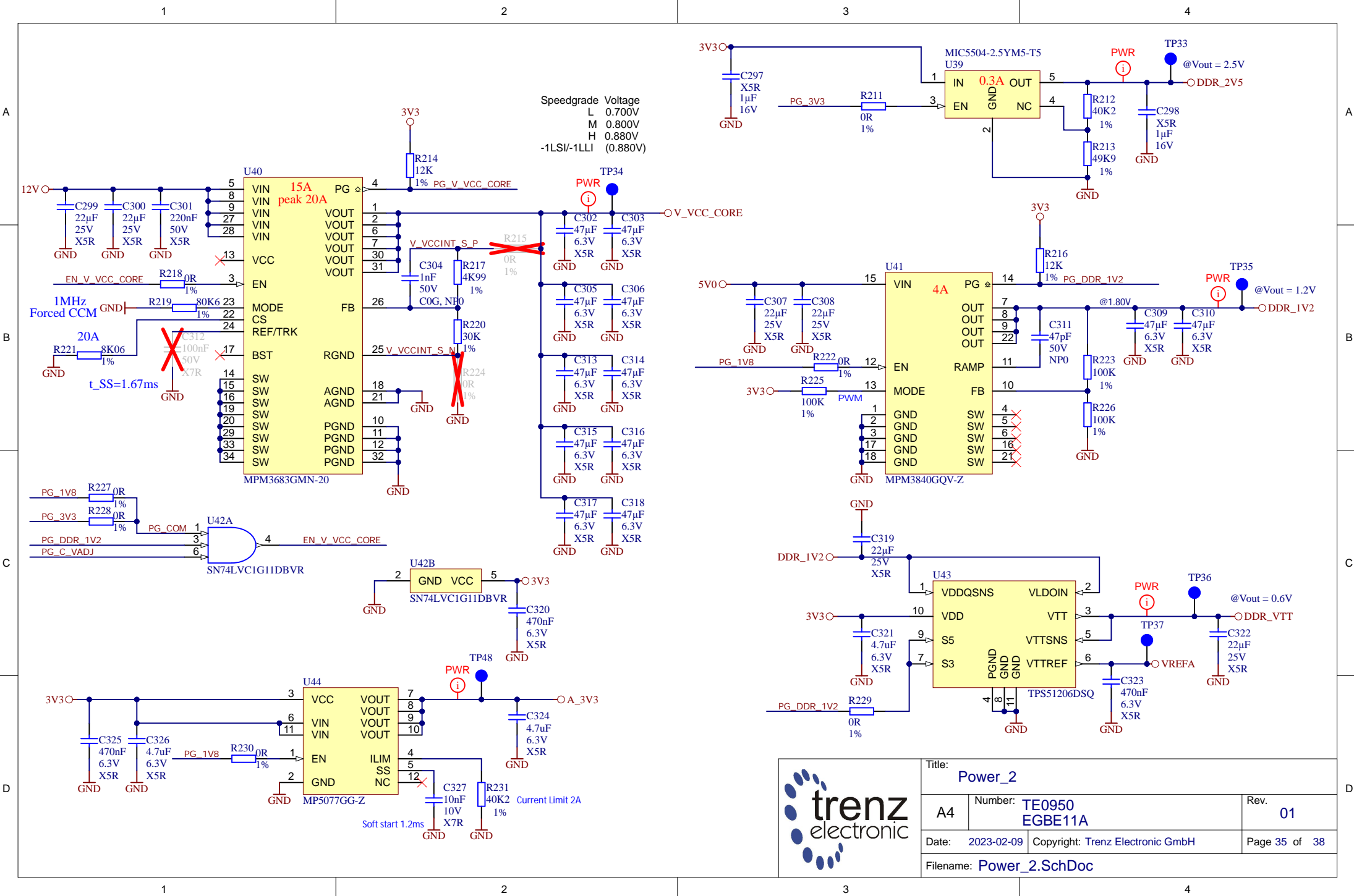
4





Title: Power_0		
A4	Number: TE0950 EGBE11A	Rev. 01
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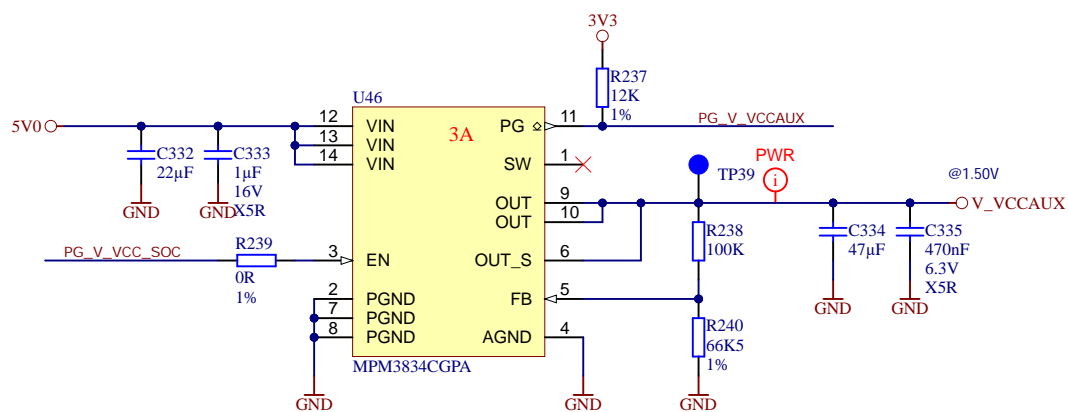
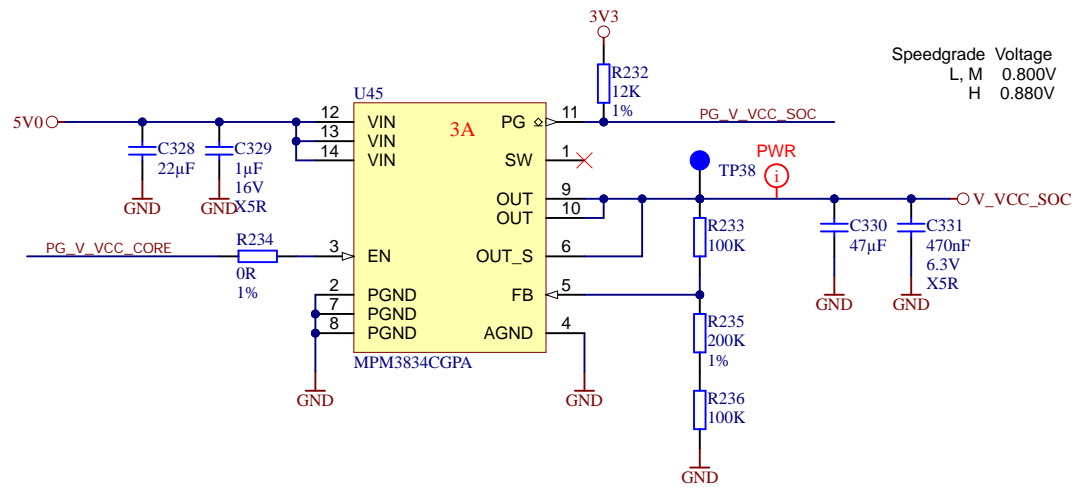




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Title: Power\_2

A4	Number: TE0950 EGBE11A	Rev: 01
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Title: Power_3		
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1

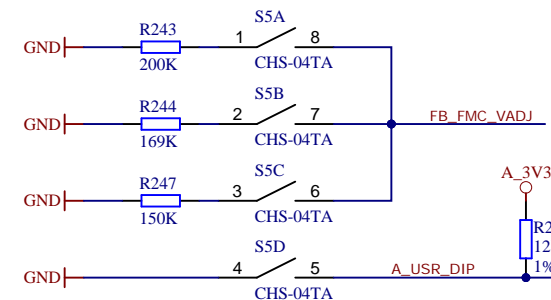
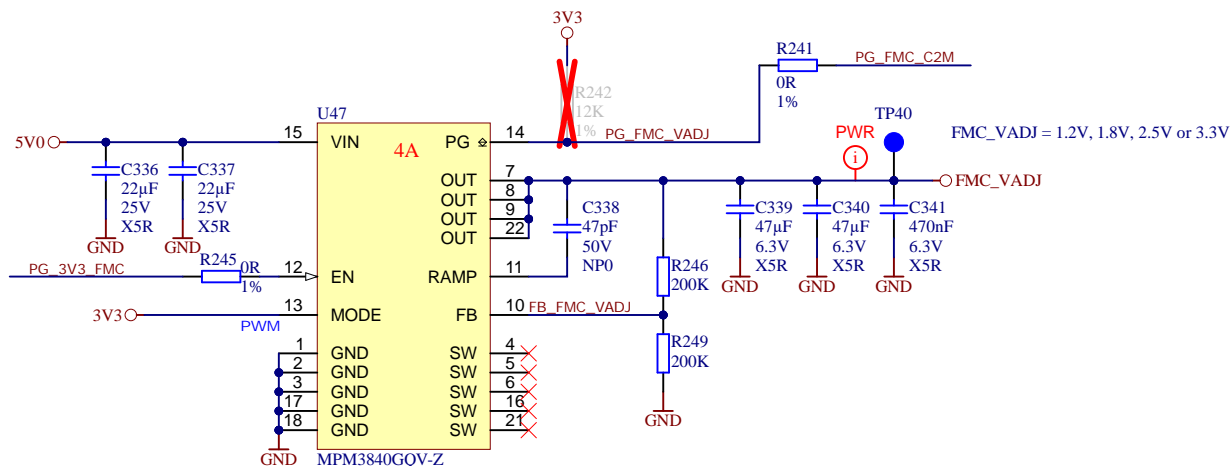
2

3

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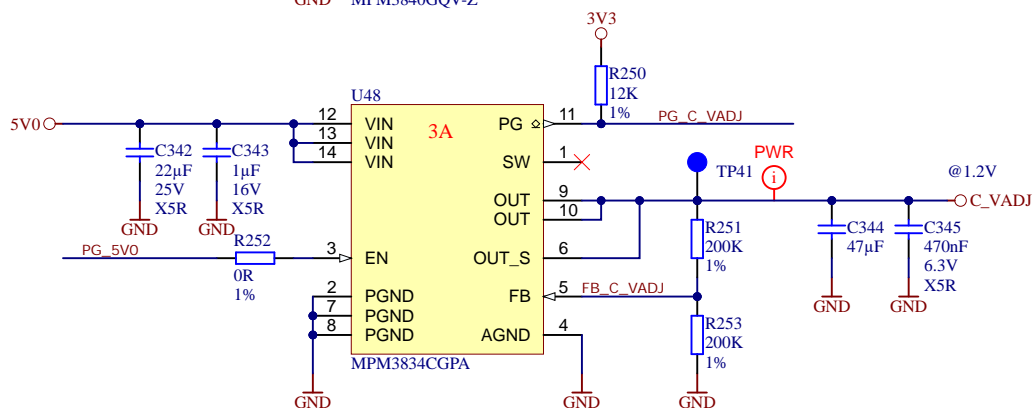
A

A



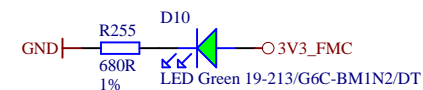
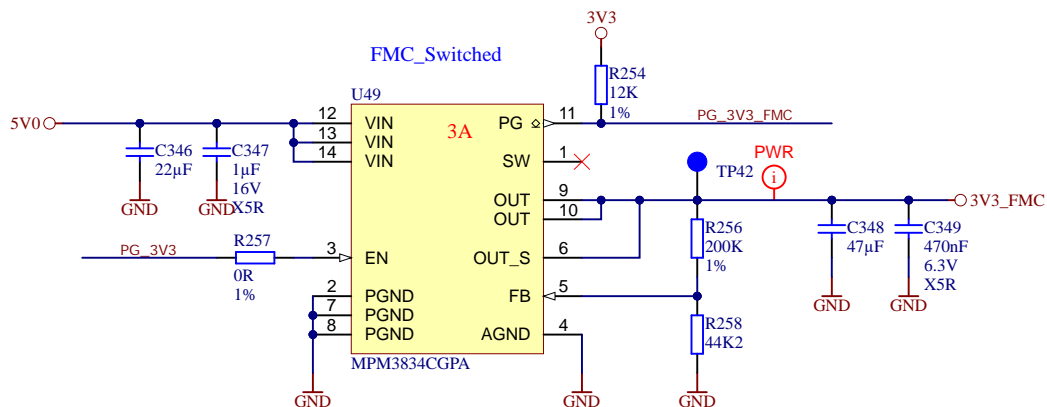
B

B



C

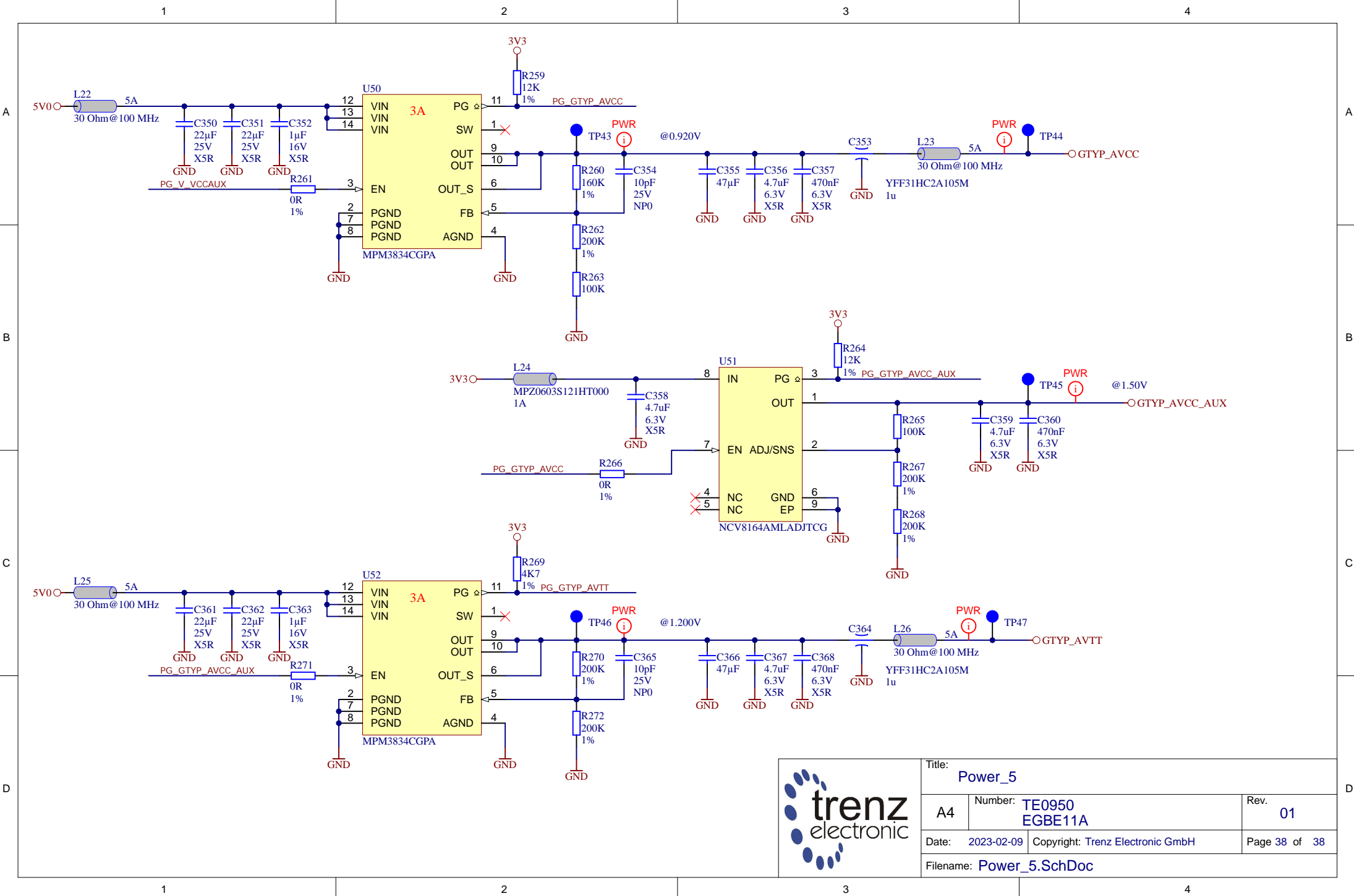
C



D

D

Title: <b>Power_4</b>		
A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
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Filename: <b>Power_4.SchDoc</b>		



Title: <b>Power_5</b>		
A4	Number: <b>TE0950 EGBE11A</b>	Rev. <b>01</b>
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Filename: <b>Power_5.SchDoc</b>		