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Schematics and other handouts serve for informational purposes only!

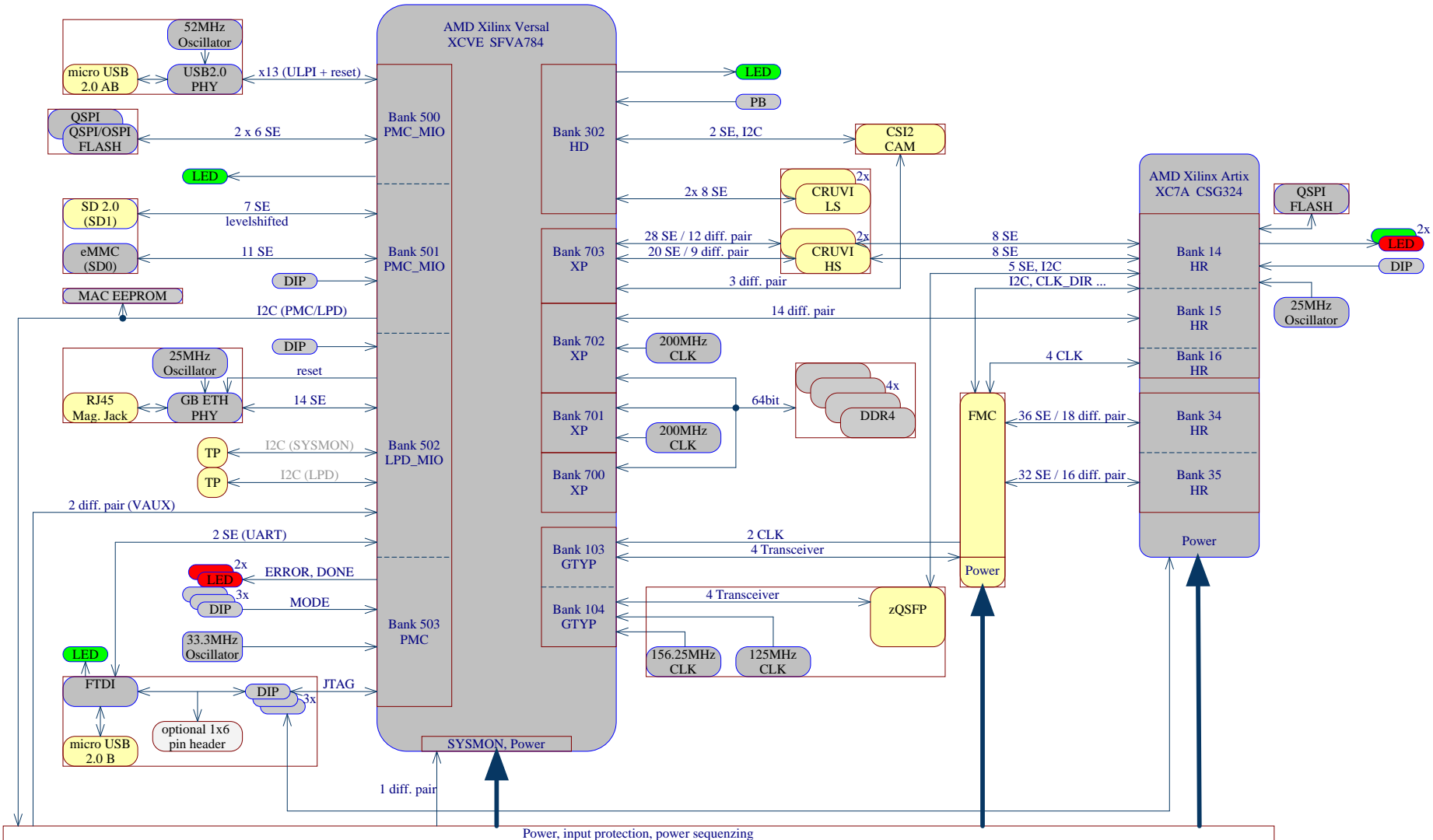
Drawn by	MR
Checked by	ED
Assembly variant	EGBE21A
Created by	MR
Modified by	MR
Modified at	2023-11-22



Title: Legal Notices		
A4	Number: TE0950 EGBE21A	Rev. 03
Date: 12.01.2024	Copyright: Trenz Electronic GmbH	Page 1 of 39
Filename: Legal Notices TE0950.SchDoc		

REV	Description	
-01	Initial revision	MR
-02	<ol style="list-style-type: none"> 1. Inverted card detect (pullup-> pulldown) 2. Increased number of capacitors on VTT (C388,C389) 3. Added 1K pullup on FAULTn_12V (R5) 4. Added 4-pin connector J17 for FAN and corresponding circuit. PWM and TACHO connected to ARTIX 5. VERSAL JTAG connection corrected 6. Added CRUVI Connector description on silkscreen 7. Changed polarity for CSI2-CAM diff pairs 8. Update from library 9. Changed R266 to 12K and added R281 10. Changed enable 3V3 after 5V0 (R99), Pullup on PG_5V0 connected to 5V0 rail. 11. Replaced C256 (2,2µF) by 2x 1µF 12. Set R131 and R132 to not fitted (2023-08-18) 	MR
-03	<ol style="list-style-type: none"> 1. Added OSPI compatibility, renamed sheet (QSPL_SD_eMMcC -> SD_eMMcC) and added sheet QSPL_OSPI. Added boot mode "OSPI" selectable via dip S2C, former connection (User PMC MIO27) moved to S4D. 2. Added D12 and pull-up R170 for correct reset levels, set R131 and R132 to assembled 3. Added Pin header J18 for direct JTAG access 4. Moved V_L22 diff. pair to clock capable pins on Atrix 5. Small improvements of MGT routing, added anti-pads, optimized VIAs, increased clearance. 6. Versal changed from Engineering Sample to production (pre-production for ES9749) chips 7. Replaced U20 by IR3899A DCDC 8. Removed U34 (I2C levelshifter for former U20) 9. Added Common mode chock L29, Fuse F1, C288, C289 and D13 to 12V input rail. 10. Moved PM1, PM2, PM5, PM6 11. Silkscreen dip switch description: <ul style="list-style-type: none"> - added OSPI boot mode, - S4D is user dip switch connected to Versal PMC (MIO27) 12. Updated all components from lib (2024-02-15) 13. Set ZigZag Placeholder for JTAG (J18) to not fitted to make it more clear that there is no header fitted 14. Updated AMD Versal (U1) Schematic Symbol 	MR

	Title: Revision History		
	A4	Number: TE0950 EGBE21A	Rev. 03
	Date: 15.02.2024	Copyright: Trenz Electronic GmbH	Page 2 of 39
	Filename: Revision Changes.SchDoc		

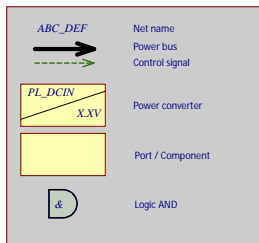
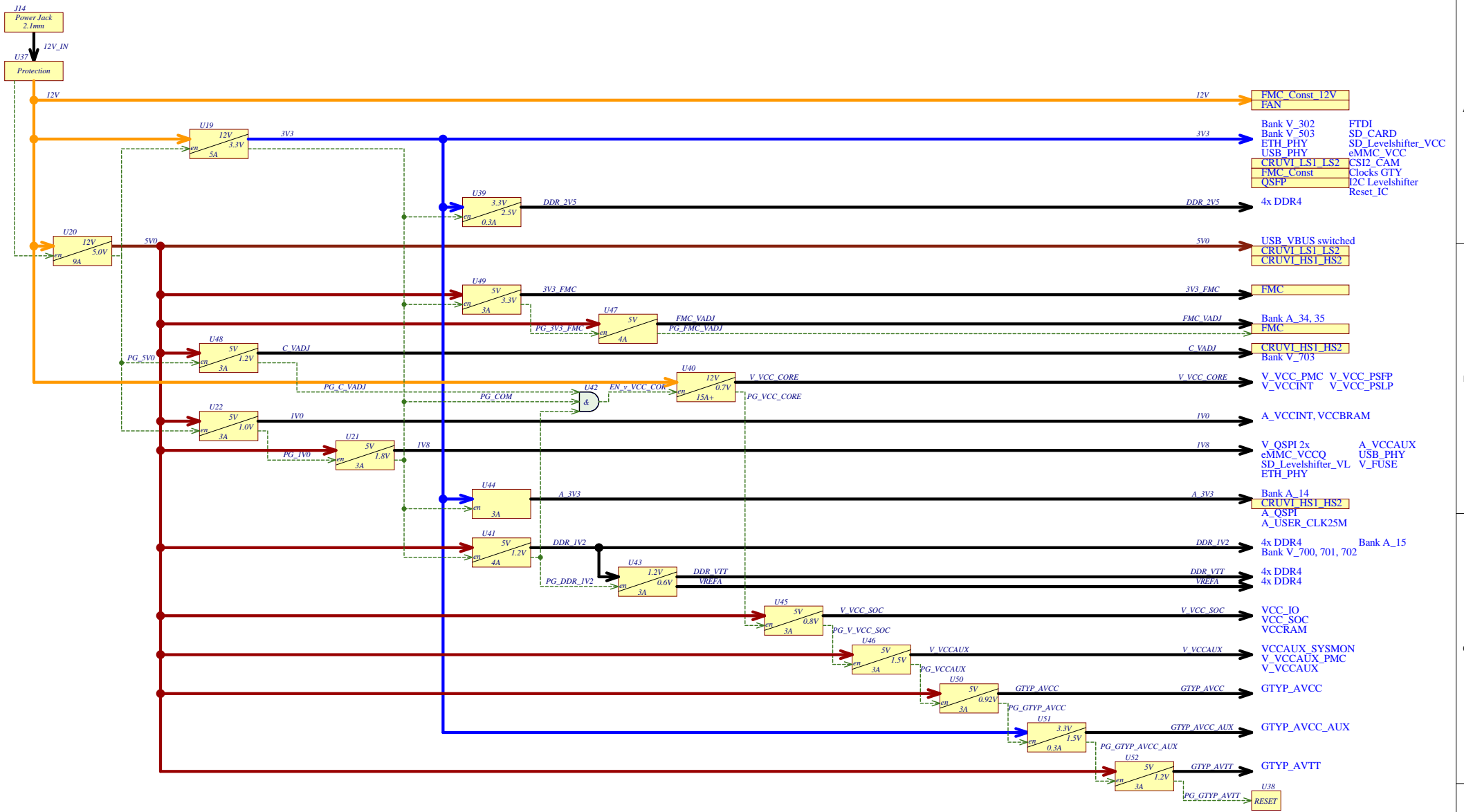


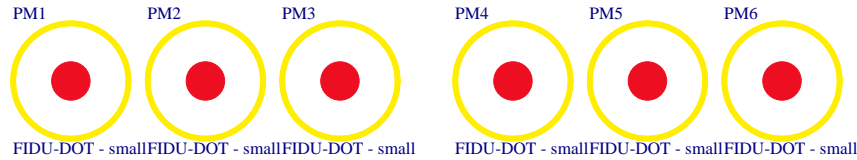
Special notes:

*Versal XCVE2302-1LSESFVA784-ES9749 is a preproduction die.
No changes to production chips (without ES number) are expected.*



Title: System Overview		
A4	Number: TE0950 EGBE21A	Rev. 03
Date: 17.01.2024	Copyright: Trenz Electronic GmbH	Page 3 of 39
Filename: Overview.SchDoc		





I2C Addresses:

Device	Bus	Address	Note
24AA025E48	PMC_I2C	1010000 50H	EEPROM for MAC with user area

MECH1

TE Address Overlay

LOGO ADDRESS

LOGO1

TE Logo PRINT Layer

LOGO PRINT

Serial1

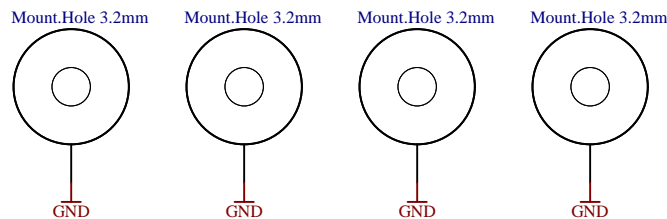
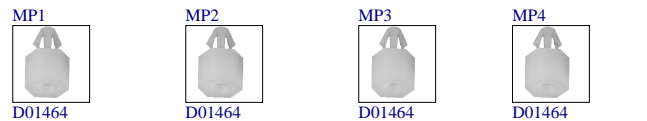
Serial

Serialnumber 6,3 x 6.3mm

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
12V_IN	IN	12V	+/-5%	Board Power	-
5V0	OUT	5.0V	+/-3%	CRUVI LS and HS 5V	Shared with onboard 5V supplies and with further switch (U29) for rail USB_VBUS_SUP via jumper (J5) connectable to USB (J8).
3V3	OUT	3.3V	+/-3%	QSFP, CRUVI LS 3.3V, CSI-2 CAM	Shared with VERSAL VCCO Bank 302 and onboard peripherals.
C_VADJ	OUT	1.2V	+/-3%	CRUVI HS IO	Shared with VERSAL VCCIO XPIO Bank 703.
A_3V3	OUT	3.3V	+/-3%	CRUVI HS 3.3V	Shared with ARTIX VCCIO Bank 14 and onboard peripherals.
12V	OUT	12V	+/-5%	FMC	Derived from 12V_IN after input protection. Shared with onboard peripherals.
3V3_FMC	OUT	3.3V	+/-3%	FMC	-
FMC_VADJ	OUT	1.2V - 3.3V	+/-3%	FMC	Selectable by dip settings.

Versal XCVE2302-1LSSEFVA784-ES9749 is a preproduction die.
No changes to production chips (without ES number) are expected.



CE1

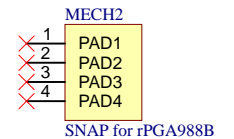
CE Logo on Top Overlay

CE-TOPOVERLAY

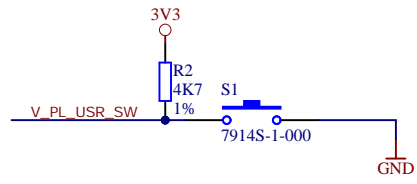
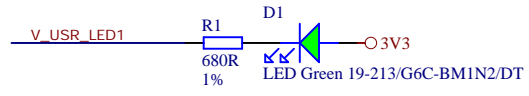
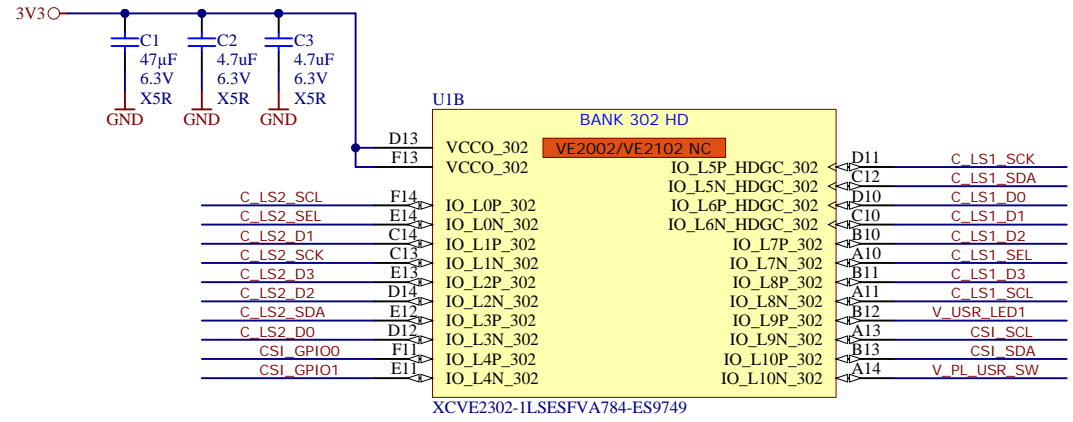
UKCA1

UKCA Logo on Top Overlay

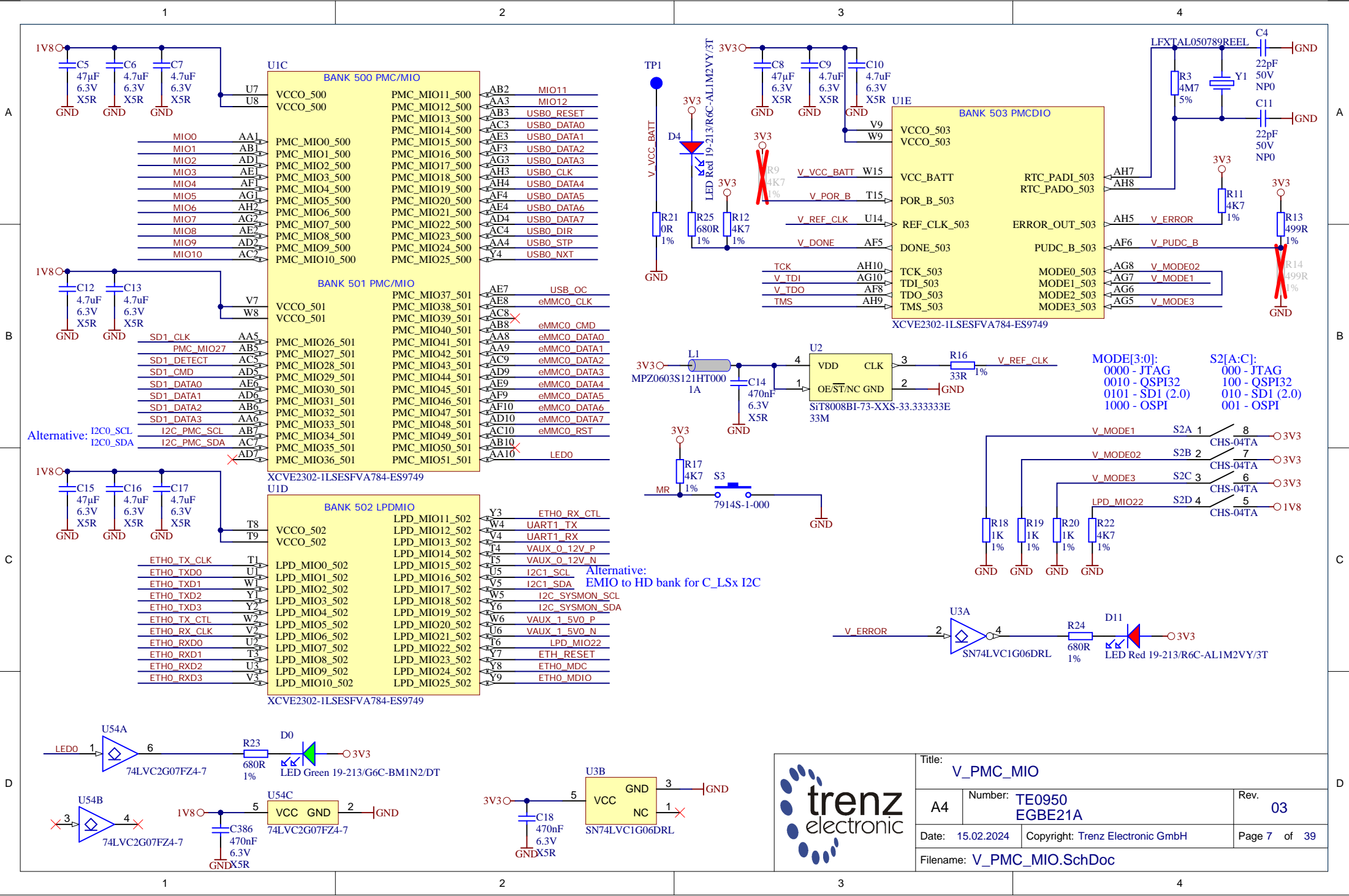
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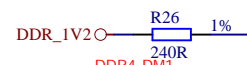
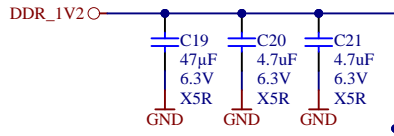
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Date: 12.01.2024		Copyright: Trenz Electronic GmbH	
Filename: TE0950.SchDoc		Page 5 of 39	



Title: V_HD		
A4	Number: TE0950 EGBE21A	Rev. 03
Date: 15.02.2024	Copyright: Trenz Electronic GmbH	Page 6 of 39
Filename: V_HD.SchDoc		



Title: V_PMC_MIO		Rev: 03
A4	Number: TE0950 EGBE21A	Page 7 of 39
Date: 15.02.2024	Copyright: Trenz Electronic GmbH	
Filename: V_PMC_MIO.SchDoc		



DDR4-DM1	AH13
DDR4-A12	AH12
DQ11	AH14
DQ9	AH15
DQ10	AH17
DQ8	AH18
DDR4-DQS1_P	AG20
DDR4-DQS1_N	AH19
DQ12	AG21
DQ14	AH20
DQ13	AG22
DQ15	AH22
DDR4-DM0	AG12
DDR4-A7	AG11
DQ3	AF13
DQ1	AG13
DQ2	AF14
DQ0	AG15
DDR4-DQS0_P	AG17
DDR4-DQS0_N	AG16
DQ4	AF18
DQ6	AG18
DQ7	AE19
DQ5	AF19

UIF

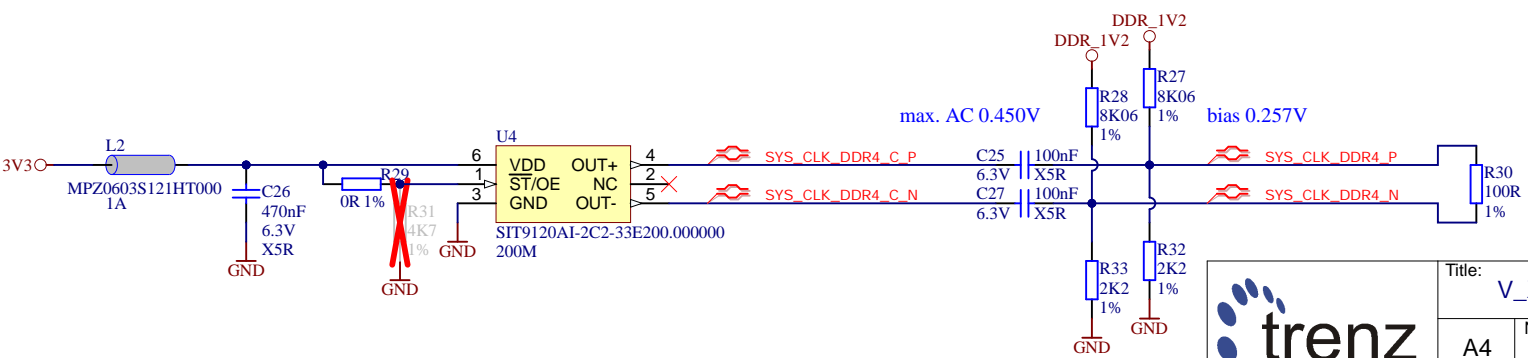
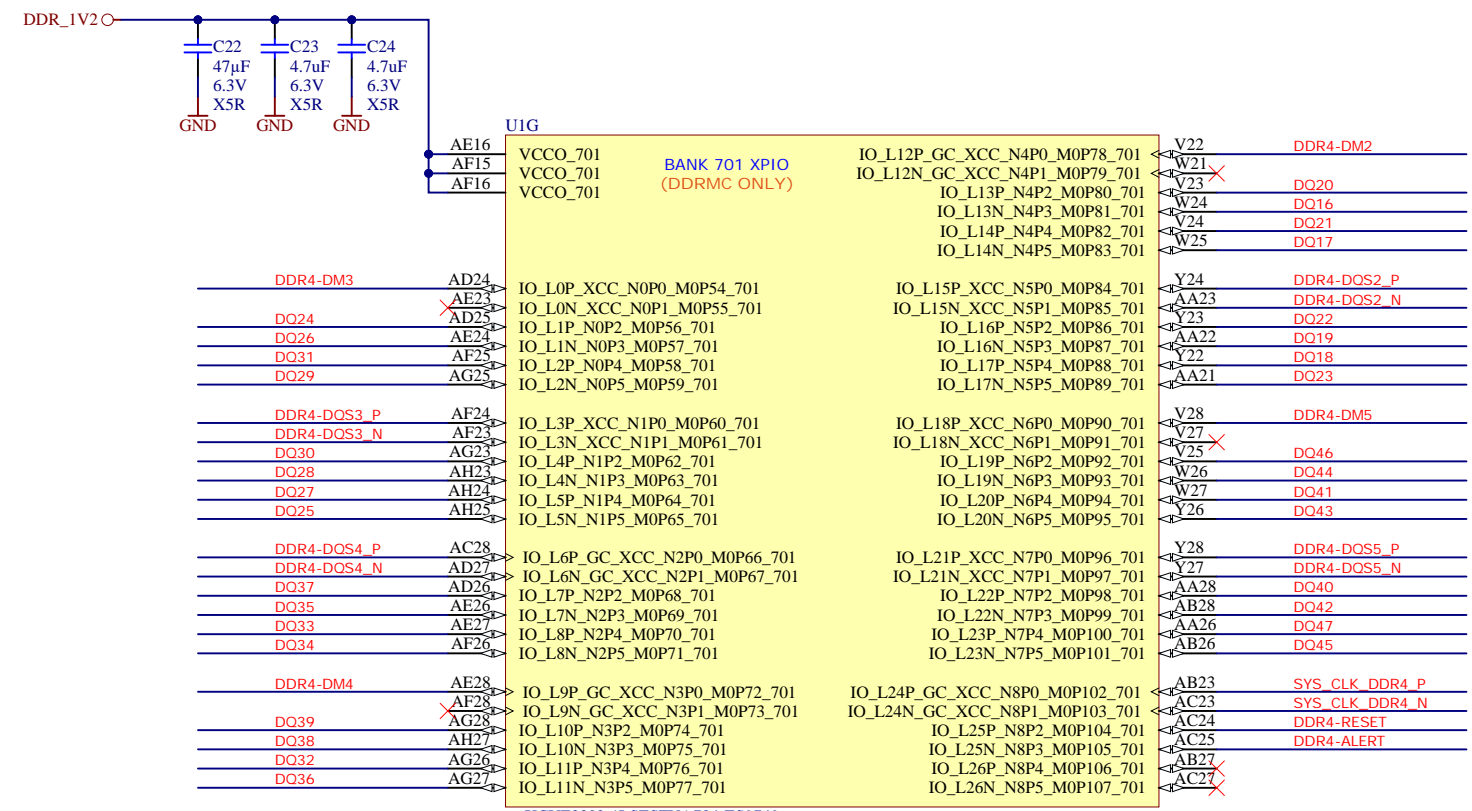
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AE12	VCCO_700		IO_L12N_GC_XCC_N4P1_M0P25_700
AF11	VCCO_700		IO_L13P_N4P2_M0P26_700
			IO_L13N_N4P3_M0P27_700
			IO_L14P_N4P4_M0P28_700
			IO_L14N_N4P5_M0P29_700
			IO_L15P_XCC_N5P0_M0P30_700
			IO_L15N_XCC_N5P1_M0P31_700
			IO_L16P_N5P2_M0P32_700
			IO_L16N_N5P3_M0P33_700
			IO_L17P_N5P4_M0P34_700
			IO_L17N_N5P5_M0P35_700
			IO_L18P_XCC_N6P0_M0P36_700
			IO_L18N_XCC_N6P1_M0P37_700
			IO_L19P_N6P2_M0P38_700
			IO_L19N_N6P3_M0P39_700
			IO_L20P_N6P4_M0P40_700
			IO_L20N_N6P5_M0P41_700
			IO_L21P_XCC_N7P0_M0P42_700
			IO_L21N_XCC_N7P1_M0P43_700
			IO_L22P_N7P2_M0P44_700
			IO_L22N_N7P3_M0P45_700
			IO_L23P_N7P4_M0P46_700
			IO_L23N_N7P5_M0P47_700
			IO_L24P_GC_XCC_N8P0_M0P48_700
			IO_L24N_GC_XCC_N8P1_M0P49_700
			IO_L25P_N8P2_M0P50_700
			IO_L25N_N8P3_M0P51_700
			IO_L26P_N8P4_M0P52_700
			IO_L26N_N8P5_M0P53_700

XCVE2302-1LSESFVA784-ES9749

AD12	DDR4-A4
AD11	DDR4-BA1
AC14	
AD14	DDR4-PAR
AC17	DDR4-CS
AD17	DDR4-A15
AC19	DDR4-CLK0_P
AD19	DDR4-CLK0_N
AD20	
AD21	DDR4-A14
AD22	DDR4-A2
AE22	DDR4-A1
AB12	DDR4-A0
AC11	DDR4-ACT
AB14	DDR4-A9
AC13	DDR4-A16
AB15	DDR4-A3
AC16	DDR4-BA0
AB18	DDR4-BG0
AB17	DDR4-A10
AB20	
AC20	
AB21	DDR4-CKE0
AC22	DDR4-ODT0
AD16	DDR4-A6
AD15	DDR4-A13
AE13	DDR4-A11
AE14	DDR4-A8
AE17	DDR4-A5
AE18	DDR4-BG1



Title: V_XPIO_700		
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Date: 2024-02-15	Copyright: Trenz Electronic GmbH	Page 8 of 39
Filename: V_XPIO_700.SchDoc		



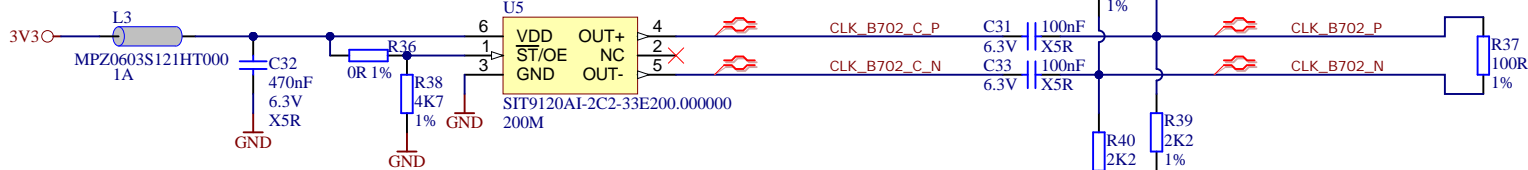
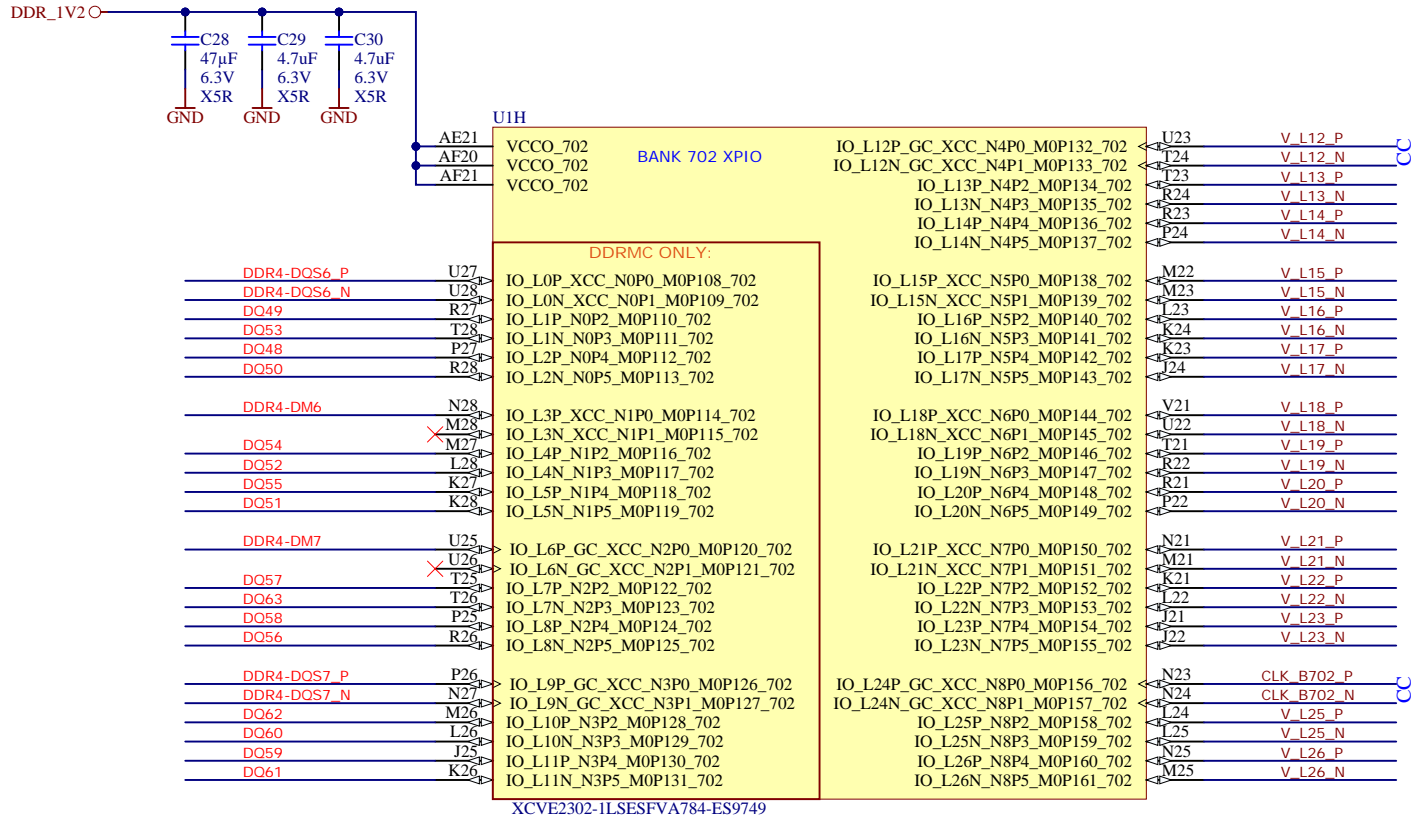
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Filename: V_XPIO_701.SchDoc		

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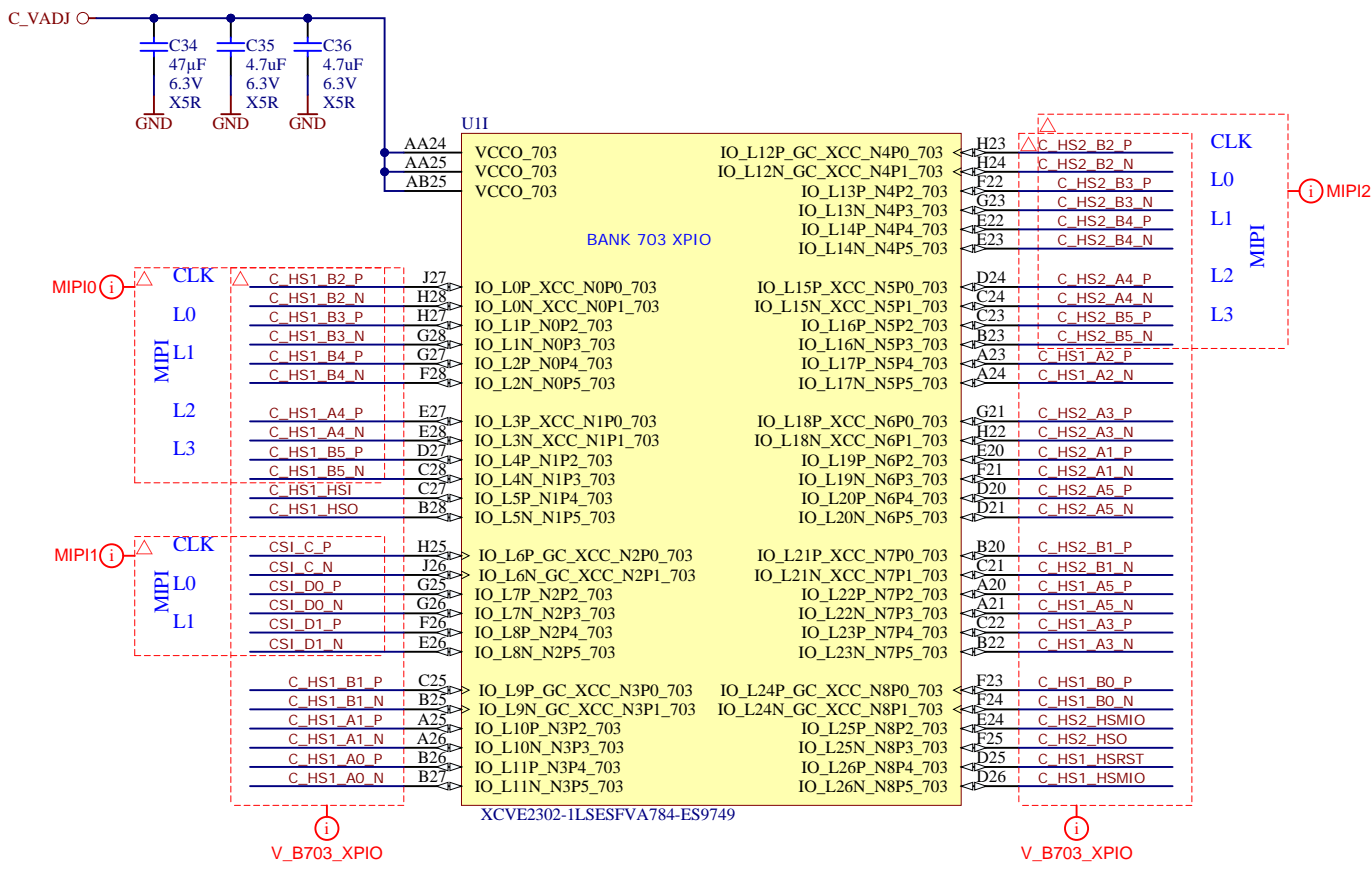
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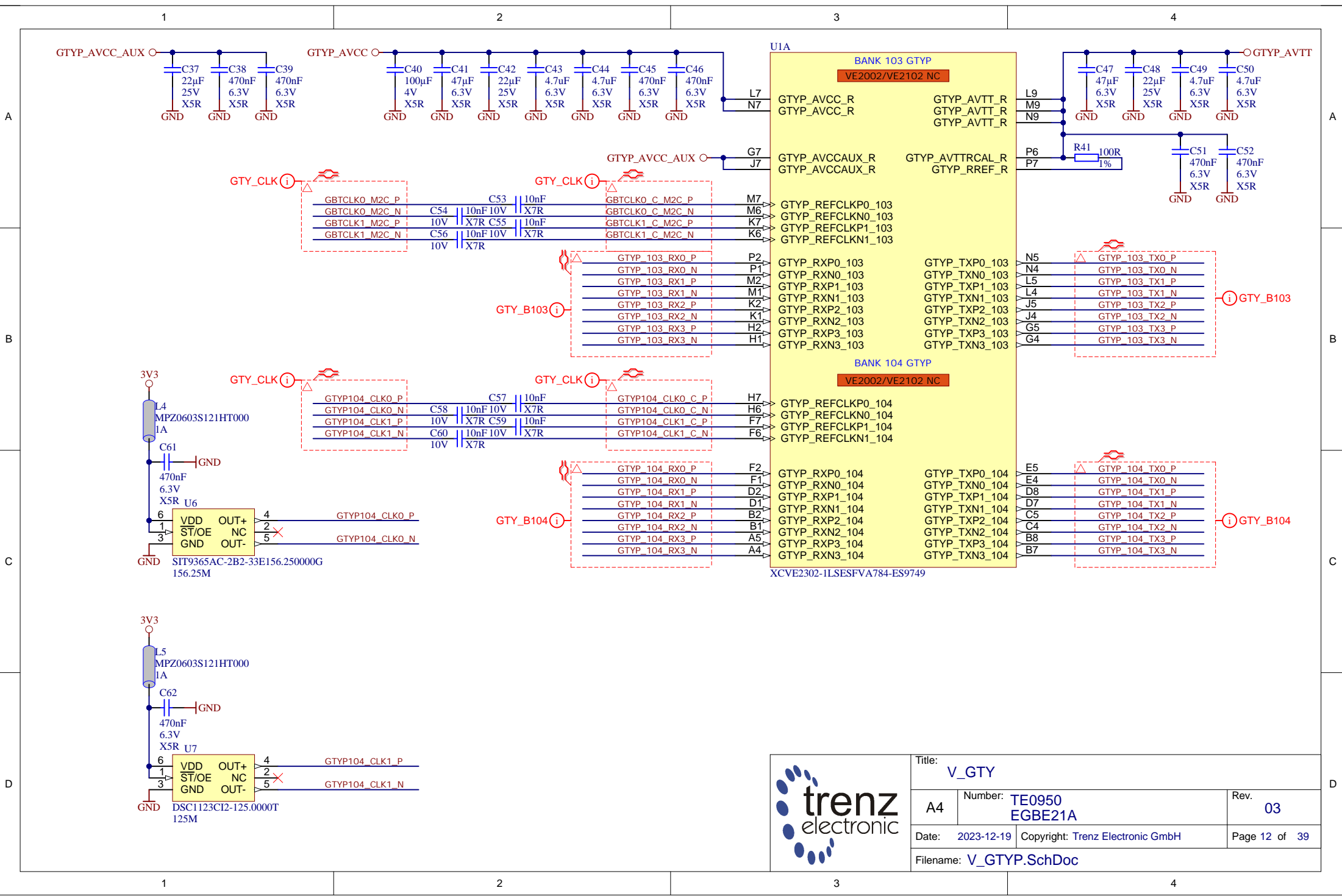
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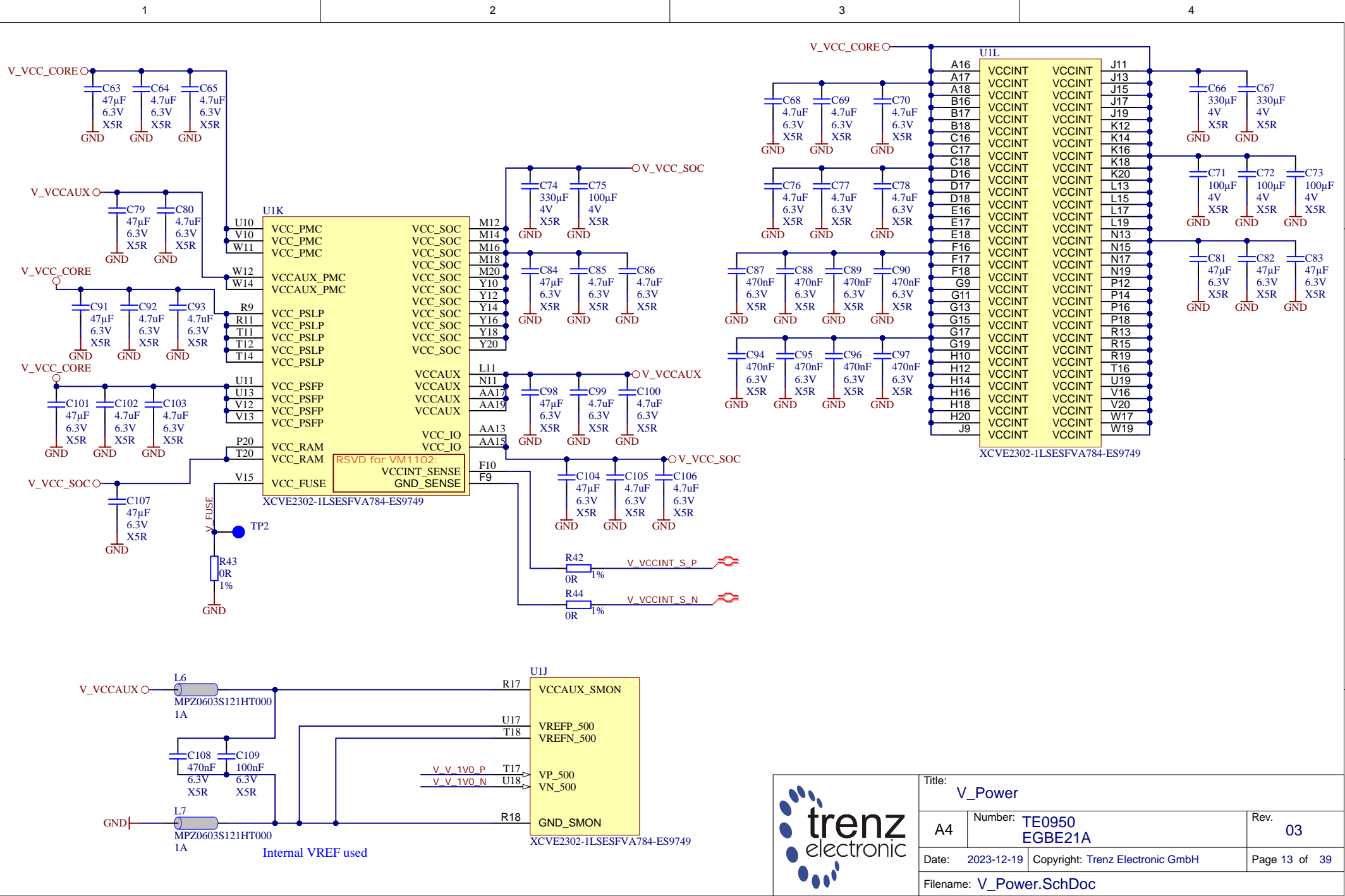
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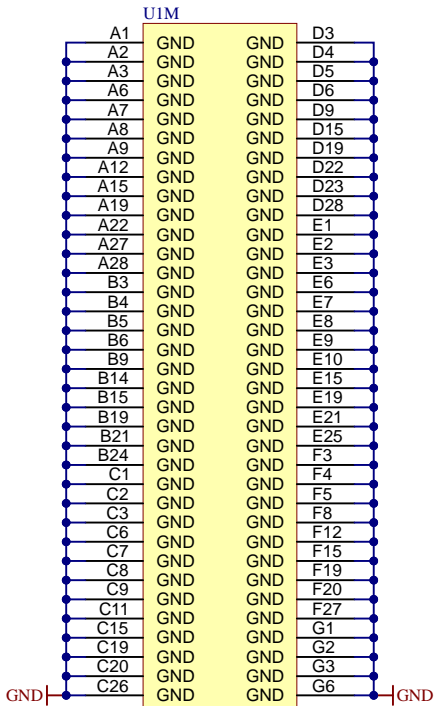
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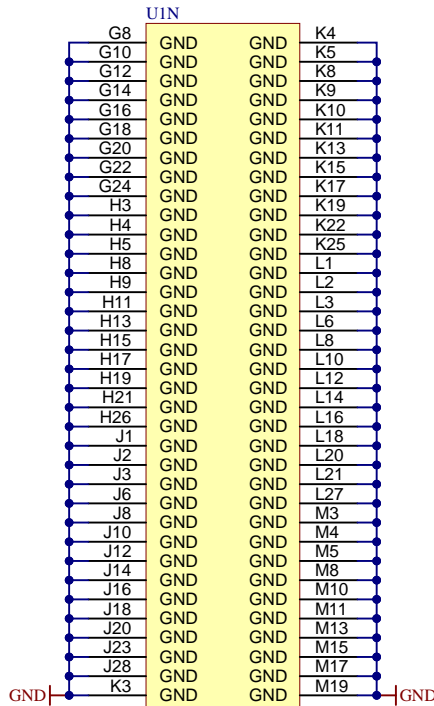
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Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 12 of 39
Filename: V_GTY.SchDoc		



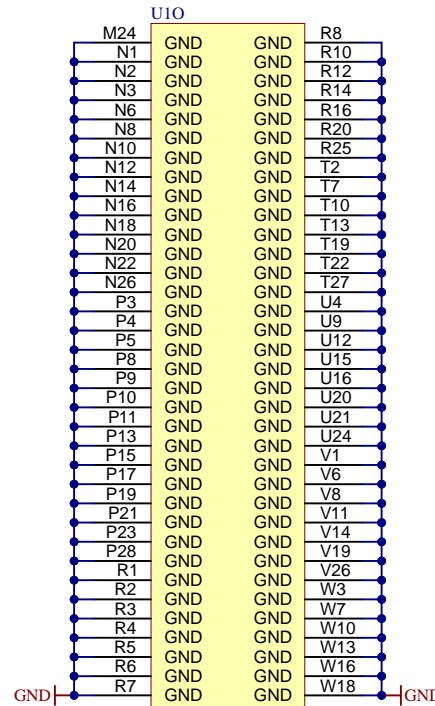
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Filename: V_Power.SchDoc		



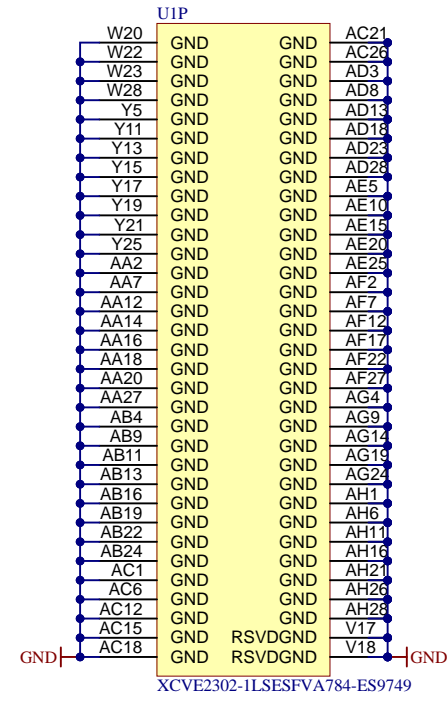
XCVE2302-1LSESFVA784-ES9749



XCVE2302-1LSESFVA784-ES9749



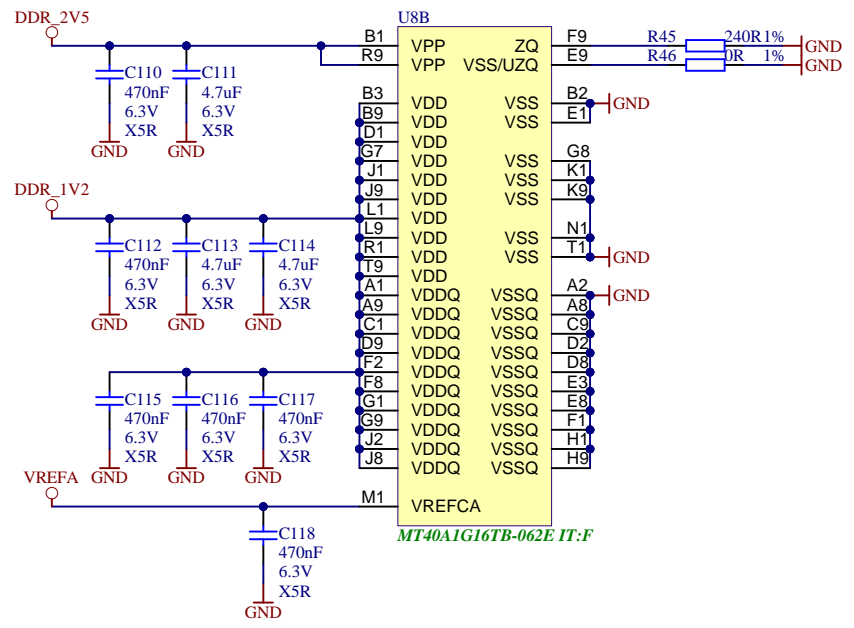
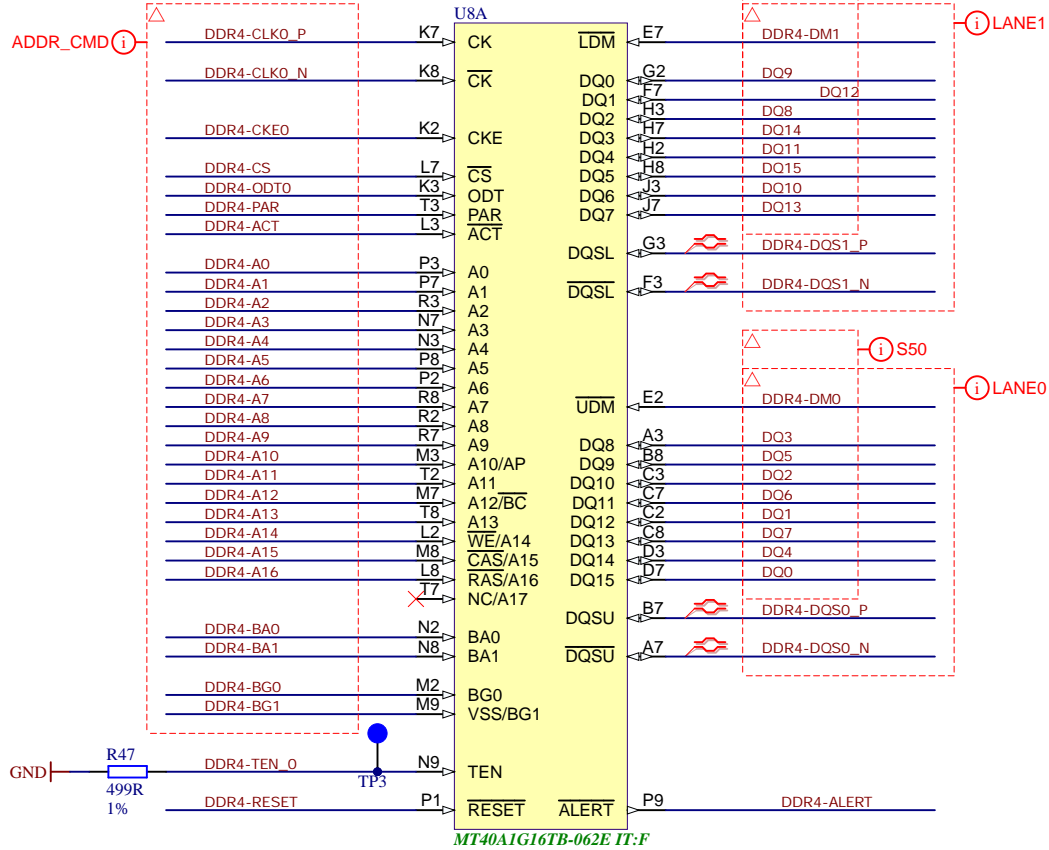
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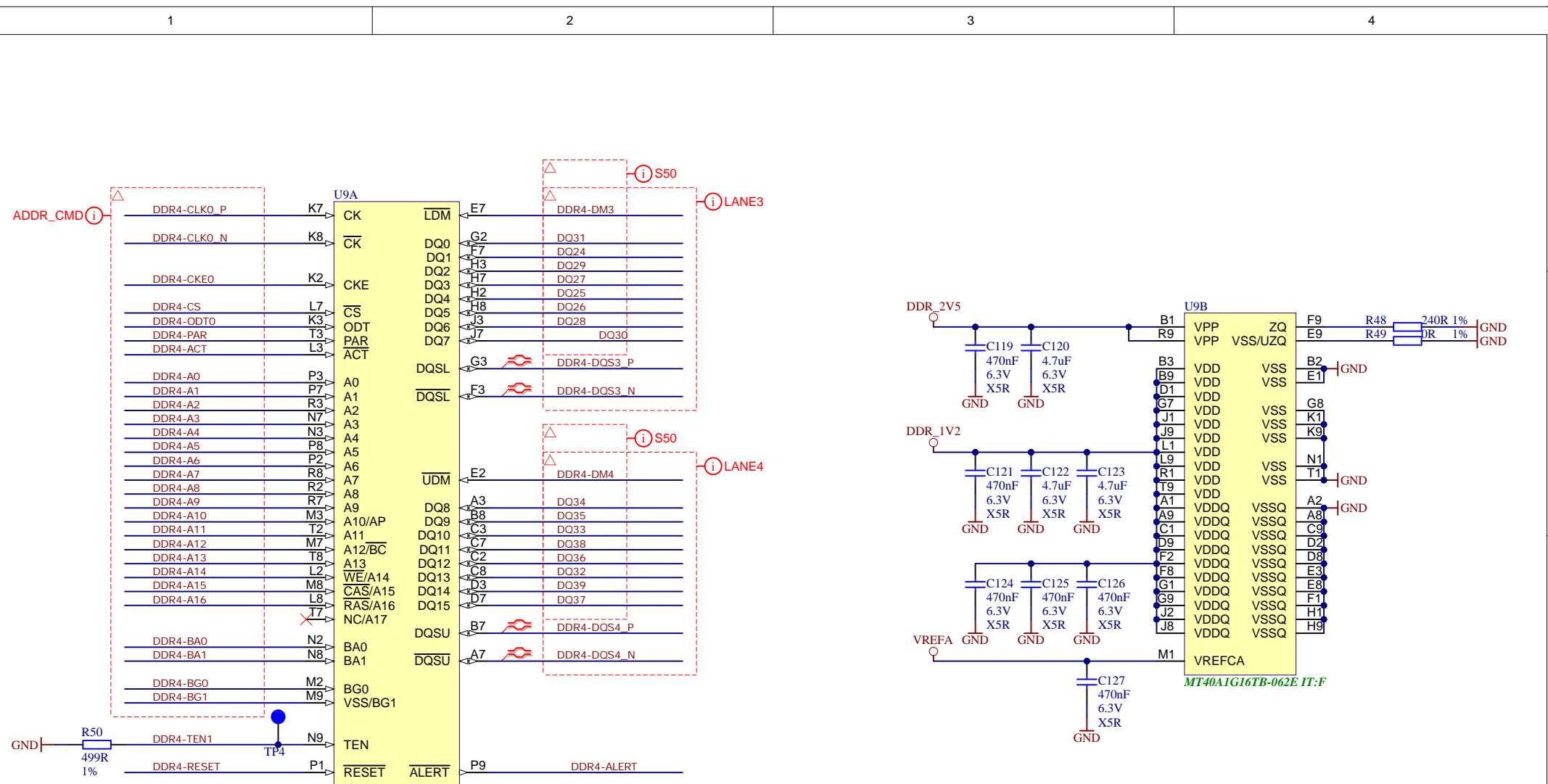


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Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 14 of 39
Filename: V_GND.SchDoc		



- DDR4_2.SchDoc
- DDR4_3.SchDoc
- DDR4_4.SchDoc
- DDR4_TERM.SchDoc

			Title: DDR4_1	
A4	Number: TE0950 EGBE21A	Rev. 03		
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 15 of 39		
Filename: DDR4_1.SchDoc				



			Title: DDR4_2	
			A4	Number: TE0950 EGBE21A
Date: 2023-12-19		Copyright: Trenz Electronic GmbH		Page 16 of 39
Filename: DDR4_2.SchDoc				

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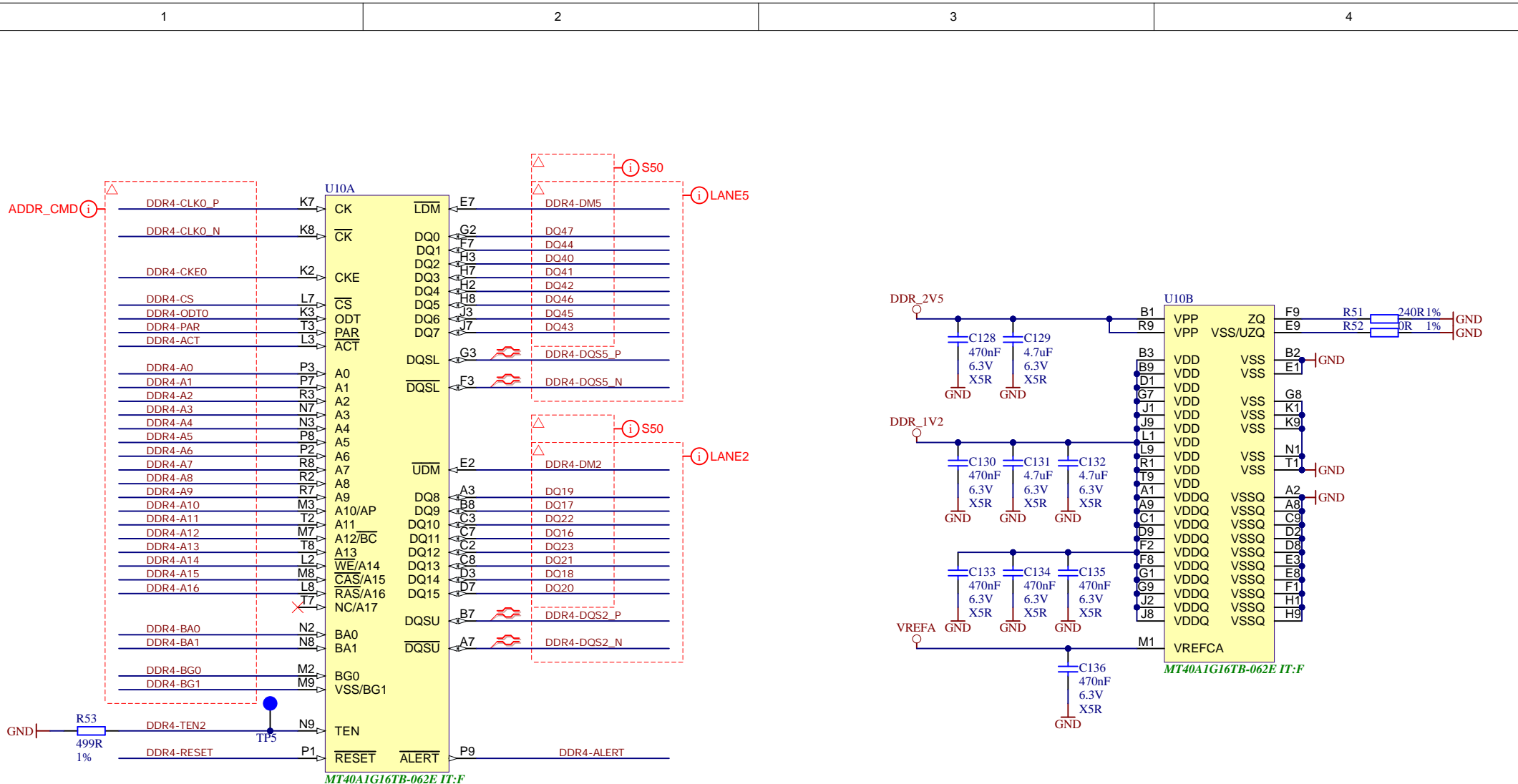
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Date: 2023-12-19		Copyright: Trenz Electronic GmbH		Page 17 of 39
Filename: DDR4_3.SchDoc				

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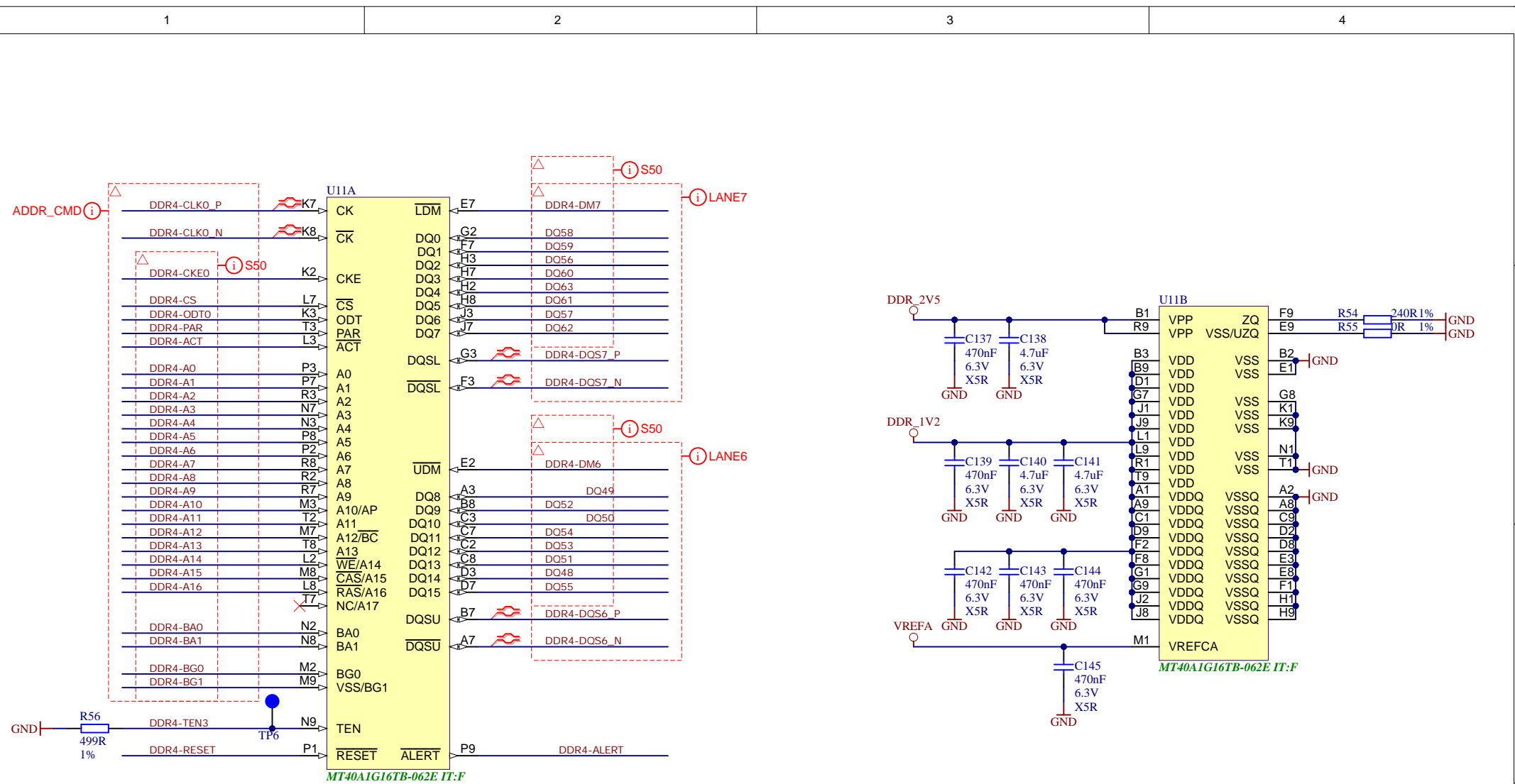
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Date: 2023-12-19		Copyright: Trenz Electronic GmbH		Page 18 of 39
Filename: DDR4_4.SchDoc				

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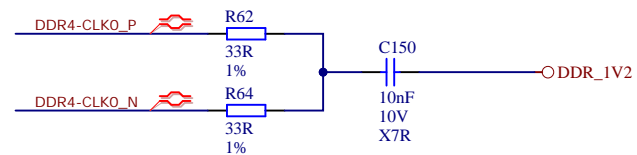
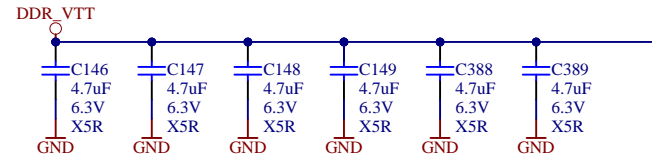
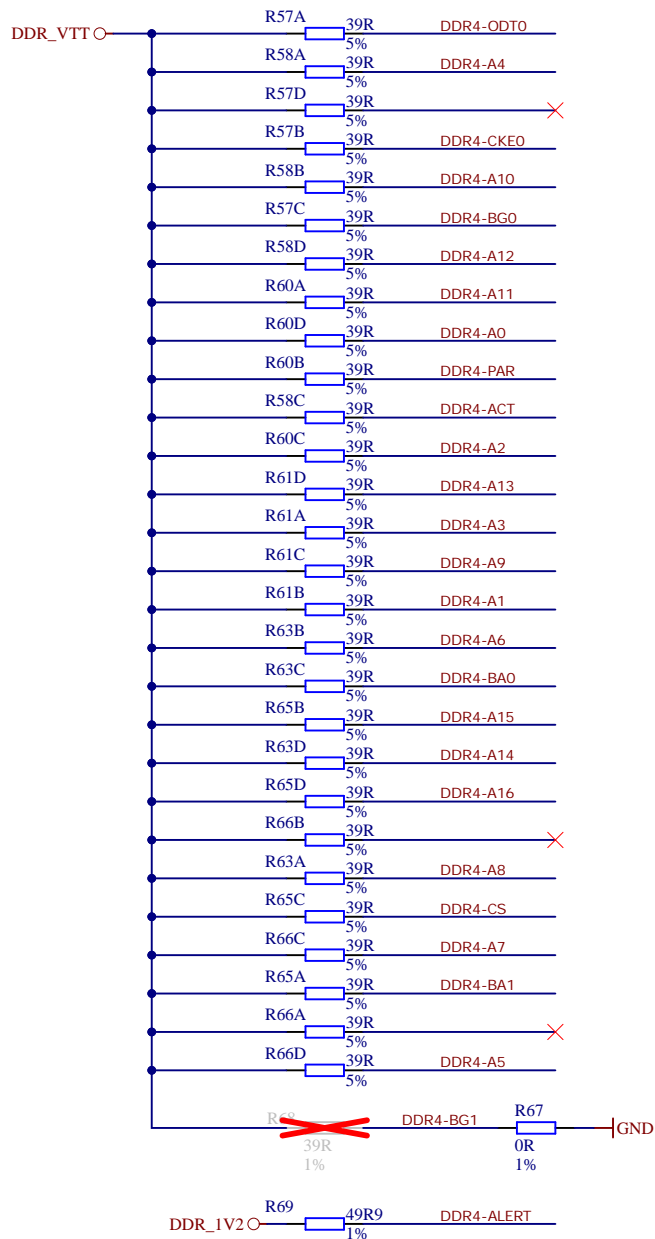
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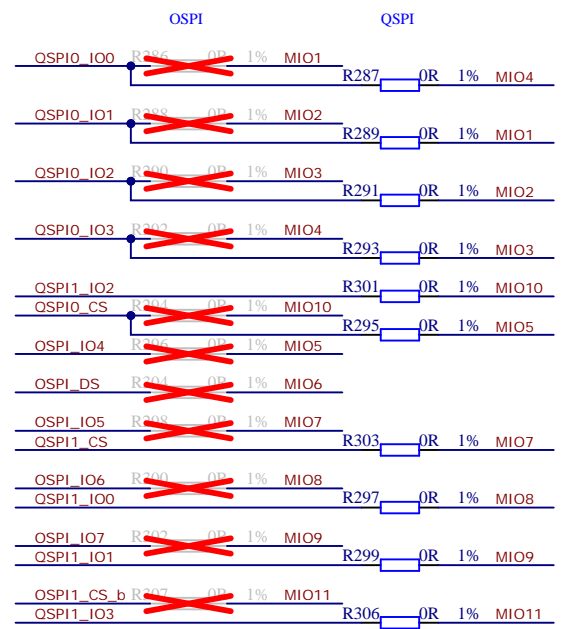
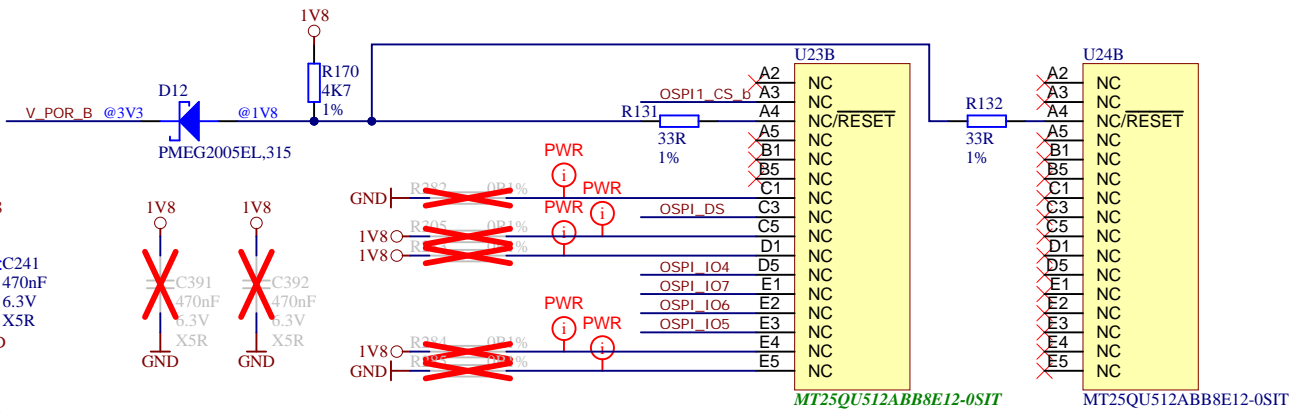
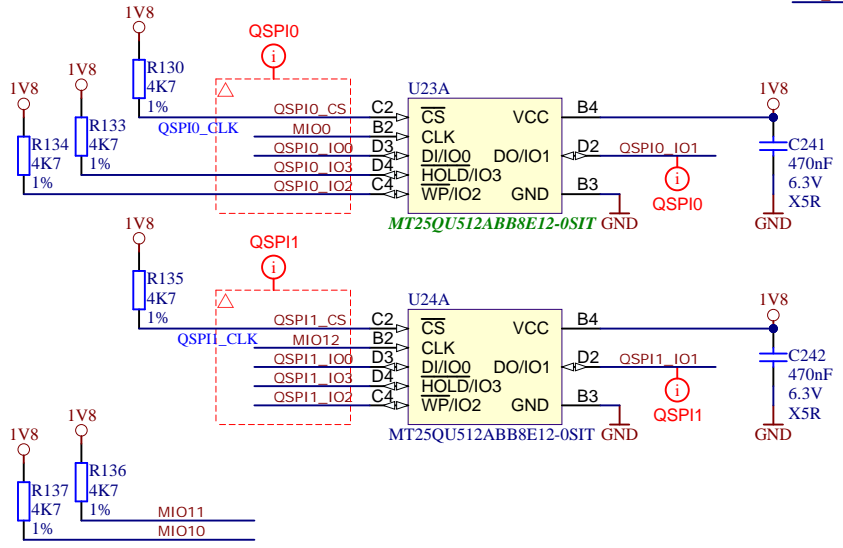
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Title: DDR4_TERM		
A4	Number: TE0950 EGBE21A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	
Page 19 of 39		
Filename: DDR4_TERM.SchDoc		

Assembly version: 2x QSPI (dual parallel U23, U24) or OSPI (U23)

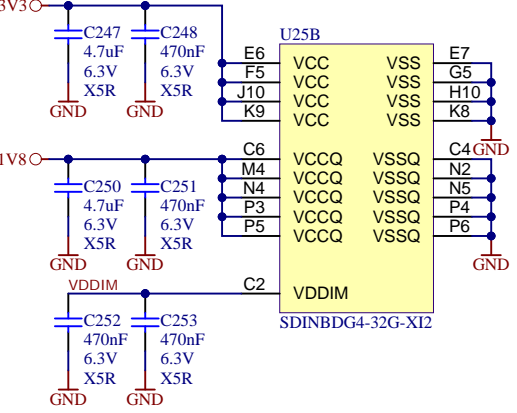
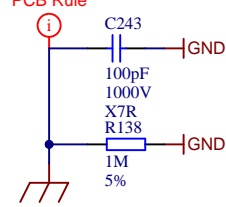
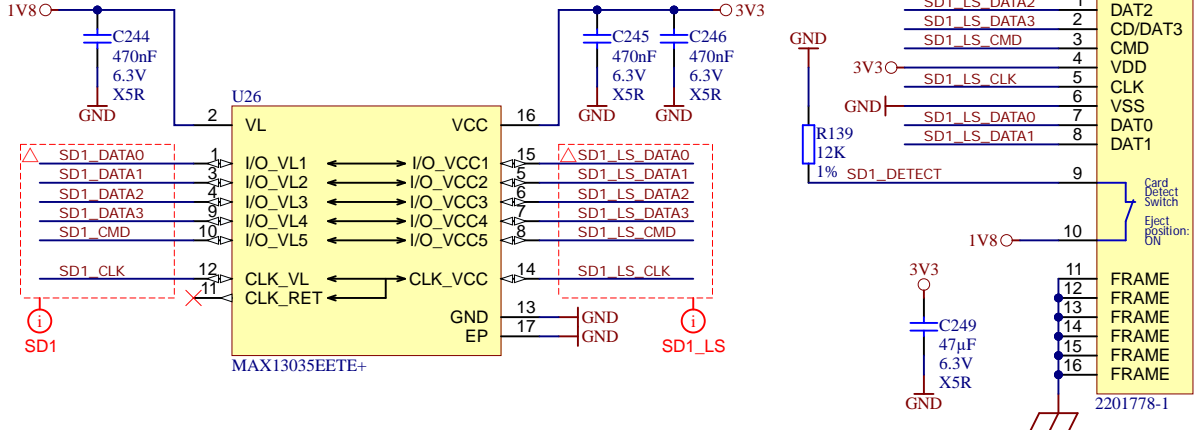


MIO	OSPI	PMC Bank 0	pull-up
MIO 0	OSPI: ospi_clk		
MIO 1	OSPI: ospi_io[0]		
MIO 2	OSPI: ospi_io[1]		
MIO 3	OSPI: ospi_io[2]		
MIO 4	OSPI: ospi_io[3]		
MIO 5	OSPI: ospi_io[4]		
MIO 6	OSPI: ospi_ds		
MIO 7	OSPI: ospi_io[5]		
MIO 8	OSPI: ospi_io[6]		
MIO 9	OSPI: ospi_io[7]		
MIO 10	OSPI: ospi_cs_b	R137 installed	
MIO 11	OSPI: ospi1_cs_b	R136 installed	
MIO 12			

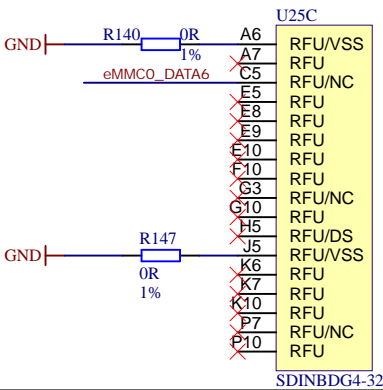
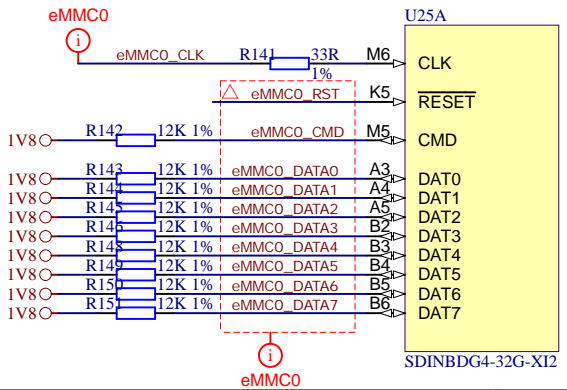
MIO	QSPI	PMC Bank 0	pull-up
MIO 0	QSPI: qspi0_clk		
MIO 1	QSPI: qspi0_io[1]		
MIO 2	QSPI: qspi0_io[2]		
MIO 3	QSPI: qspi0_io[3]	R134 installed	
MIO 4	QSPI: qspi0_io[0]	R133 installed	
MIO 5	QSPI: qspi0_cs_b	R130 installed	
MIO 6	Reserved		
MIO 7	QSPI: qspi1_cs_b	R135 installed	
MIO 8	QSPI: qspi1_io[0]		
MIO 9	QSPI: qspi1_io[1]		
MIO 10	QSPI: qspi1_io[2]	R137 installed	
MIO 11	QSPI: qspi1_io[3]	R136 installed	
MIO 12	QSPI: qspi1_clk		



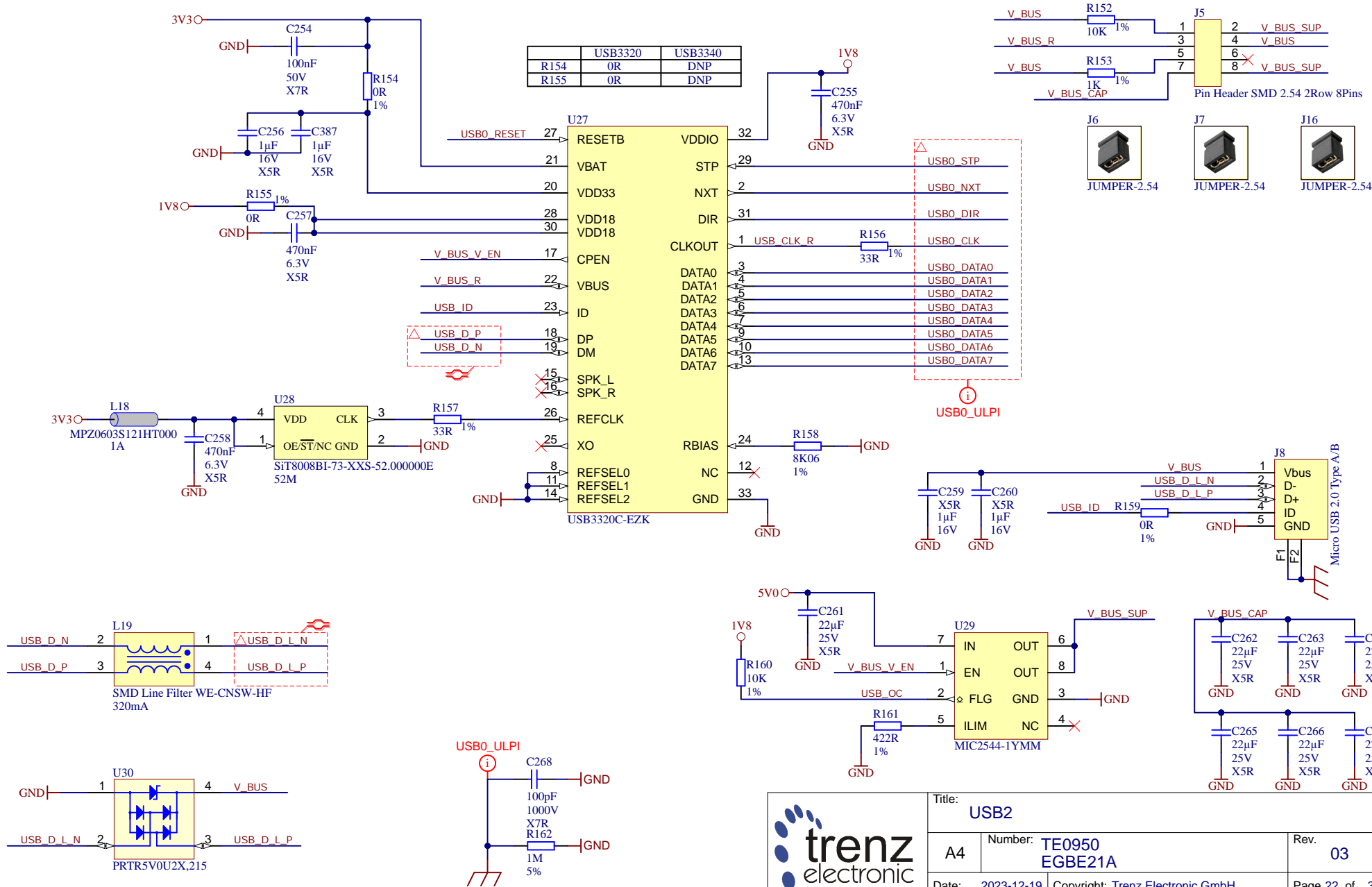
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Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 20 of 39
Filename: QSPI_OSPI.SchDoc		



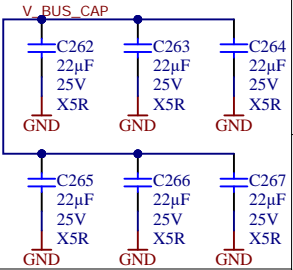
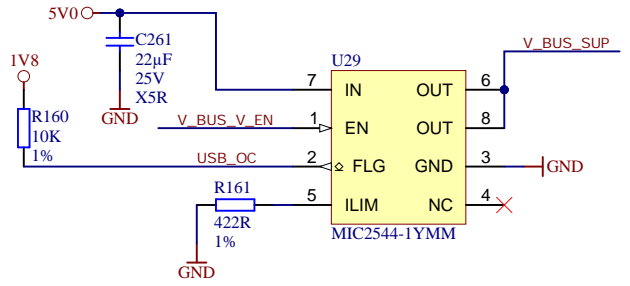
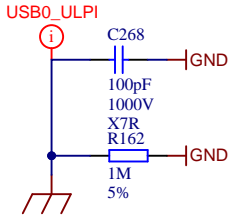
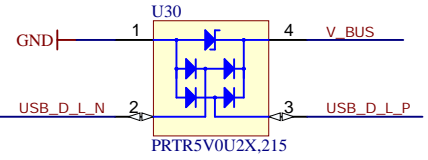
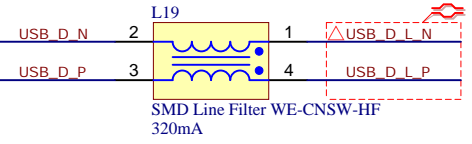
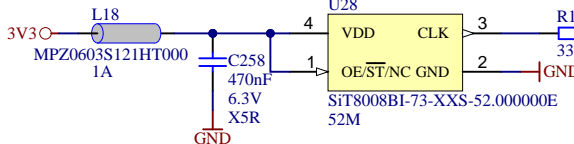
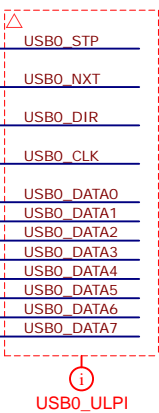
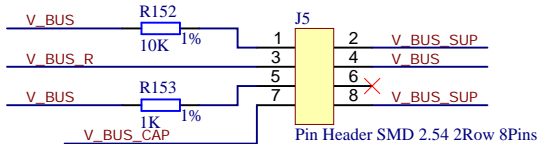
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	A8	NC	H12
	A9	NC	H13
	A10	NC	H14
	A11	NC	J1
	A12	NC	J2
	A13	NC	J3
	A14	NC	J12
eMMC_DATA3	B1	NC	J13
eMMC_DATA7	B7	NC	J14
eMMC_DATA7	B8	NC	K1
	B9	NC	K2
	B10	NC	K3
	B11	NC	K12
	B12	NC	K13
	B13	NC	K14
	B14	NC	L1
VDDIM	C1	NC	L2
eMMC_DATA5	C3	NC	L3
1V8	C7	NC	L12
eMMC_DATA7	C8	NC	L13
	C9	NC	L14
	C10	NC	M1
	C11	NC	M2
	C12	NC	M3
	C13	NC	M7
	C14	NC	M8
eMMC_DATA5	D1	NC	M9
eMMC_DATA5	D2	NC	M10
	D3	NC	M11
	D4	NC	M12
	D12	NC	M13
	D13	NC	M14
	D14	NC	N1
	E1	NC	N3
	E2	NC	N6
	E3	NC	N7
	E12	NC	N8
	E13	NC	N9
	E14	NC	N10
	F1	NC	N11
	F2	NC	N12
	F3	NC	N13
	F12	NC	N14
	F13	NC	P1
	F14	NC	P2
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	H1	NC	P14



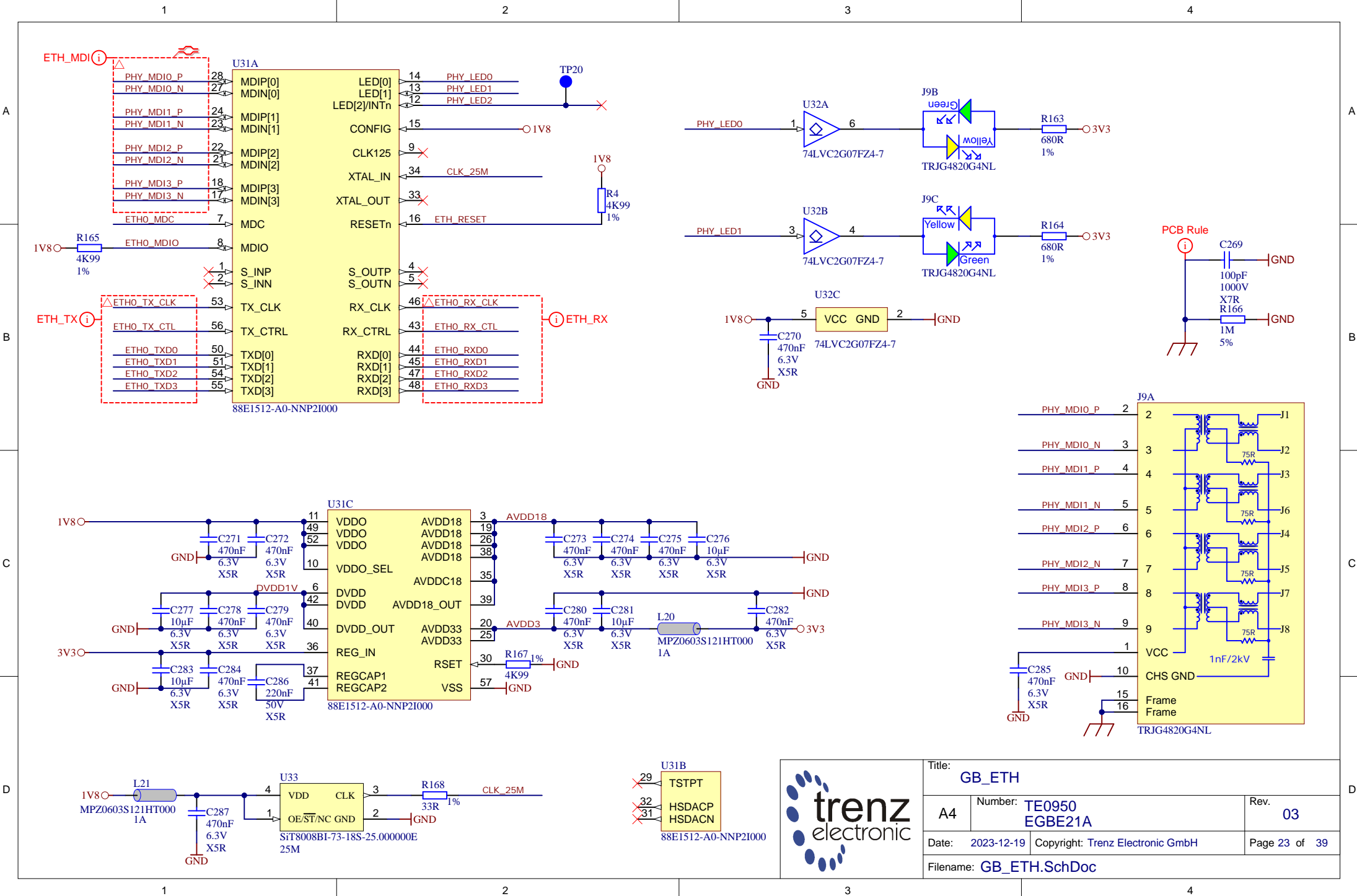
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A4	Number: TE0950 EGBE21A	Page 21 of 39	
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Filename: SD_eMMC.SchDoc	



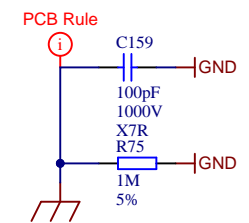
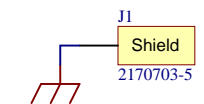
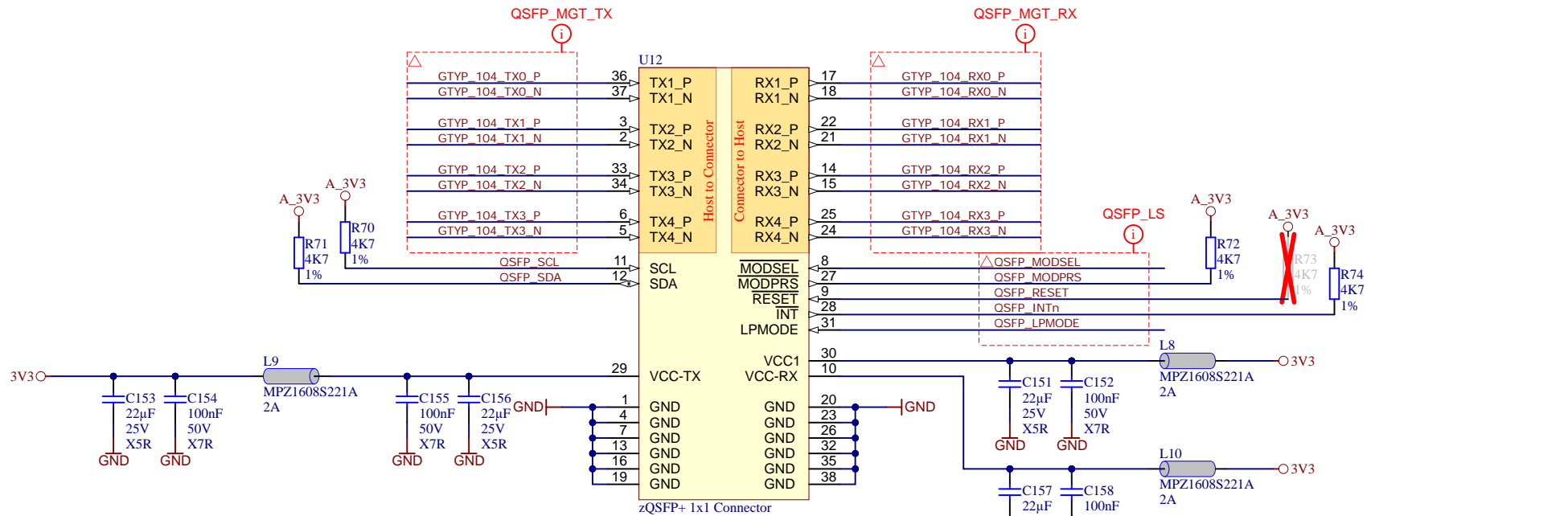
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R154	0R	DNP
R155	0R	DNP



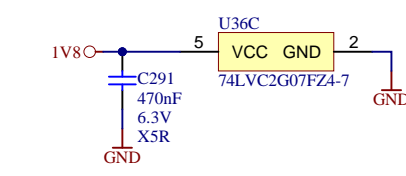
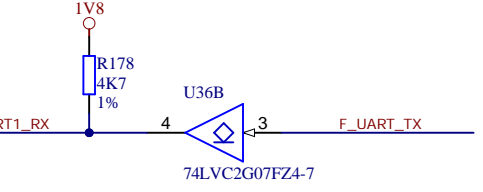
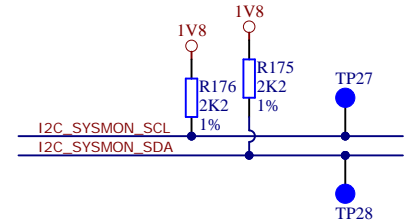
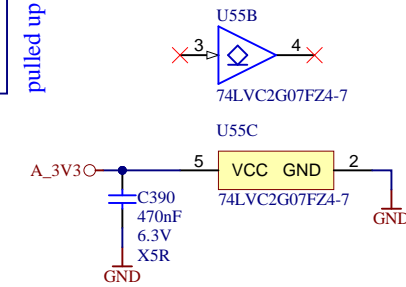
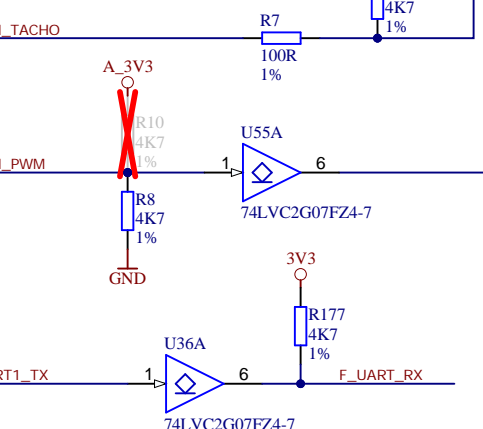
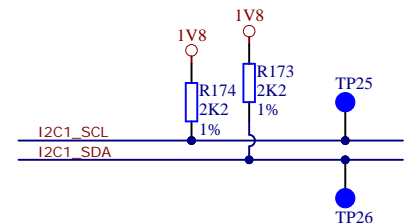
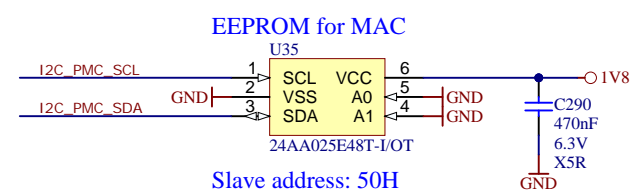
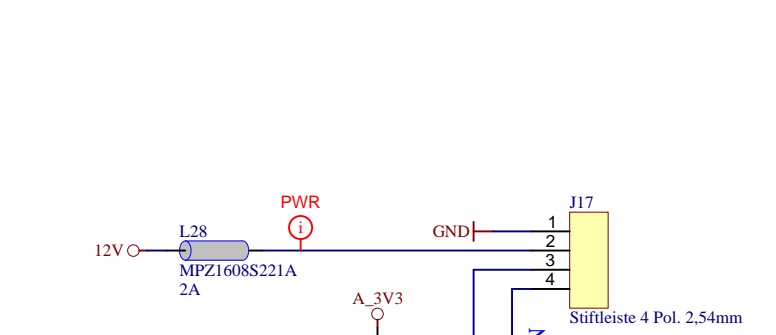
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	A4	Number: TE0950 EGBE21A
	Date: 2023-12-19	Rev: 03
	Page 22 of 39	
Copyright: Trenz Electronic GmbH		Filename: USB2.SchDoc



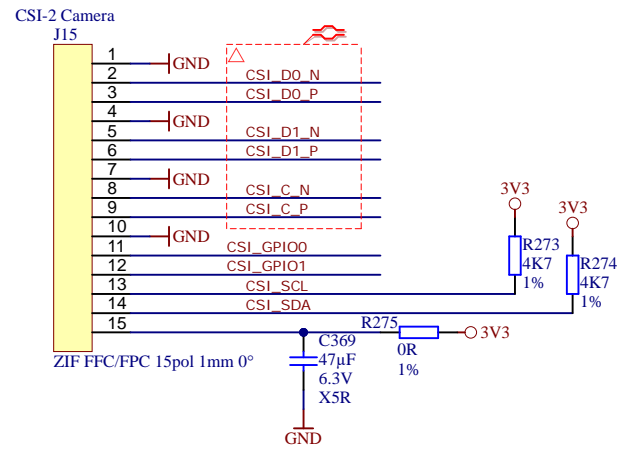
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A4	Number: TE0950 EGBE21A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 23 of 39
Filename: GB_ETH.SchDoc		




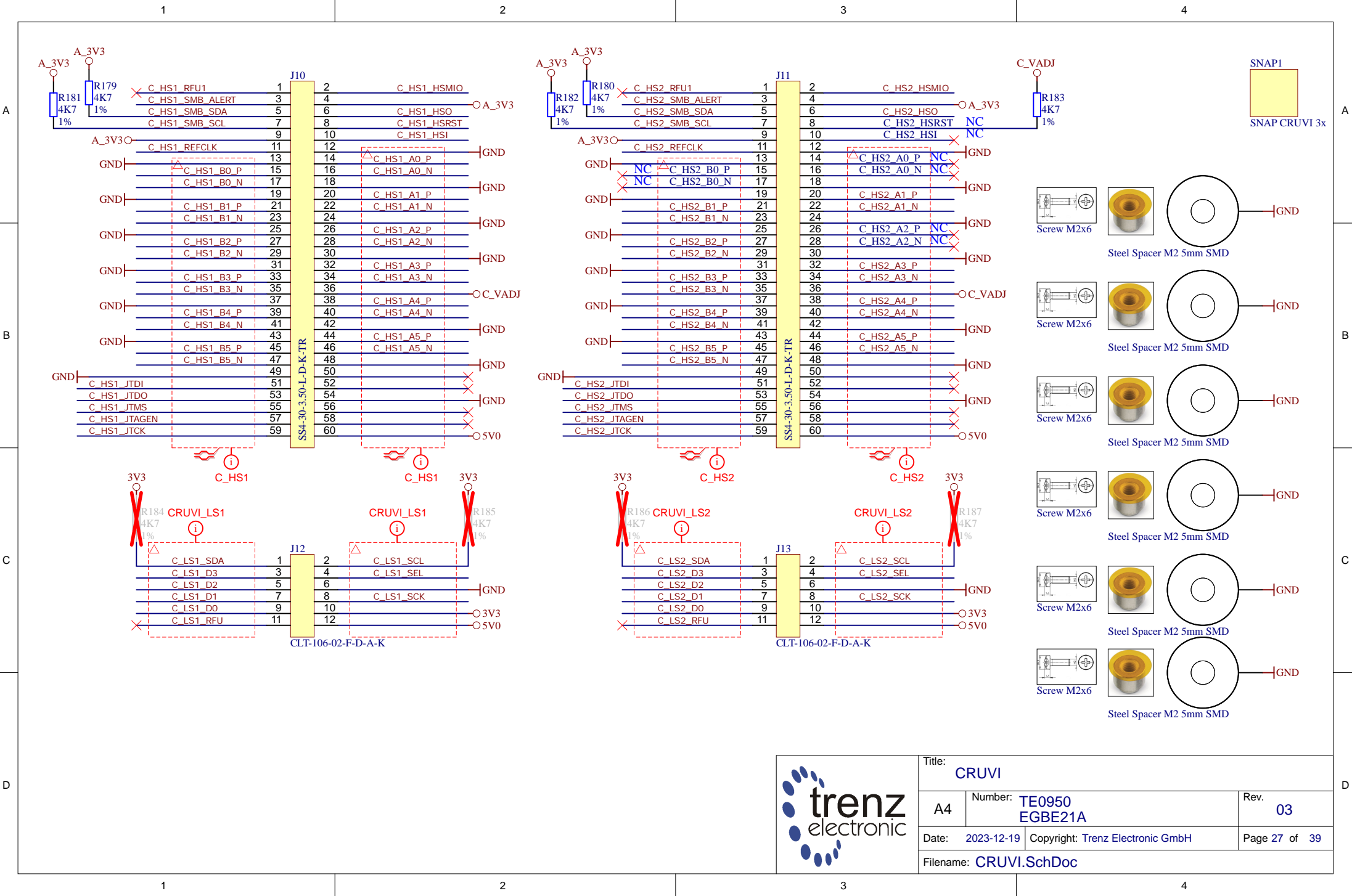
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	A4	Number: TE0950 EGBE21A	Rev. 03
	Date: 2023-12-19	Copyright: Trenz Electronic GmbH	
	Page 24 of 39		
Filename: QSFP.SchDoc			



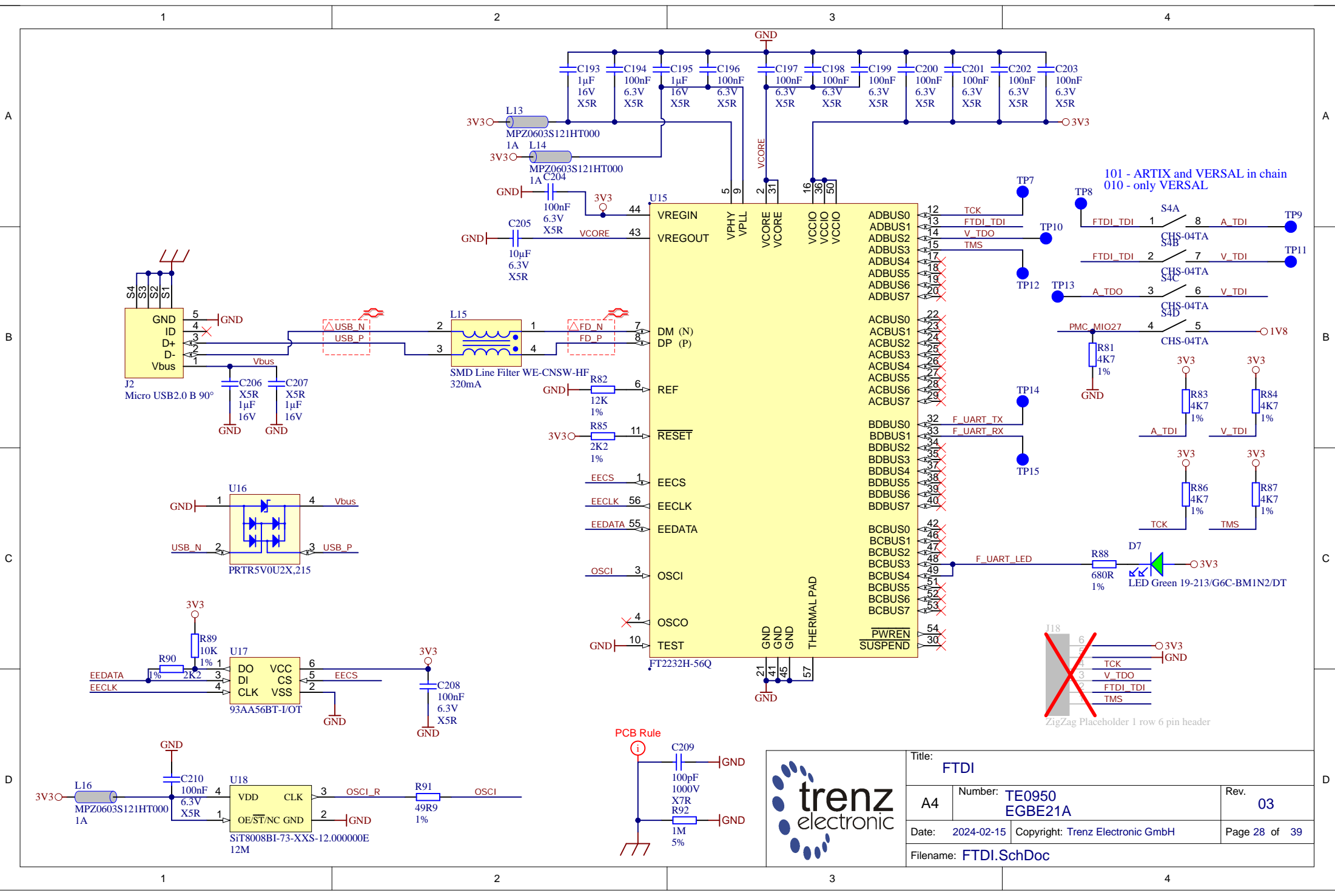
Title: I2C		
A4	Number: TE0950 EGBE21A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	
Filename: I2C.SchDoc		Page 25 of 39



	Title: CSI2_CAM	
	A4	Number: TE0950 EGBE21A
	Date: 2023-12-19	Rev. 03
	Copyright: Trenz Electronic GmbH	
Page 26 of 39		
Filename: CSI2_CAM.SchDoc		



Title: CRUVI		
A4	Number: TE0950 EGBE21A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 27 of 39
Filename: CRUVI.SchDoc		

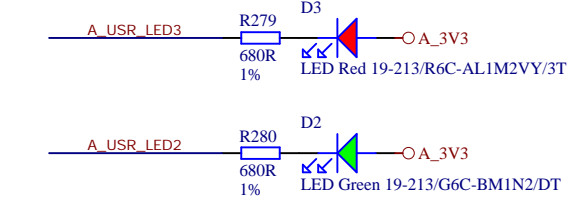
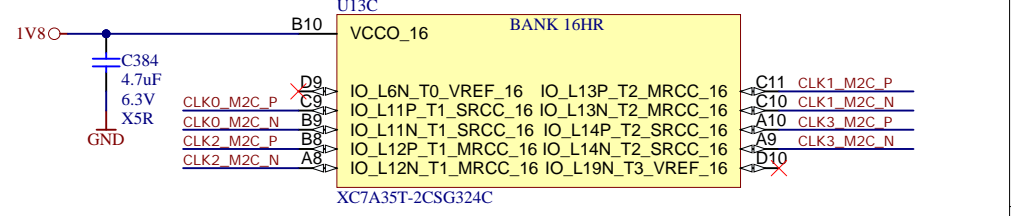
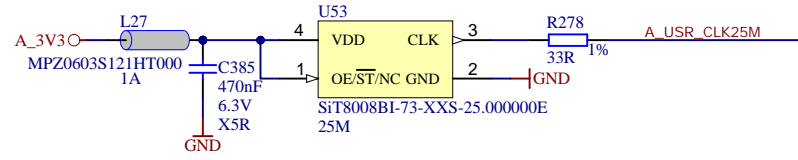
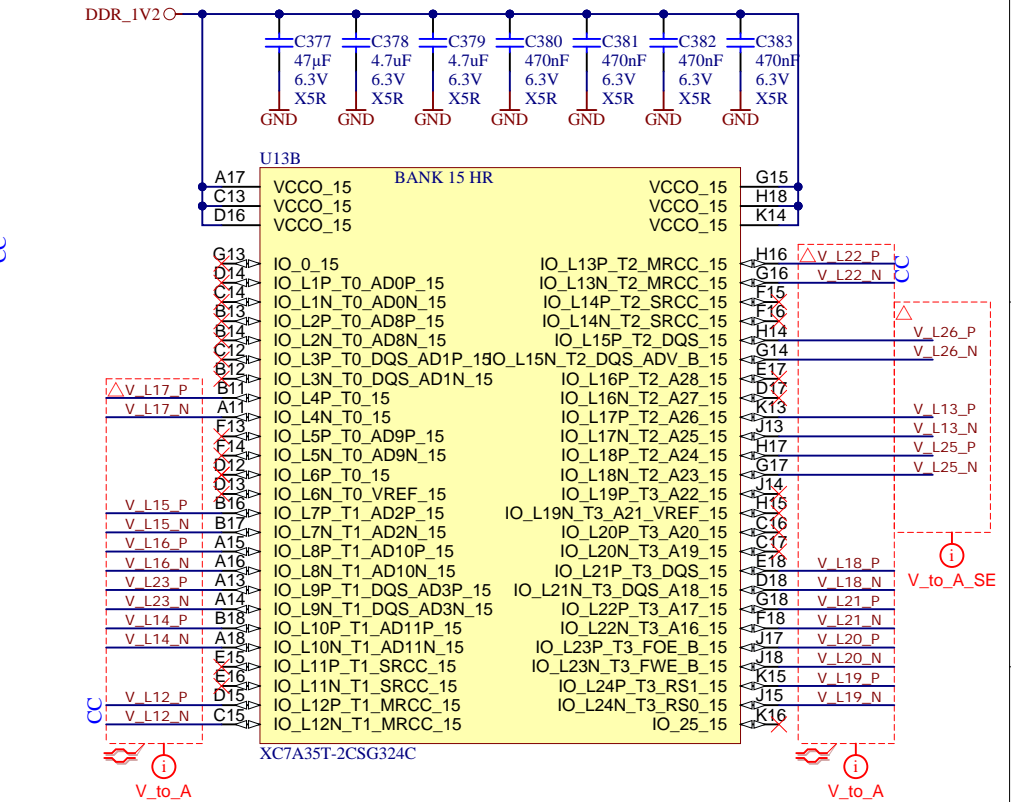
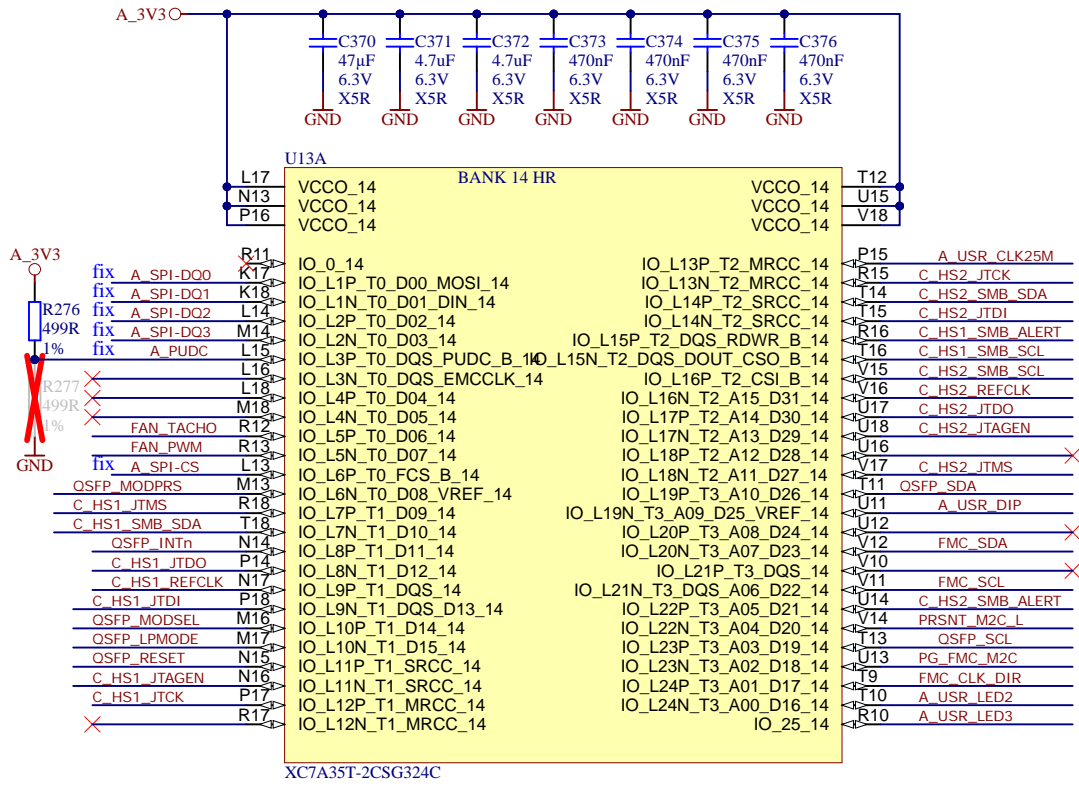


101 - ARTIX and VERSAL in chain
010 - only VERSAL

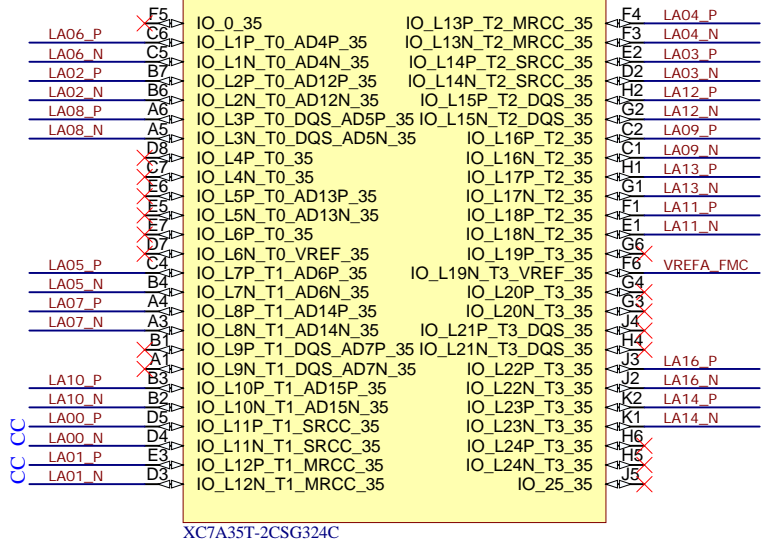
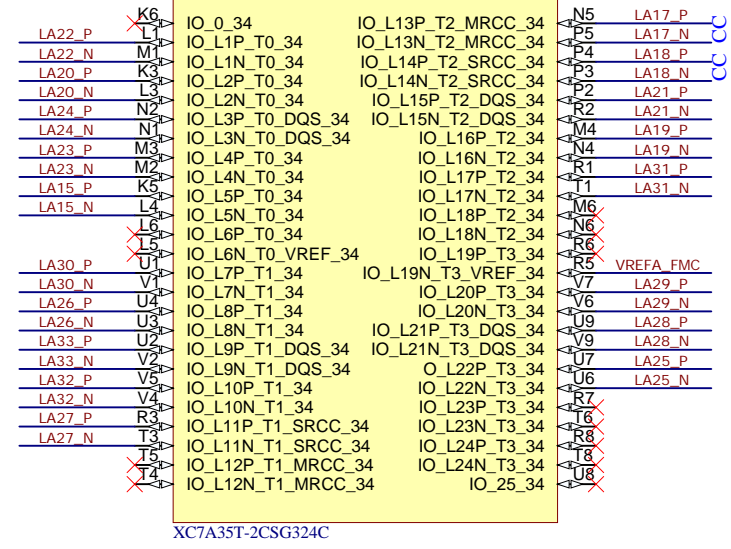
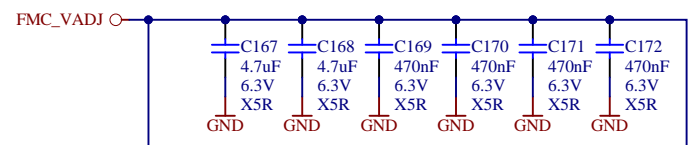
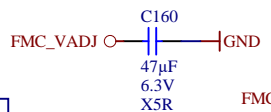
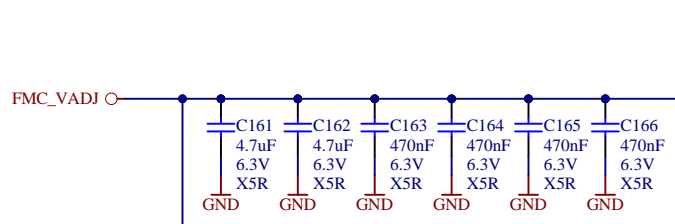
~~J18~~
ZigZag Placeholder 1 row 6 pin header



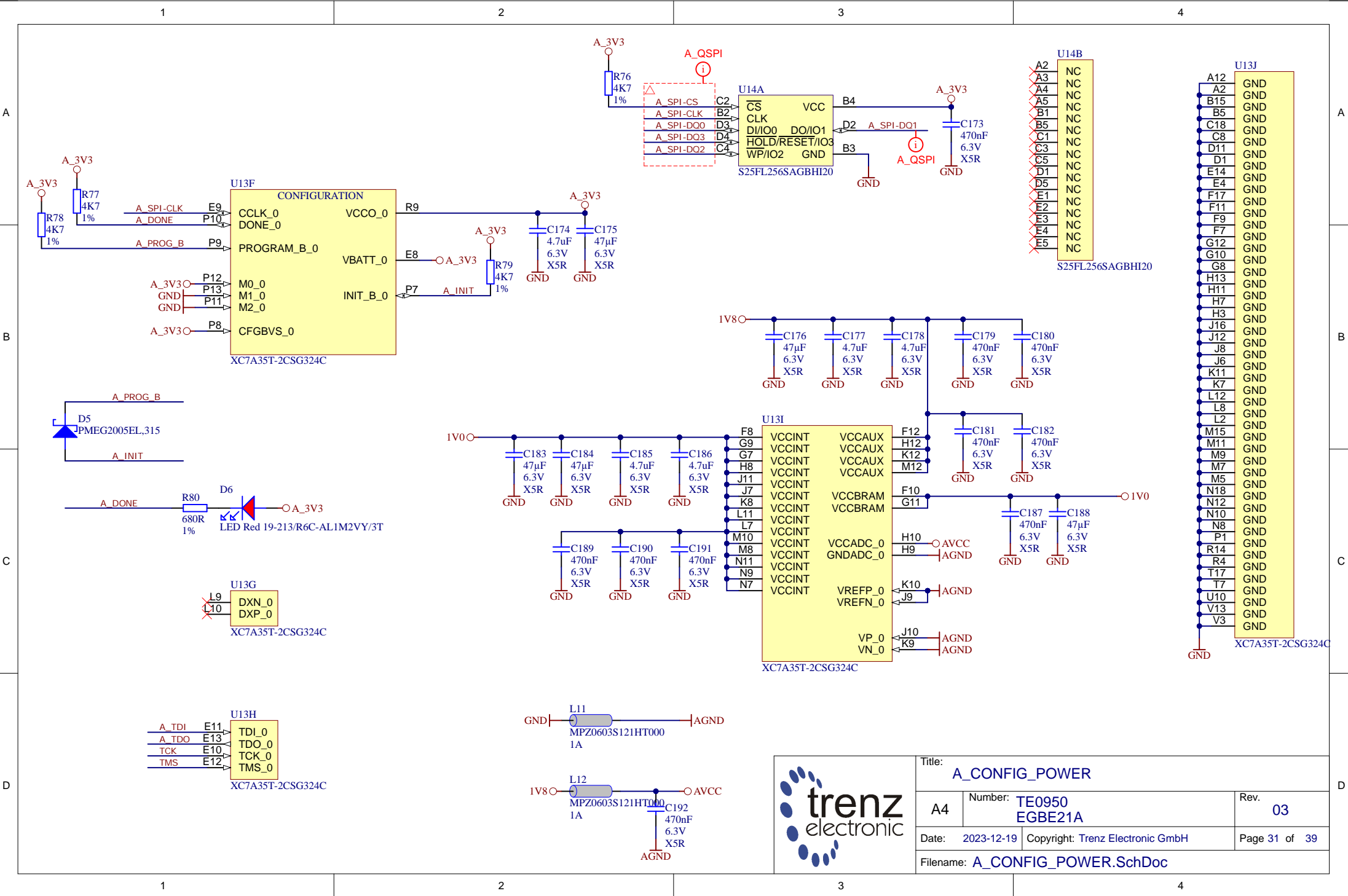
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Date: 2024-02-15	Copyright: Trenz Electronic GmbH	
Filename: FTDI.SchDoc		Page 28 of 39




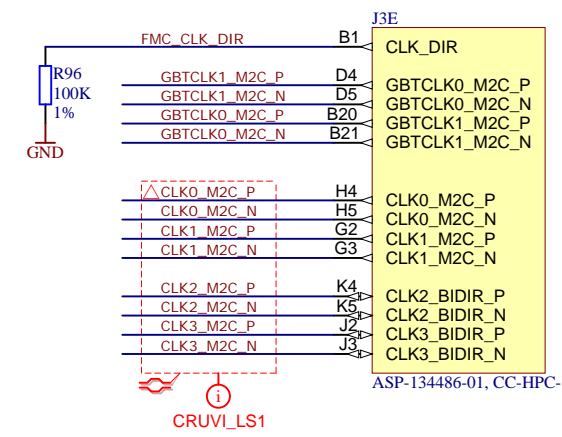
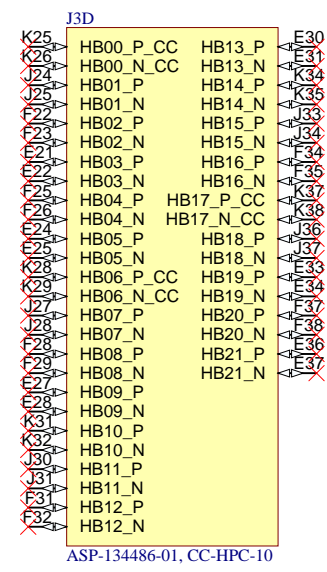
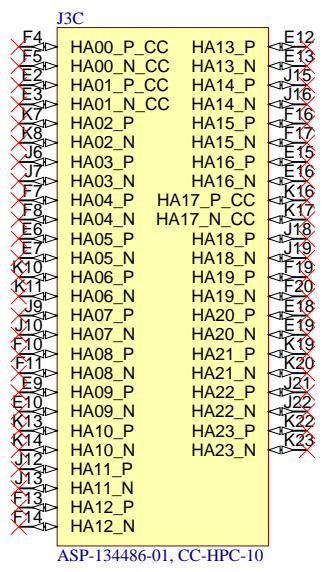
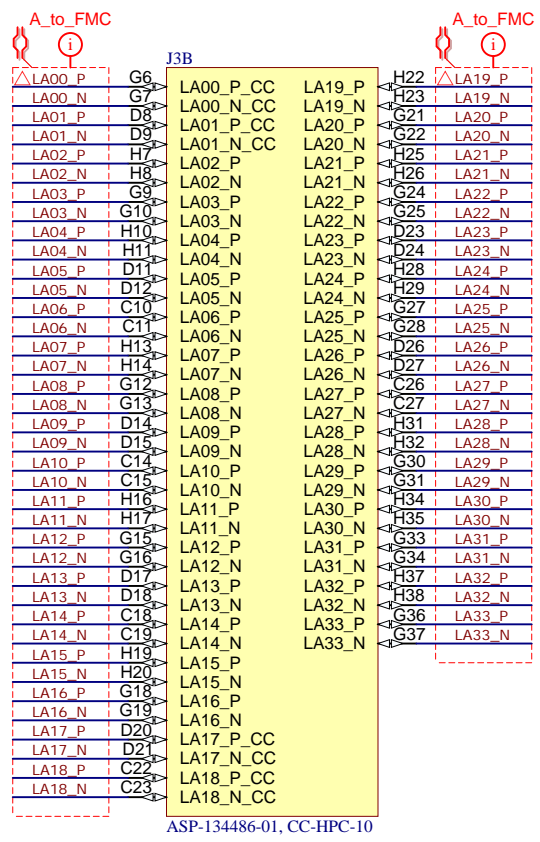
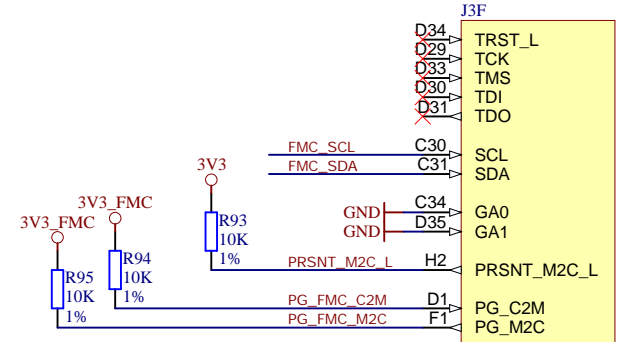
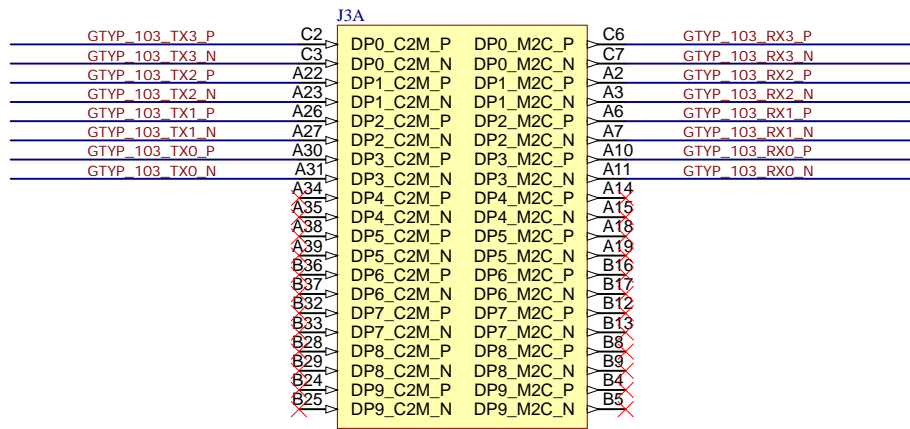
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Date: 2023-12-19	Copyright: Trenz Electronic GmbH	
Page 29 of 39		
Filename: A_HR_14_15_16.SchDoc		



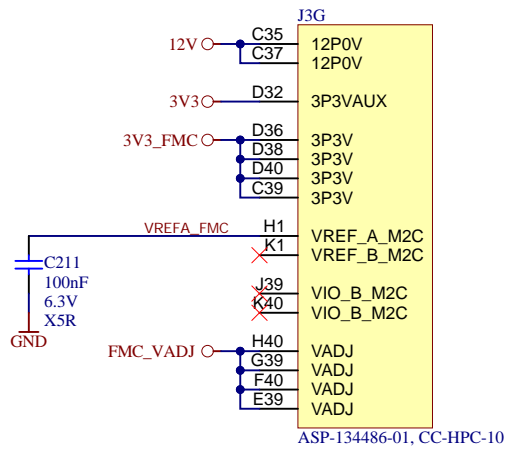
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Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 30 of 39
Filename: A_HR_34_35.SchDoc		



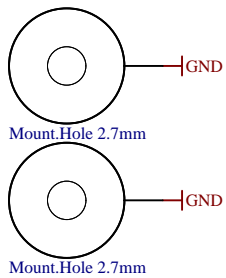
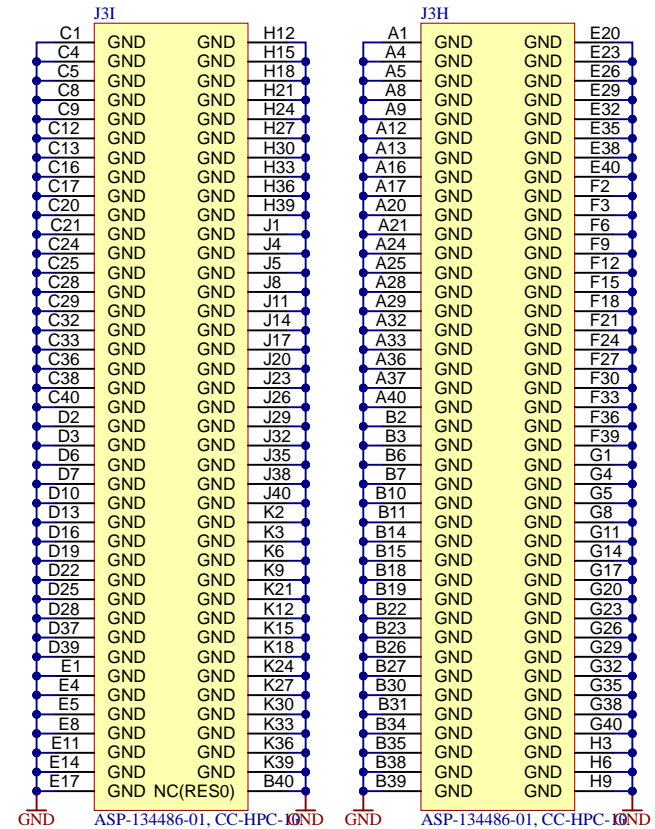
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		A4	Number: TE0950 EGBE21A
Date: 2023-12-19		Copyright: Trenz Electronic GmbH	
Page 31 of 39		Page 31 of 39	
Filename: A_CONFIG_POWER.SchDoc			



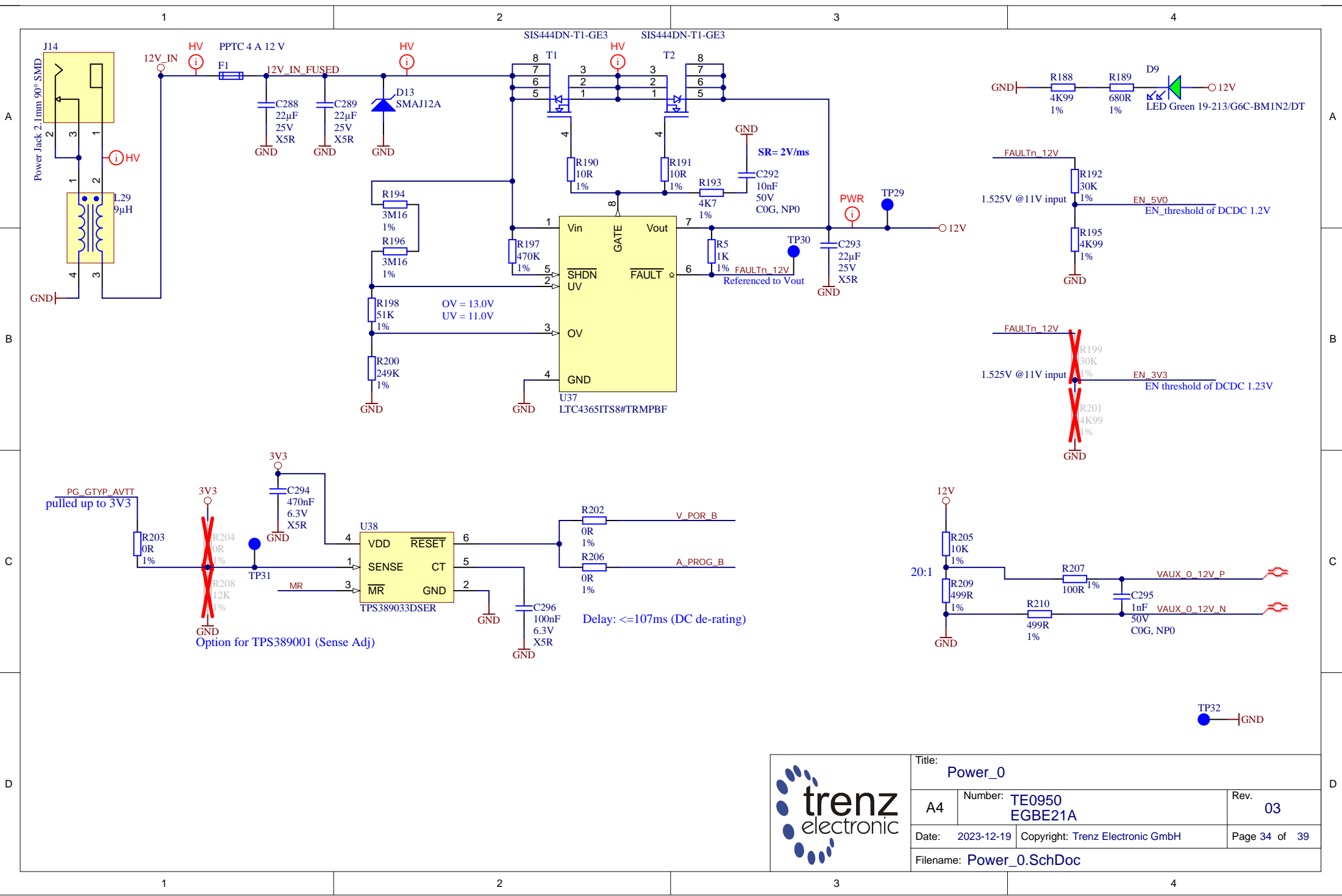
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A4	Number: TE0950 EGBE21A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 32 of 39
Filename: FMC.SchDoc		



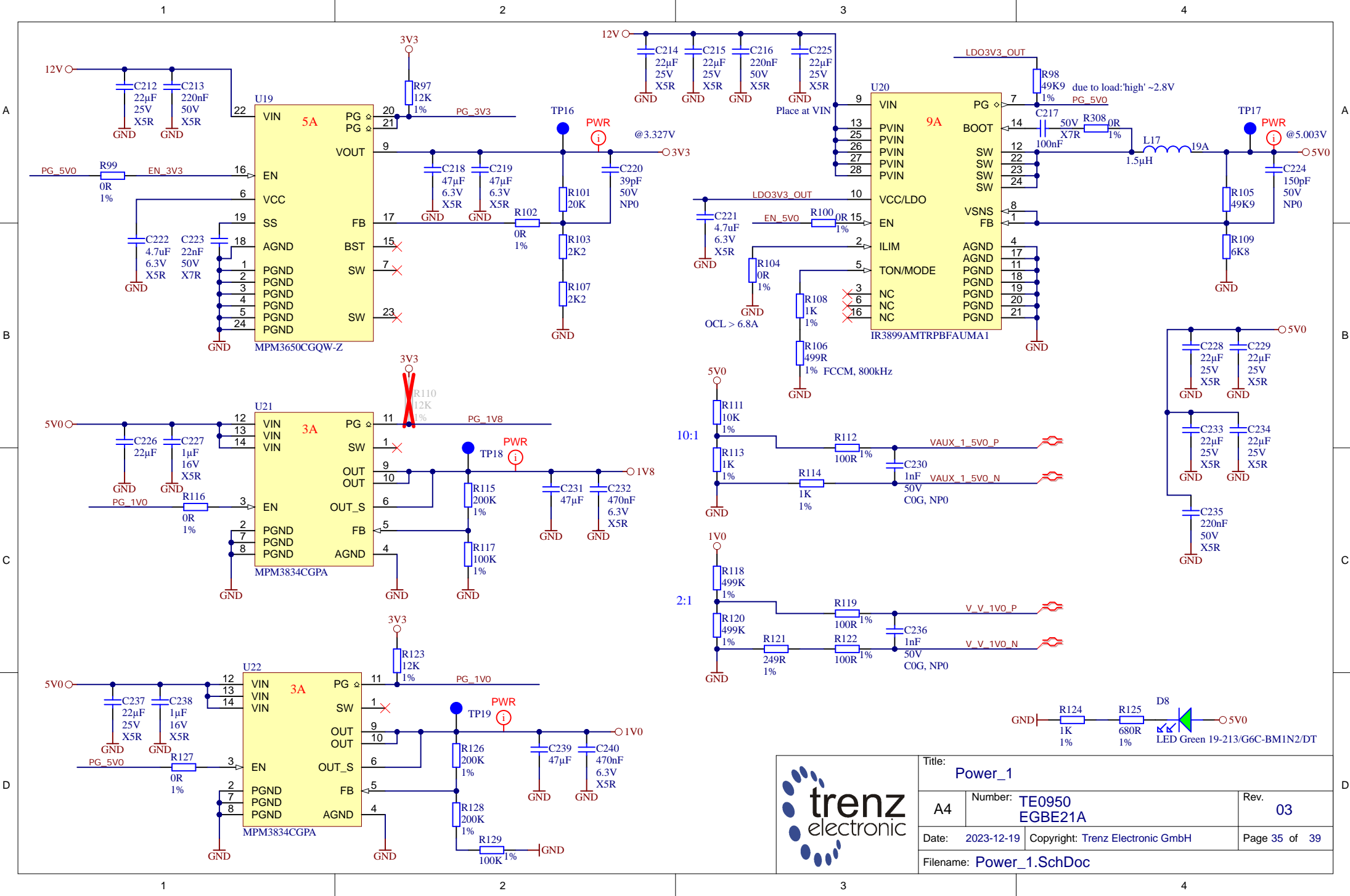
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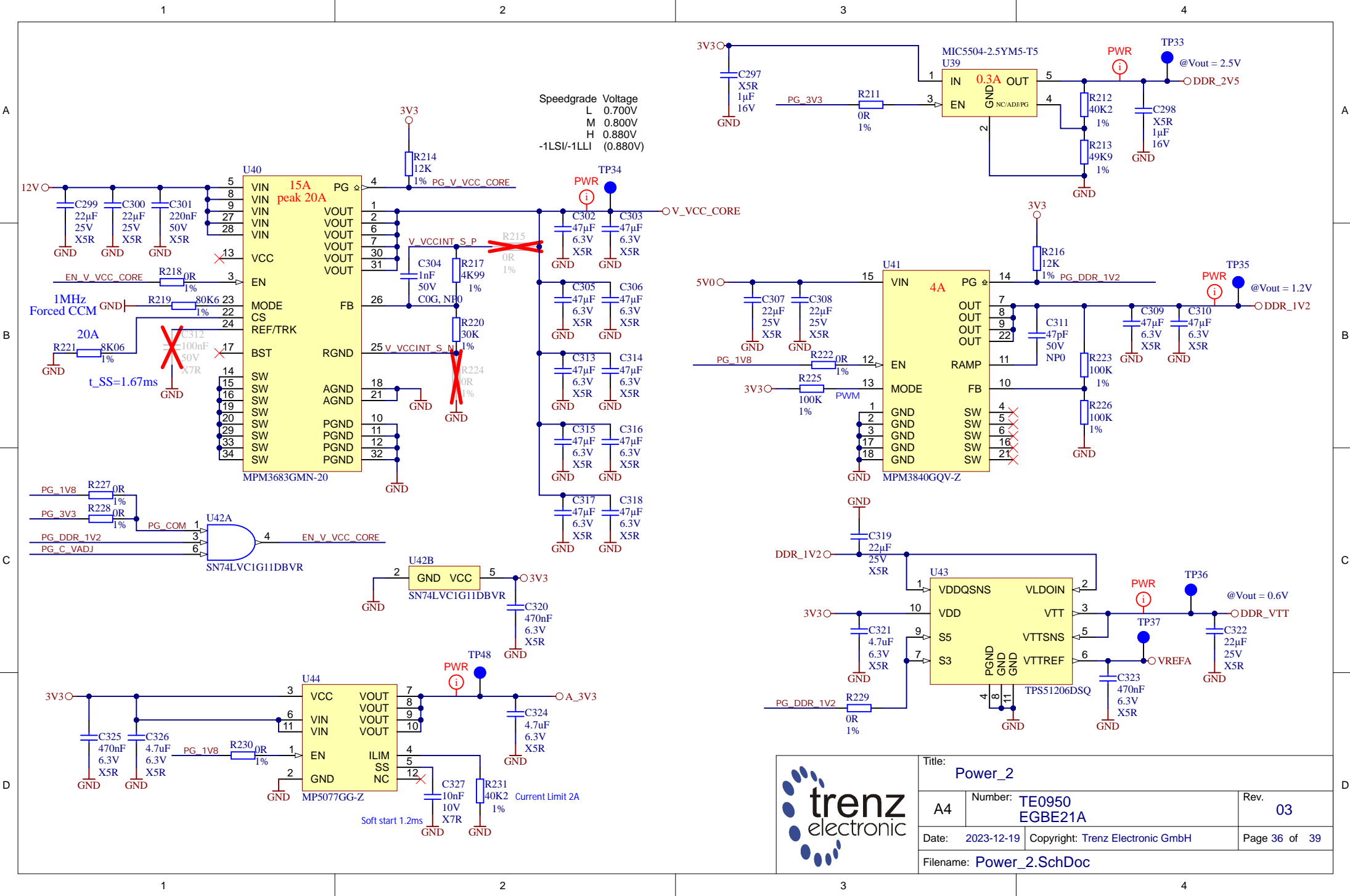


Title: FMC_Power		
A4	Number: TE0950 EGBE21A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 33 of 39
Filename: FMC_Power.SchDoc		



Title: Power_0		
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Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 34 of 39
Filename: Power_0.SchDoc		

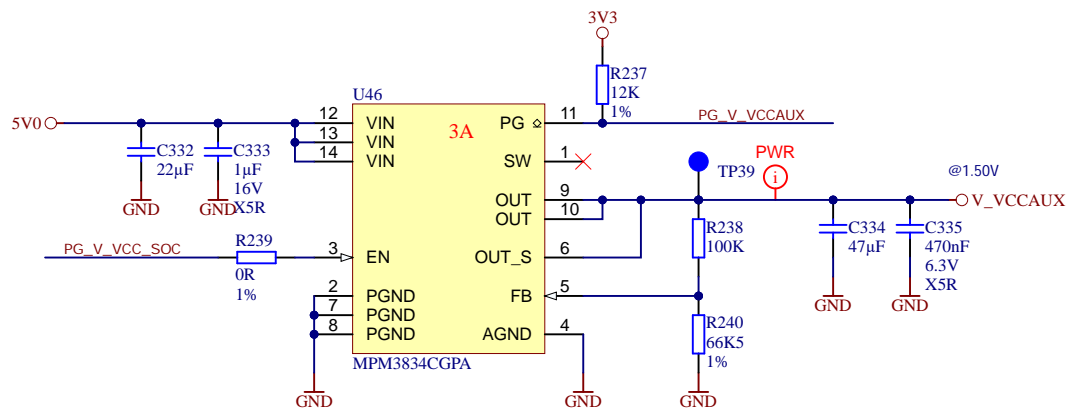
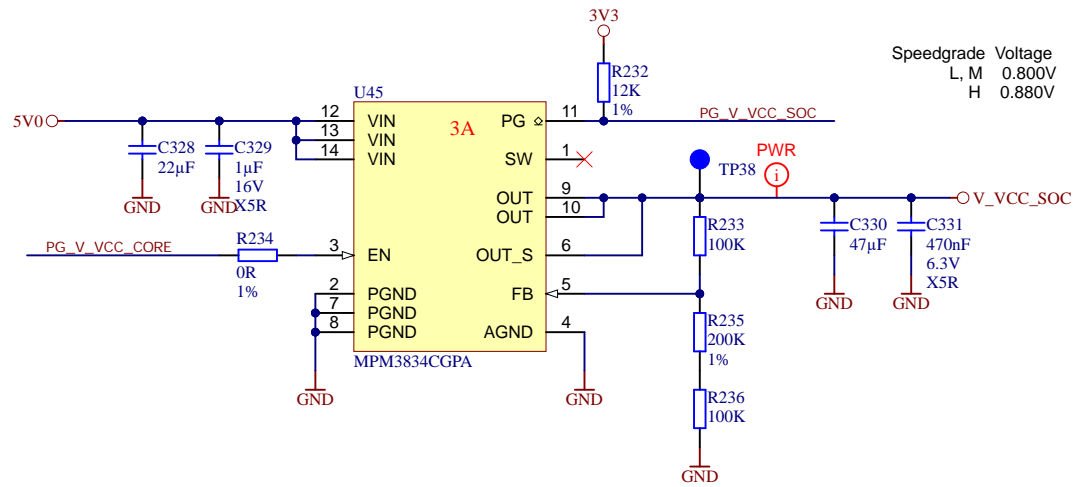




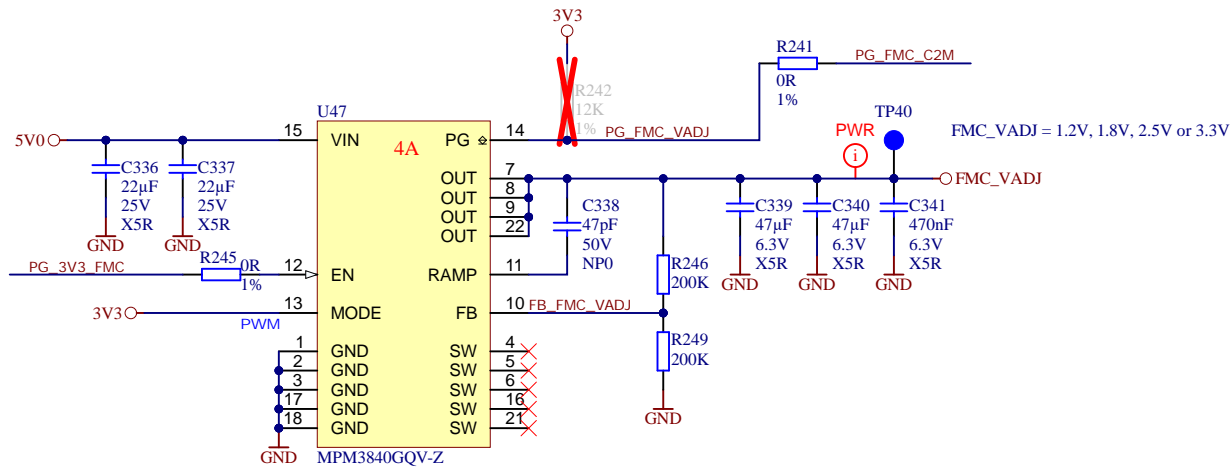
trenz electronic

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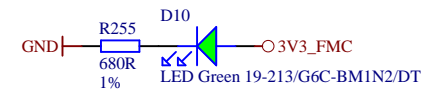
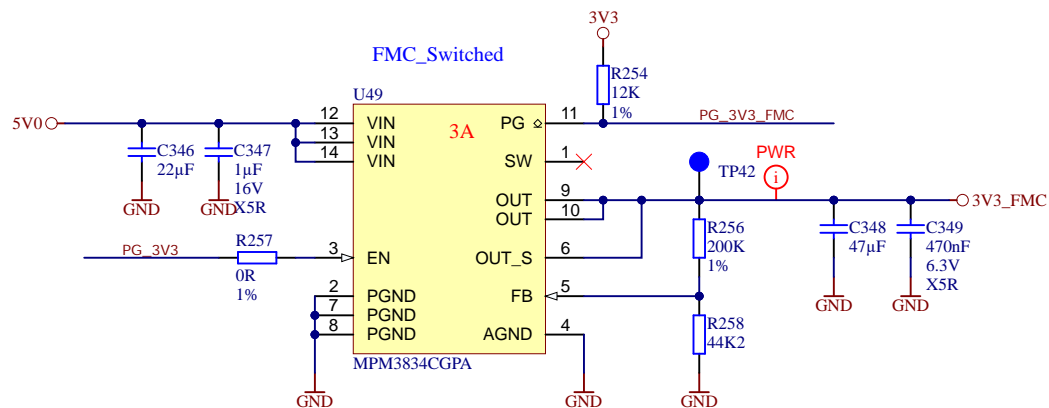
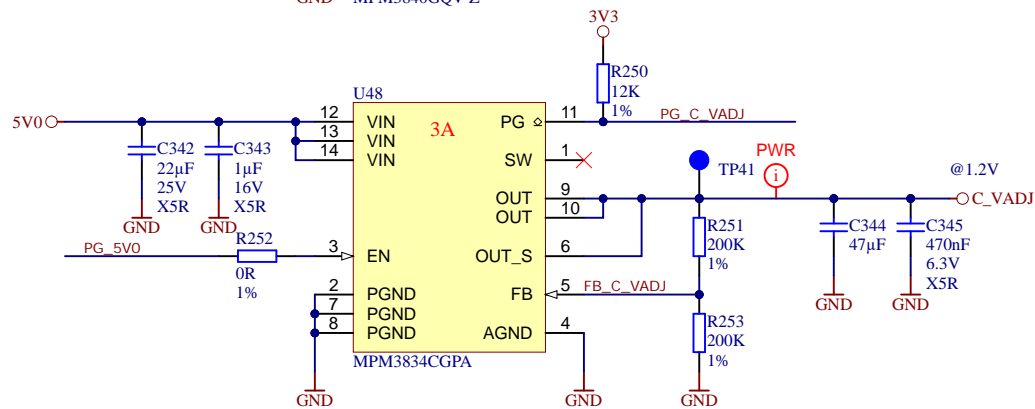
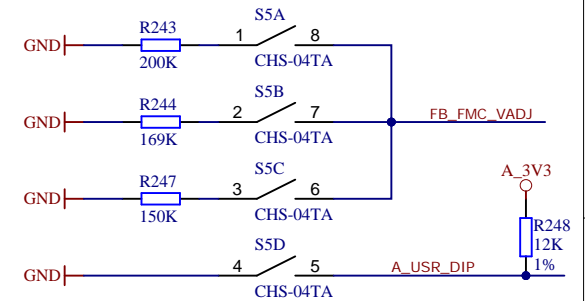
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Date: 2023-12-19	Copyright: Trenz Electronic GmbH	
Filename: Power_2.SchDoc		Page 36 of 39



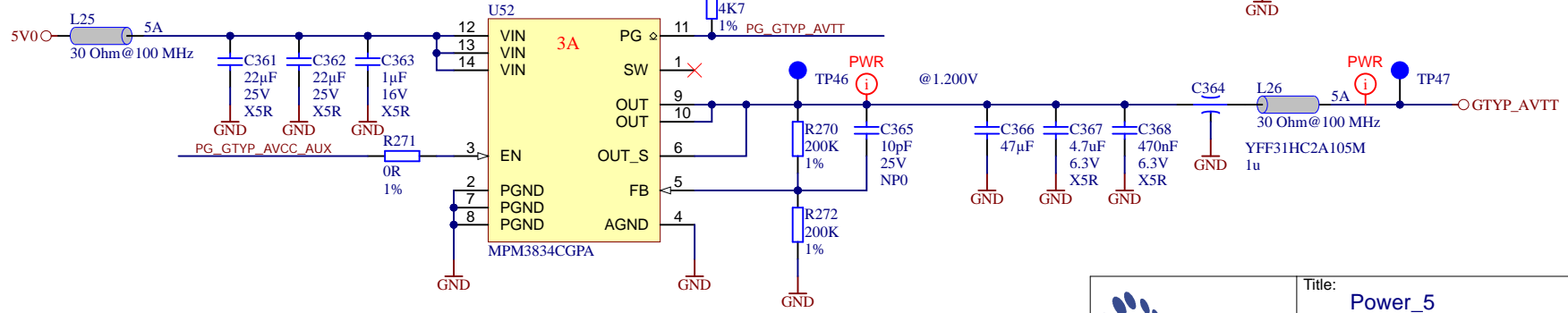
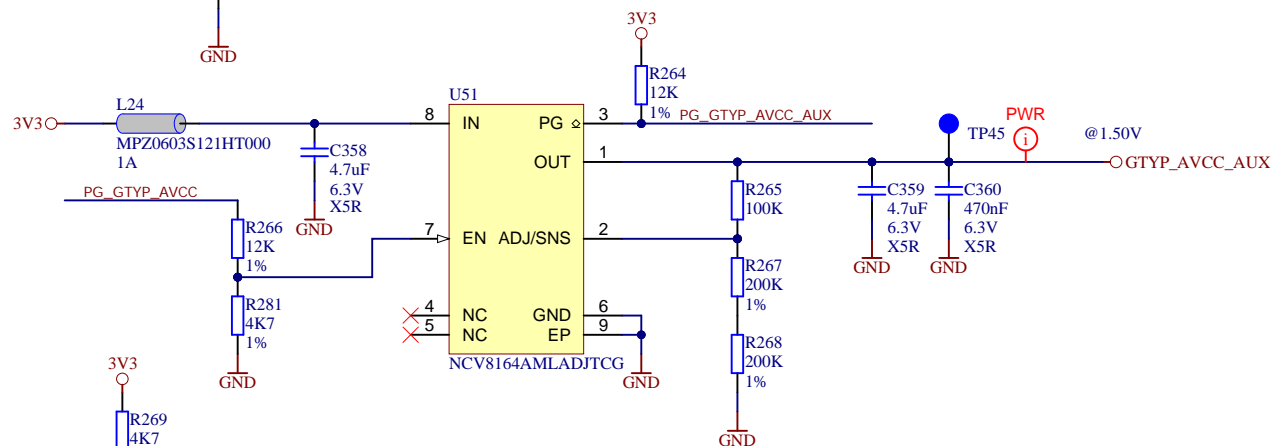
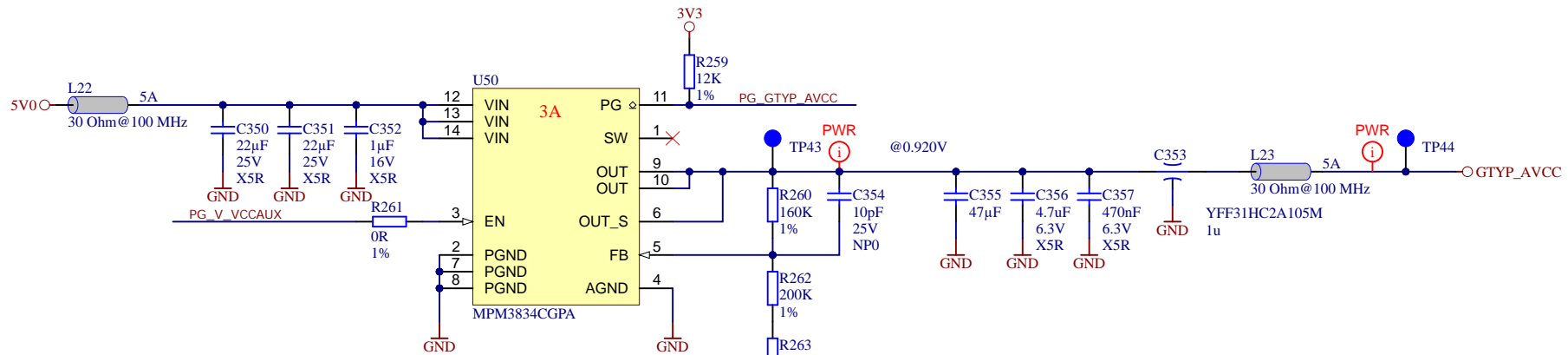
Title: Power_3		
A4	Number: TE0950 EGBE21A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	
Filename: Power_3.SchDoc		Page 37 of 39




1.2V 1.8V 2.5V 3.3V
 OFF ON ON ON
 OFF OFF ON ON
 OFF OFF OFF ON



Title: Power_4		
A4	Number: TE0950 EGBE21A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 38 of 39
Filename: Power_4.SchDoc		



			Title: Power_5	
			A4	Number: TE0950 EGBE21A
Date: 2023-12-19		Copyright: Trenz Electronic GmbH		Page 39 of 39
Filename: Power_5.SchDoc				