

Regarding the usage of our schematics and alike documentation for Trenz module TE0950.

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Schematics and other handouts serve for informational purposes only!

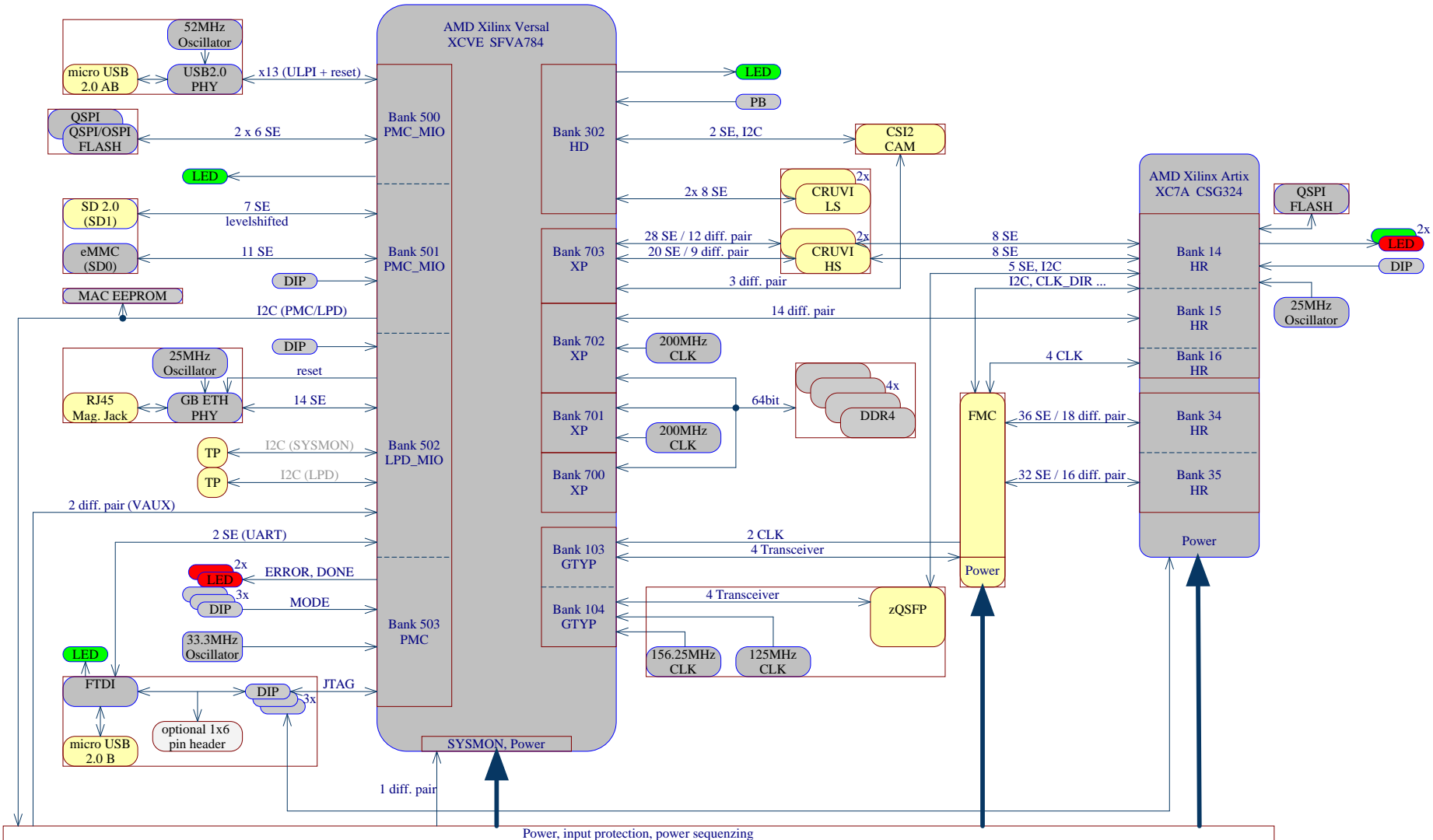
Drawn by	MR
Checked by	ED
Assembly variant	EGBE22A
Created by	MR
Modified by	MR
Modified at	2023-12-19



Title: Legal Notices		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 12.01.2024	Copyright: Trenz Electronic GmbH	Page 1 of 39
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REV	Description	
-01	Initial revision	MR
-02	<ol style="list-style-type: none"> 1. Inverted card detect (pullup-> pulldown) 2. Increased number of capacitors on VTT (C388,C389) 3. Added 1K pullup on FAULTn_12V (R5) 4. Added 4-pin connector J17 for FAN and corresponding circuit. PWM and TACHO connected to ARTIX 5. VERSAL JTAG connection corrected 6. Added CRUVI Connector description on silkscreen 7. Changed polarity for CSI2-CAM diff pairs 8. Update from library 9. Changed R266 to 12K and added R281 10. Changed enable 3V3 after 5V0 (R99), Pullup on PG_5V0 connected to 5V0 rail. 11. Replaced C256 (2,2µF) by 2x 1µF 12. Set R131 and R132 to not fitted (2023-08-18) 	MR
-03	<ol style="list-style-type: none"> 1. Added OSPI compatibility, renamed sheet (QSPI_SD_eMMcC -> SD_eMMcC) and added sheet QSPI_OSPI. Added boot mode "OSPI" selectable via dip S2C, former connection (User PMC MIO27) moved to S4D. 2. Added D12 and pull-up R170 for correct reset levels, set R131 and R132 to assembled 3. Added Pin header J18 for direct JTAG access 4. Moved V_L22 diff. pair to clock capable pins on Atrix 5. Small improvements of MGT routing, added anti-pads, optimized VIAs, increased clearance. 6. Versal changed from Engineering Sample to production (pre-production for ES9749) chips 7. Replaced U20 by IR3899A DCDC 8. Removed U34 (I2C levelshifter for former U20) 9. Added Common mode chock L29, Fuse F1, C288, C289 and D13 to 12V input rail. 10. Moved PM1, PM2, PM5, PM6 11. Silkscreen dip switch description: <ul style="list-style-type: none"> - added OSPI boot mode, - S4D is user dip switch connected to Versal PMC (MIO27) 12. Updated all components from lib (2024-02-15) 13. Set ZigZag Placeholder for JTAG (J18) to not fitted to make it more clear that there is no header fitted 14. Updated AMD Versal (U1) Schematic Symbol 	MR

	Title: Revision History		
	A4	Number: TE0950 EGBE22A	Rev. 03
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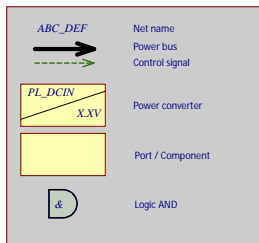
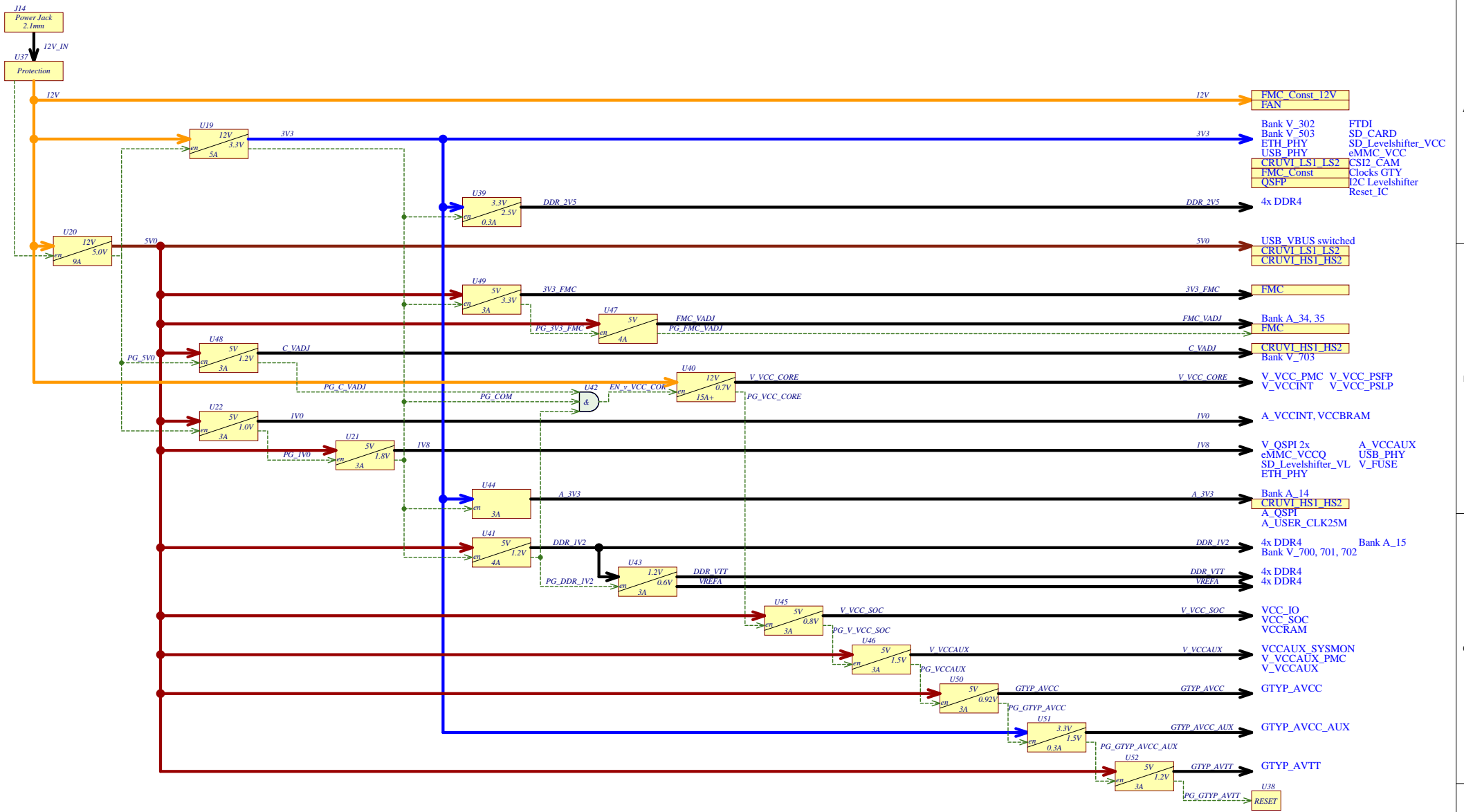


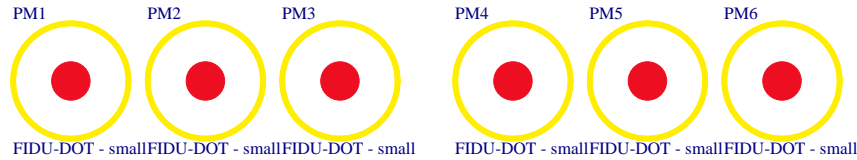
Special notes:

*Versal XCVE2302-1LSESFVA784-ES9749 is a preproduction die.
No changes to production chips (without ES number) are expected.*



Title: System Overview		
A4	Number: TE0950 EGBE22A	Rev. 03
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I2C Addresses:

Device	Bus	Address	Note
24AA025E48	PMC_I2C	1010000 50H	EEPROM for MAC with user area

MECH1
TE Address Overlay

LOGO ADDRESS

LOGO1
TE Logo PRINT Layer

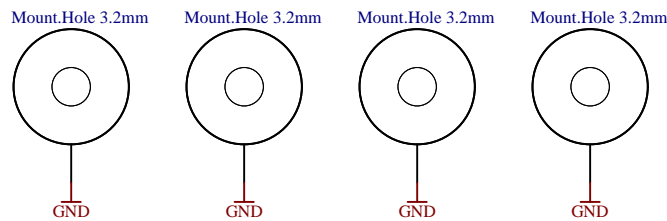
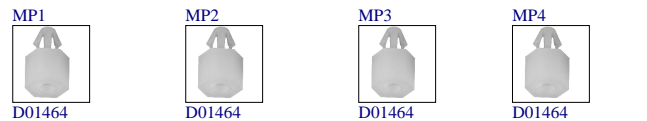
LOGO PRINT

Serial1
Serial
Serialnumber 6,3 x 6.3mm

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
12V_IN	IN	12V	+/-5%	Board Power	-
5V0	OUT	5.0V	+/-3%	CRUVI LS and HS 5V	Shared with onboard 5V supplies and with further switch (U29) for rail USB_VBUS_SUP via jumper (J5) connectable to USB (J8).
3V3	OUT	3.3V	+/-3%	QSFP, CRUVI LS 3.3V, CSI-2 CAM	Shared with VERSAL VCCO Bank 302 and onboard peripherals.
C_VADJ	OUT	1.2V	+/-3%	CRUVI HS IO	Shared with VERSAL VCCIO XPIO Bank 703.
A_3V3	OUT	3.3V	+/-3%	CRUVI HS 3.3V	Shared with ARTIX VCCIO Bank 14 and onboard peripherals.
12V	OUT	12V	+/-5%	FMC	Derived from 12V_IN after input protection. Shared with onboard peripherals.
3V3_FMC	OUT	3.3V	+/-3%	FMC	-
FMC_VADJ	OUT	1.2V - 3.3V	+/-3%	FMC	Selectable by dip settings.

Versal XCVE2302-1LSESFVA784-ES9749 is a preproduction die.
No changes to production chips (without ES number) are expected.

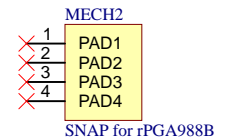


CE1
CE Logo on Top Overlay

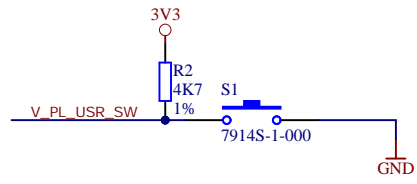
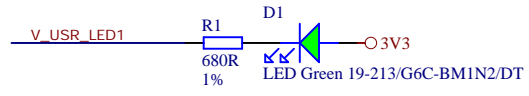
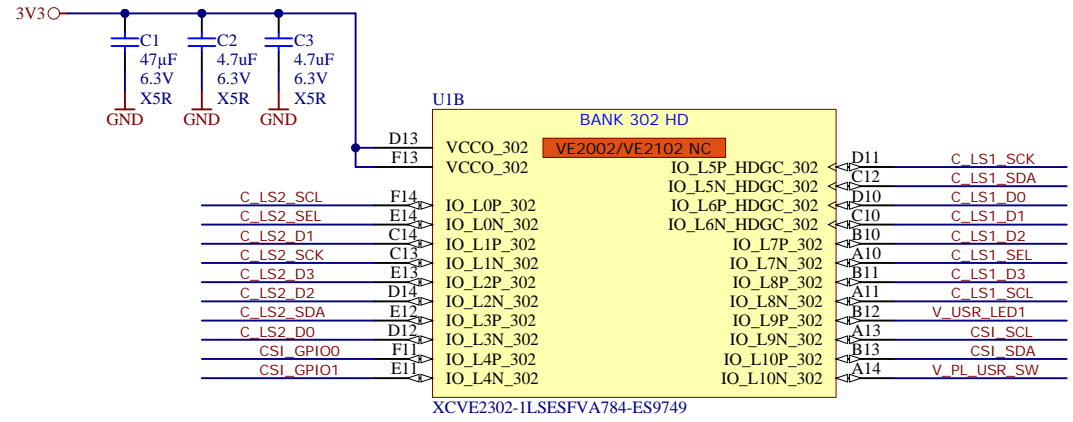
CE-TOPOVERLAY


UKCA1
UKCA Logo on Top Overlay

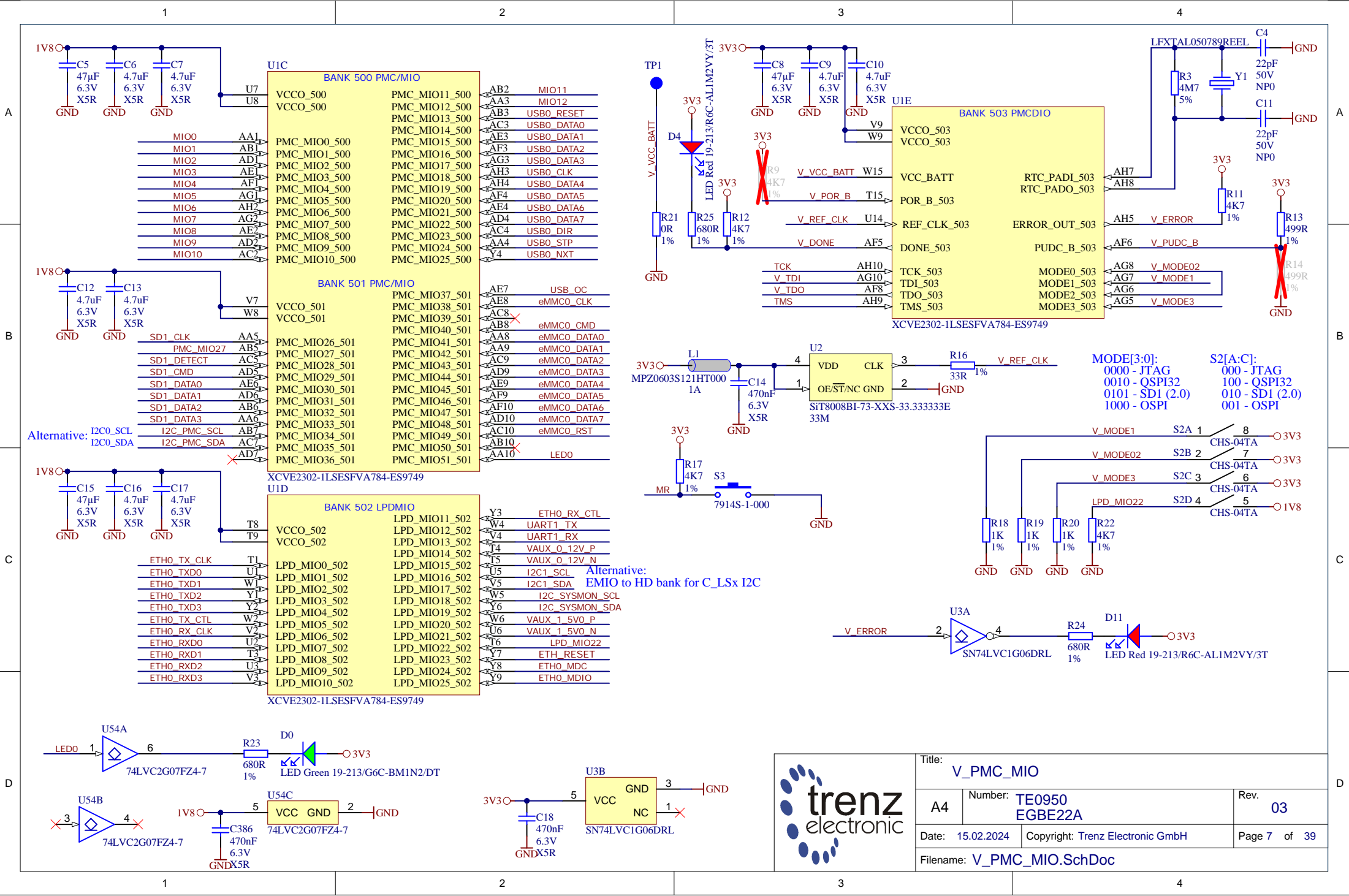
UKCA-TOPOVERLAY



	Title: TEB0850	
	A4	Number: TE0950 EGBE22A
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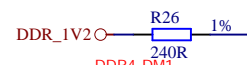
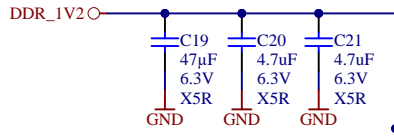
		Title: V_HD	
		A4	Number: TE0950 EGBE22A
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Title: **V_PMC_MIO**

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UIF

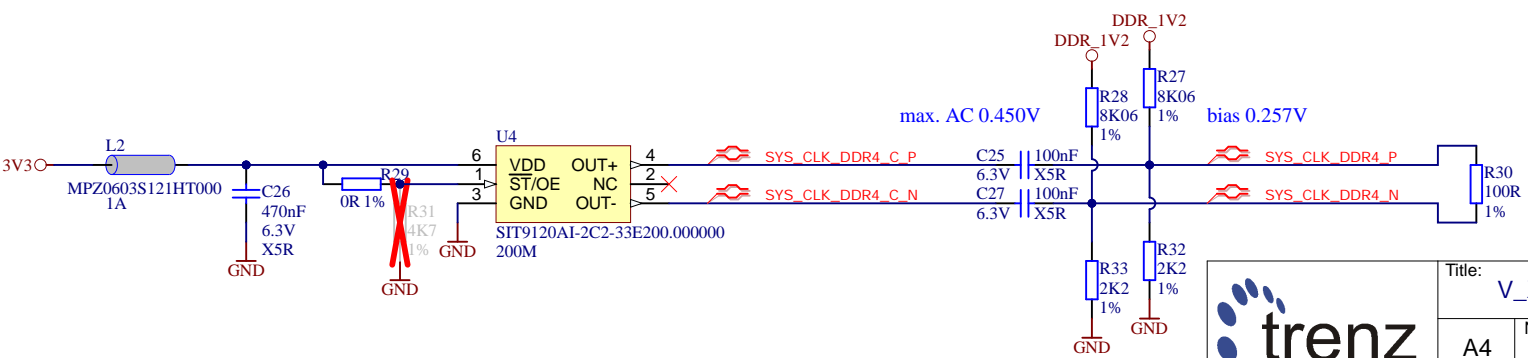
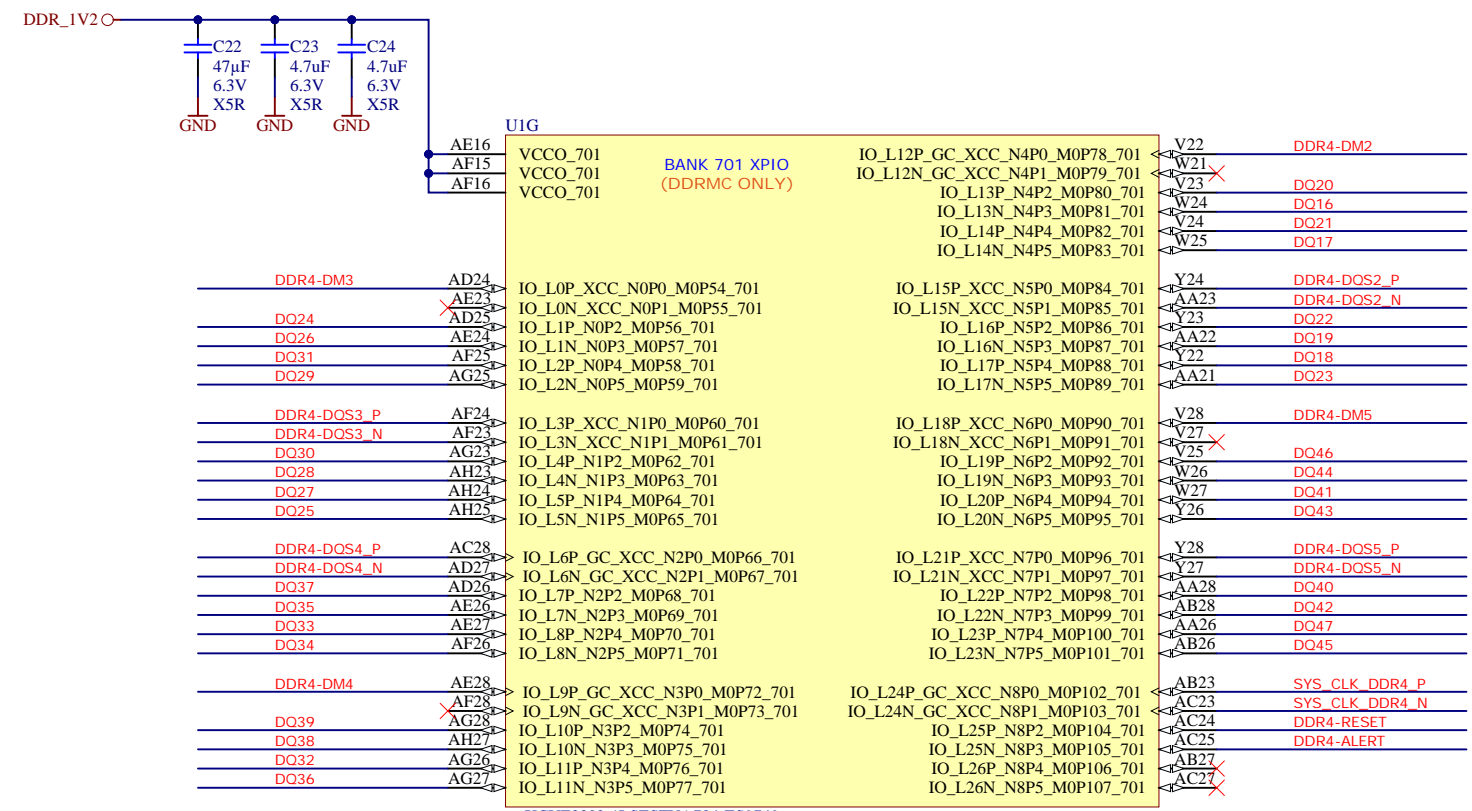
AE11	VCCO_700	BANK 700 XPIO (DDRMIC ONLY)	IO_L12P_GC_XCC_N4P0_M0P24_700	AD12	DDR4-A4
AE12	VCCO_700		IO_L12N_GC_XCC_N4P1_M0P25_700	AD11	DDR4-BA1
AF11	VCCO_700		IO_L13P_N4P2_M0P26_700	AC14	
			IO_L13N_N4P3_M0P27_700	AD14	DDR4-PAR
			IO_L14P_N4P4_M0P28_700	AC17	DDR4-CS
			IO_L14N_N4P5_M0P29_700	AD17	DDR4-A15
				AC19	DDR4-CLK0_P
			IO_L15P_XCC_N5P0_M0P30_700	AD19	DDR4-CLK0_N
			IO_L15N_XCC_N5P1_M0P31_700	AD20	
			IO_L16P_N5P2_M0P32_700	AD21	DDR4-A14
			IO_L16N_N5P3_M0P33_700	AD22	DDR4-A2
			IO_L17P_N5P4_M0P34_700	AE22	DDR4-A1
			IO_L17N_N5P5_M0P35_700		
				AB12	DDR4-A0
			IO_L18P_XCC_N6P0_M0P36_700	AC11	DDR4-ACT
			IO_L18N_XCC_N6P1_M0P37_700	AB14	DDR4-A9
			IO_L19P_N6P2_M0P38_700	AC13	DDR4-A16
			IO_L19N_N6P3_M0P39_700	AB15	DDR4-A3
			IO_L20P_N6P4_M0P40_700	AC16	DDR4-BA0
			IO_L20N_N6P5_M0P41_700		
				AB18	DDR4-BG0
			IO_L21P_XCC_N7P0_M0P42_700	AB17	DDR4-A10
			IO_L21N_XCC_N7P1_M0P43_700	AB20	
			IO_L22P_N7P2_M0P44_700	AC20	
			IO_L22N_N7P3_M0P45_700	AB21	DDR4-CKE0
			IO_L23P_N7P4_M0P46_700	AC22	DDR4-ODT0
			IO_L23N_N7P5_M0P47_700		
				AD16	DDR4-A6
			IO_L24P_GC_XCC_N8P0_M0P48_700	AD15	DDR4-A13
			IO_L24N_GC_XCC_N8P1_M0P49_700	AE13	DDR4-A11
			IO_L25P_N8P2_M0P50_700	AE14	DDR4-A8
			IO_L25N_N8P3_M0P51_700	AE17	DDR4-A5
			IO_L26P_N8P4_M0P52_700	AE18	DDR4-BG1
			IO_L26N_N8P5_M0P53_700		

AA11	IO_VR_700
AH13	IO_L0P_XCC_N0P0_M0P0_700
AH12	IO_L0N_XCC_N0P1_M0P1_700
AH14	IO_L1P_N0P2_M0P2_700
AH15	IO_L1N_N0P3_M0P3_700
AH17	IO_L2P_N0P4_M0P4_700
AH18	IO_L2N_N0P5_M0P5_700
AG20	IO_L3P_XCC_N1P0_M0P6_700
AH19	IO_L3N_XCC_N1P1_M0P7_700
AG21	IO_L4P_N1P2_M0P8_700
AH20	IO_L4N_N1P3_M0P9_700
AG22	IO_L5P_N1P4_M0P10_700
AH22	IO_L5N_N1P5_M0P11_700
AG12	IO_L6P_GC_XCC_N2P0_M0P12_700
AG11	IO_L6N_GC_XCC_N2P1_M0P13_700
AF13	IO_L7P_N2P2_M0P14_700
AG13	IO_L7N_N2P3_M0P15_700
AF14	IO_L8P_N2P4_M0P16_700
AG15	IO_L8N_N2P5_M0P17_700
AG17	IO_L9P_GC_XCC_N3P0_M0P18_700
AG16	IO_L9N_GC_XCC_N3P1_M0P19_700
AF18	IO_L10P_N3P2_M0P20_700
AG18	IO_L10N_N3P3_M0P21_700
AE19	IO_L11P_N3P4_M0P22_700
AF19	IO_L11N_N3P5_M0P23_700

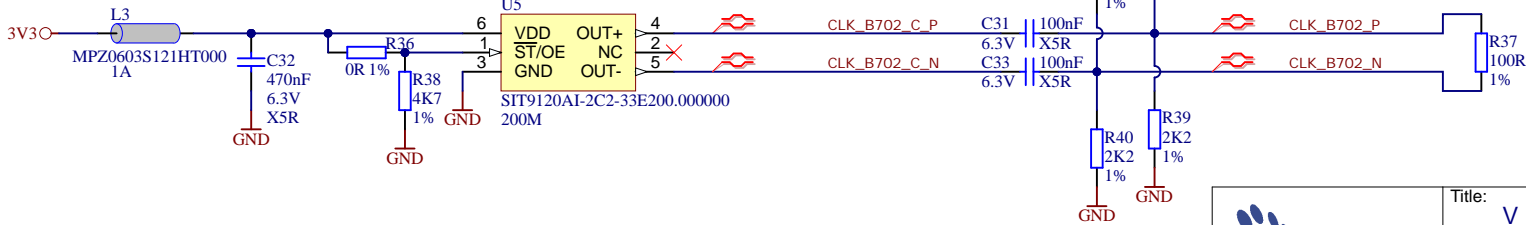
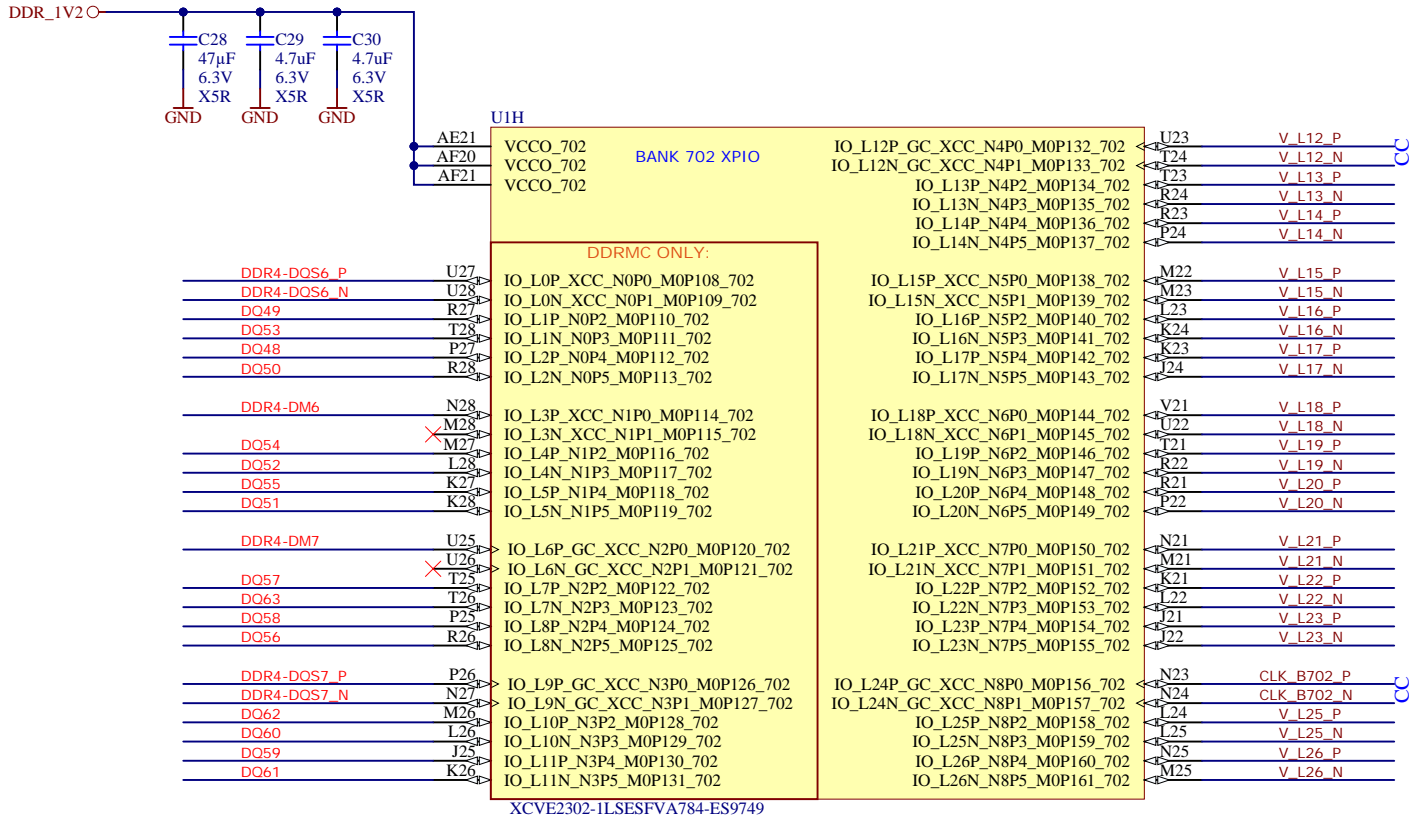
XCVE2302-1LSESFVA784-ES9749



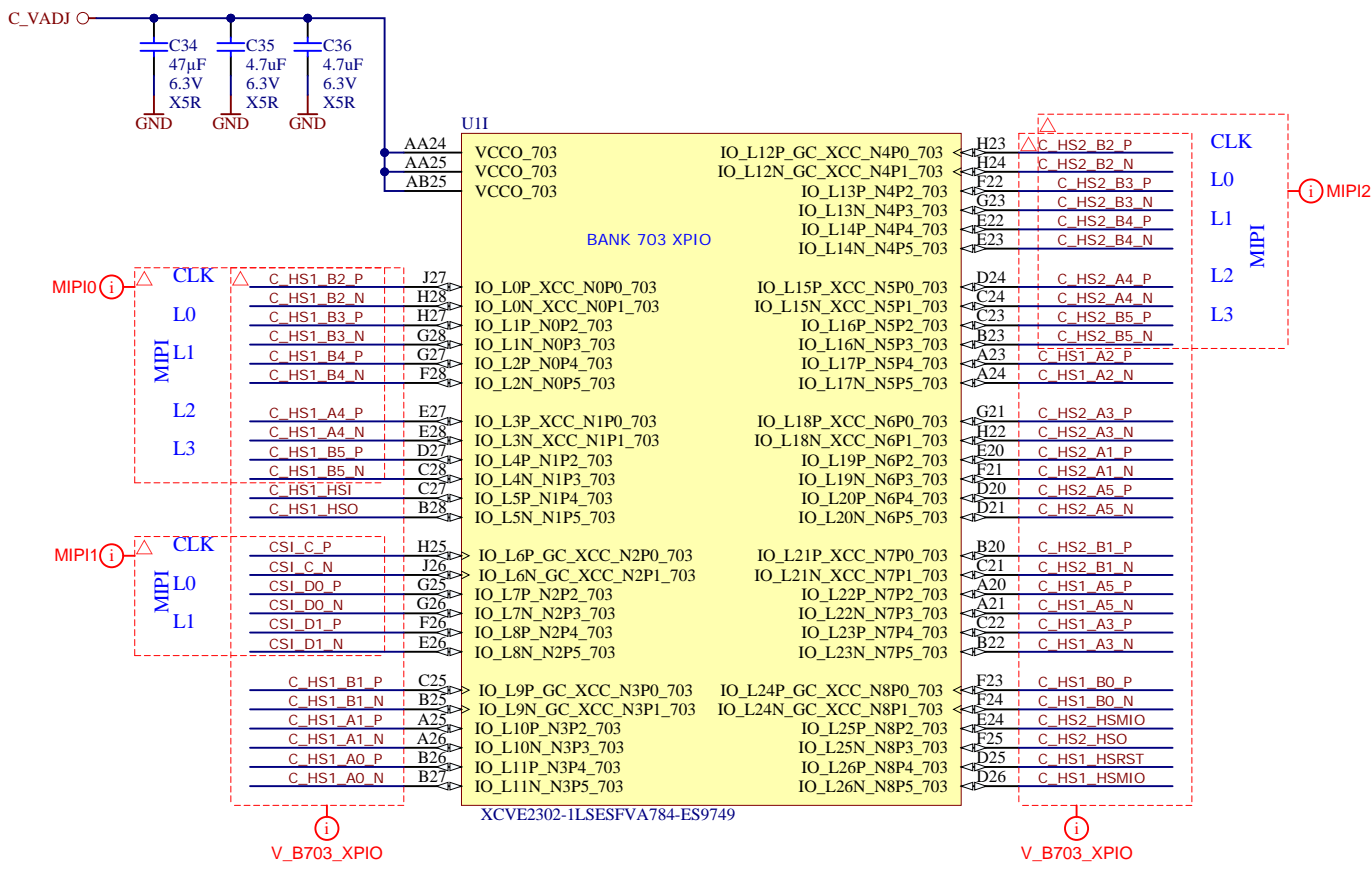
Title: V_XPIO_700		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2024-02-15	Copyright: Trenz Electronic GmbH	Page 8 of 39
Filename: V_XPIO_700.SchDoc		



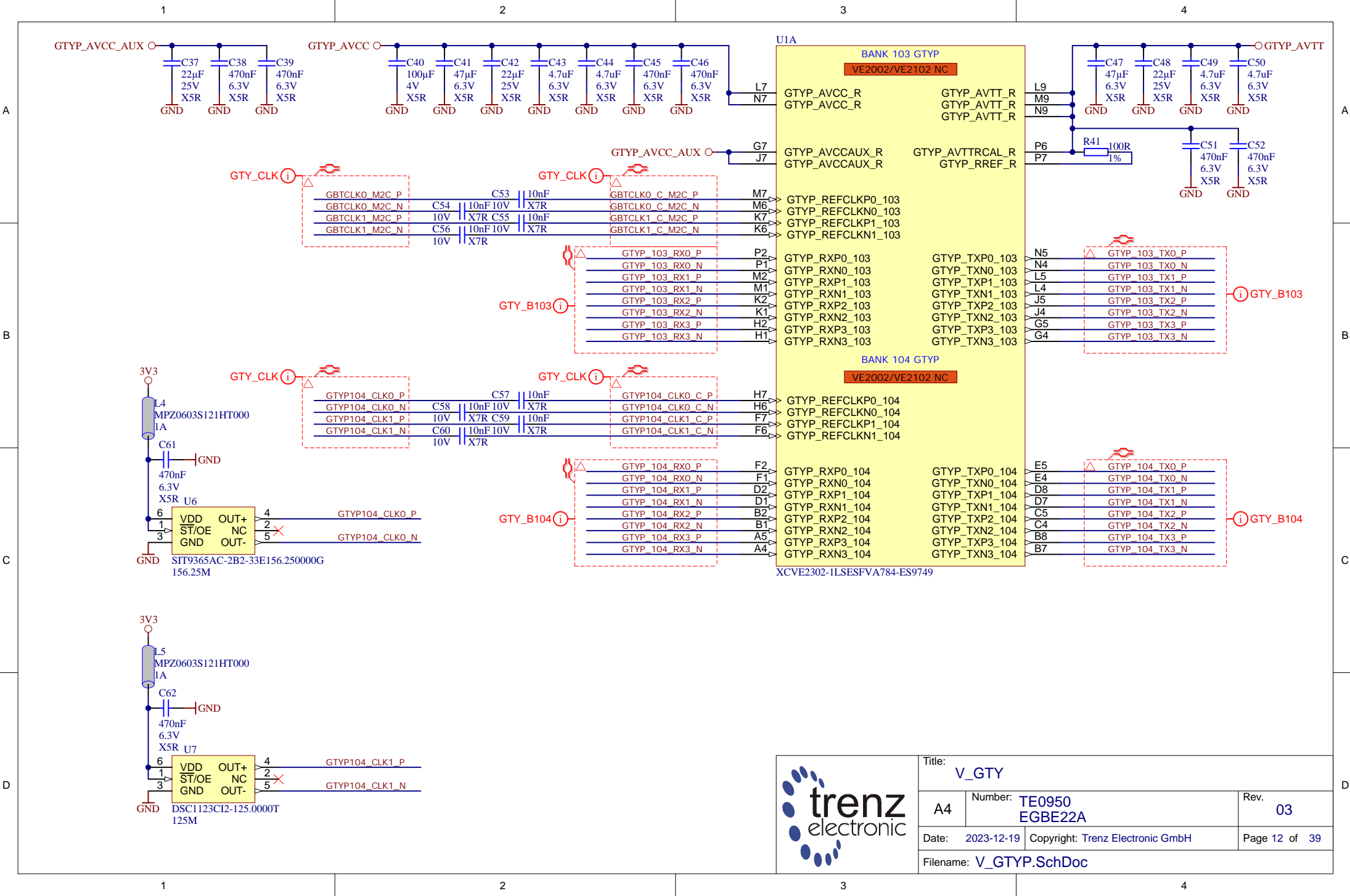
Title: V_XPIO_701		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2024-02-15	Copyright: Trenz Electronic GmbH	Page 9 of 39
Filename: V_XPIO_701.SchDoc		



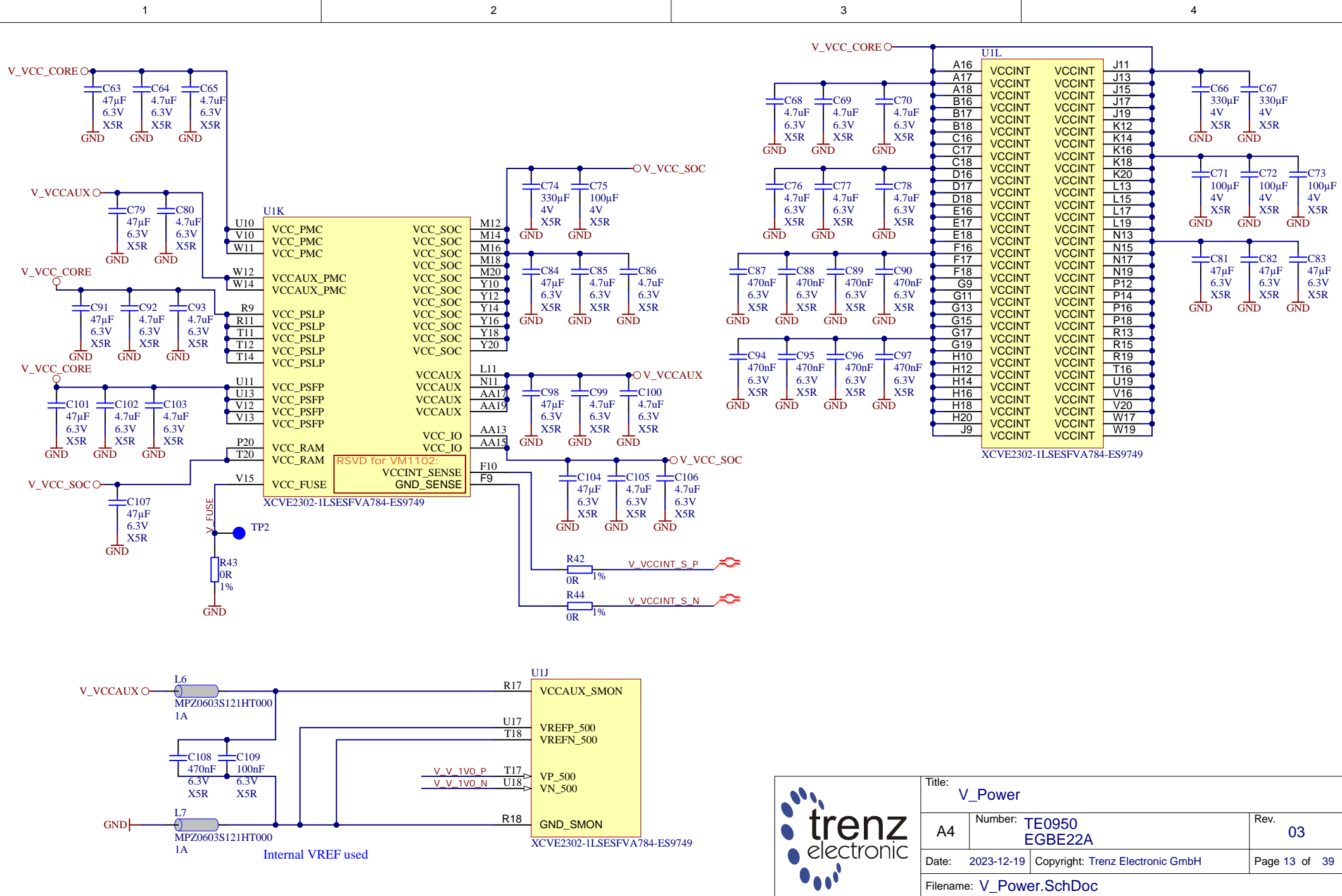
Title: V_XPIO_702		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2024-02-15	Copyright: Trenz Electronic GmbH	Page 10 of 39
Filename: V_XPIO_702.SchDoc		



Title: V_XPIO_703		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2024-02-15	Copyright: Trenz Electronic GmbH	Page 11 of 39
Filename: V_XPIO_703.SchDoc		



Title: V_GTY		
A4	Number: TE0950 EGBE22A	Rev. 03
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Filename: V_GTYP.SchDoc		



Title: V_Power		
A4	Number: TE0950 EGBE22A	Rev. 03
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Filename: V_Power.SchDoc		Page 13 of 39

1

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4

A

A

B

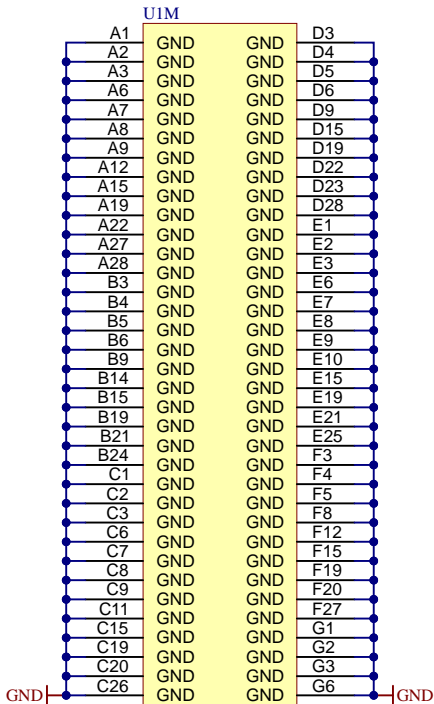
B

C

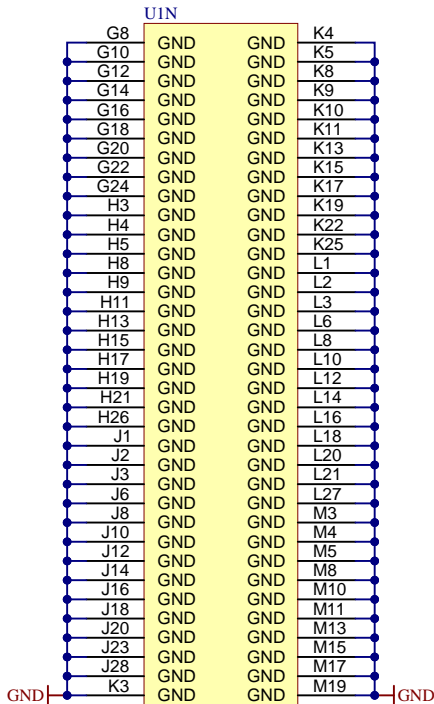
C

D

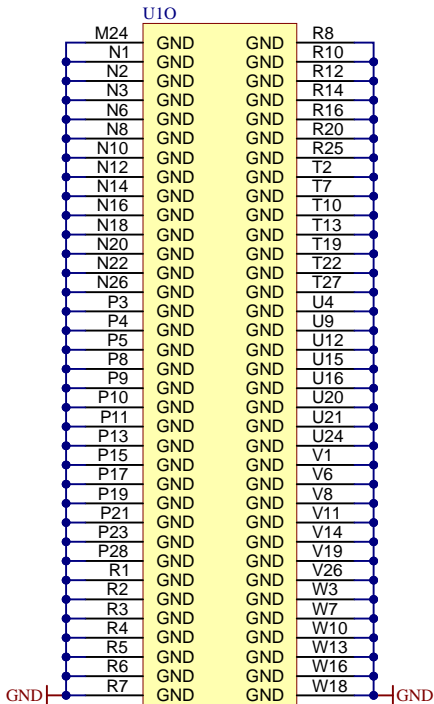
D



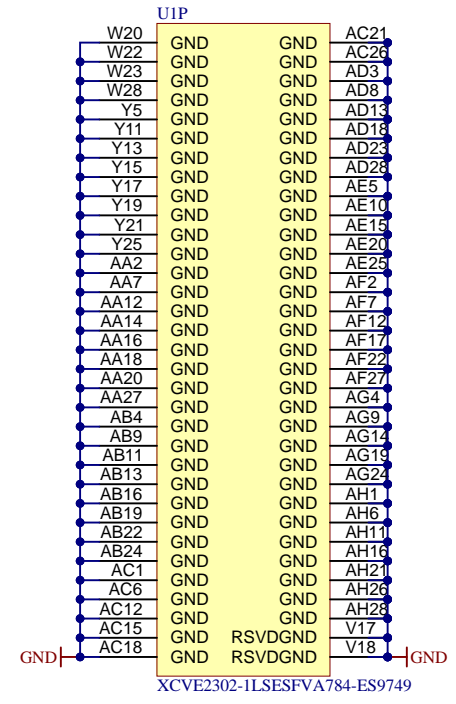
XCVE2302-1LSESFVA784-ES9749



XCVE2302-1LSESFVA784-ES9749



XCVE2302-1LSESFVA784-ES9749



XCVE2302-1LSESFVA784-ES9749



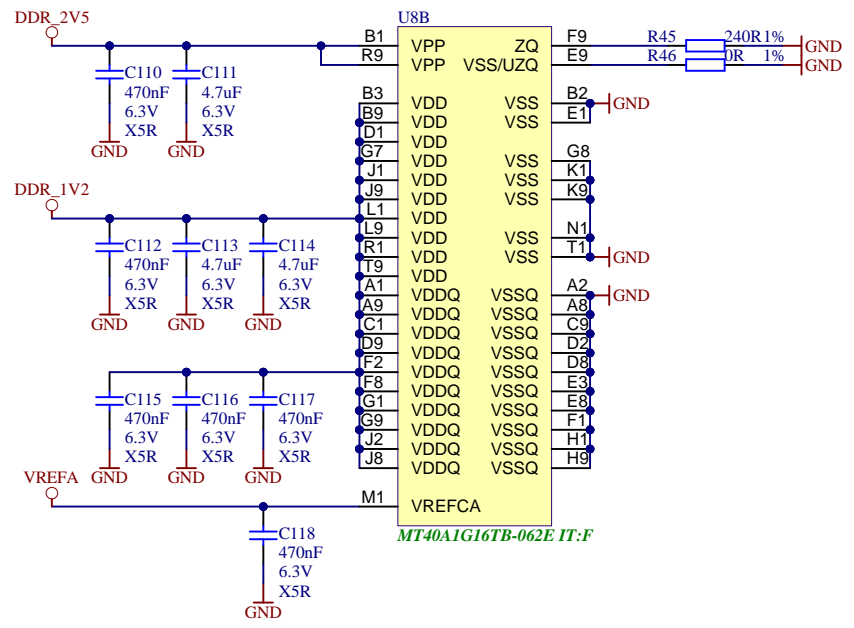
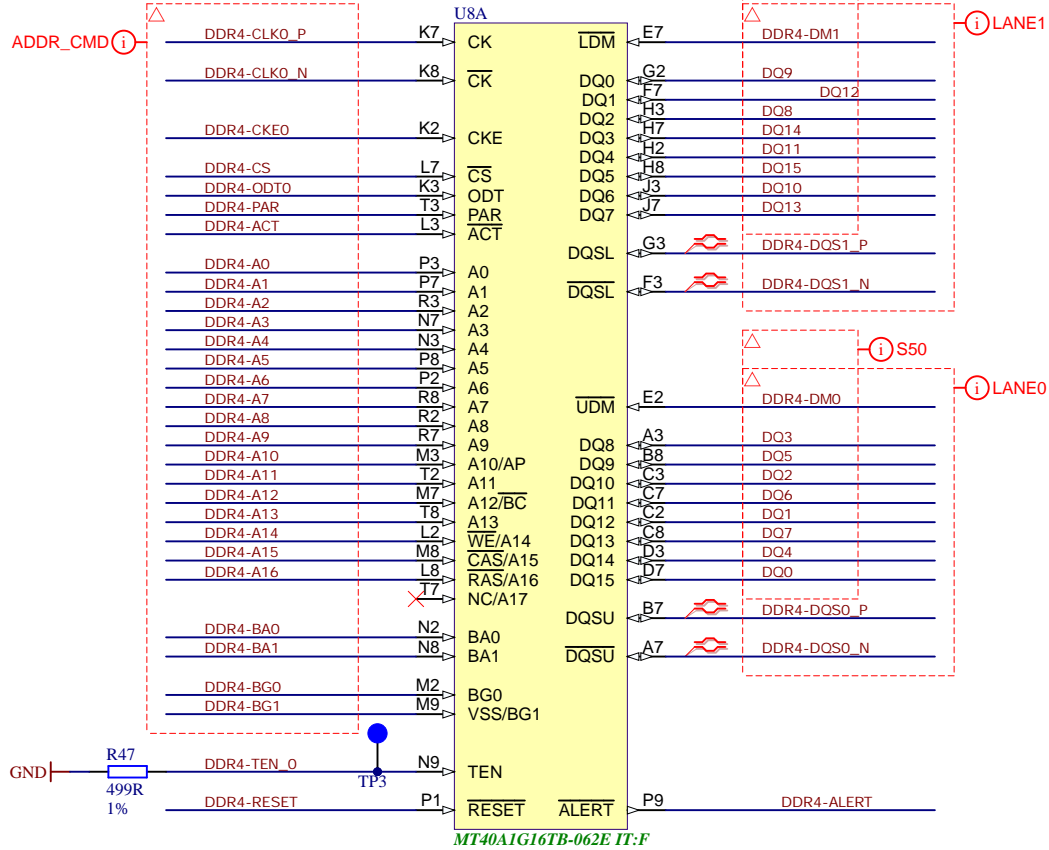
Title: V_GND		
A4	Number: TE0950 EGBE22A	Rev. 03
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Filename: V_GND.SchDoc		

1

2

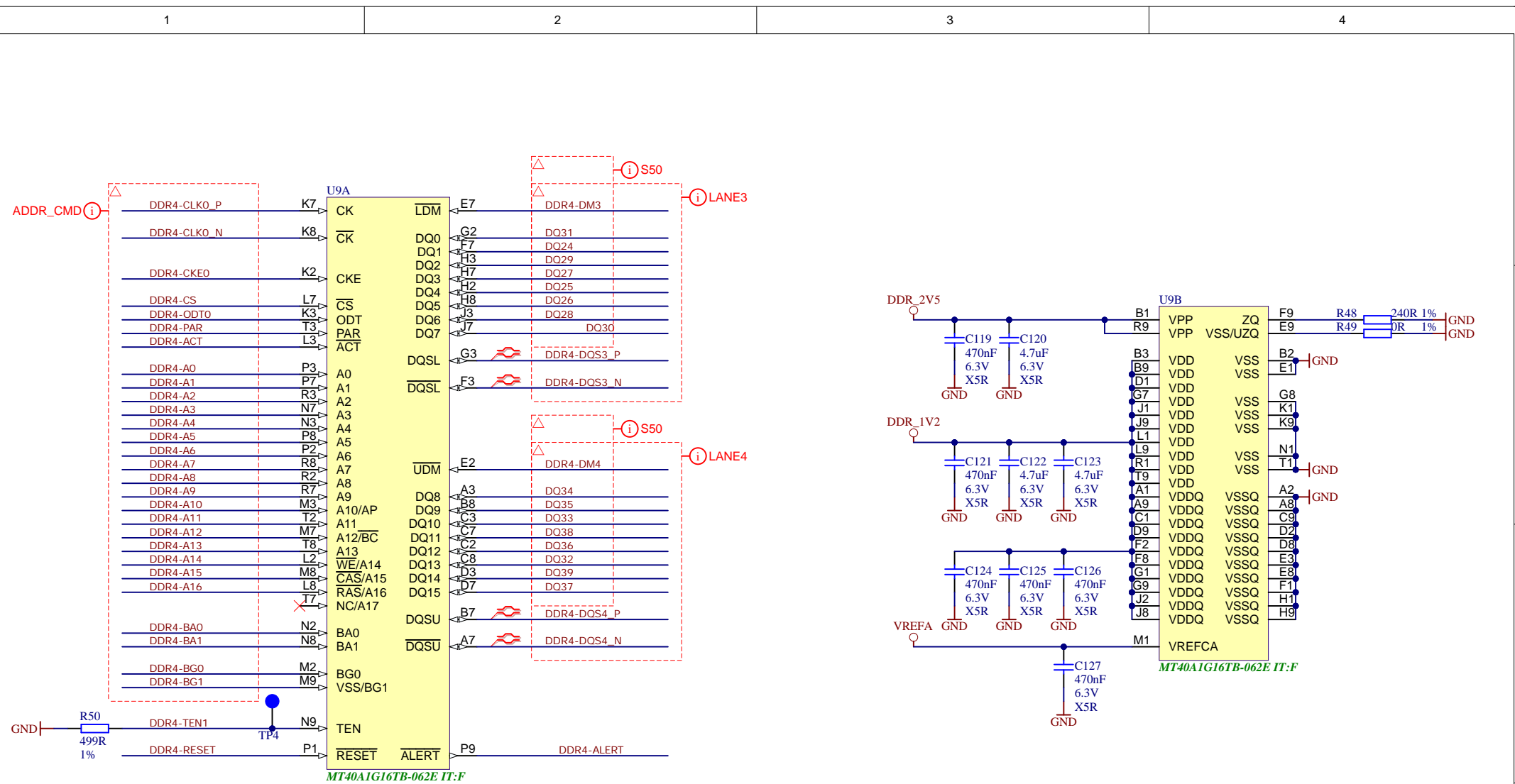
3


4



- DDR4_2.SchDoc
- DDR4_3.SchDoc
- DDR4_4.SchDoc
- DDR4_TERM.SchDoc

			Title: DDR4_1		
A4	Number: TE0950 EGBE22A		Rev.	03	
Date:	2023-12-19	Copyright: Trenz Electronic GmbH	Page 15 of 39		
Filename: DDR4_1.SchDoc					



			Title: DDR4_2	
			A4	Number: TE0950 EGBE22A
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Filename: DDR4_2.SchDoc				

1

2

3

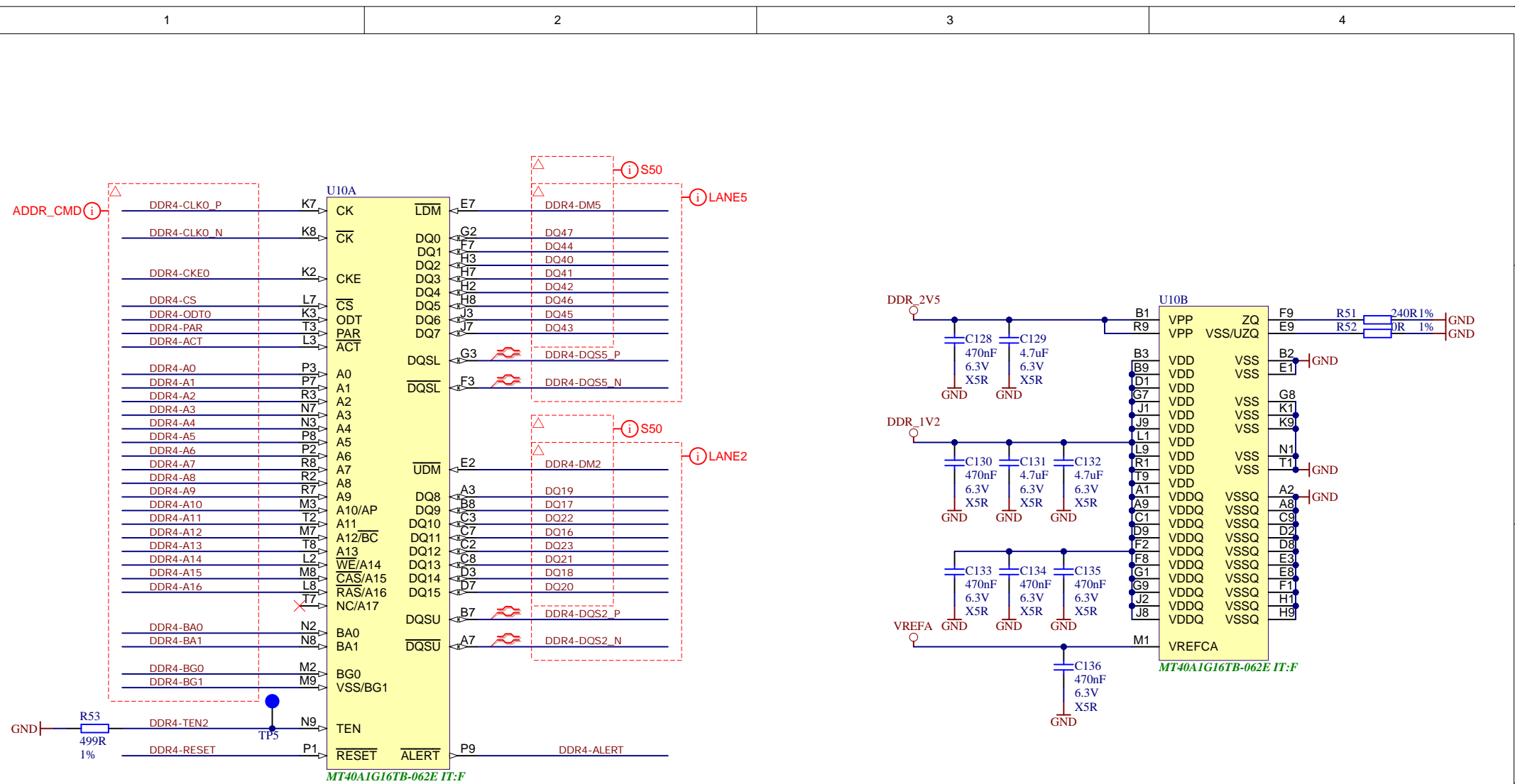
4


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4



			Title: DDR4_3	
			A4	Number: TE0950 EGBE22A
Date: 2023-12-19		Copyright: Trenz Electronic GmbH		Page 17 of 39
Filename: DDR4_3.SchDoc				

1

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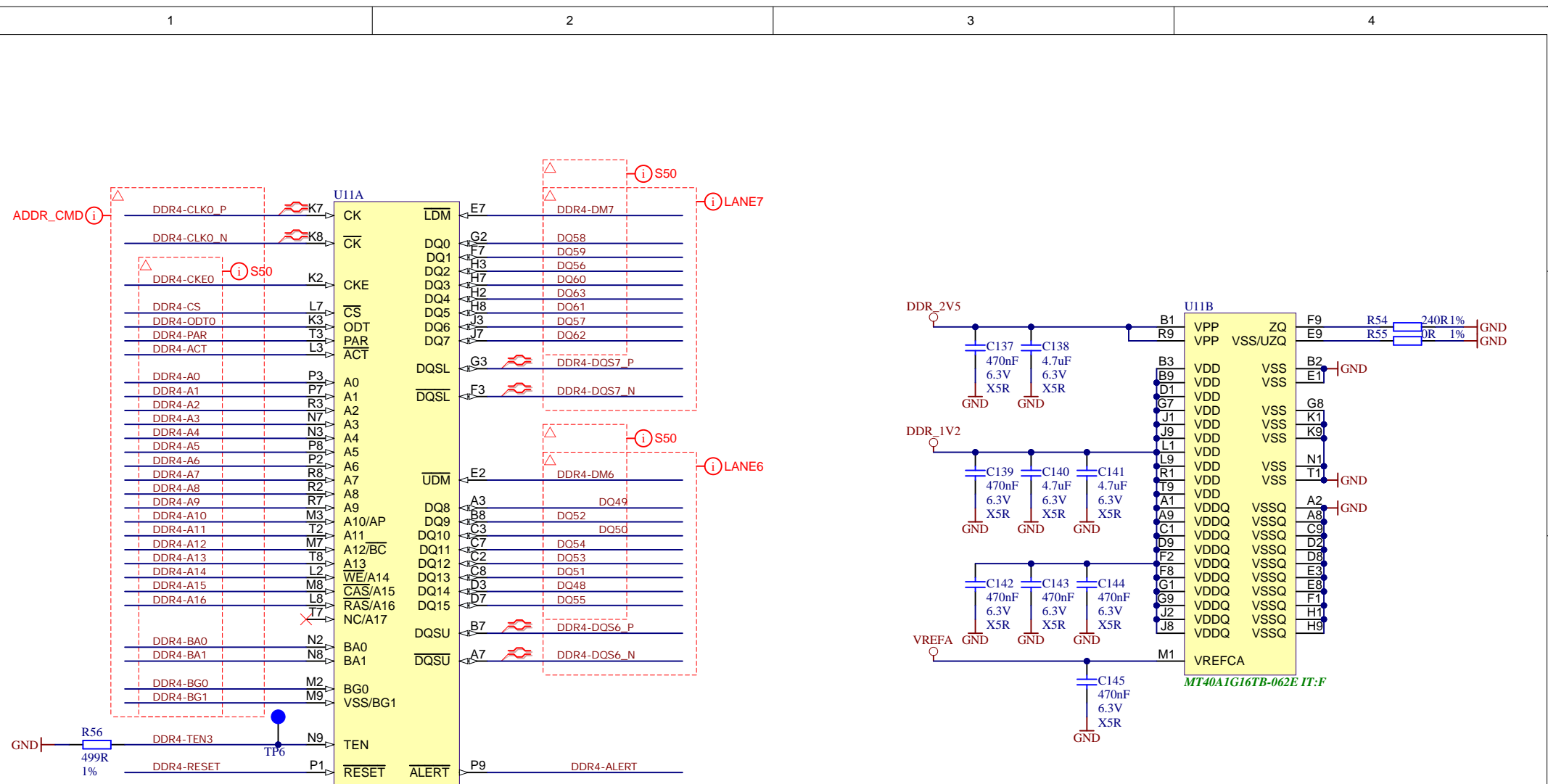
4

1

2


3

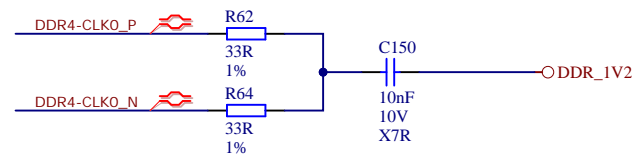
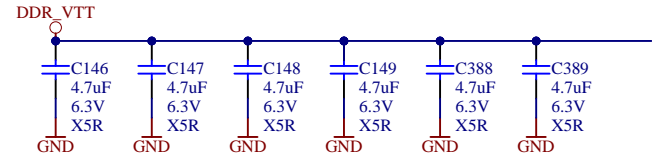
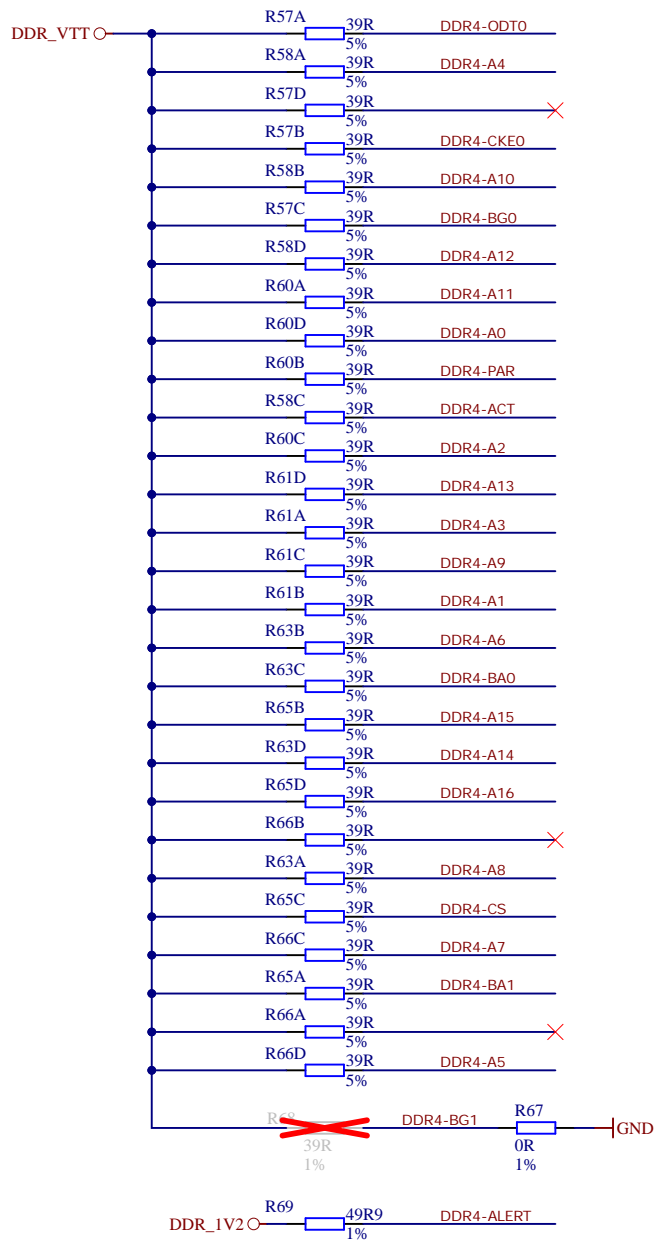
4



MT40A1G16TB-062E IT:F

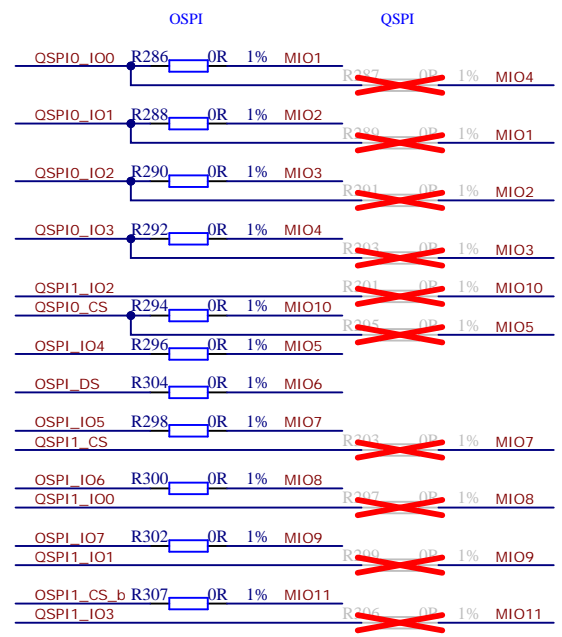
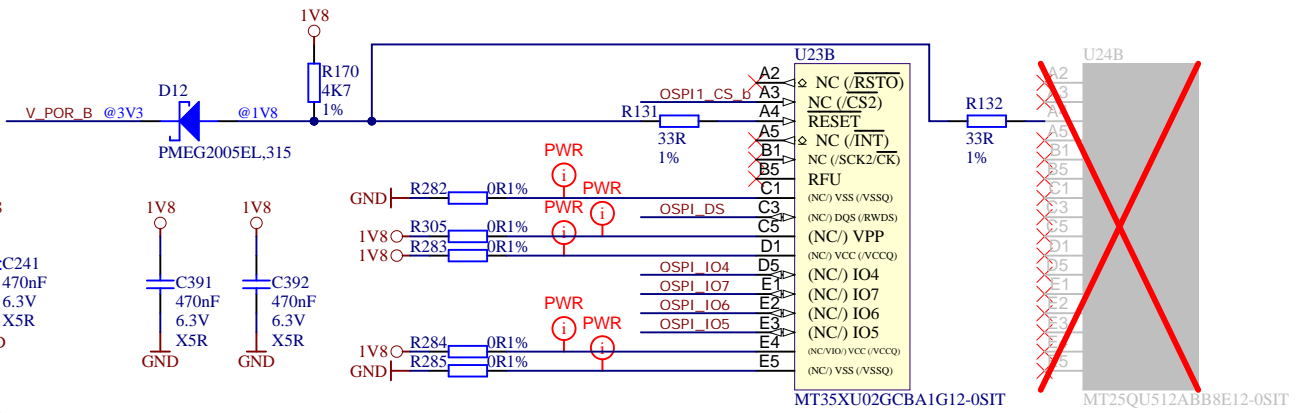
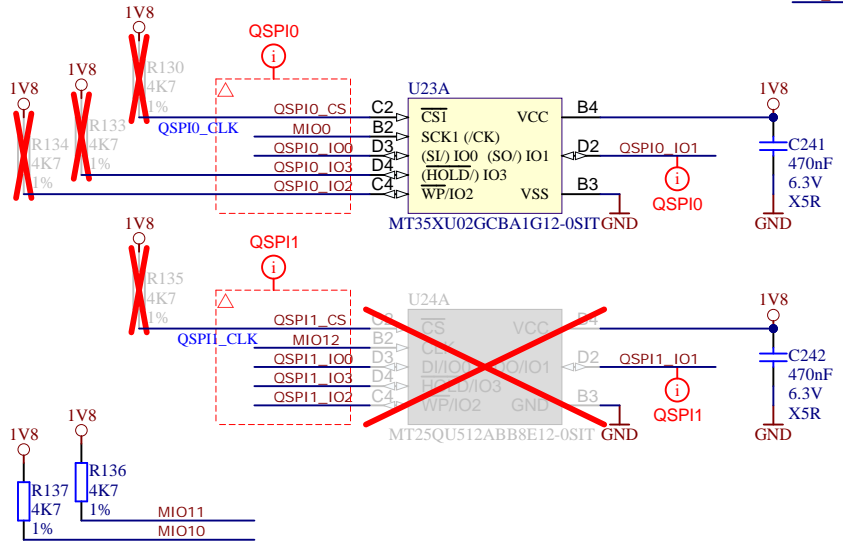
MT40A1G16TB-062E IT:F

			Title: DDR4_4	
			A4	Number: TE0950 EGBE22A
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Filename: DDR4_4.SchDoc				



Title: DDR4_TERM		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	
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Filename: DDR4_TERM.SchDoc		

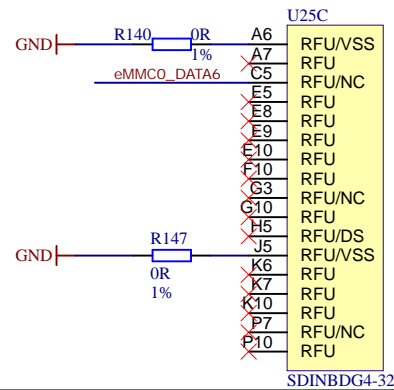
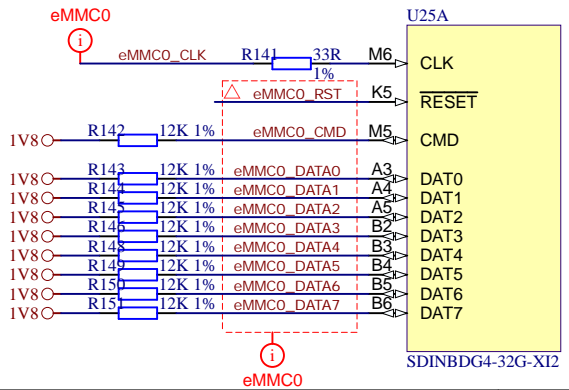
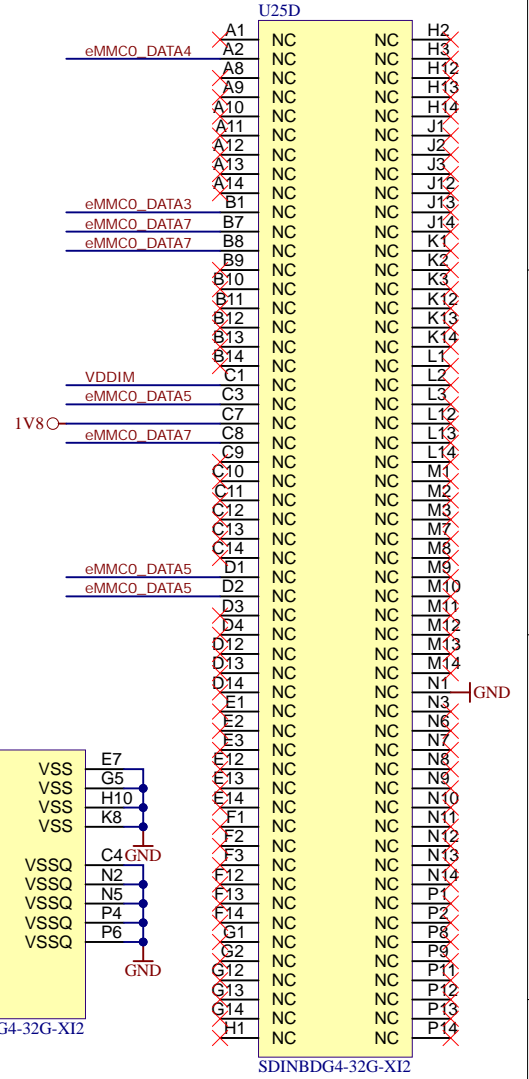
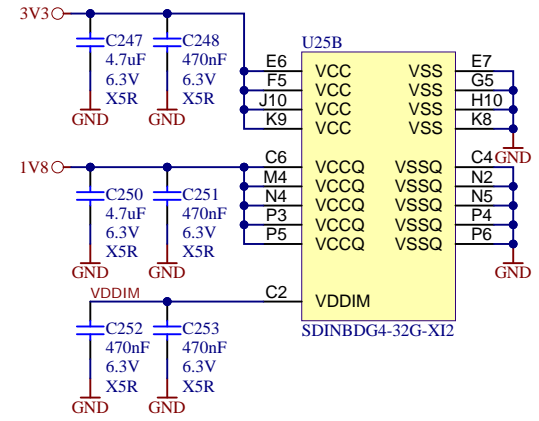
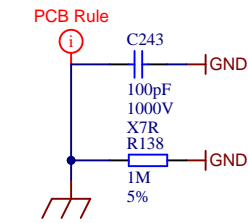
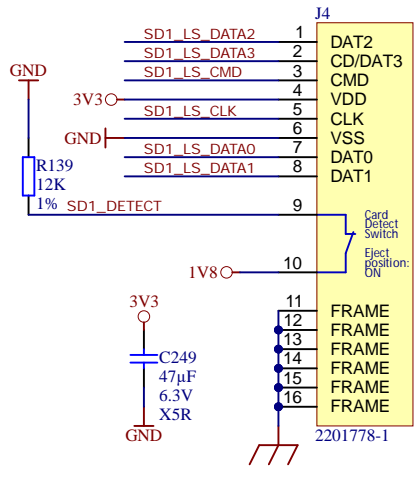
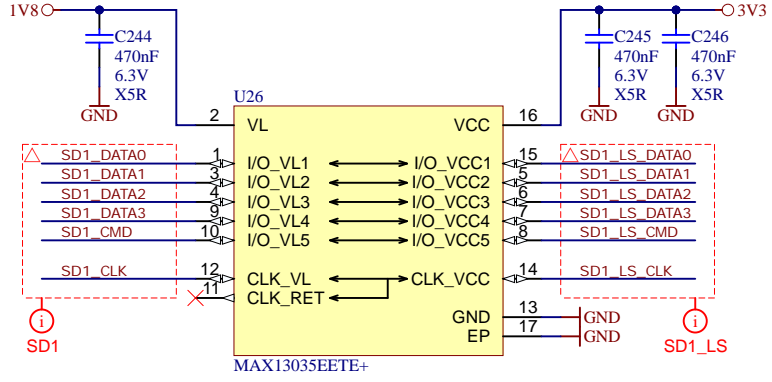
Assembly version: 2x QSPI (dual parallel U23, U24) or OSPI (U23)



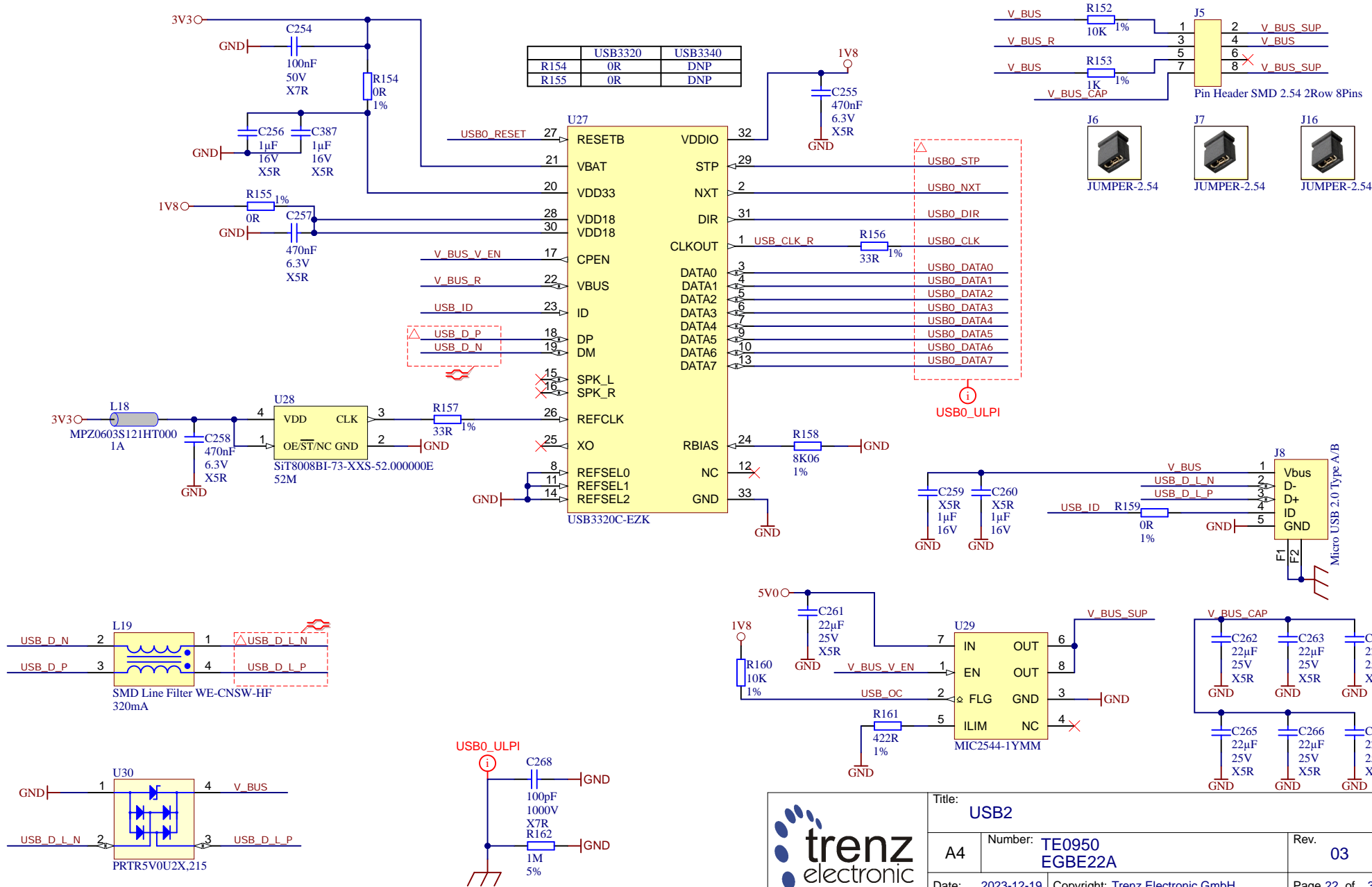
OSPI		pull-up		QSPI		pull-up	
MIO	Signal	Resistor	Value	MIO	Signal	Resistor	Value
MIO 0	OSPI: ospi_clk			MIO 0	QSPI: qspi0_clk		
MIO 1	OSPI: ospi_io[0]			MIO 1	QSPI: qspi0_io[1]		
MIO 2	OSPI: ospi_io[1]			MIO 2	QSPI: qspi0_io[2]	R134	installed
MIO 3	OSPI: ospi_io[2]			MIO 3	QSPI: qspi0_io[3]	R133	installed
MIO 4	OSPI: ospi_io[3]			MIO 4	QSPI: qspi0_io[0]		
MIO 5	OSPI: ospi_io[4]			MIO 5	QSPI: qspi0_cs_b	R130	installed
MIO 6	OSPI: ospi_ds			MIO 6	Reserved		
MIO 7	OSPI: ospi_io[5]			MIO 7	QSPI: qspi1_cs_b	R135	installed
MIO 8	OSPI: ospi_io[6]			MIO 8	QSPI: qspi1_io[0]		
MIO 9	OSPI: ospi_io[7]			MIO 9	QSPI: qspi1_io[1]		
MIO 10	OSPI: ospi0_cs_b	R137	installed	MIO 10	QSPI: qspi1_io[2]	R137	installed
MIO 11	OSPI: ospi1_cs_b	R136	installed	MIO 11	QSPI: qspi1_io[3]	R136	installed
MIO 12				MIO 12	QSPI: qspi1_clk		



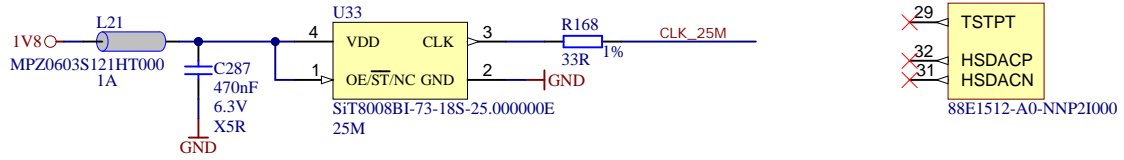
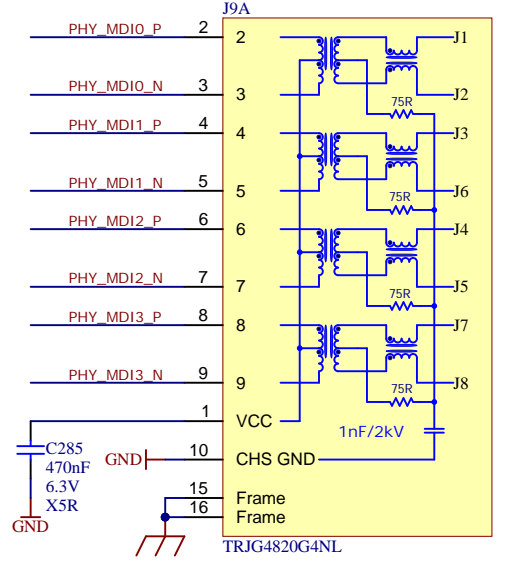
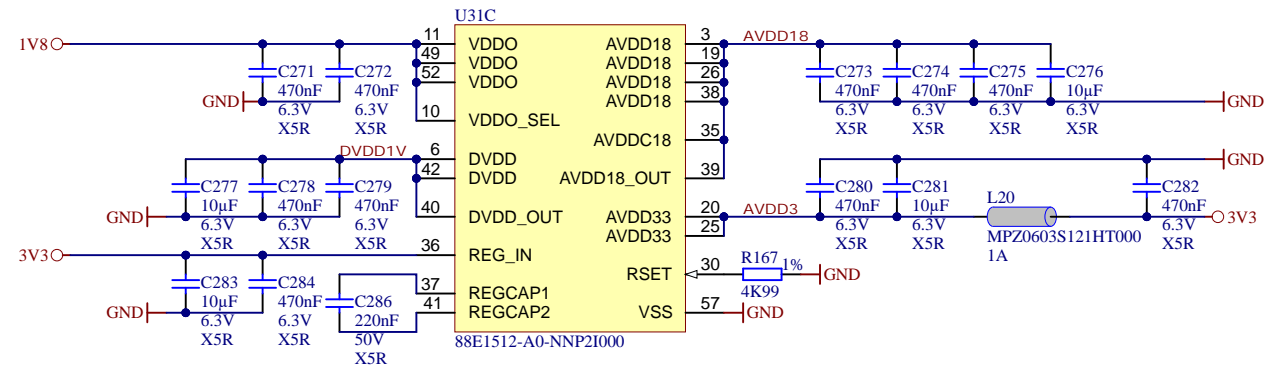
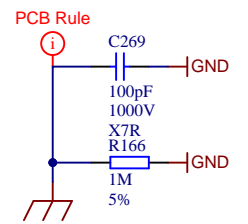
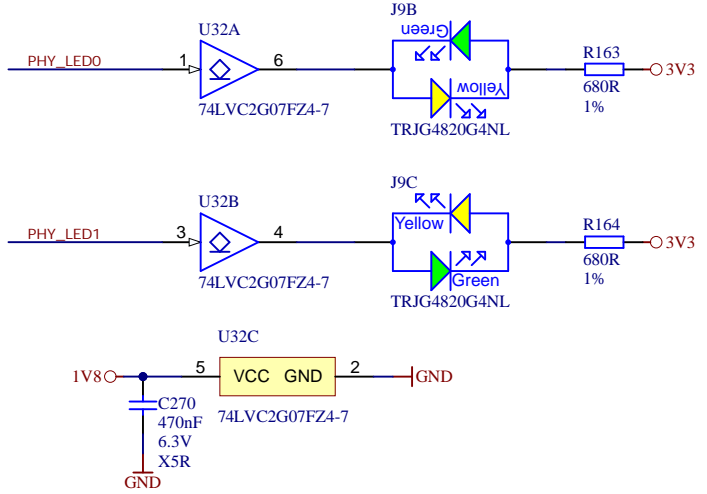
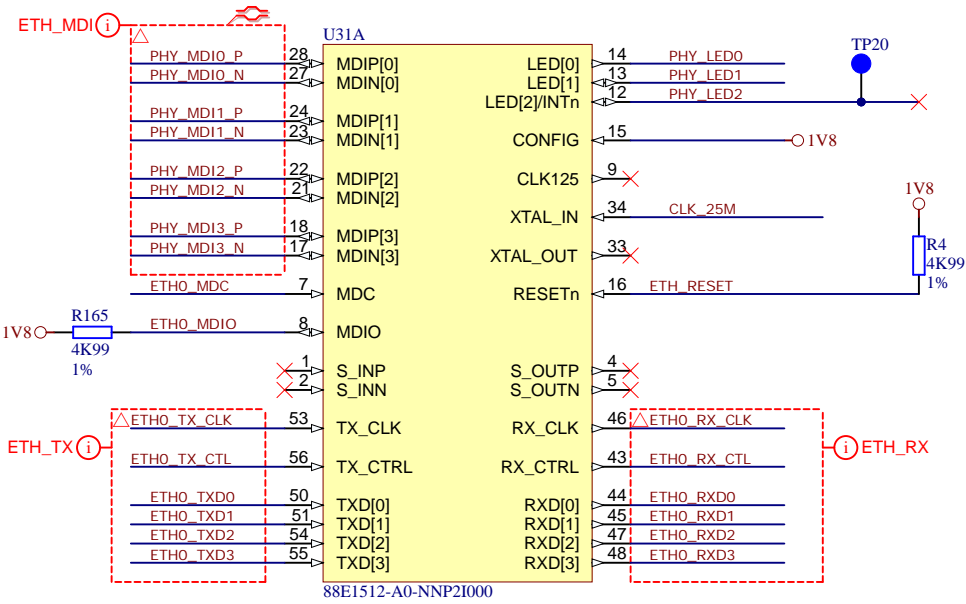
Title: QSPI_OSPI		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 20 of 39
Filename: QSPI_OSPI.SchDoc		



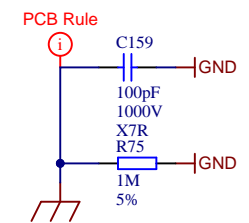
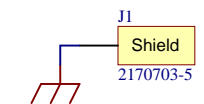
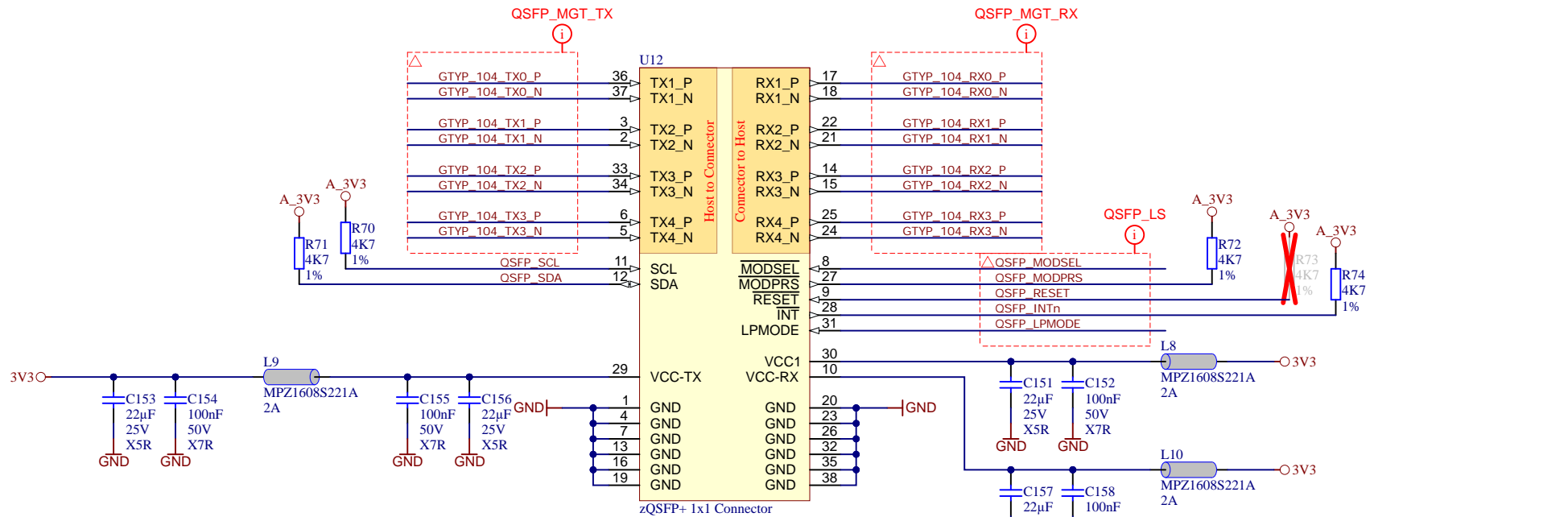
Title: SD_eMMC		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 21 of 39
Filename: SD_eMMC.SchDoc		



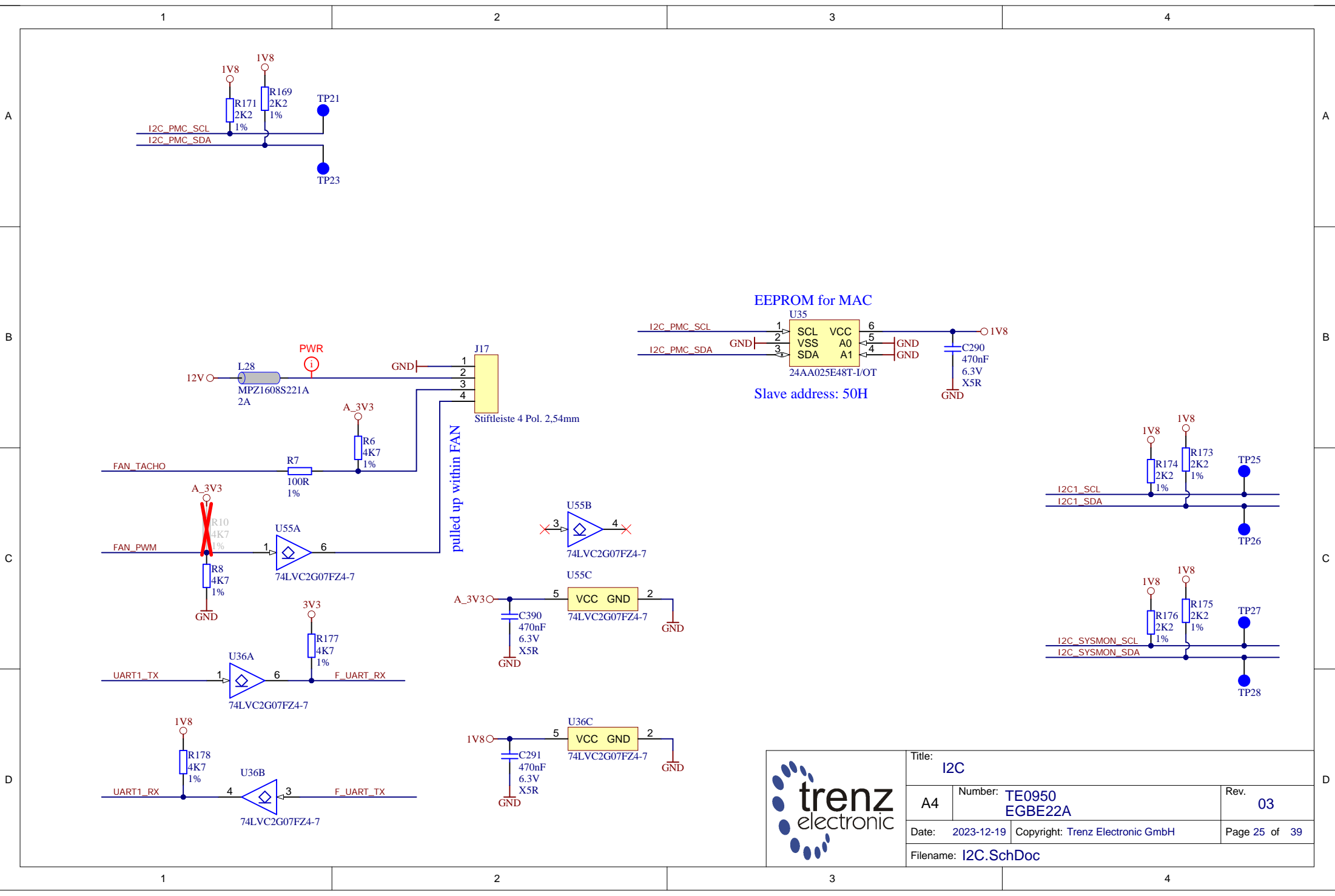
Title: USB2		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 22 of 39
Filename: USB2.SchDoc		



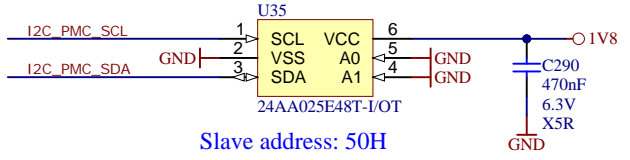
Title: GB_ETH		
A4	Number: TE0950 EGBE22A	Rev. 03
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Filename: GB_ETH.SchDoc		



	Title: QSFP		
	A4	Number: TE0950 EGBE22A	Rev. 03
	Date: 2023-12-19	Copyright: Trenz Electronic GmbH	
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Filename: QSFP.SchDoc			



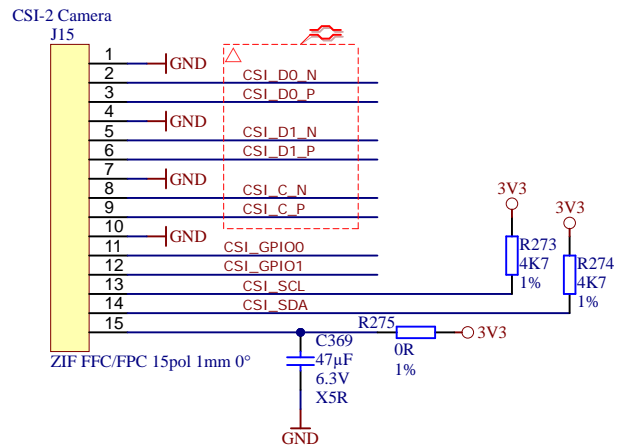
EEPROM for MAC




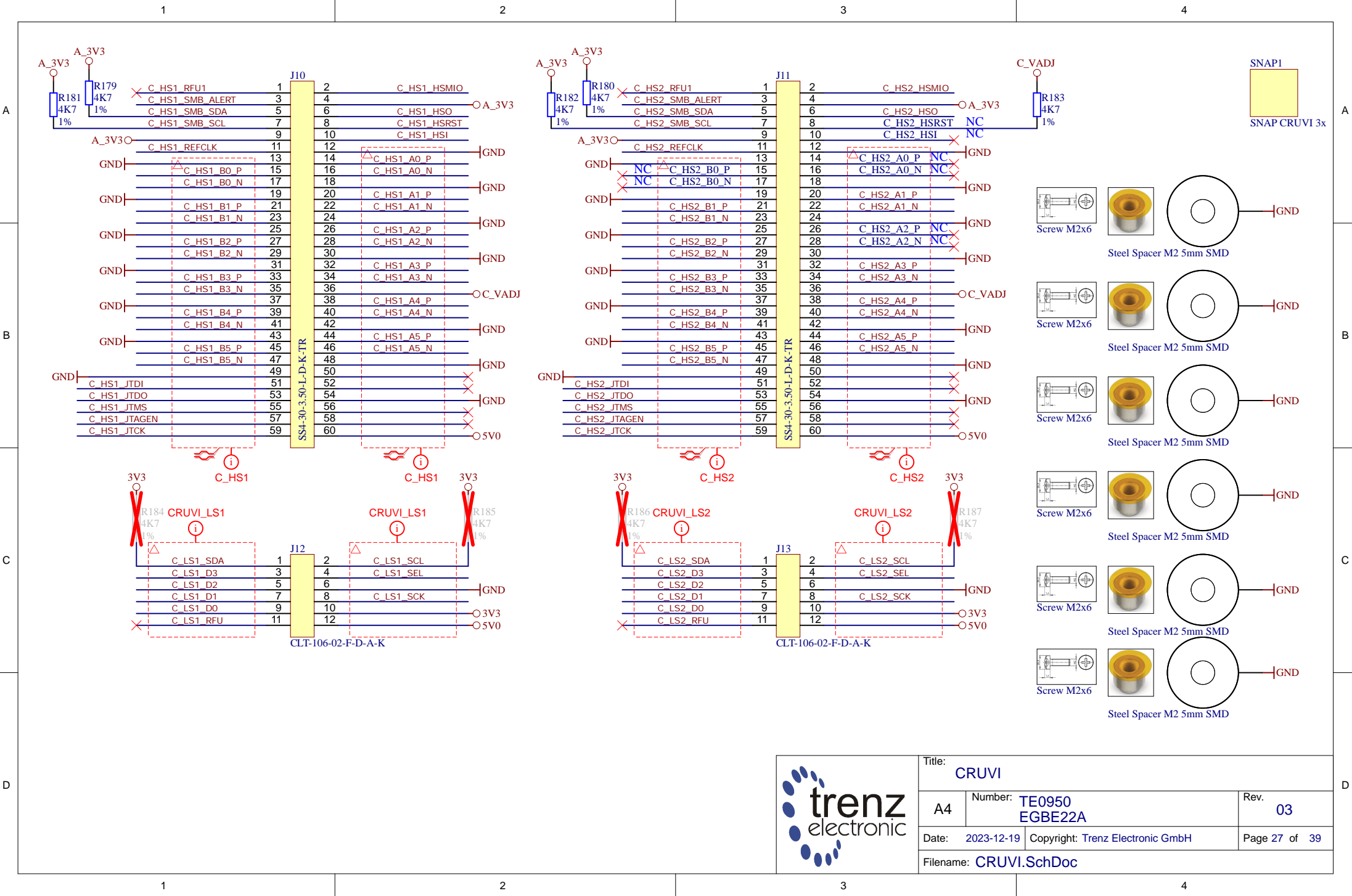
pulled up within FAN



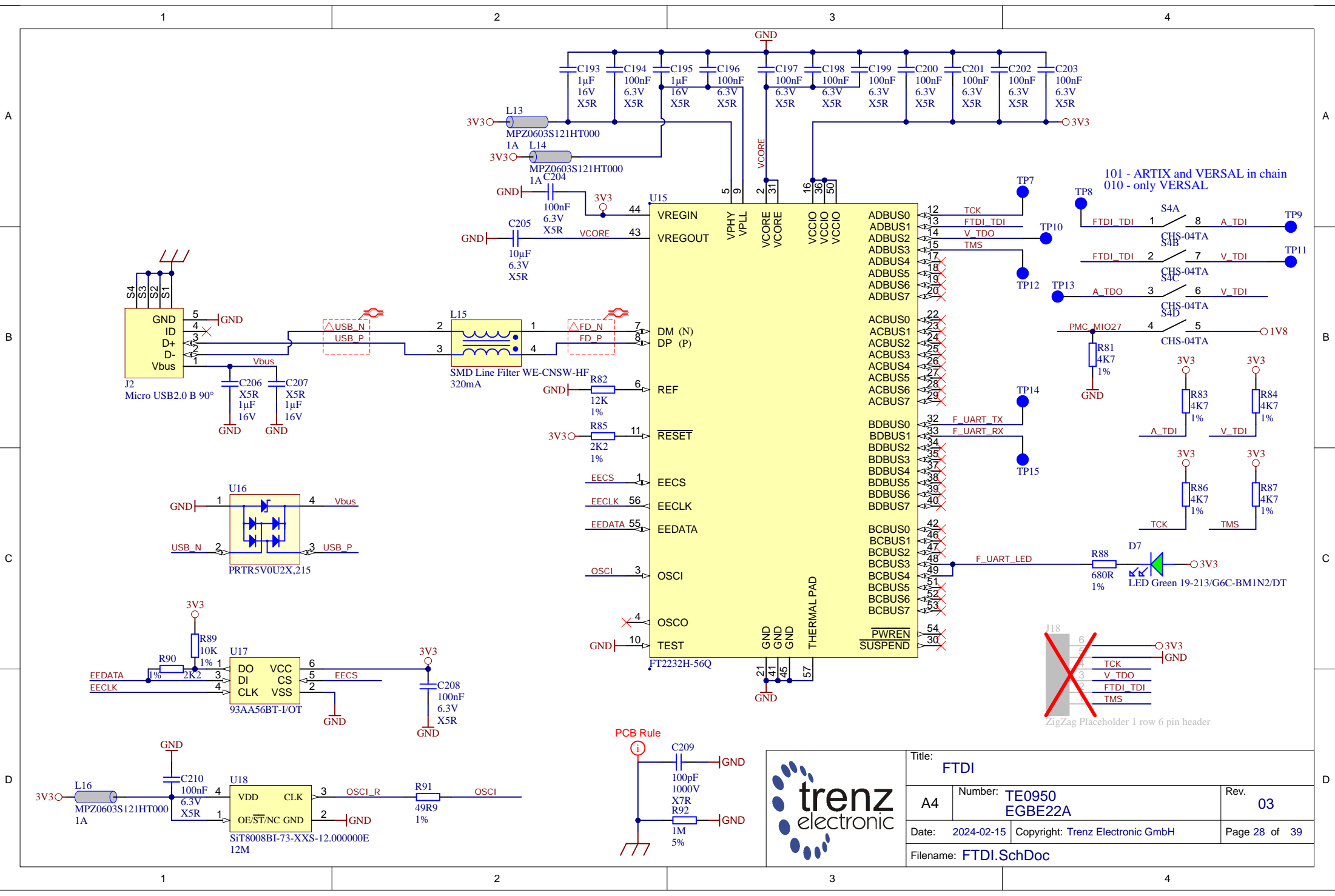
Title: I2C		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	
Filename: I2C.SchDoc		Page 25 of 39



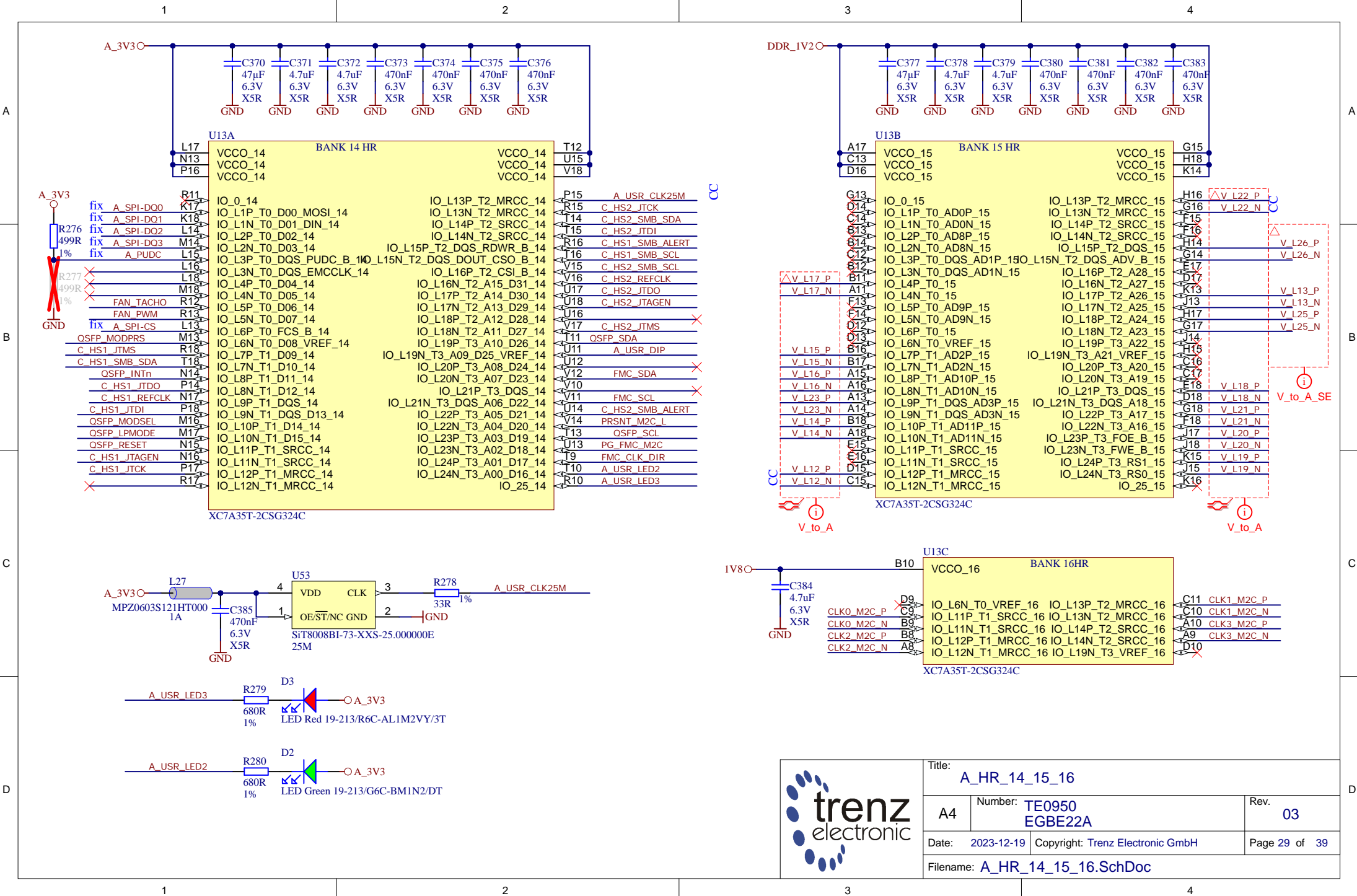
	Title: CSI2_CAM		
	A4	Number: TE0950 EGBE22A	Rev. 03
	Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 26 of 39
	Filename: CSI2_CAM.SchDoc		



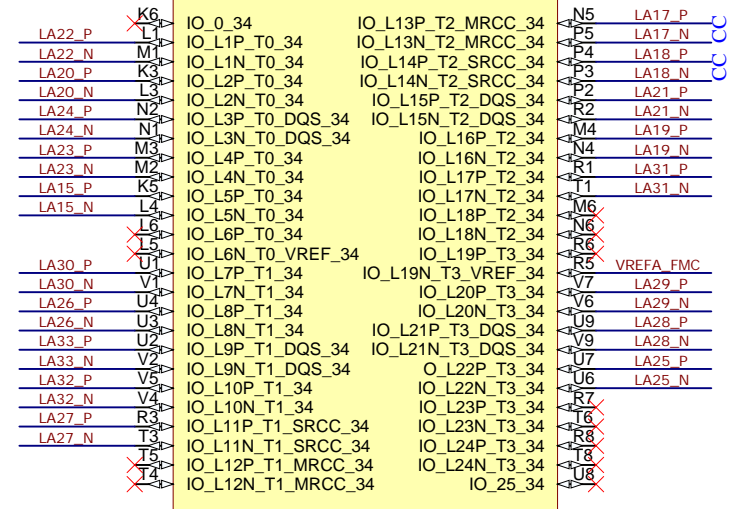
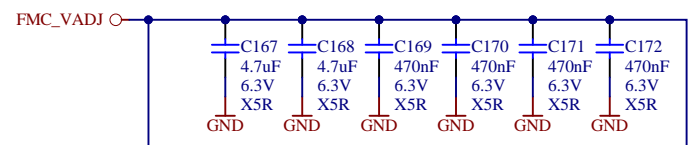
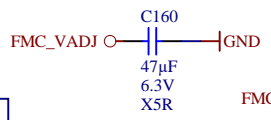
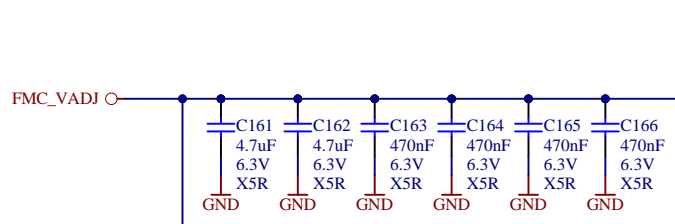
Title: CRUVI		
A4	Number: TE0950 EGBE22A	Rev. 03
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Filename: CRUVI.SchDoc		



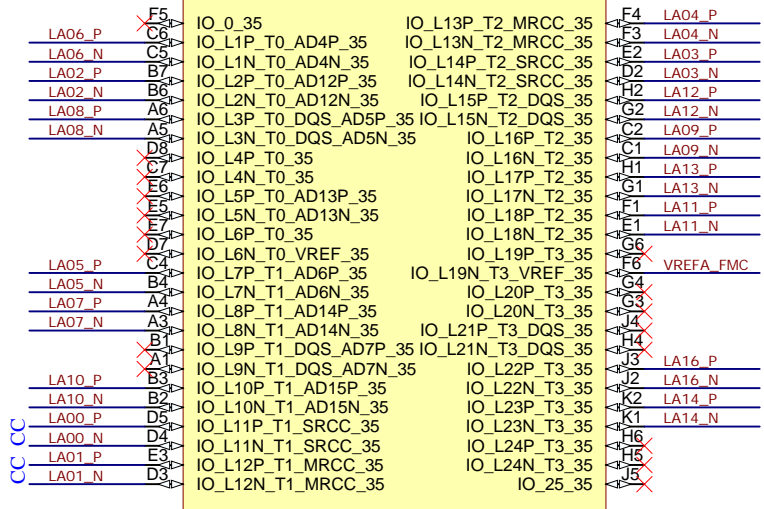
Title: FTDI		
A4	Number: TE0950 EGBE22A	Rev. 03
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Filename: FTDI.SchDoc		



Title: A_HR_14_15_16		
A4	Number: TE0950 EGBE22A	Rev. 03
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Filename: A_HR_14_15_16.SchDoc		



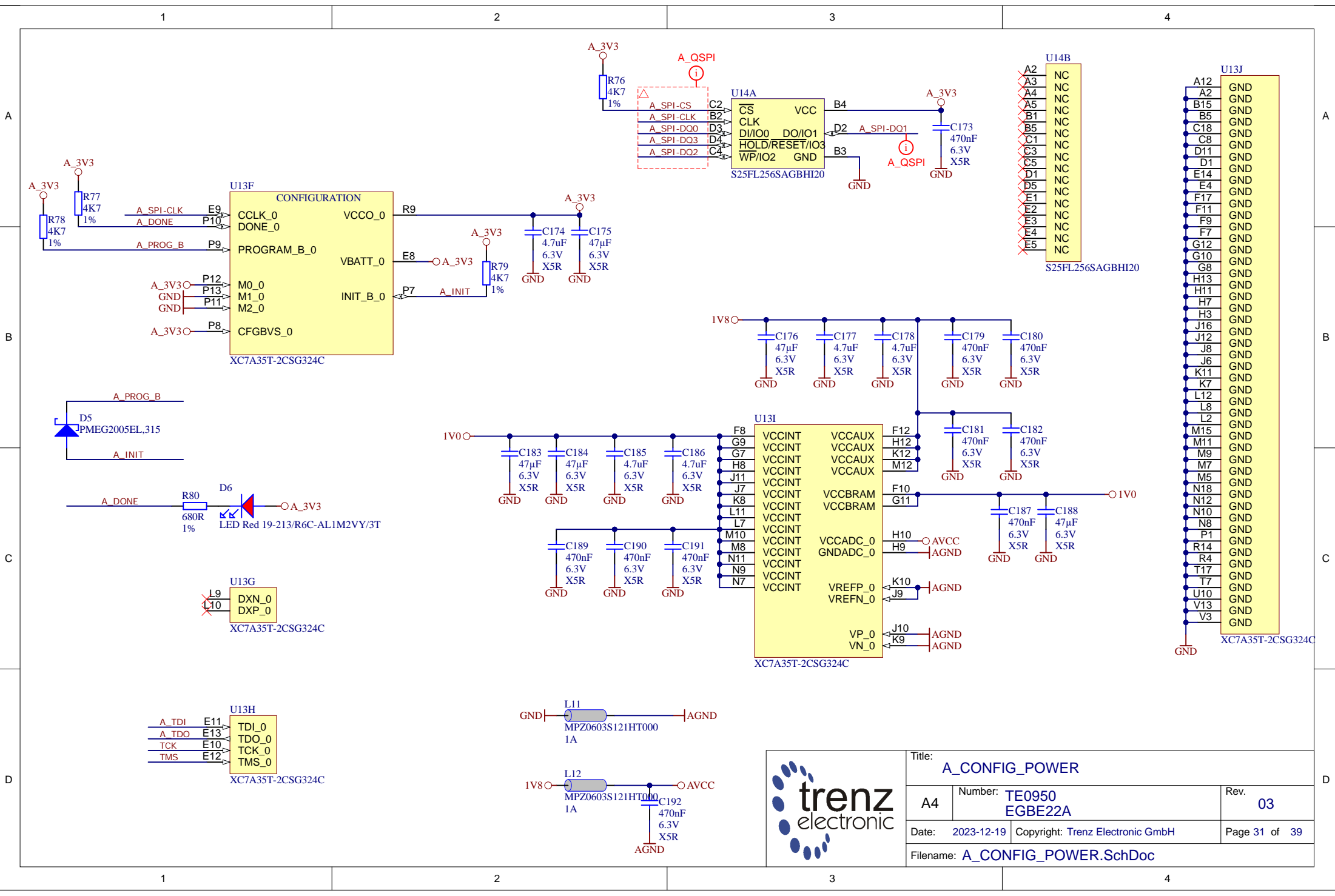
XC7A35T-2CSG324C




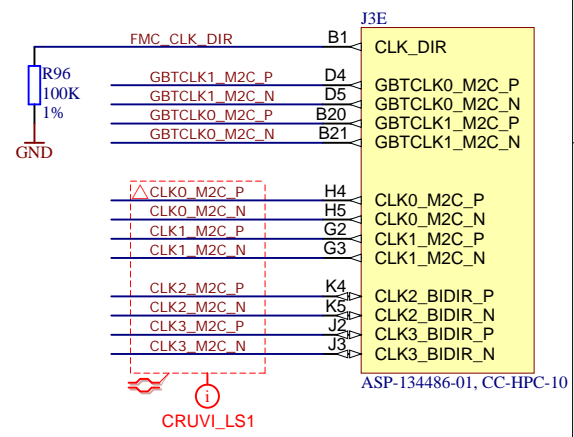
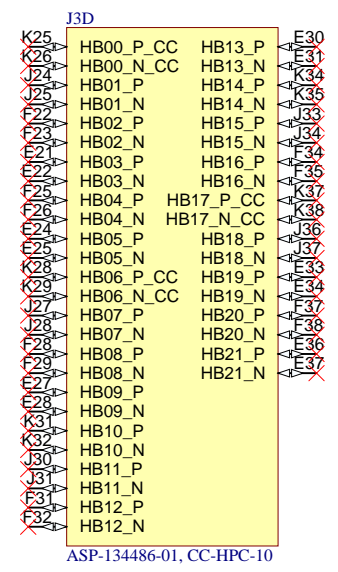
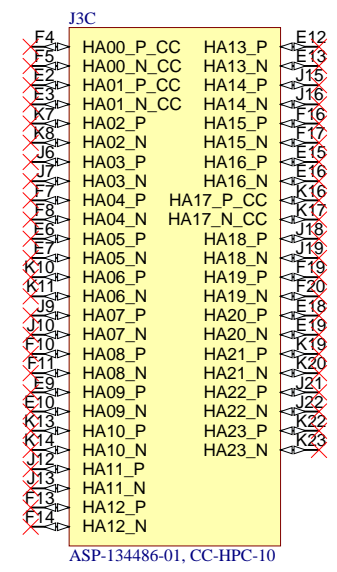
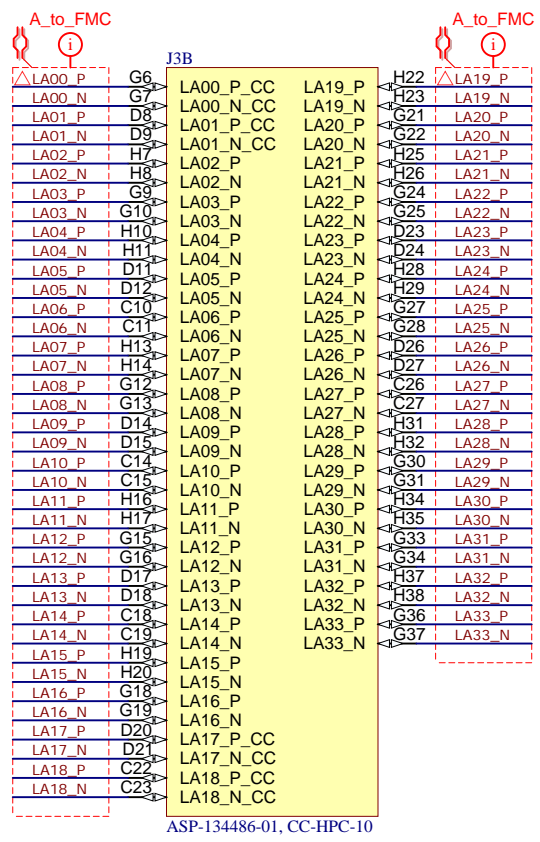
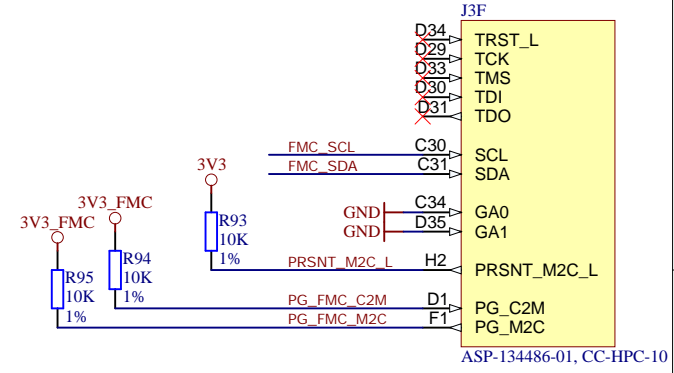
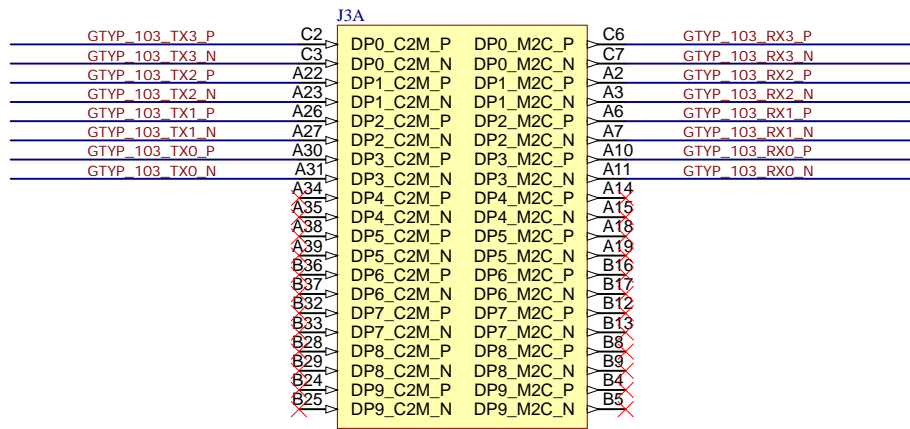
XC7A35T-2CSG324C



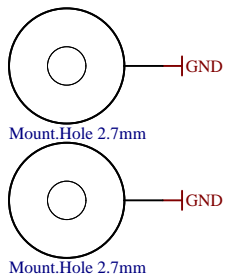
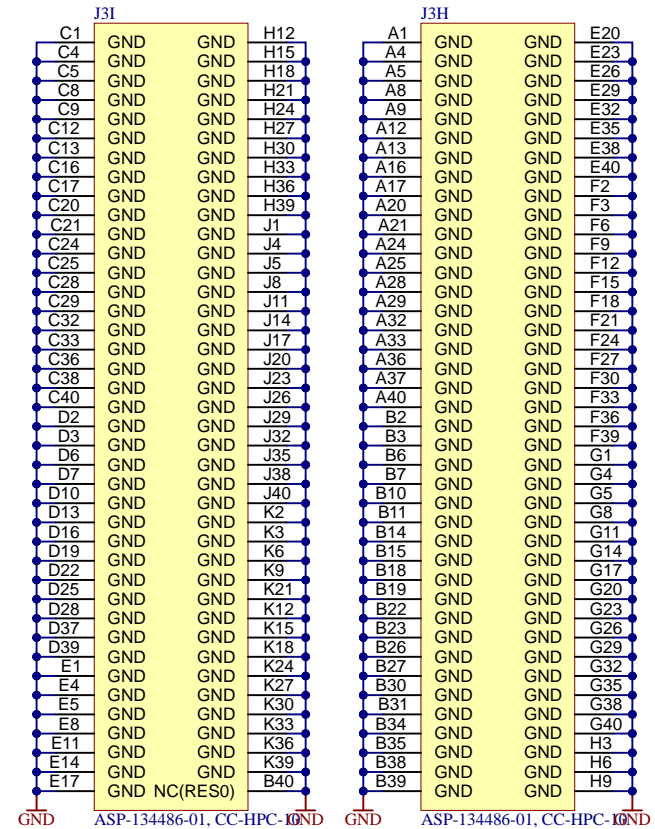
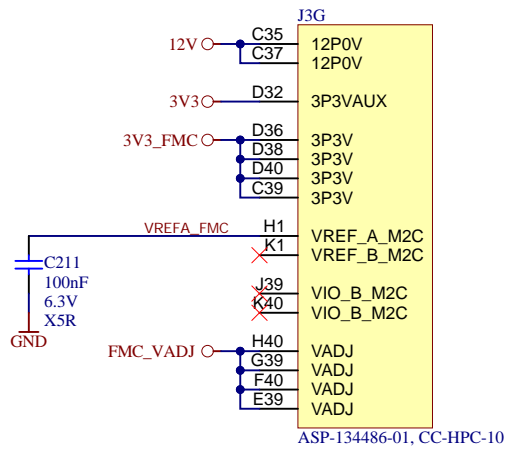
Title: A_HR_34_35		
A4	Number: TE0950 EGBE22A	Rev. 03
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Filename: A_HR_34_35.SchDoc		



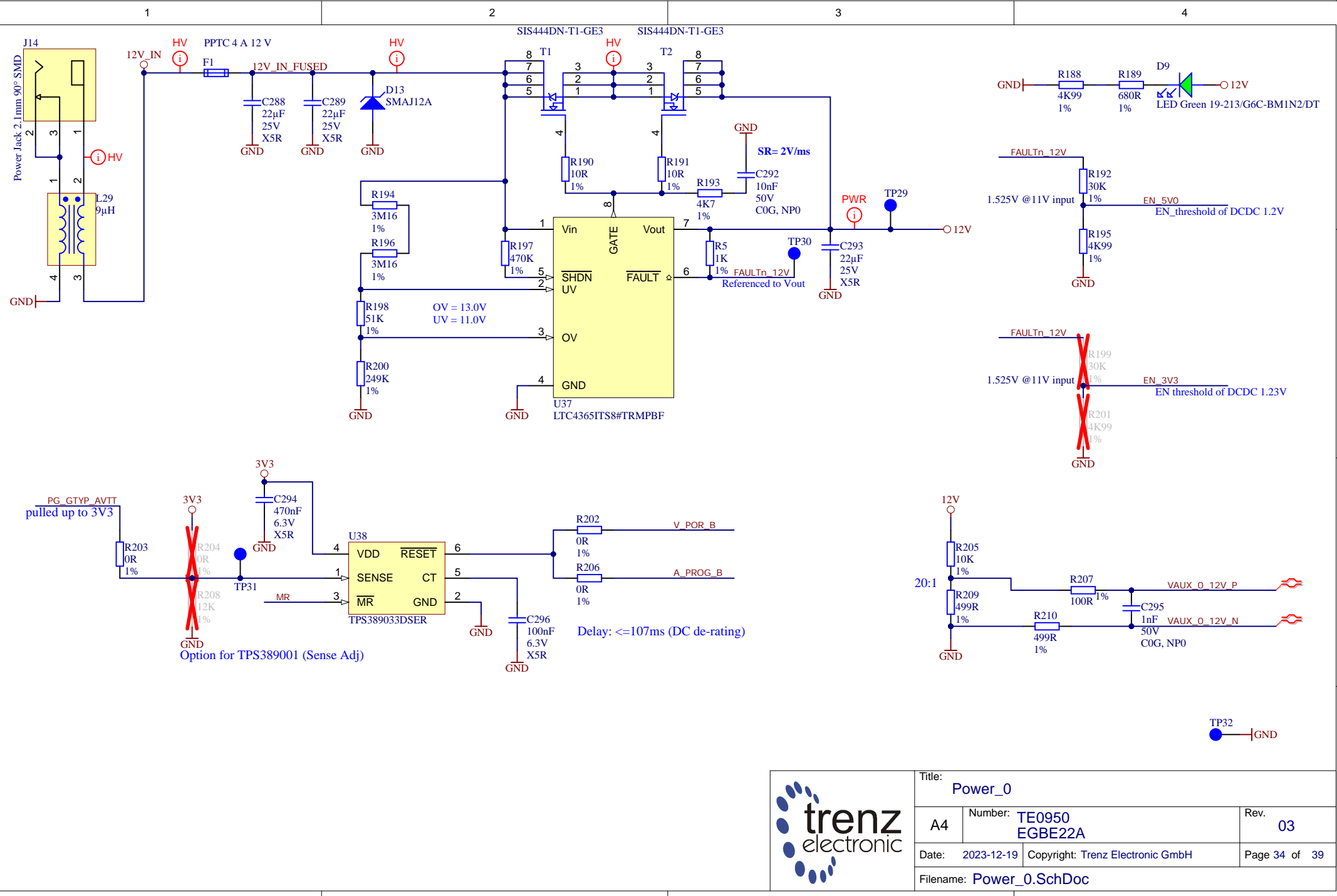
			Title: A_CONFIG_POWER	
			A4	Number: TE0950 EGBE22A
Date: 2023-12-19		Copyright: Trenz Electronic GmbH		Page 31 of 39
Filename: A_CONFIG_POWER.SchDoc				



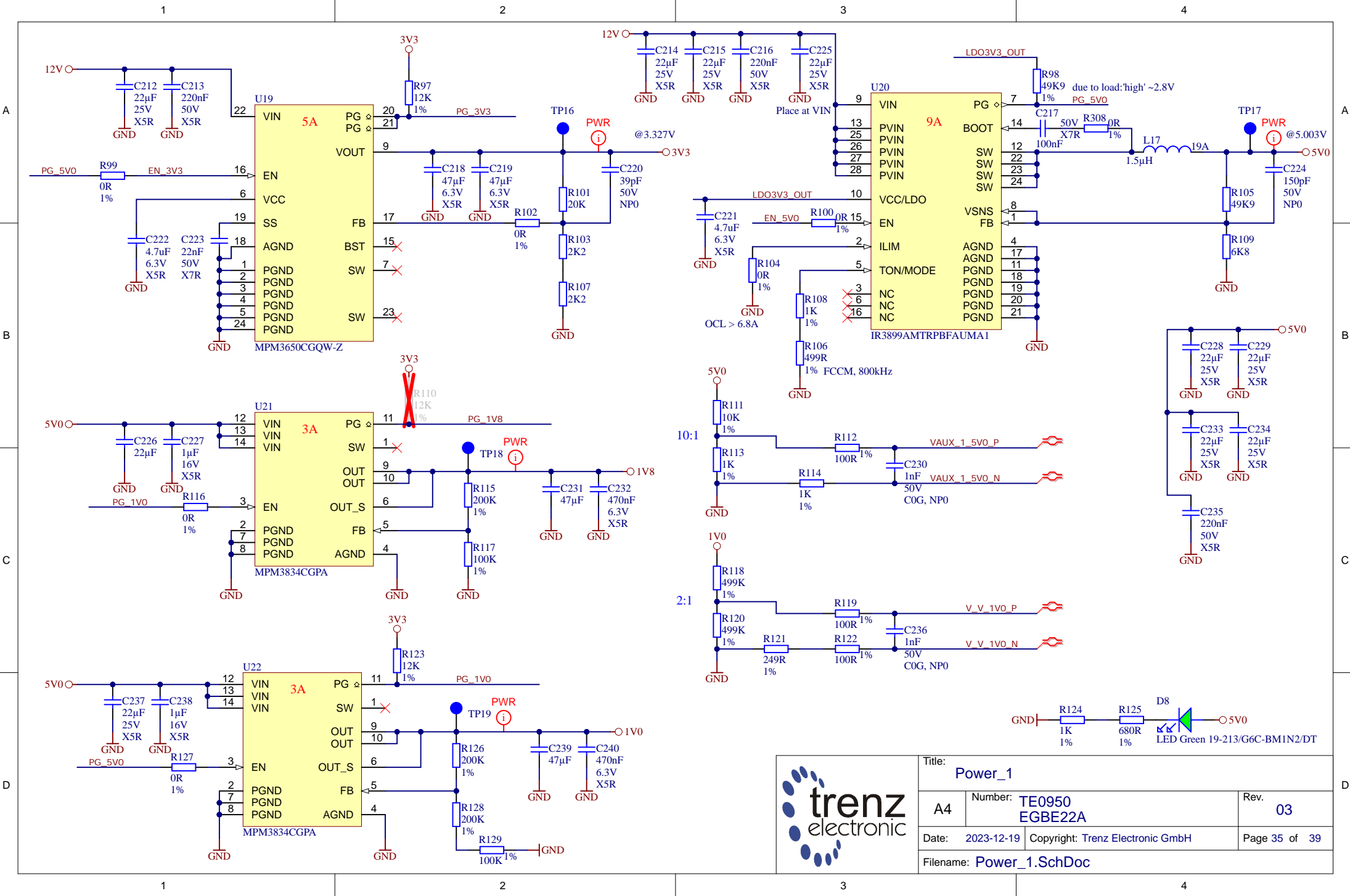
Title: FMC		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 32 of 39
Filename: FMC.SchDoc		



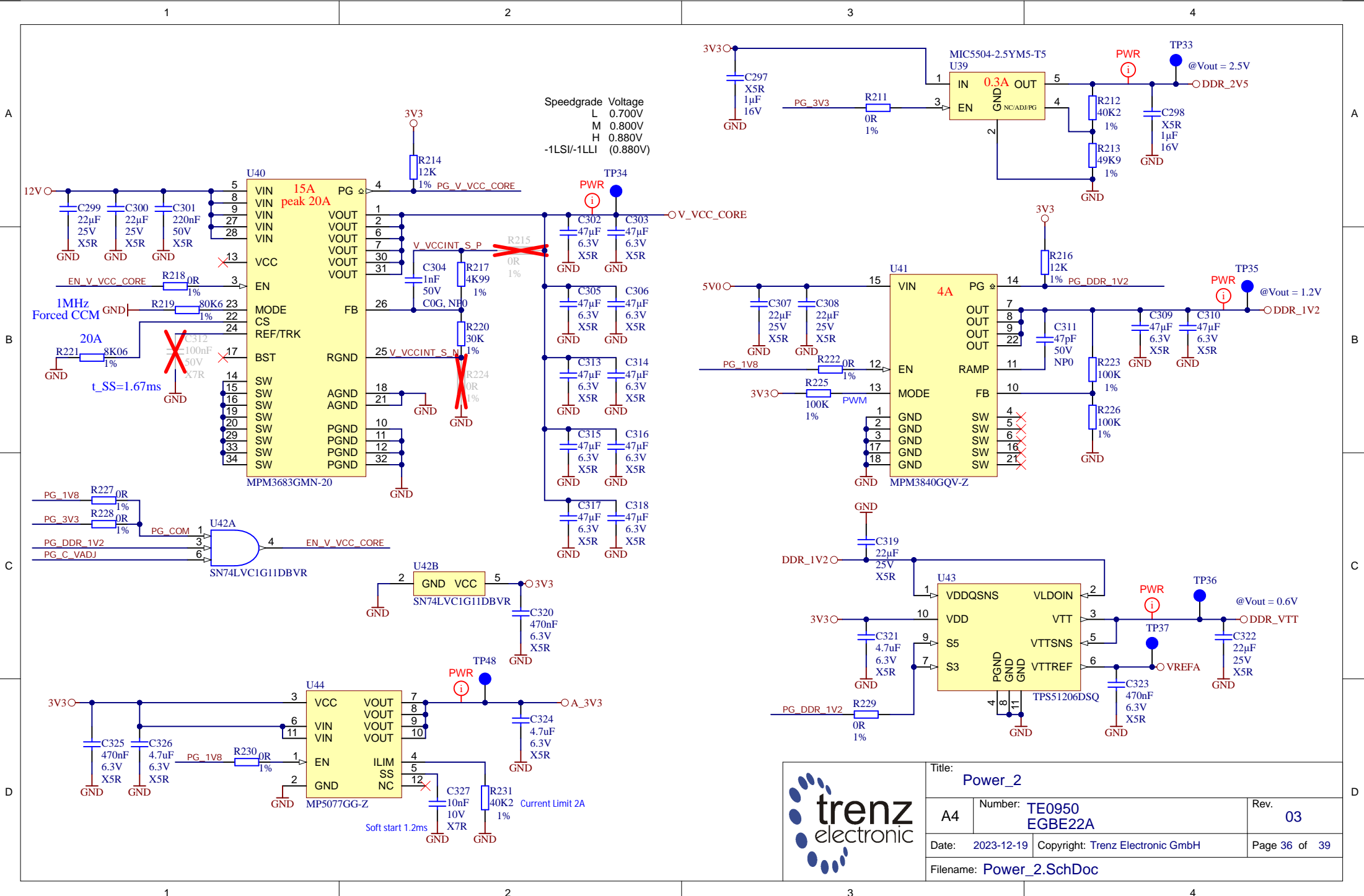
Title: FMC_Power		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 33 of 39
Filename: FMC_Power.SchDoc		



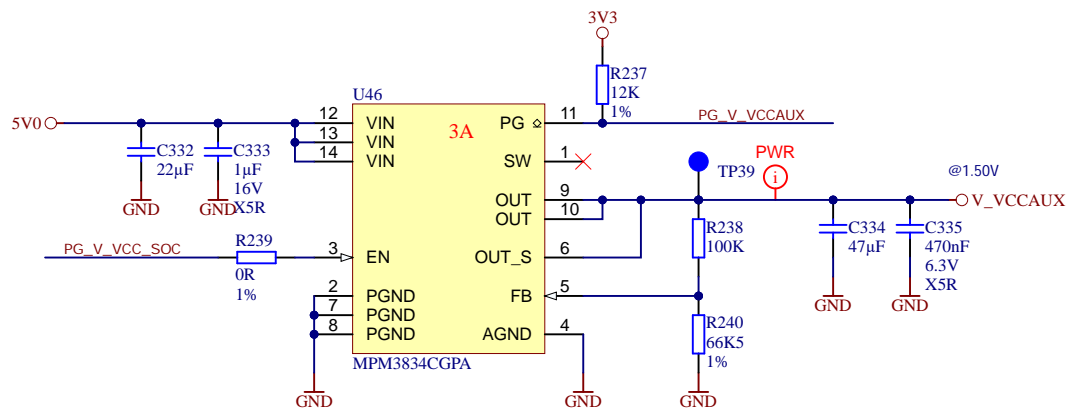
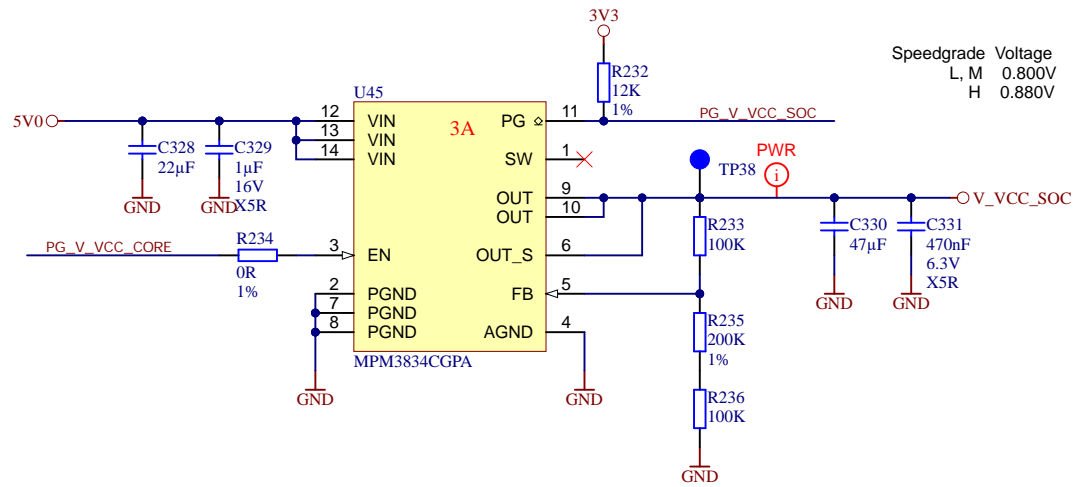
Title: Power_0		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 34 of 39
Filename: Power_0.SchDoc		



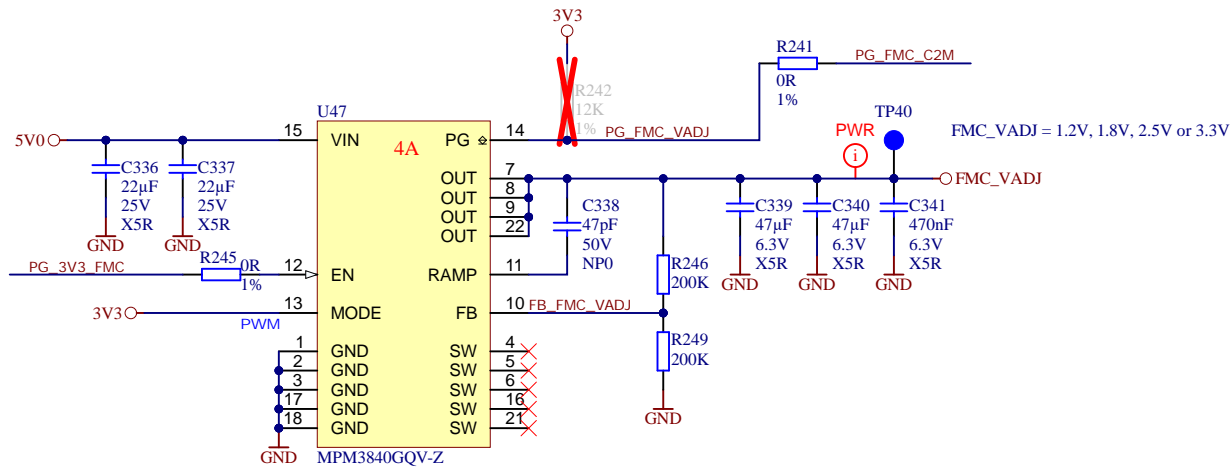
Title: Power_1		
A4	Number: TE0950 EGBE22A	Rev. 03
Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 35 of 39
Filename: Power_1.SchDoc		



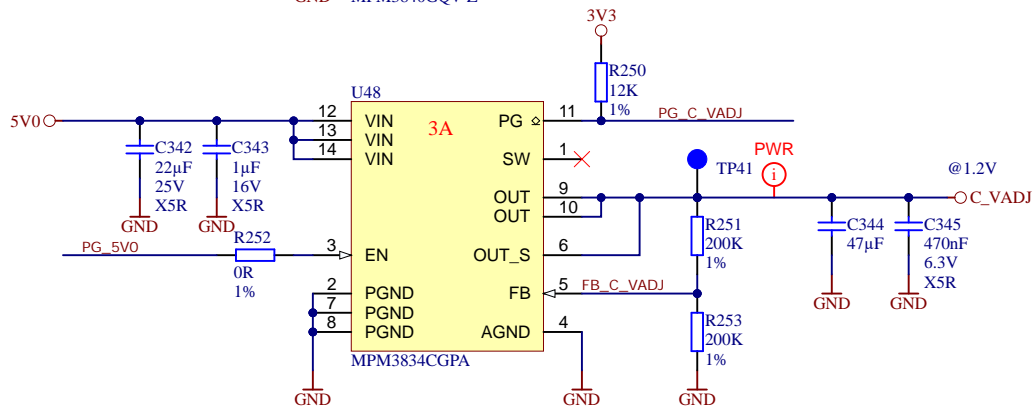
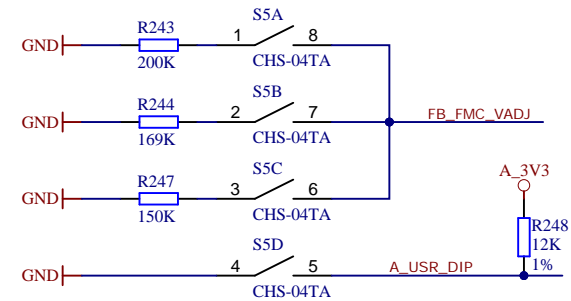
		Title: Power_2	
		A4	Number: TE0950 EGBE22A
Date: 2023-12-19		Copyright: Trenz Electronic GmbH	
Filename: Power_2.SchDoc		Page 36 of 39	
		Rev: 03	



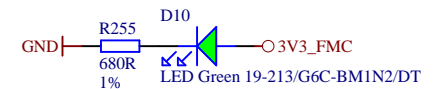
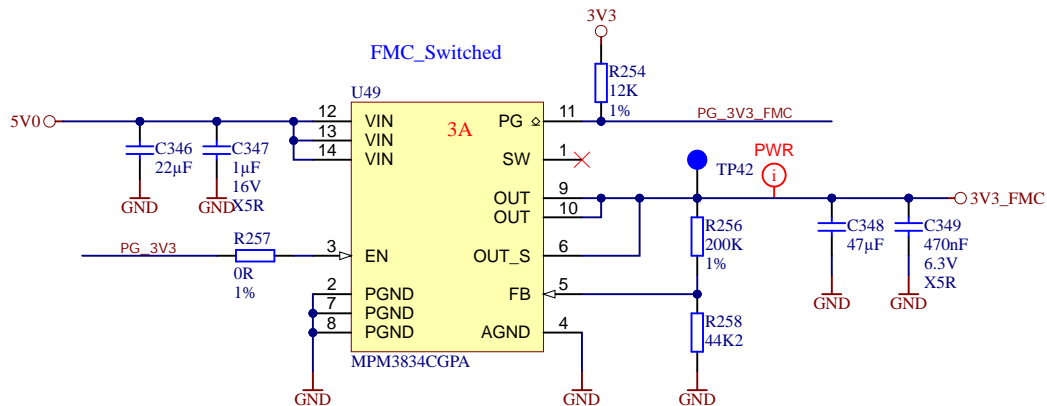
Title: Power_3		
A4	Number: TE0950 EGBE22A	Rev. 03
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Filename: Power_3.SchDoc		Page 37 of 39



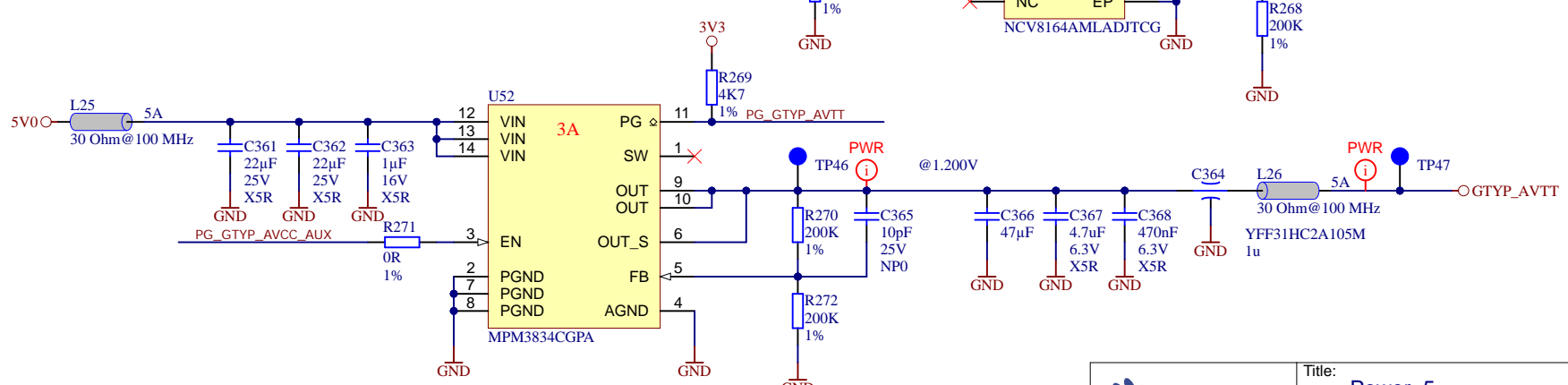
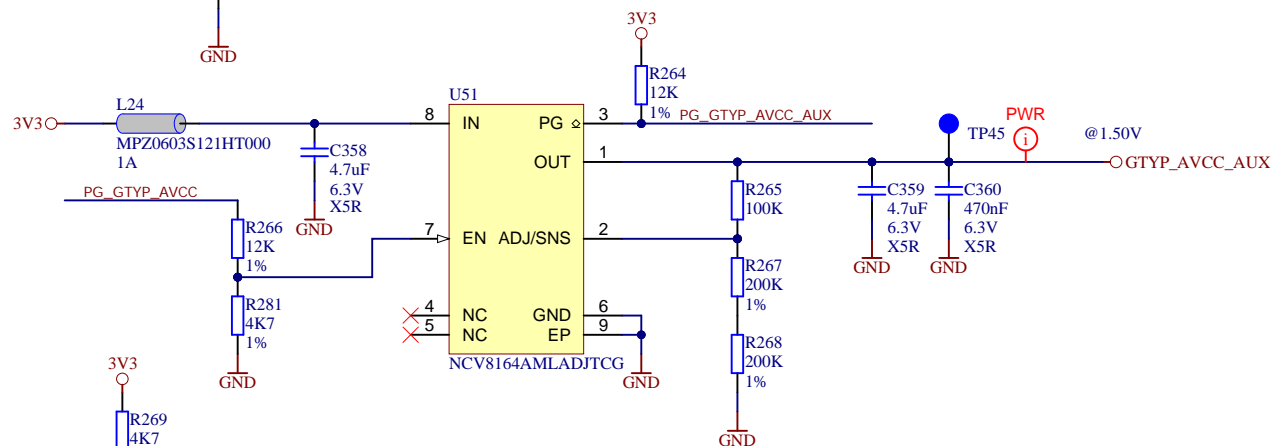
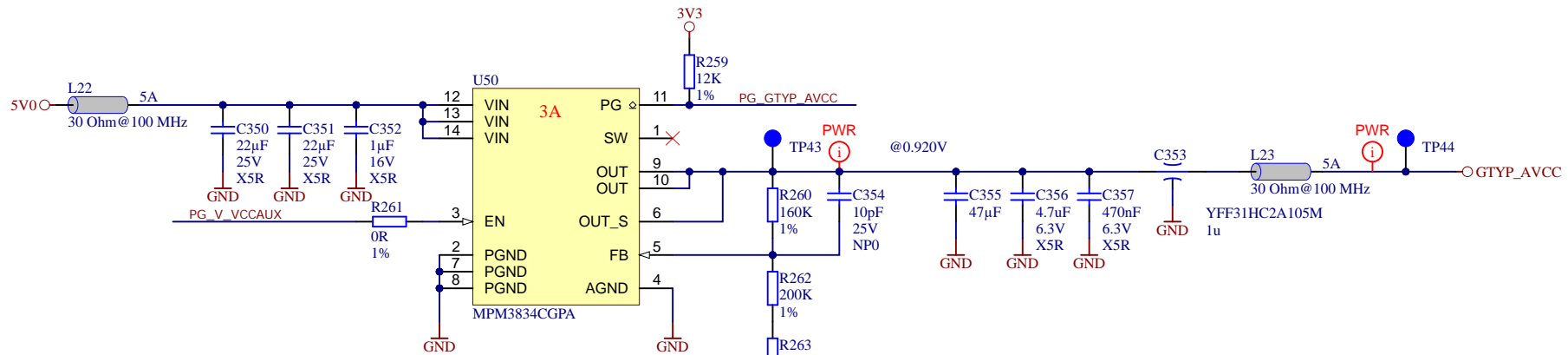
1.2V 1.8V 2.5V 3.3V
 OFF ON ON ON
 OFF OFF ON ON
 OFF OFF OFF ON



FMC_Switched



Title: Power_4		
A4	Number: TE0950 EGBE22A	Rev. 03
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Title: Power_5		
A4	Number: TE0950 EGBE22A	Rev. 03
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Filename: Power_5.SchDoc		