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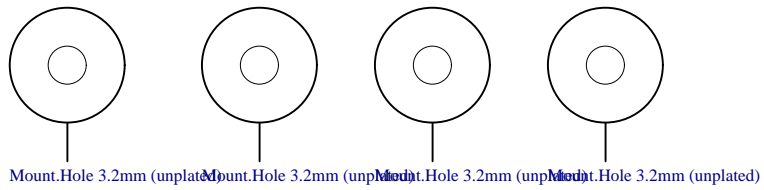
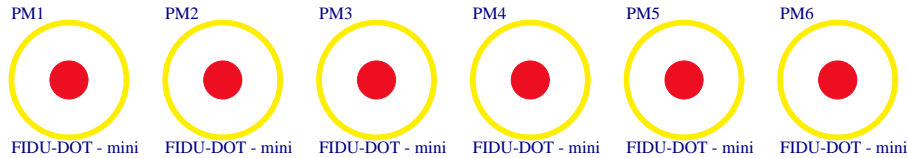
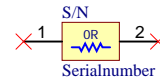
D


LOGO1

TE Logo PRINT Layer

LOGO PRINT

Serial  
Serial  
Serialnumber 6,3 x 6.3mm



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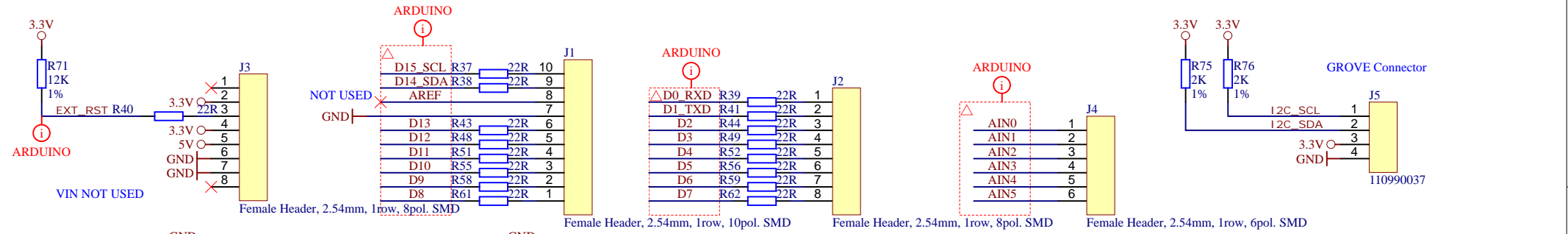
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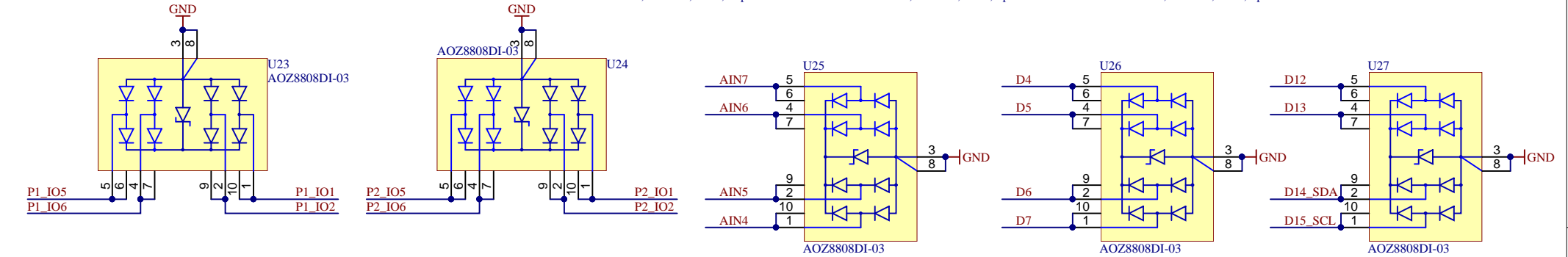
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A



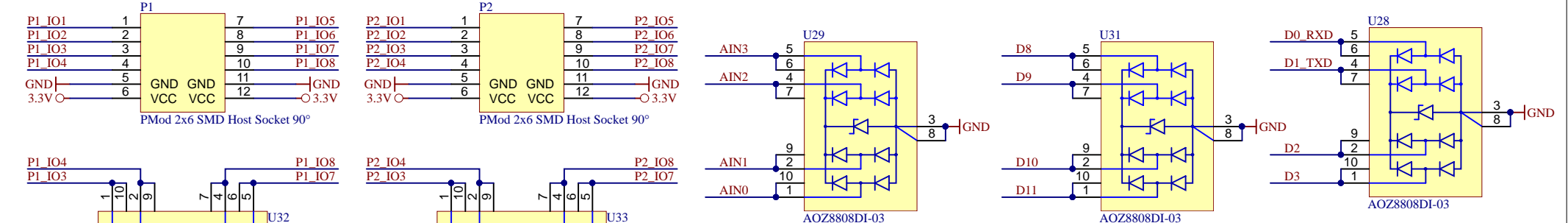
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B



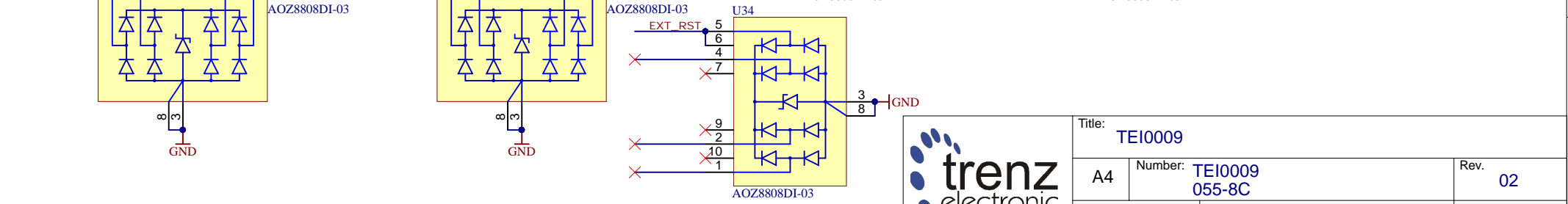
C

C



D

D



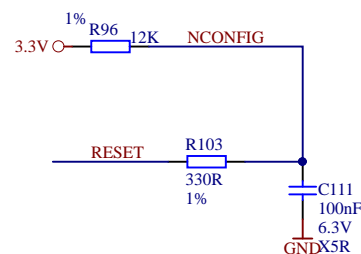
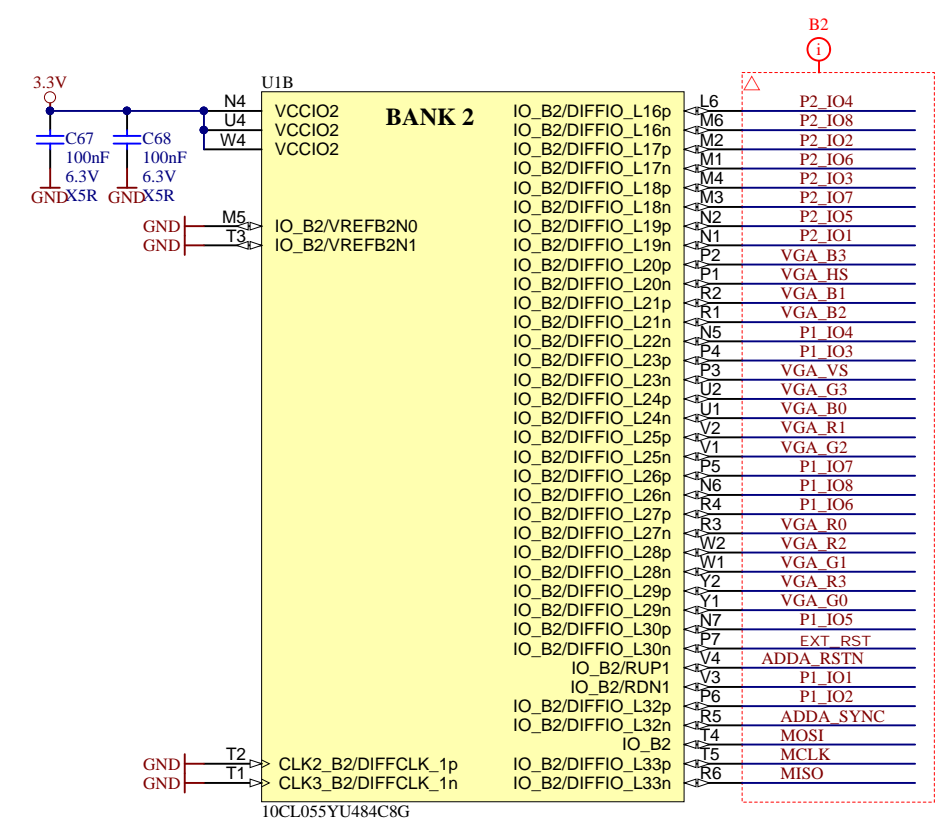
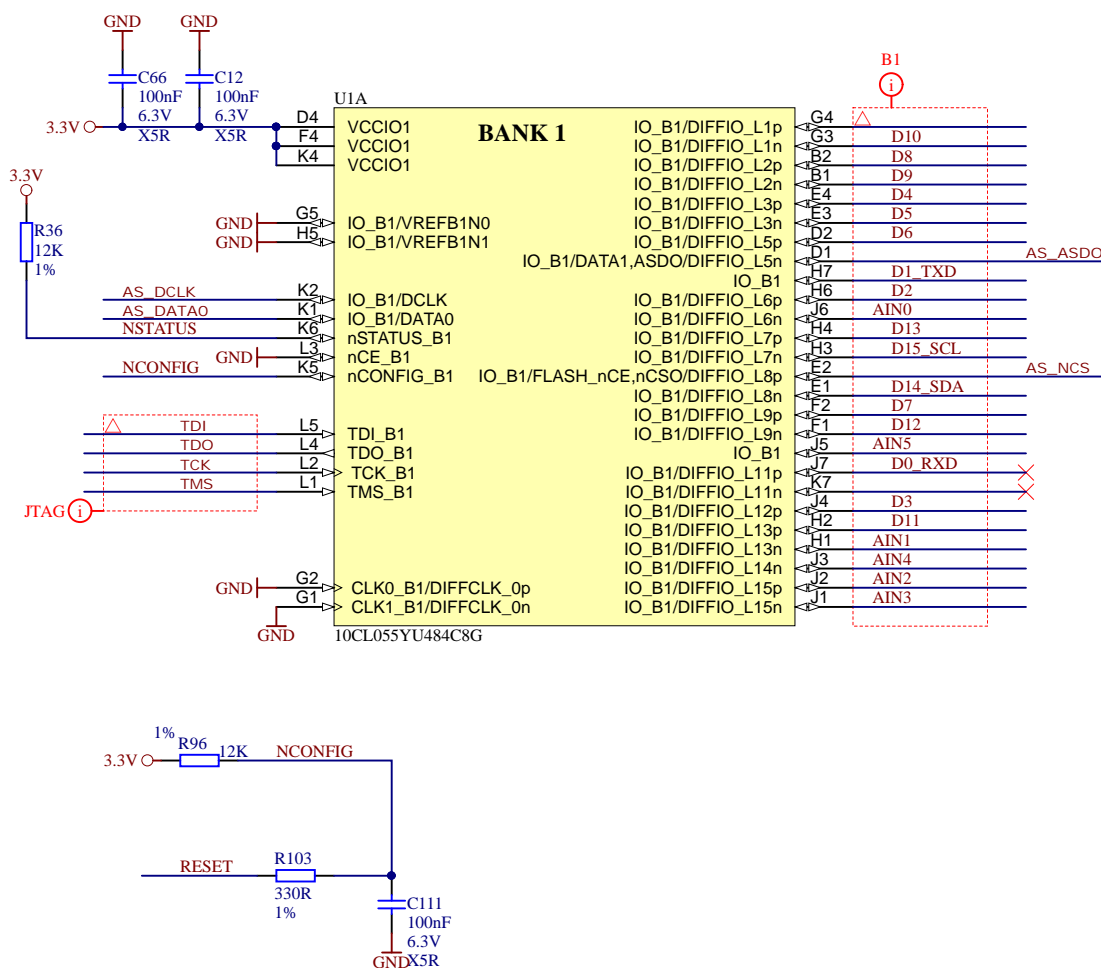
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1

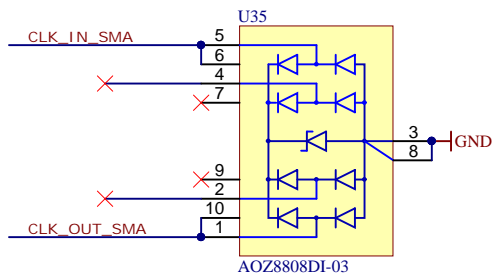
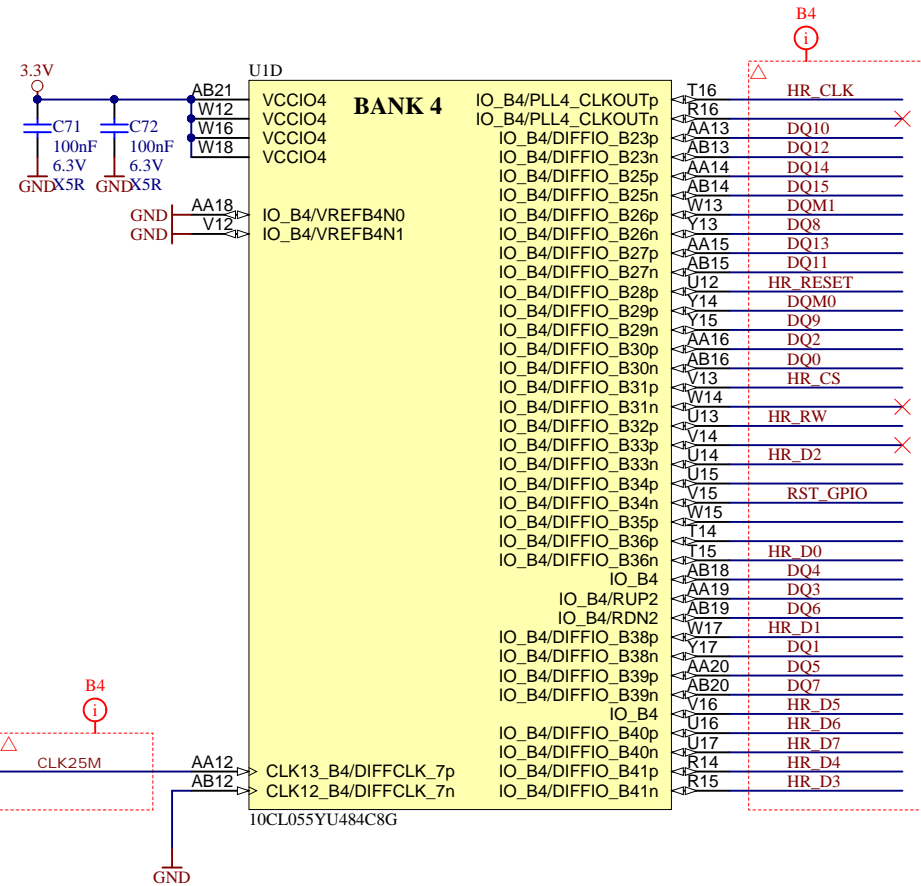
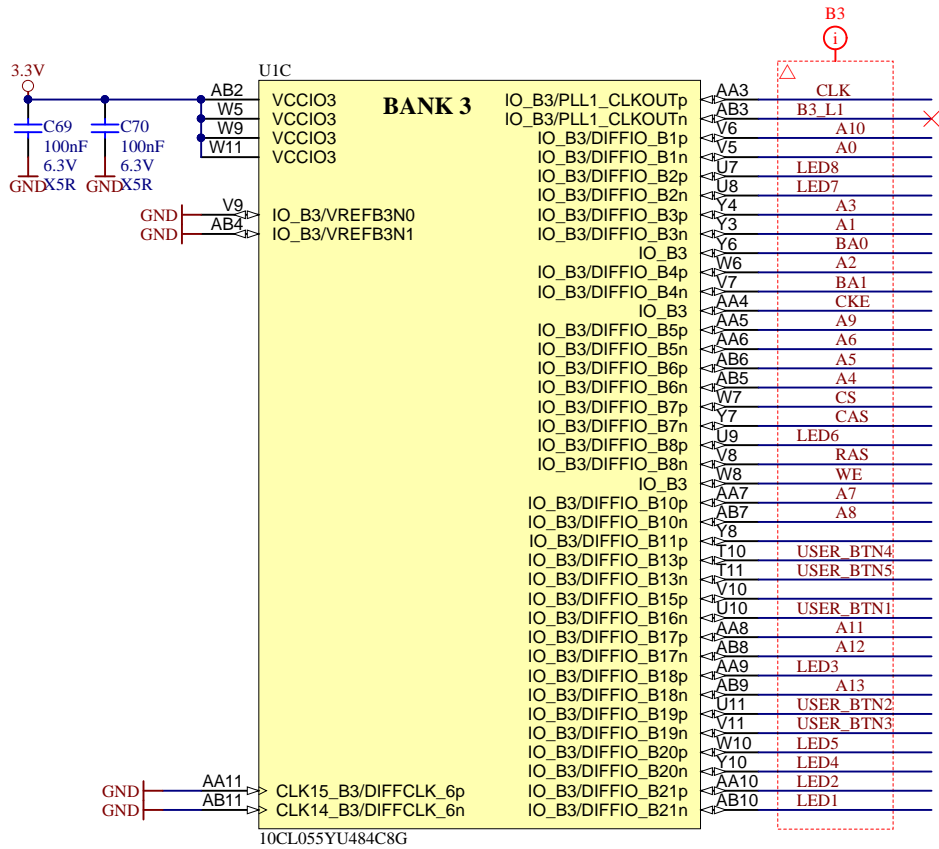
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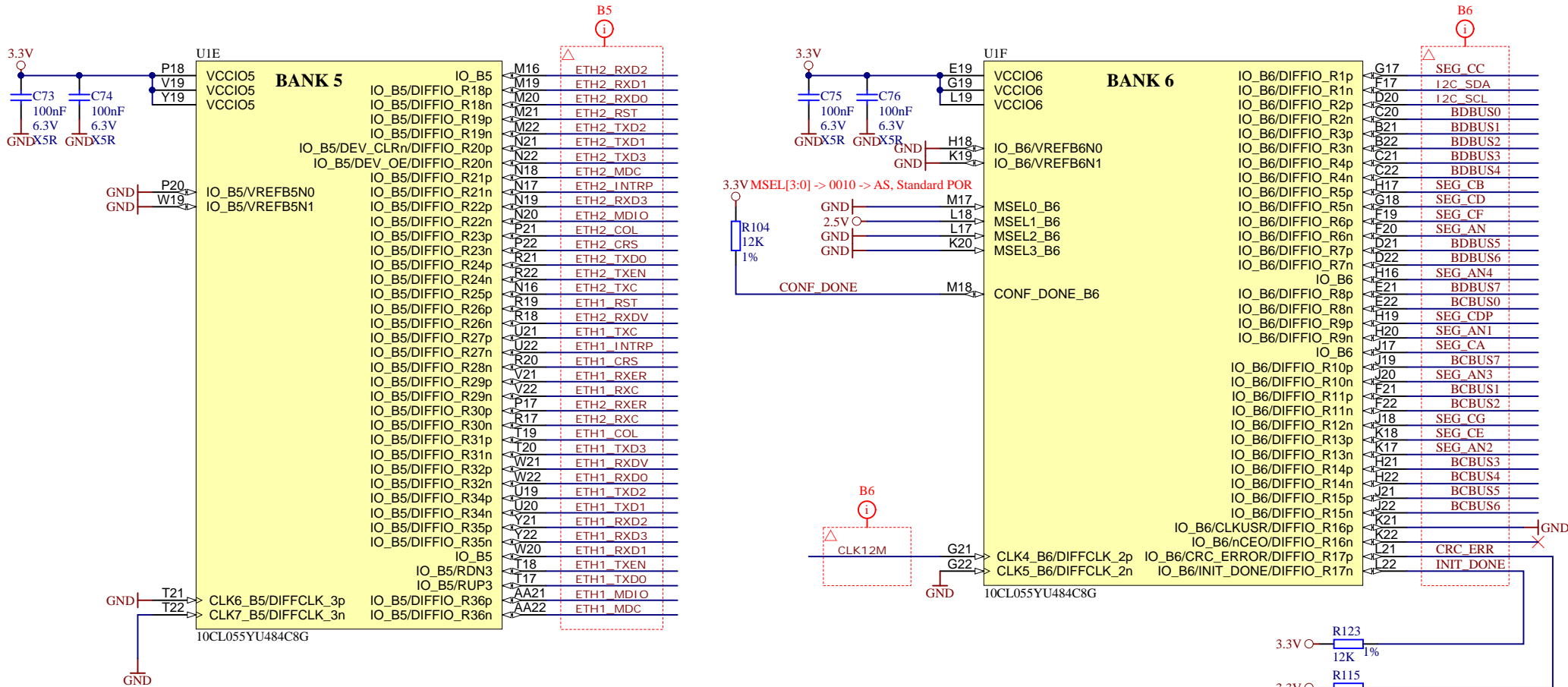


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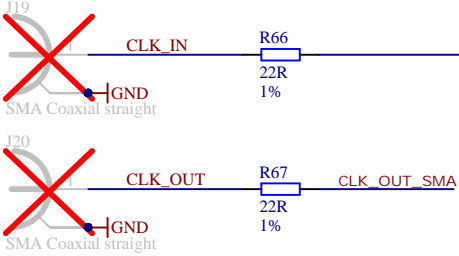
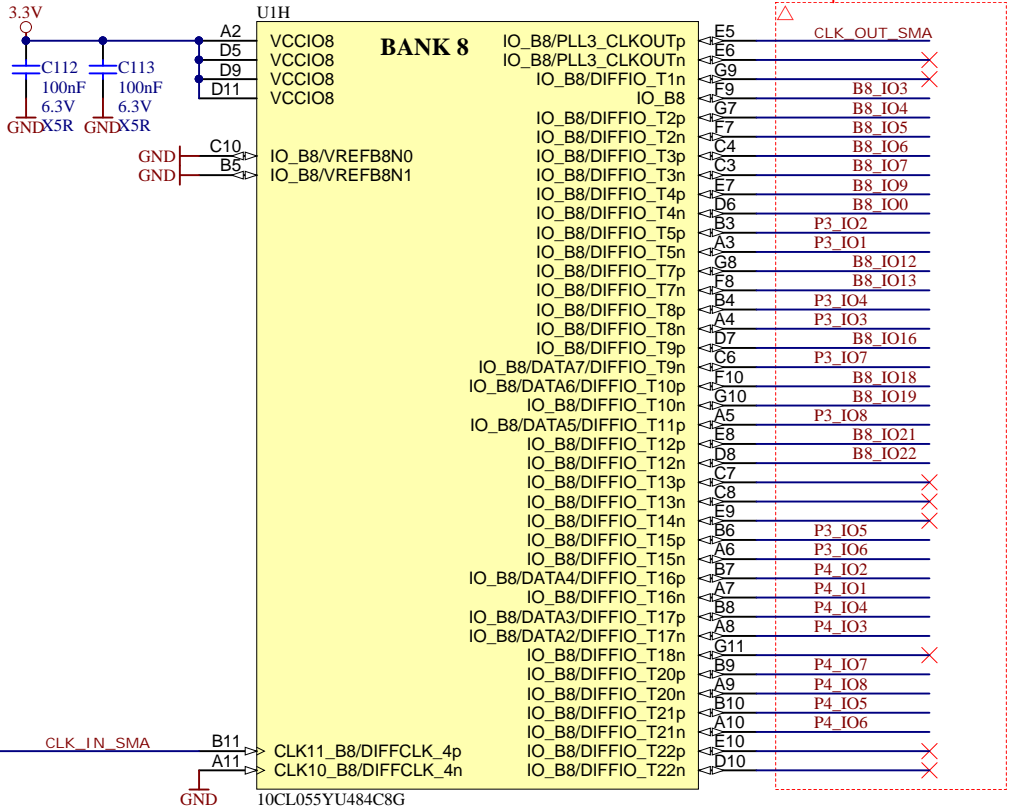
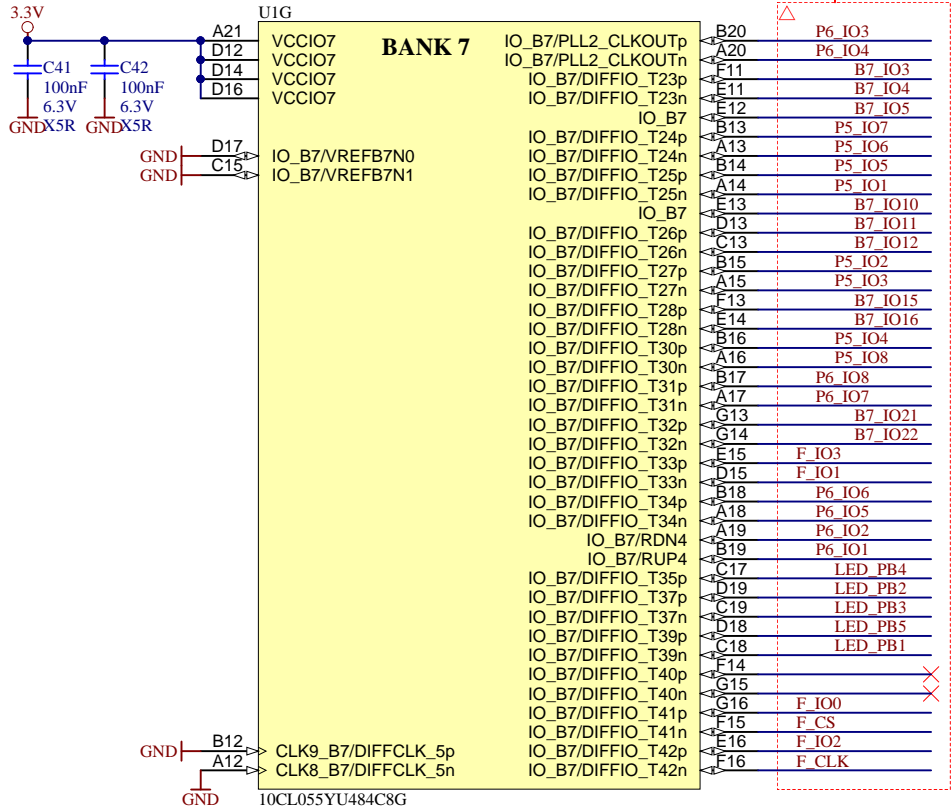


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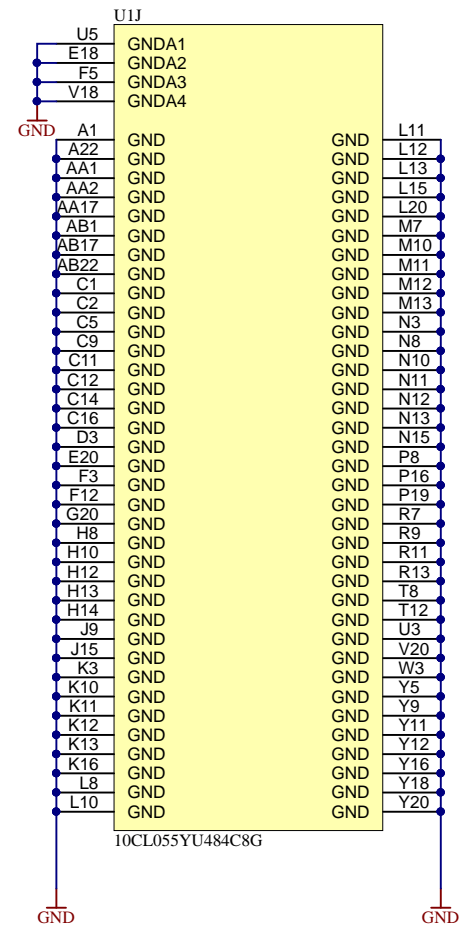
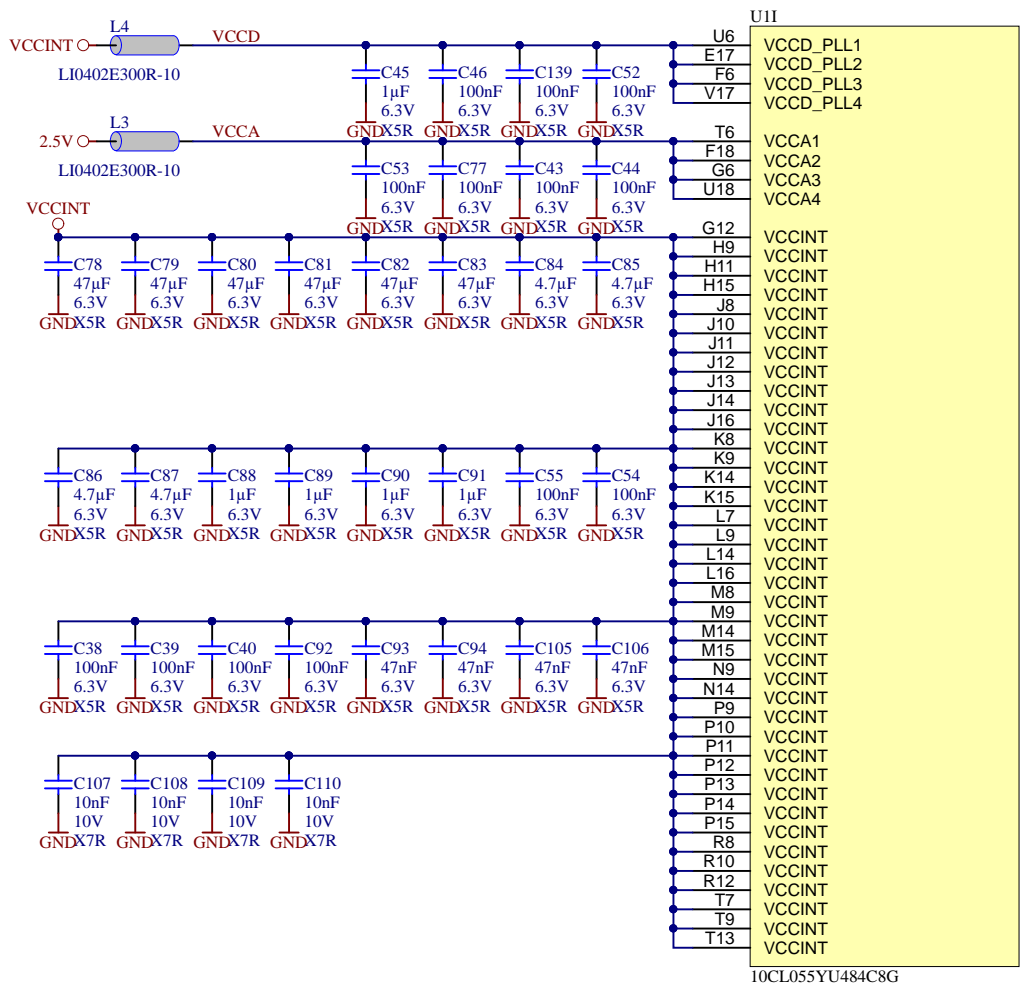
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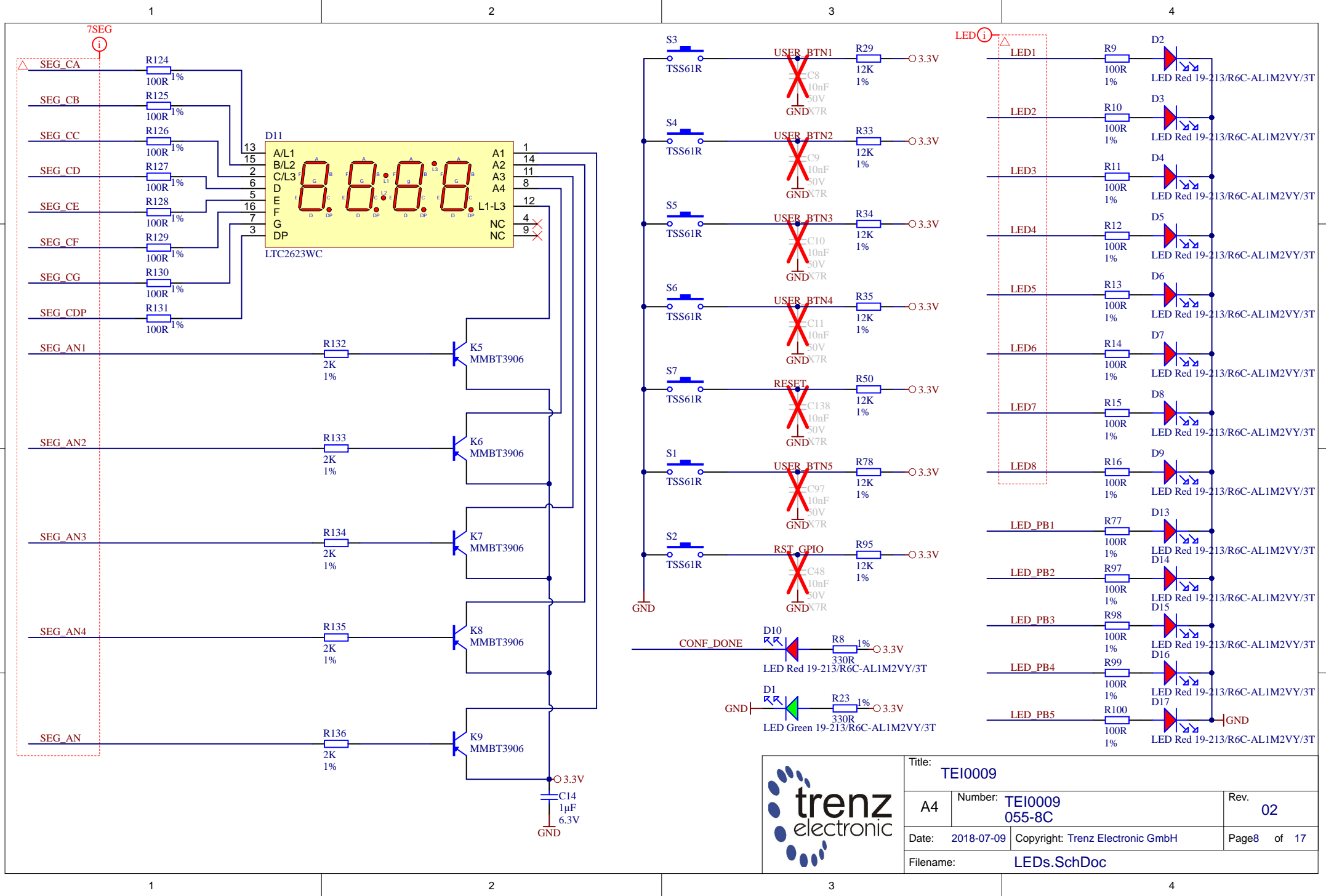
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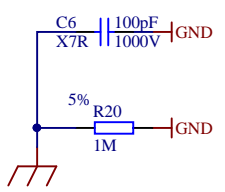
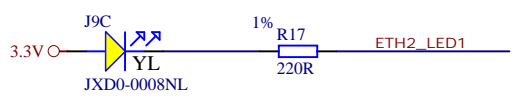
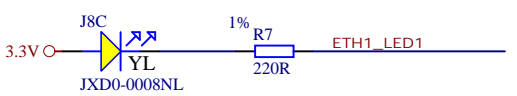
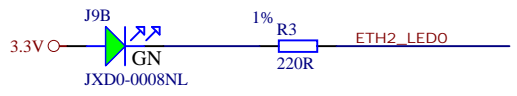
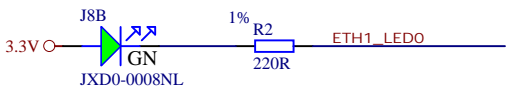
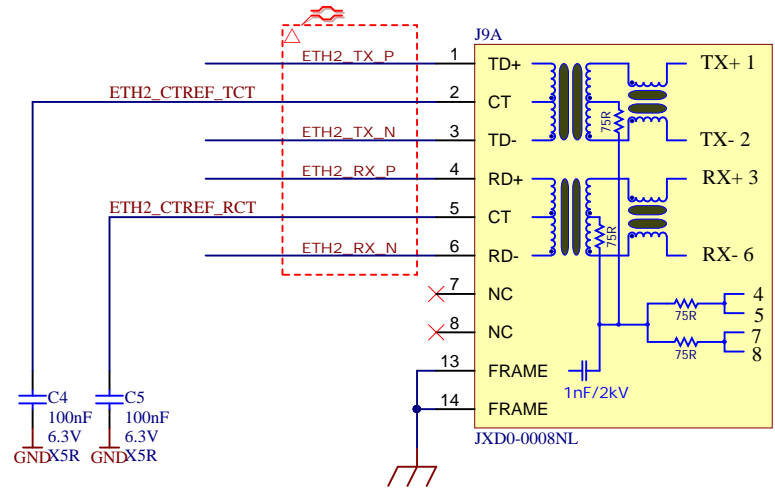
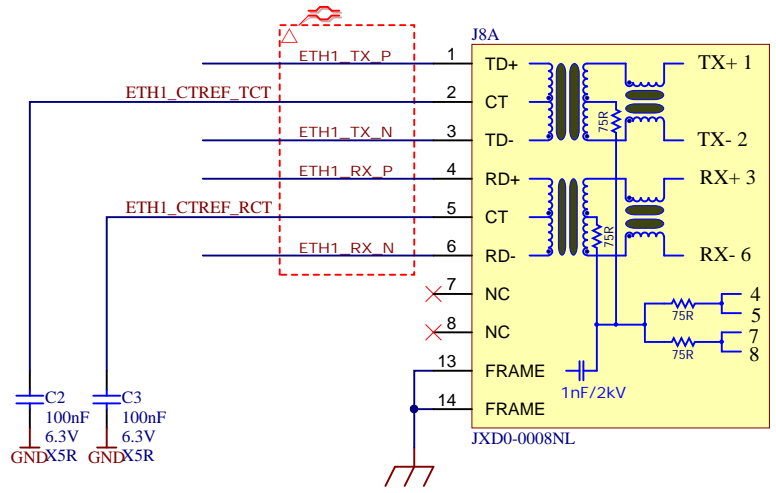


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Filename: <b>FPGA_PWR.SchDoc</b>		

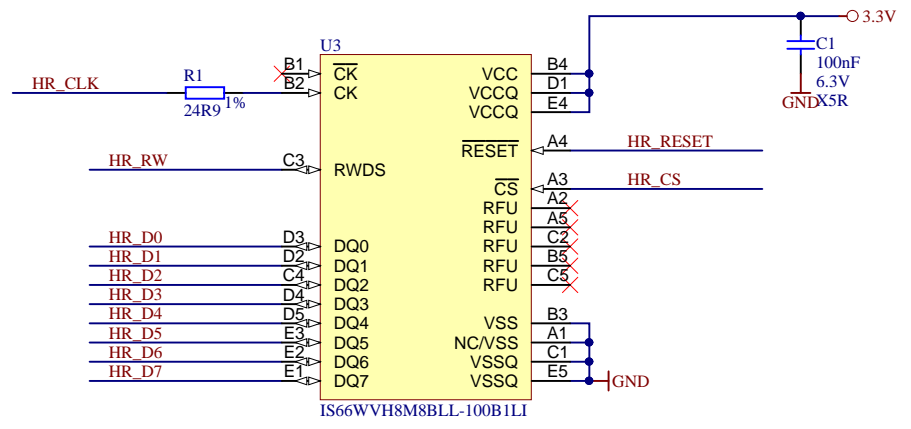
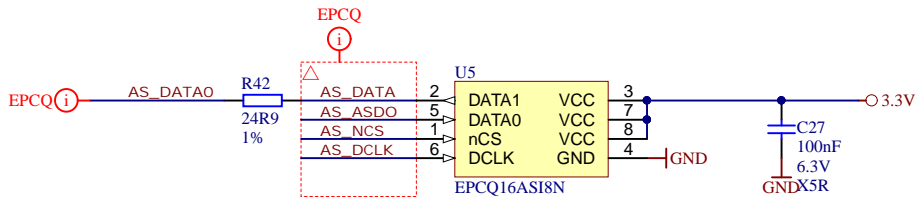
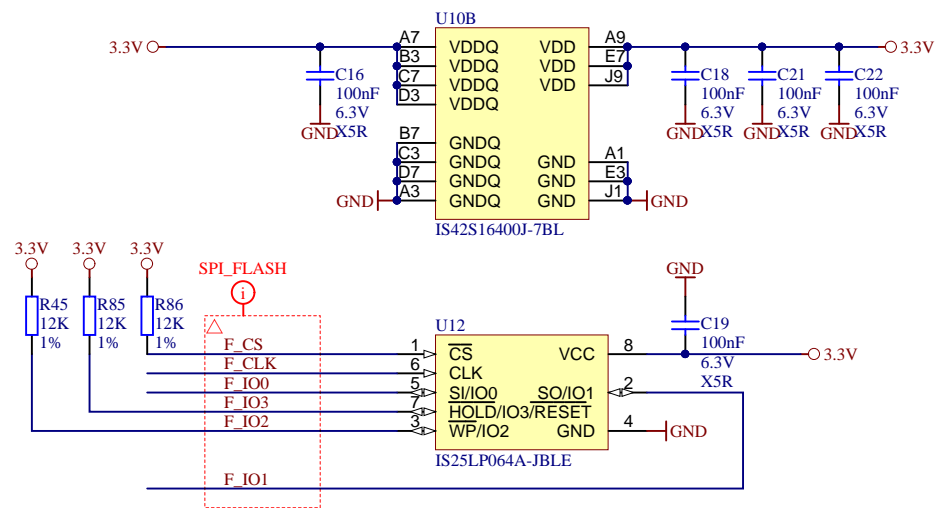
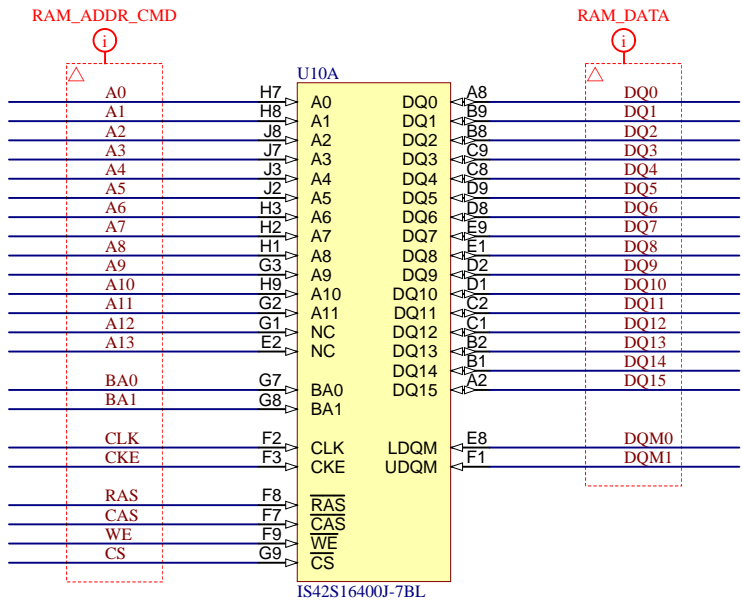



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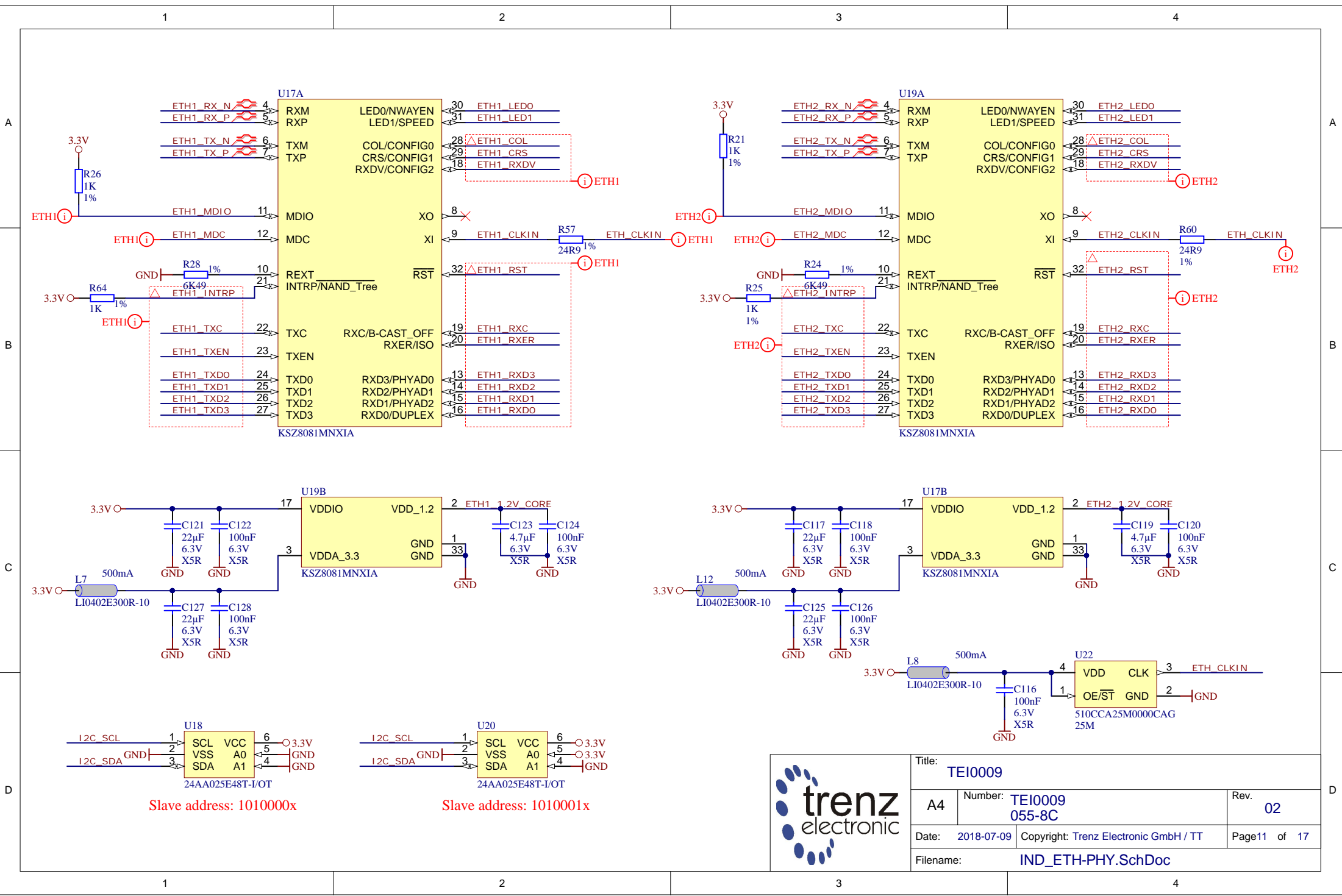




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Filename: Flash_RAM.SchDoc		



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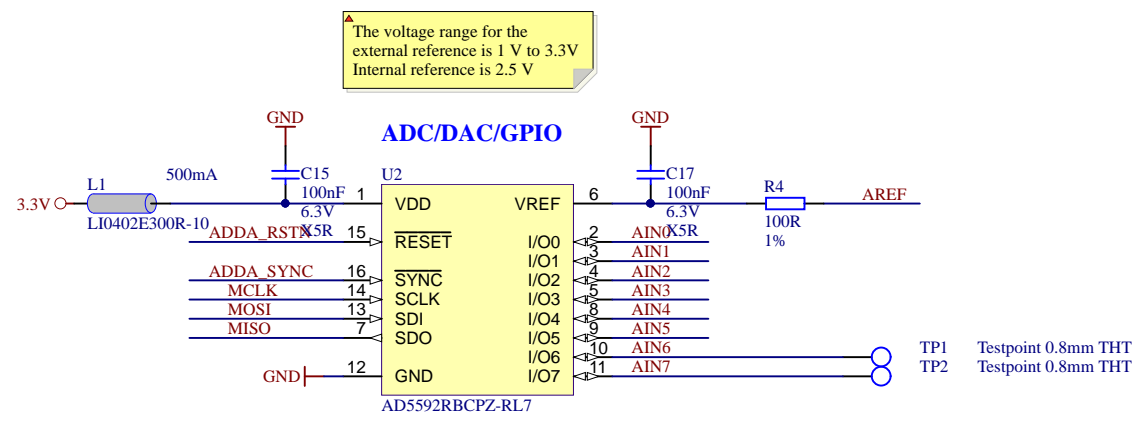
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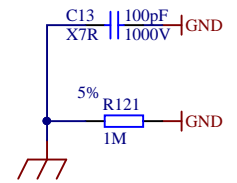
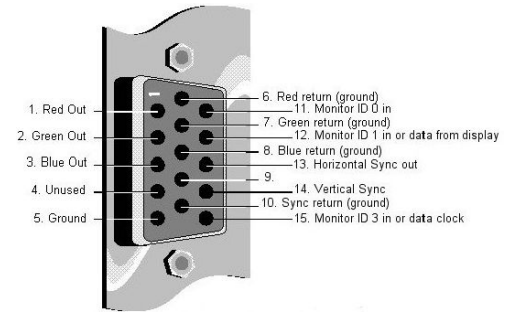
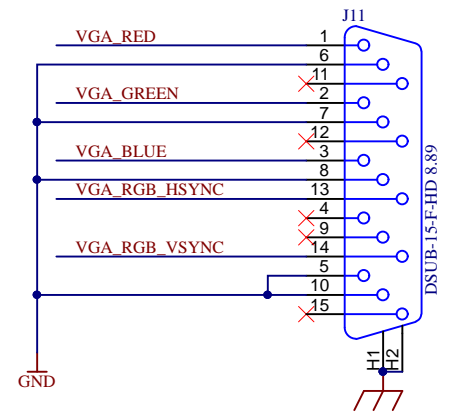
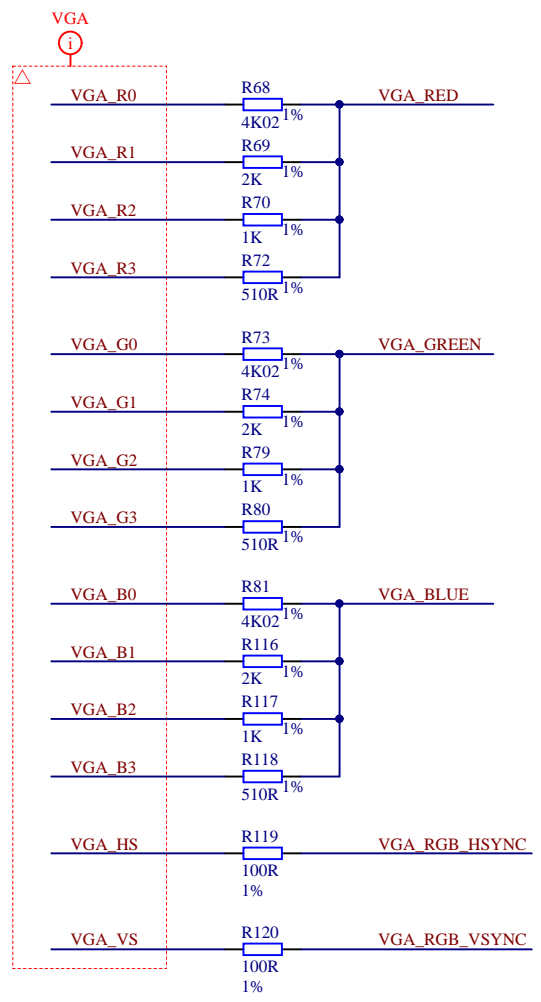
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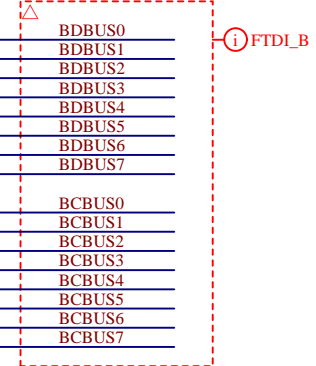
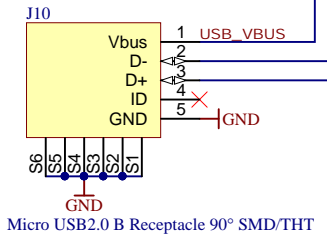
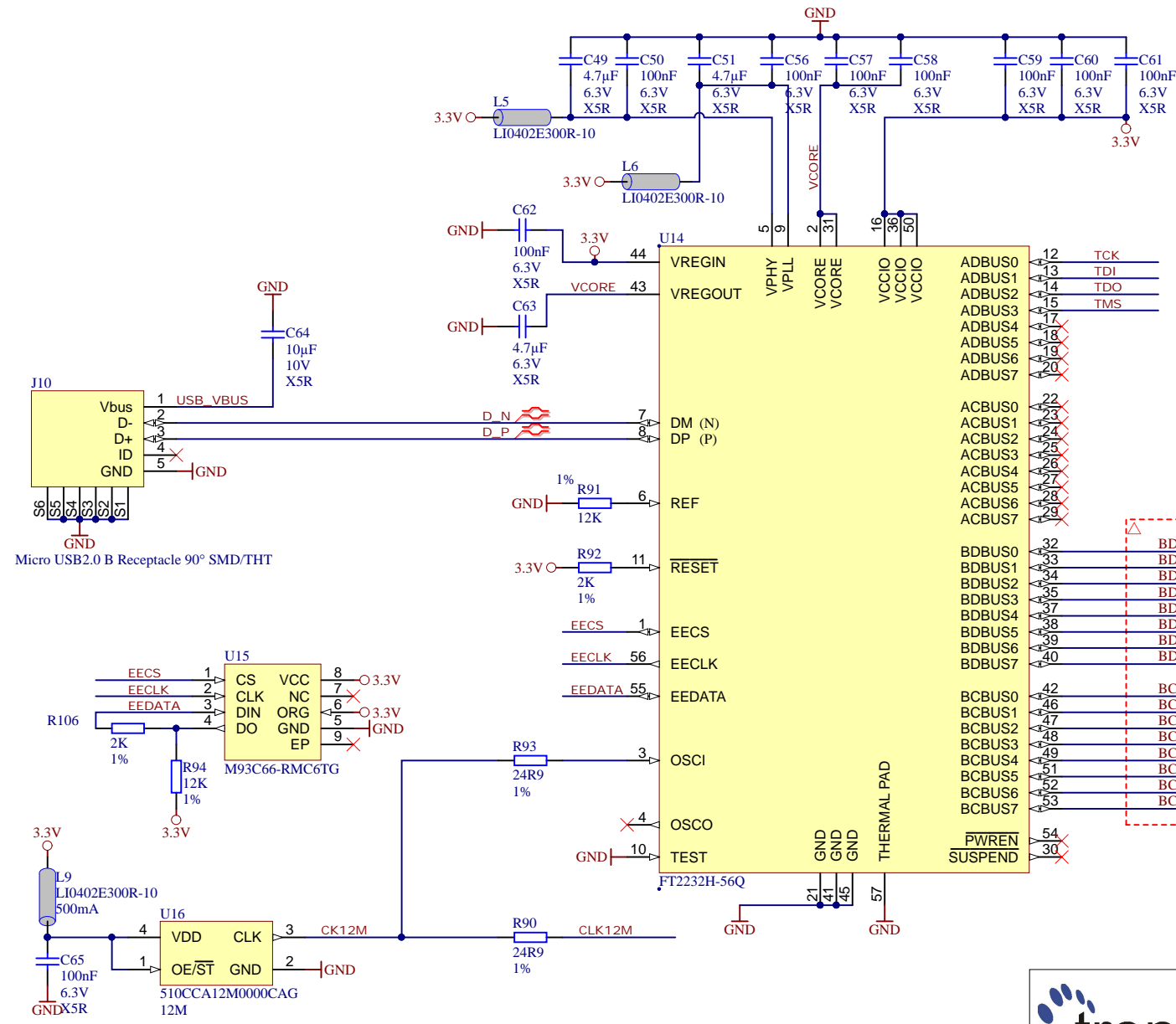
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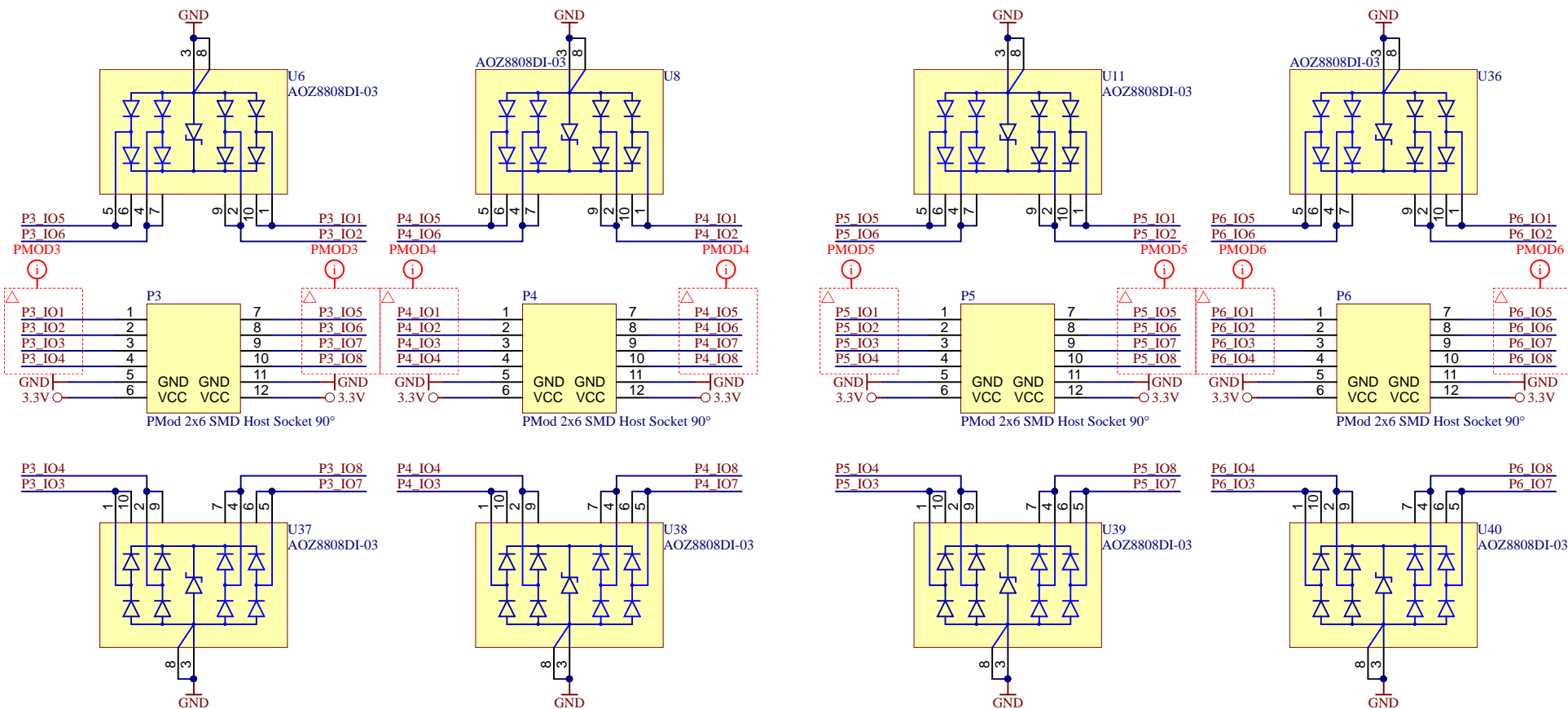
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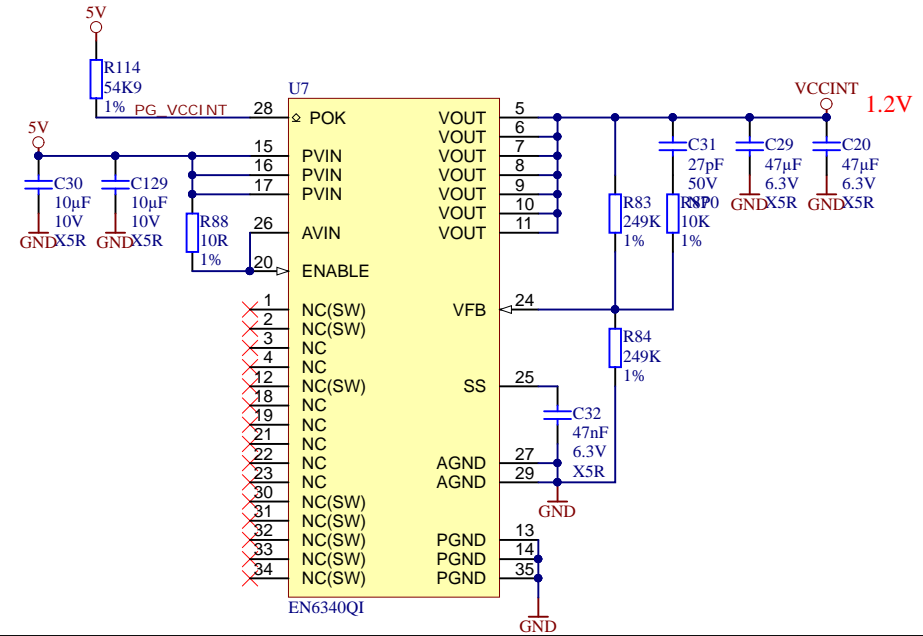
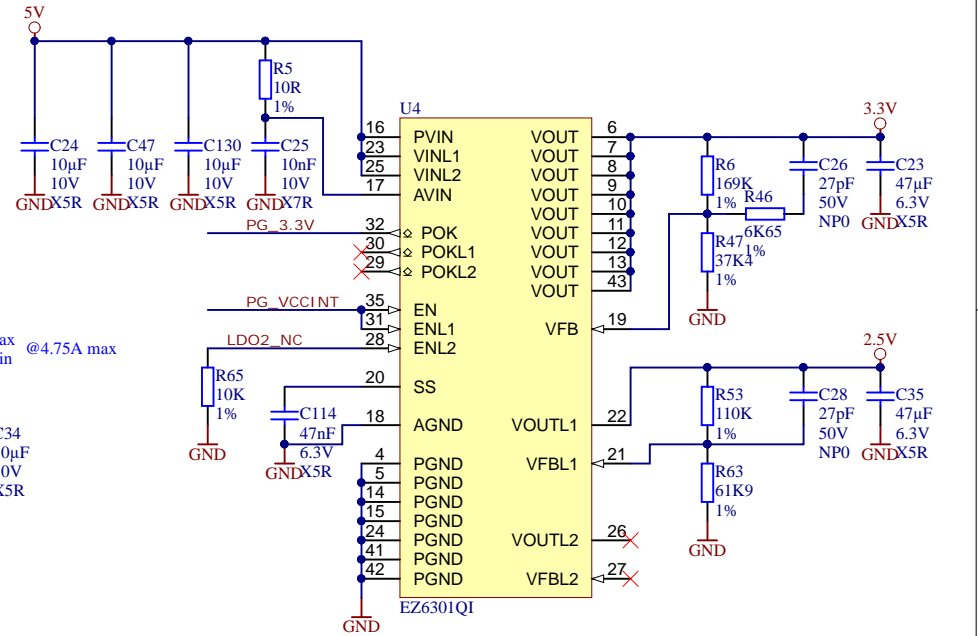
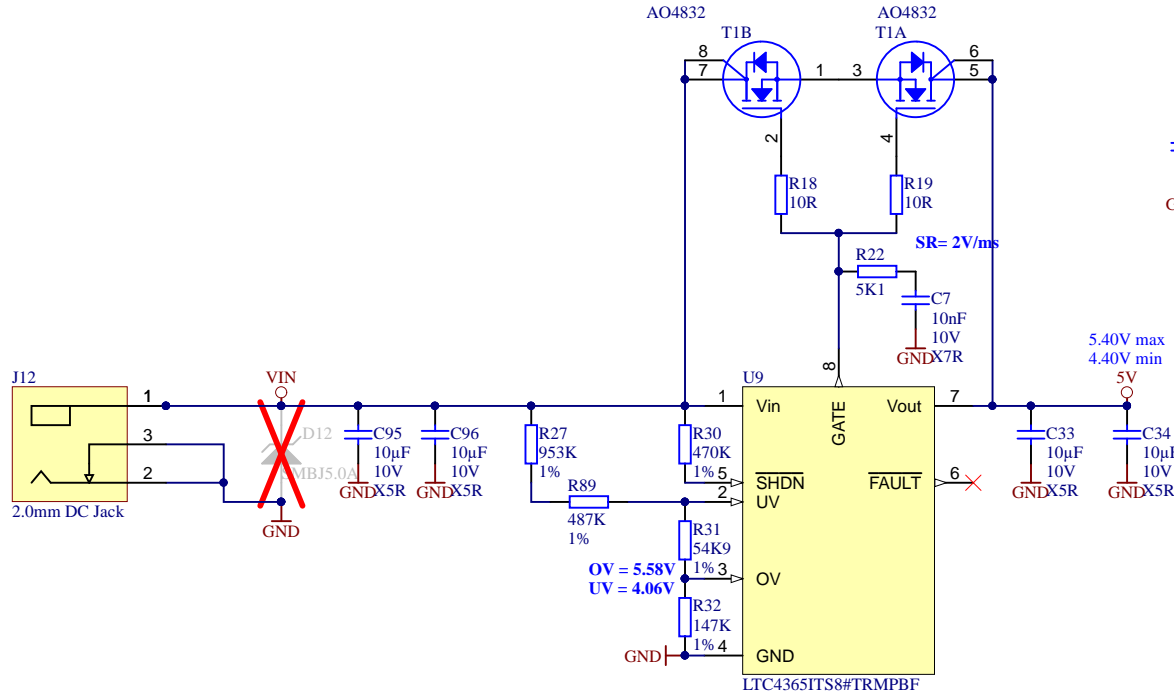
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REV01: Prototype only

REV02: Mass production  
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2019-08-30  
1) Replaced R27 by 953k and R32 by 147k

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