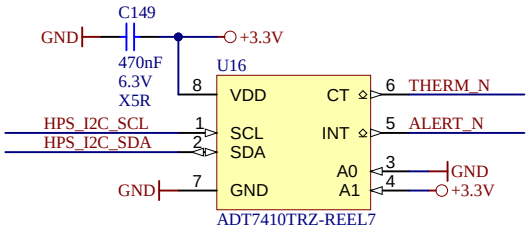
FrontPanel
FrontPanel.SchDoc
FPGA
FPGA.SchDoc
FTDI_JTAG
FTDI_JTAG.SchDoc
FTDI_UART
FTDI_UART.SchDoc
HDMI
HDMI.SchDoc
DDR3-RAM_FPGA
DDR3-RAM_FPGA.SchDoc
DDR3-RAM_HPS
DDR3-RAM_HPS.SchDoc
Ethernet
Ethernet.SchDoc

FMC
FMC.SchDoc
PMOD
PMOD.SchDoc
USB
USB.SchDoc
USB-HUB
USB-HUB.SchDoc
USB-PHY
USB-PHY.SchDoc
Power
Power.SchDoc
MGMT_FPGA
MGMT_FPGA.SchDoc
MGMT_FPGA_Misc
MGMT_FPGA_Misc.SchDoc



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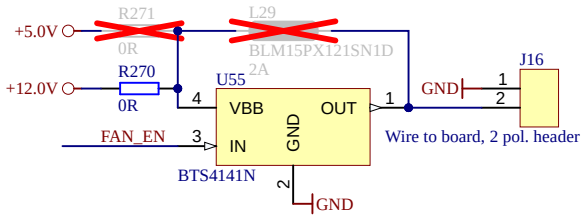
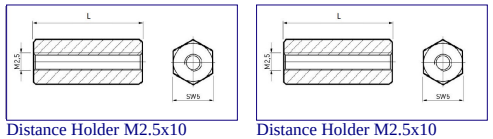
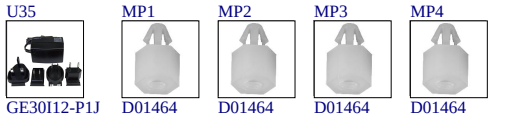
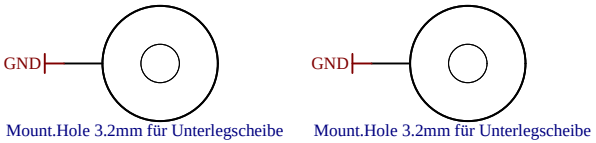
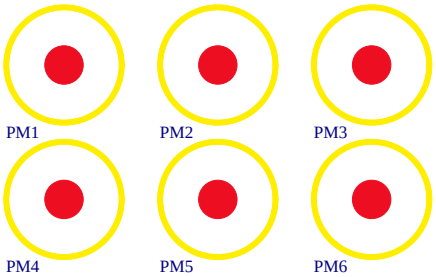
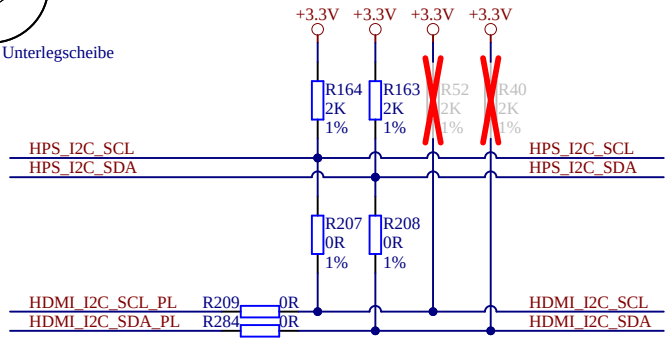


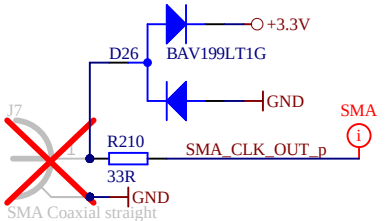


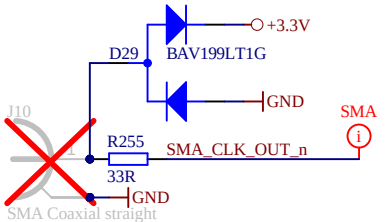


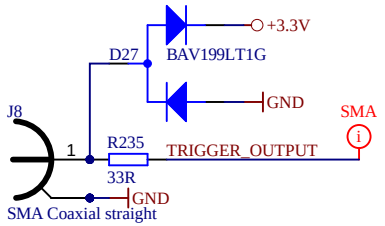


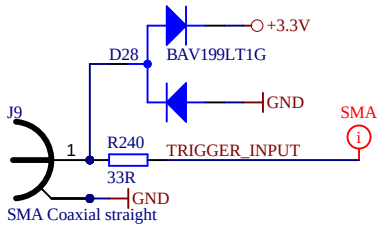


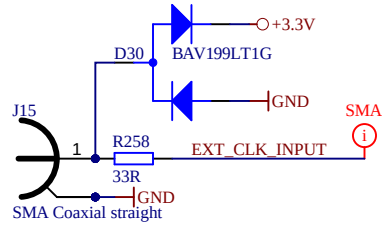


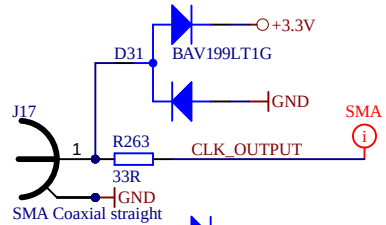


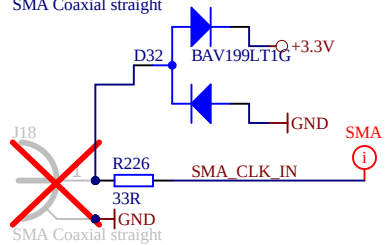










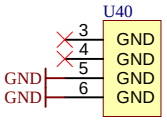


HPS I2C Addr:	Component
0x4A	Temperatur Sensor
0x50	EEPROM
0x70	Clock

HDMI I2C Addr:	Component
0x72	HDMI

HPS FMC I2C Addr:	Component
0x50	FMC

Serial1
Serial
Serialnumber 6,3 x 6.3mm



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Single FMC Commercial Baseboard Snap

Design drawn by:	ED
Checked by:	VT
Assembly variant:	Default
Created by:	ED
Modified by:	ED
Modified at:	2020-05-29

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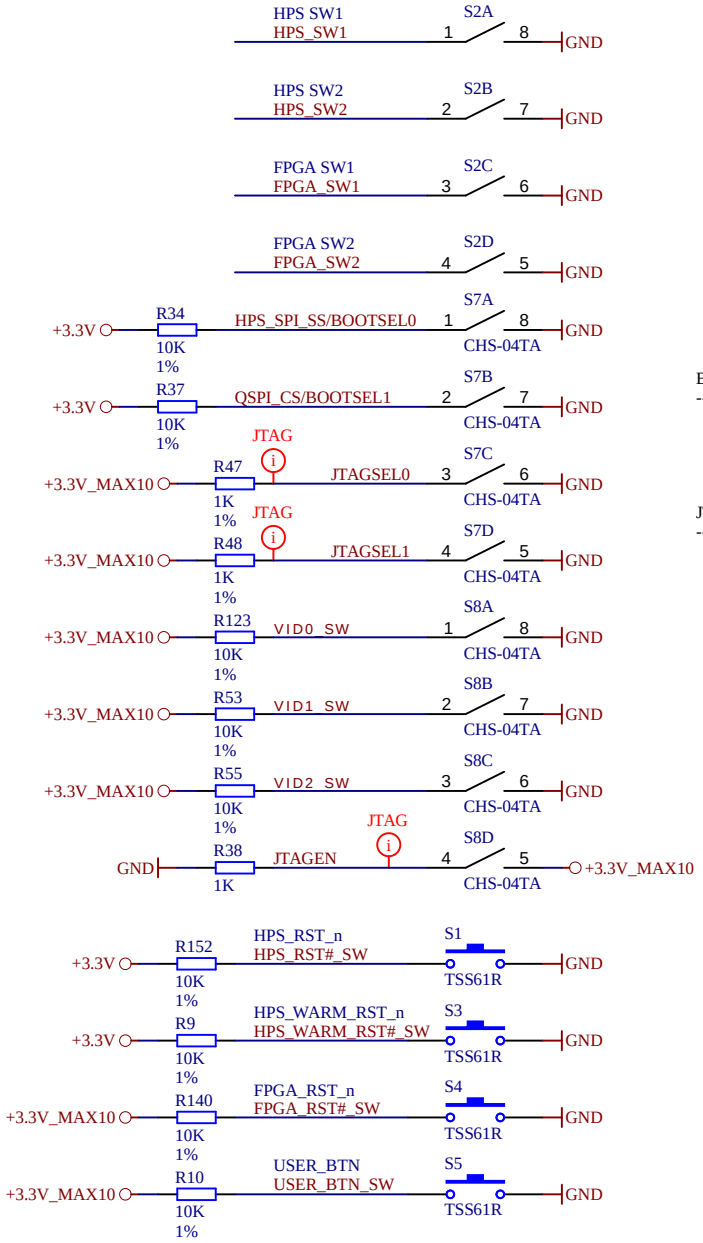
Title: TEI0022		
A4	Number: TEI0022.PrjPCB Default	Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 1 of 34
Drawn by: ED	Filename: TEI0022.SchDoc	

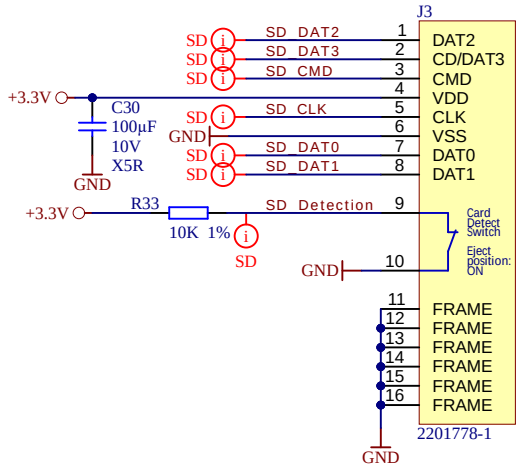


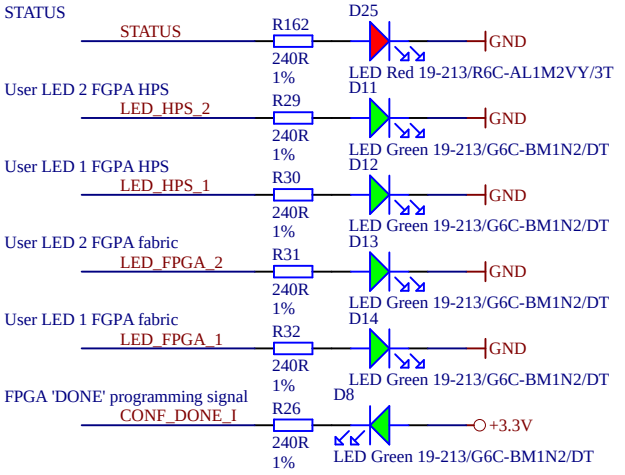
BOOTSEL0 | BOOTSEL1 | BOOTSEL2 | Boot Select

0	0	1	FPGA
1	0	1	SD/MMC (3.3V)
1	1	1	SPI(3.3V)

JTAGSEL0 | JTAGSEL1 | JTAGEN | JTAG Selection

X	X	1 - (ON)	MAX10
0 - (ON)	0 - (ON)	0 - (OFF)	CYCLONE V HPS
0 - (ON)	1 - (OFF)	0 - (OFF)	CYCLONE V FPGA
1 - (OFF)	0 - (ON)	0 - (OFF)	FMC





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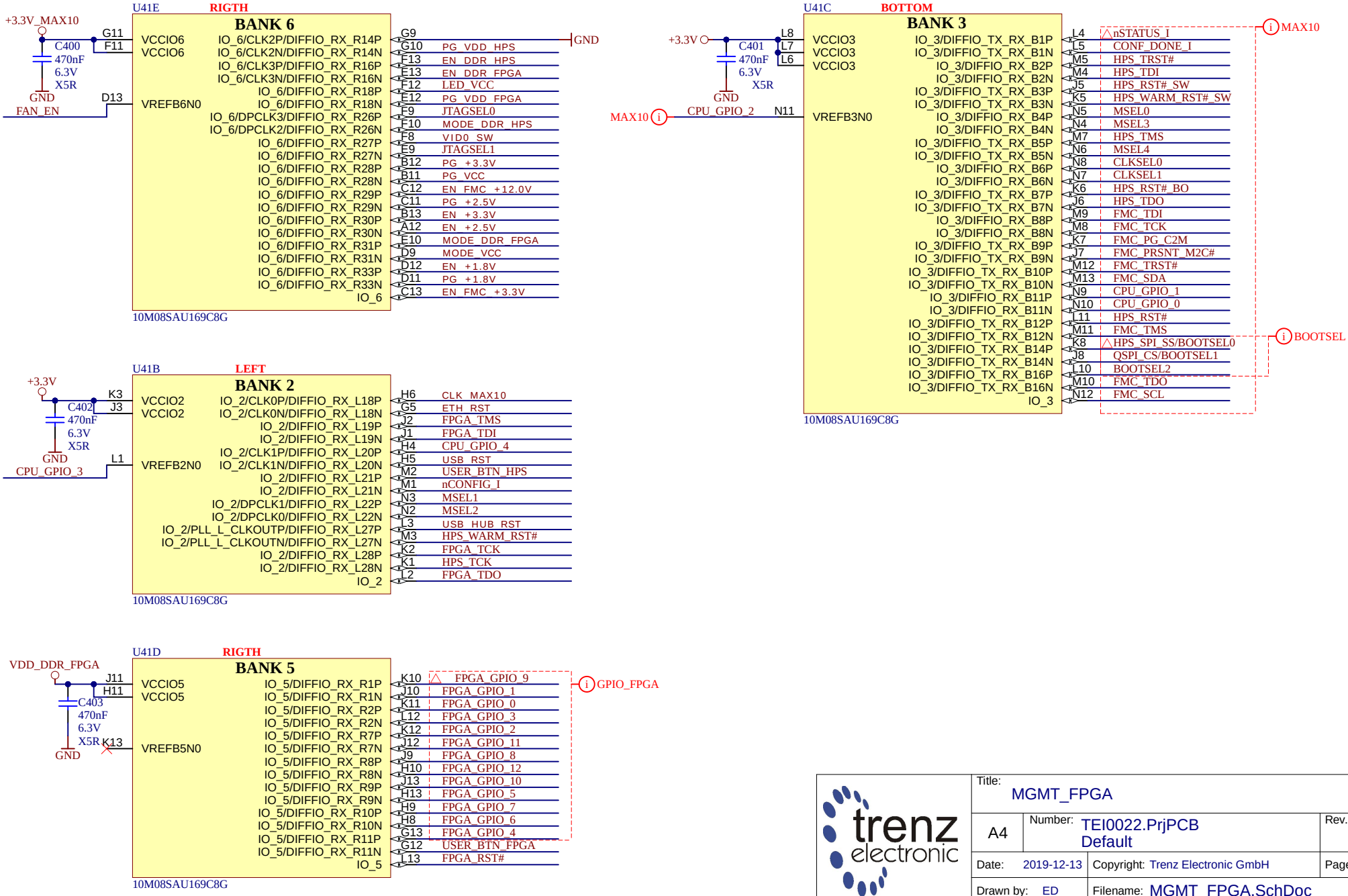
Title: FrontPanel		
A4	Number: TEI0022.PrjPCB Default	Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 2 of 34
Drawn by: ED	Filename: FrontPanel.SchDoc	


U41E
RIGTH
BANK 6
+3.3V_MAX10
C400
470nF
6.3V
X5R
GND
FAN_EN
D13
VCCIO6
VCCIO6
VREFB6N0
IO_6/CLK2P/DIFFIO_RX_R14P
IO_6/CLK2N/DIFFIO_RX_R14N
IO_6/CLK3P/DIFFIO_RX_R16P
IO_6/CLK3N/DIFFIO_RX_R16N
IO_6/DIFFIO_RX_R18P
IO_6/DIFFIO_RX_R18N
IO_6/DPCLK3/DIFFIO_RX_R26P
IO_6/DPCLK2/DIFFIO_RX_R26N
IO_6/DIFFIO_RX_R27P
IO_6/DIFFIO_RX_R27N
IO_6/DIFFIO_RX_R28P
IO_6/DIFFIO_RX_R28N
IO_6/DIFFIO_RX_R29P
IO_6/DIFFIO_RX_R29N
IO_6/DIFFIO_RX_R30P
IO_6/DIFFIO_RX_R30N
IO_6/DIFFIO_RX_R31P
IO_6/DIFFIO_RX_R31N
IO_6/DIFFIO_RX_R33P
IO_6/DIFFIO_RX_R33N
IO_6
PG_VDD_HPS
EN_DDR_HPS
EN_DDR_FPGA
LED_VCC
PG_VDD_FPGA
JTAGSEL0
MODE_DDR_HPS
VID0_SW
JTAGSEL1
PG_+3.3V
PG_VCC
EN_FMC_+12.0V
PG_+2.5V
EN_+3.3V
EN_+2.5V
MODE_DDR_FPGA
MODE_VCC
EN_+1.8V
PG_+1.8V
EN_FMC_+3.3V
GND
10M08SAU169C8G
U41C
BOTTOM
BANK 3
+3.3V
C401
470nF
6.3V
X5R
GND
MAX10
CPU_GPIO_2
VCCIO3
VCCIO3
VCCIO3
VREFB3N0
IO_3/DIFFIO_TX_RX_B1P
IO_3/DIFFIO_TX_RX_B1N
IO_3/DIFFIO_RX_B2P
IO_3/DIFFIO_RX_B2N
IO_3/DIFFIO_TX_RX_B3P
IO_3/DIFFIO_TX_RX_B3N
IO_3/DIFFIO_RX_B4P
IO_3/DIFFIO_RX_B4N
IO_3/DIFFIO_TX_RX_B5P
IO_3/DIFFIO_TX_RX_B5N
IO_3/DIFFIO_RX_B6P
IO_3/DIFFIO_RX_B6N
IO_3/DIFFIO_TX_RX_B7P
IO_3/DIFFIO_TX_RX_B7N
IO_3/DIFFIO_RX_B8P
IO_3/DIFFIO_RX_B8N
IO_3/DIFFIO_TX_RX_B9P
IO_3/DIFFIO_TX_RX_B9N
IO_3/DIFFIO_TX_RX_B10P
IO_3/DIFFIO_TX_RX_B10N
IO_3/DIFFIO_RX_B11P
IO_3/DIFFIO_RX_B11N
IO_3/DIFFIO_TX_RX_B12P
IO_3/DIFFIO_TX_RX_B12N
IO_3/DIFFIO_TX_RX_B14P
IO_3/DIFFIO_TX_RX_B14N
IO_3/DIFFIO_TX_RX_B16P
IO_3/DIFFIO_TX_RX_B16N
IO_3
nSTATUS_I
CONF_DONE_I
HPS_TRST#
HPS_TDI
HPS_RST#_SW
HPS_WARM_RST#_SW
MSEL0
MSEL3
HPS_TMS
MSEL4
CLKSEL0
CLKSEL1
HPS_RST#_BO
HPS_TDO
FMC_TDI
FMC_TCK
FMC_PG_C2M
FMC_PRSNT_M2C#
FMC_TRST#
FMC_SDA
CPU_GPIO_1
CPU_GPIO_0
HPS_RST#
FMC_TMS
HPS_SPI_SS/BOOTSEL0
QSPI_CS/BOOTSEL1
BOOTSEL2
FMC_TDO
FMC_SCL
MAX10
BOOTSEL
10M08SAU169C8G
U41B
LEFT
BANK 2
+3.3V
C402
470nF
6.3V
X5R
GND
CPU_GPIO_3
VCCIO2
VCCIO2
VREFB2N0
IO_2/CLK0P/DIFFIO_RX_L18P
IO_2/CLK0N/DIFFIO_RX_L18N
IO_2/DIFFIO_RX_L19P
IO_2/DIFFIO_RX_L19N
IO_2/CLK1P/DIFFIO_RX_L20P
IO_2/CLK1N/DIFFIO_RX_L20N
IO_2/DIFFIO_RX_L21P
IO_2/DIFFIO_RX_L21N
IO_2/DPCLK1/DIFFIO_RX_L22P
IO_2/DPCLK0/DIFFIO_RX_L22N
IO_2/PLL_L_CLKOUTP/DIFFIO_RX_L27P
IO_2/PLL_L_CLKOUTN/DIFFIO_RX_L27N
IO_2/DIFFIO_RX_L28P
IO_2/DIFFIO_RX_L28N
IO_2
CLK_MAX10
ETH_RST
FPGA_TMS
FPGA_TDI
CPU_GPIO_4
USB_RST
USER_BTN_HPS
nCONFIG_I
MSEL1
MSEL2
USB_HUB_RST
HPS_WARM_RST#
FPGA_TCK
HPS_TCK
FPGA_TDO
10M08SAU169C8G
U41D
RIGTH
BANK 5
VDD_DDR_FPGA
C403
470nF
6.3V
X5R
GND
VCCIO5
VCCIO5
VREFB5N0
IO_5/DIFFIO_RX_R1P
IO_5/DIFFIO_RX_R1N
IO_5/DIFFIO_RX_R2P
IO_5/DIFFIO_RX_R2N
IO_5/DIFFIO_RX_R7P
IO_5/DIFFIO_RX_R7N
IO_5/DIFFIO_RX_R8P
IO_5/DIFFIO_RX_R8N
IO_5/DIFFIO_RX_R9P
IO_5/DIFFIO_RX_R9N
IO_5/DIFFIO_RX_R10P
IO_5/DIFFIO_RX_R10N
IO_5/DIFFIO_RX_R11P
IO_5/DIFFIO_RX_R11N
IO_5
FPGA_GPIO_9
FPGA_GPIO_1
FPGA_GPIO_0
FPGA_GPIO_3
FPGA_GPIO_2
FPGA_GPIO_11
FPGA_GPIO_8
FPGA_GPIO_12
FPGA_GPIO_10
FPGA_GPIO_5
FPGA_GPIO_7
FPGA_GPIO_6
FPGA_GPIO_4
USER_BTN_FPGA
FPGA_RST#
GPIO_FPGA
10M08SAU169C8G
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Title: MGMT_FPGA
A4
Number: TEI0022.PrjPCB Default
Rev. 03
Date: 2019-12-13
Copyright: Trenz Electronic GmbH
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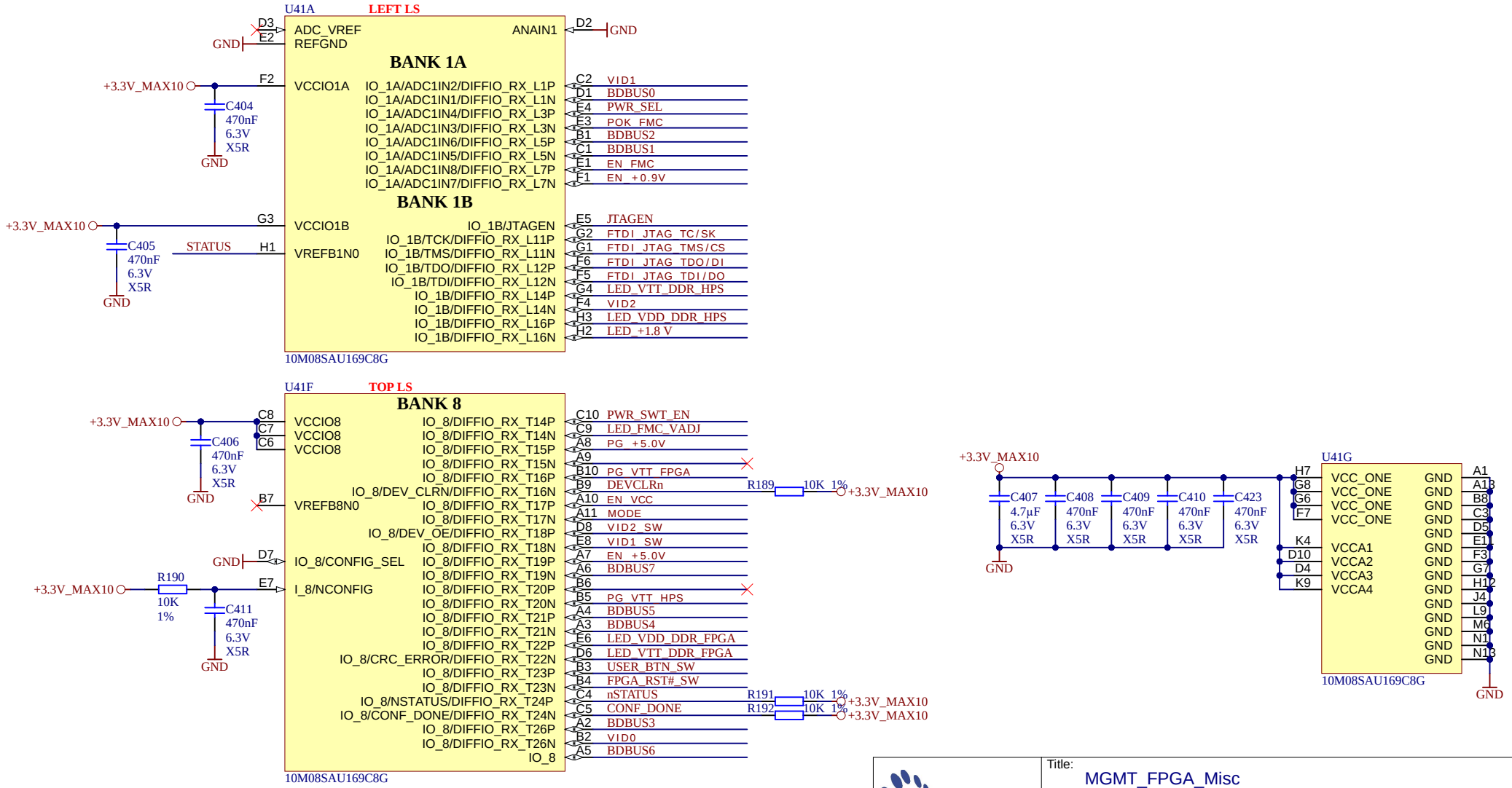
Drawn by: ED
Filename: MGMT_FPGA.SchDoc



Title: MGMT_FPGA_Misc			
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 4 of 34
Drawn by: ED	Filename: MGMT_FPGA_Misc.SchDoc		

FPGA_Bank_3A
FPGA_Bank_3A.SchDoc
FPGA_Bank_3B
FPGA_Bank_3B.SchDoc
FPGA_Bank_4A
FPGA_Bank_4A.SchDoc
FPGA_Bank_5
FPGA_Bank_5.SchDoc
FPGA_Bank_6A
FPGA_Bank_6A.SchDoc
FPGA_Bank_6B
FPGA_Bank_6B.SchDoc
FPGA_Bank_7A_7B
FPGA_Bank_7A_7B.SchDoc
FPGA_Bank_7C_7D.SchDoc
FPGA_Bank_7C_7D.SchDoc
FPGA_Bank_8_9
FPGA_Bank_8_9.SchDoc
FPGA_Power
FPGA_Power.SchDoc
FPGA_Decoupling
FPGA_Decoupling.SchDoc

Testpoints HPS IO

CPU_GPIO_0 — TP1 Testpoint 1mm
CPU_GPIO_1 — TP2 Testpoint 1mm

Testpoints I2C SDL/SCL

HPS_I2C_SDA — TP4 Testpoint 1mm
HPS_I2C_SCL — TP5 Testpoint 1mm
FMC_SDA — TP10 Testpoint 1mm
FMC_SCL — TP11 Testpoint 1mm

Testpoints FPGA IO

FPGA_TP_0 — TP6 Testpoint 1mm
FPGA_TP_1 — TP7 Testpoint 1mm
FPGA_TP_2 — TP12 Testpoint 1mm
FPGA_TP_3 — TP13 Testpoint 1mm
FPGA_TP_4 — TP14 Testpoint 1mm
FPGA_TP_5 — TP15 Testpoint 1mm

U6A
MT25QL256ABA8E12-1SIT
QSPI_CS/BOOTSEL1
QSPI_CLK
QSPI_DATA0
QSPI_DATA3
QSPI_DATA2
QSPI_DATA1
R18 R17 R16 R15 R20 10K
C29 470nF 6.3V X5R

U6B
MT25QL256ABA8E12-1SIT
R13 10K 1%

U15A
MT25QL256ABA8E12-1SIT
nCSO
AS_DCLK
AS_DATA0
AS_DATA3
AS_DATA2
AS_DATA1
R169 R170 R172 R173 R174 R171
C146 470nF 6.3V X5R

U15B
MT25QL256ABA8E12-1SIT
R141 10K 1%

U3
SI5338A-B-GM-TEI0022-Standard
L1 BLM15PX121SN1D 2A
C412 C438 C397 C398 C399 C396 470nF 6.3V X5R
C35 100nF 25V X5R
R264 49R9
C426 100nF 25V X5R
SMA_CLK_IN
SMA_CLK_OUT_p
SMA_CLK_OUT_n
CLK_B3B_p
CLK_B3B_n
CLK_MAX10
HPS_CLK2
CLK_B4A_p
CLK_B4A_n
HPS_I2C_SCL
HPS_I2C_SDA
R193 100R 1%
R265 100R 1%
D100

L9 BLM15PX121SN1D 2A
U48 SiT8208AI-G1-33S-25.000000Y
C439 470nF 6.3V X5R
CLK_25MHz
CLK_25MHz_R
HPS_CLK1_25MHz
ETH_XTAL_IN
R180 R229 R248 33R

I2C addr: 0x70

ATS-FPX040040035-66-C2-R0
J14
MECH1
ATS-HK127-R0

U38
24AA025E48T-I/OT
C287 470nF 6.3V X5R
I2C Slave ADDR: 0x50

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Title: FPGA			
A4	Number: TEI0022.PrjPCB Default		Rev. 03
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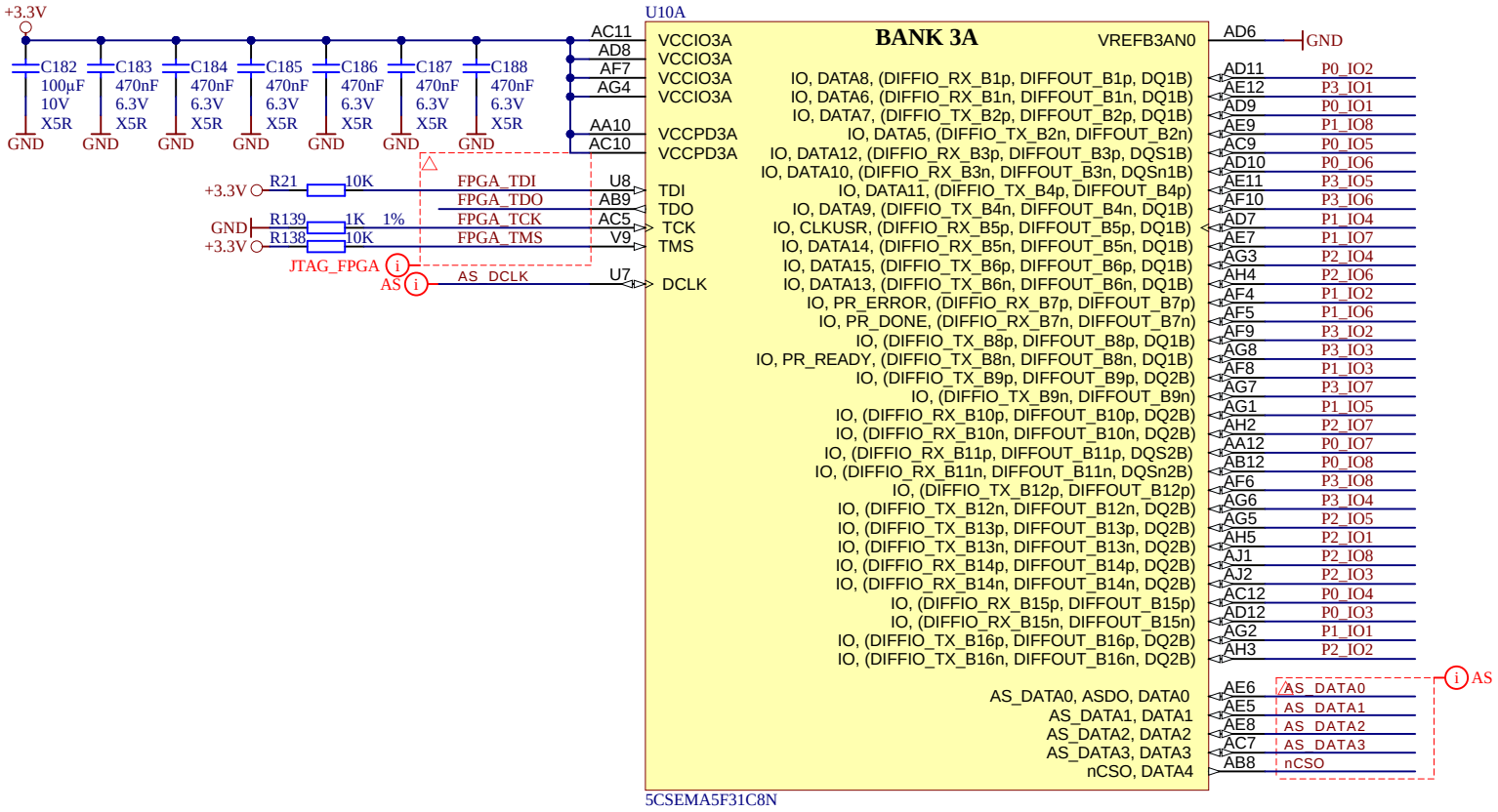
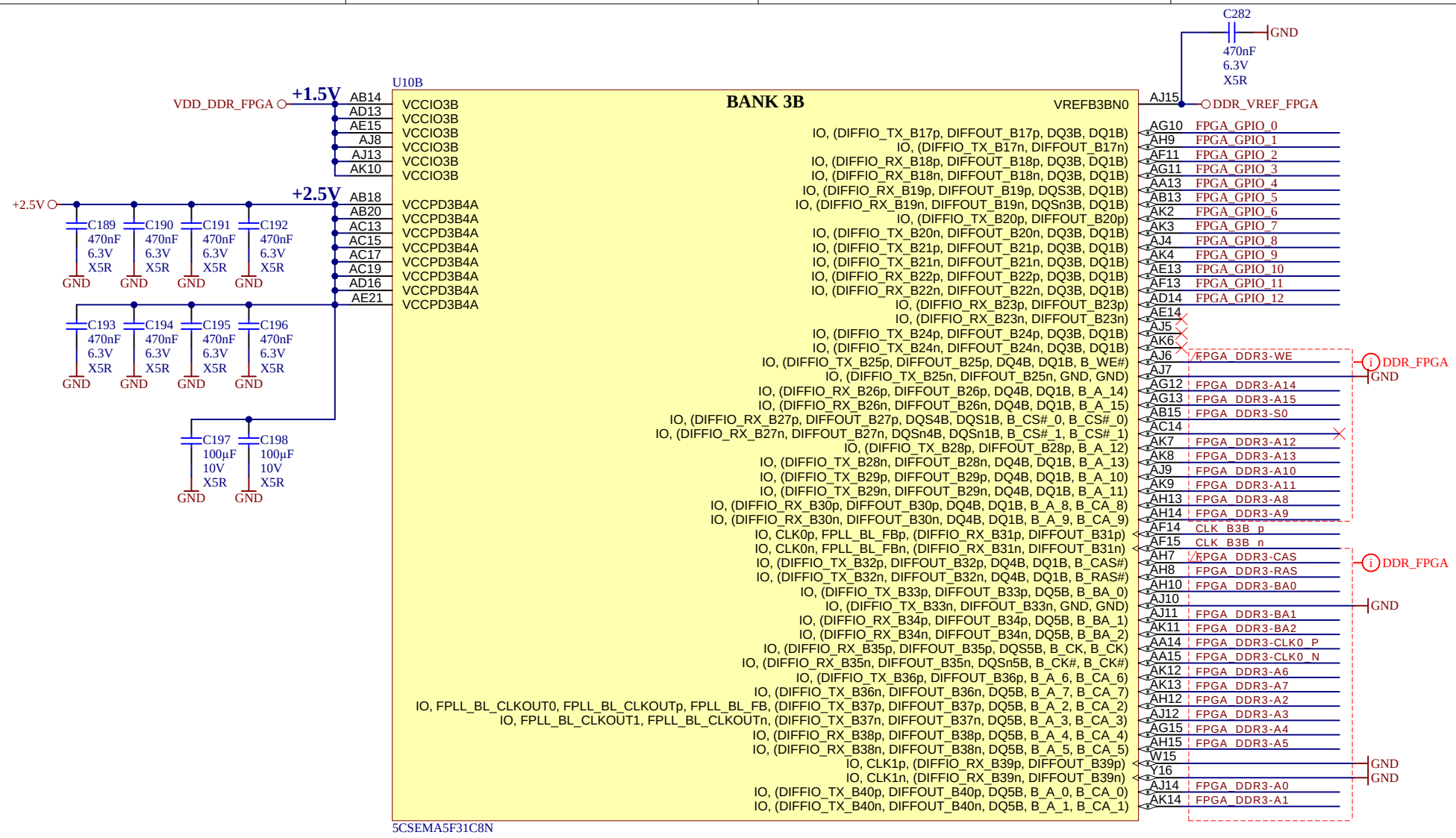


trenz electronic	Title: FPGA_Bank_3A		
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 6 of 34
Drawn by: ED	Filename: FPGA_Bank_3A.SchDoc		



Title: FPGA_Bank_3B			
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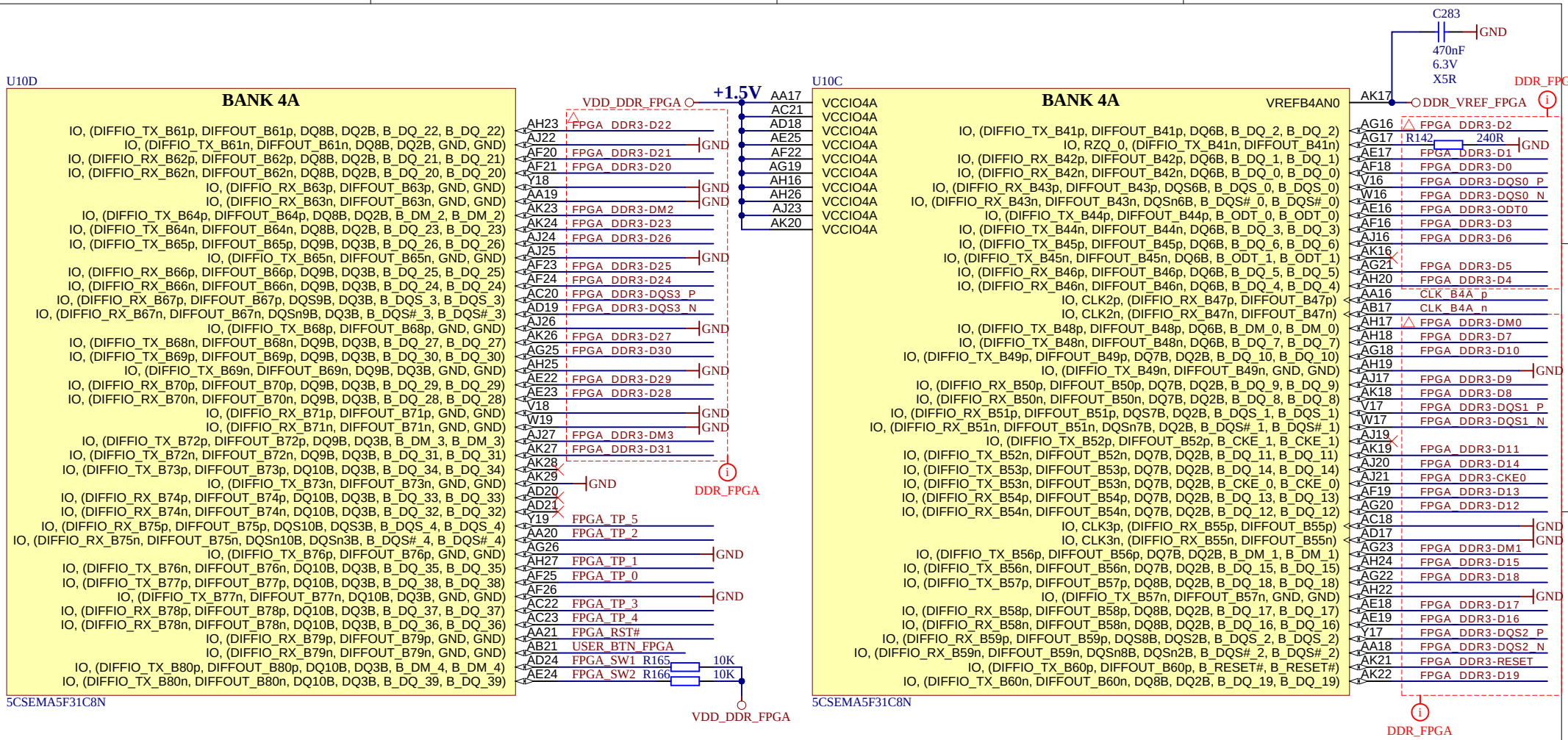
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 7 of 34
Drawn by: ED	Filename: FPGA_Bank_3B.SchDoc		



Title: FPGA_Bank_4A			
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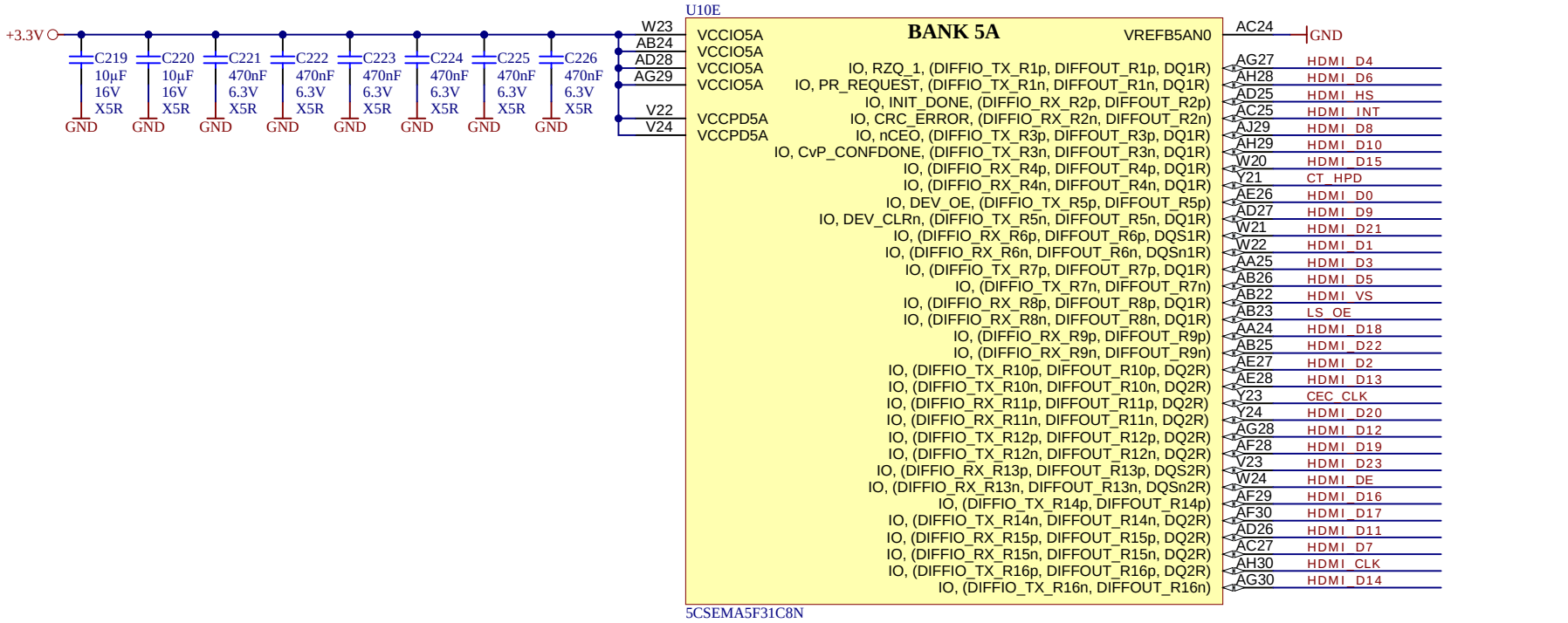
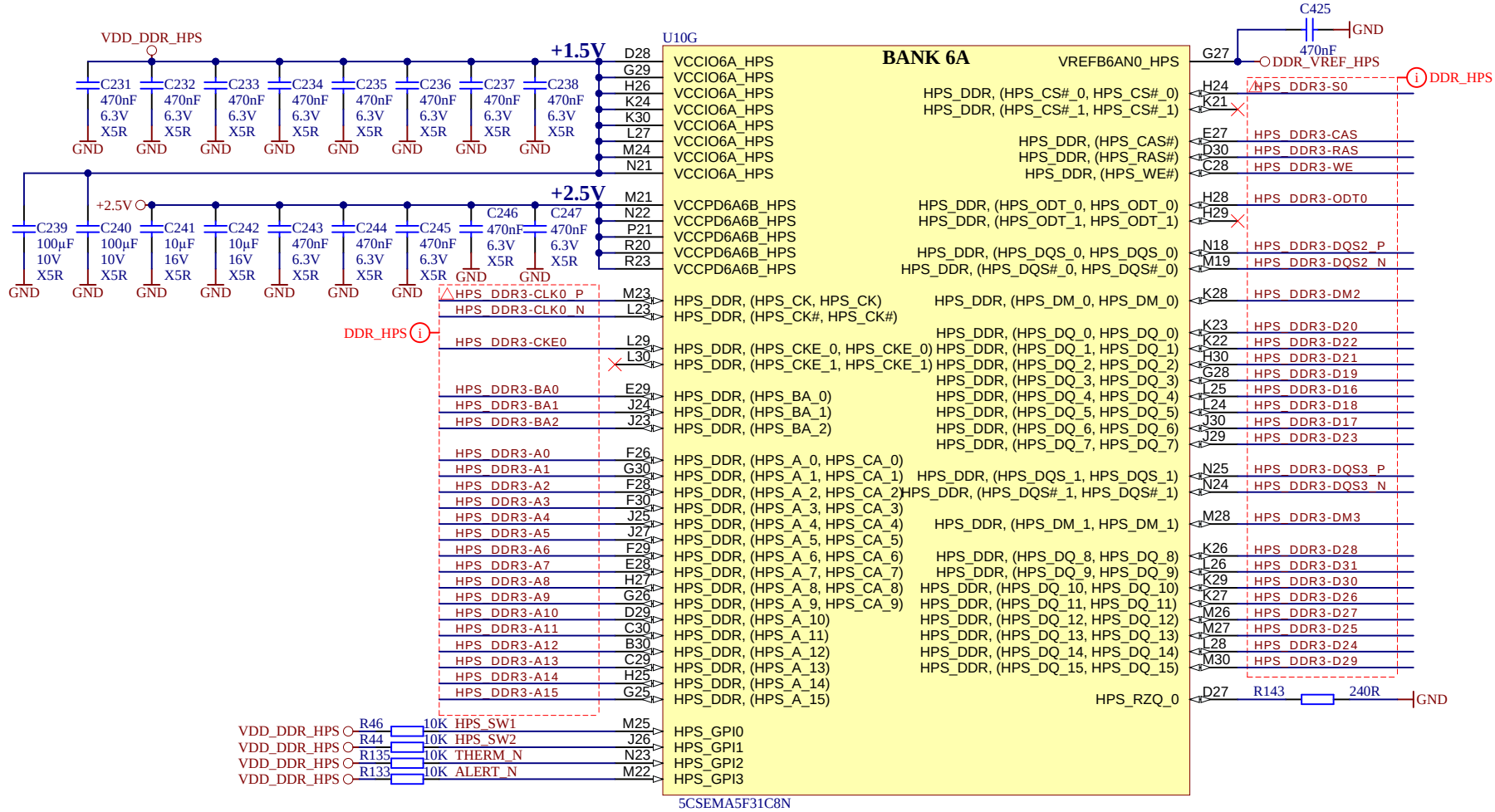
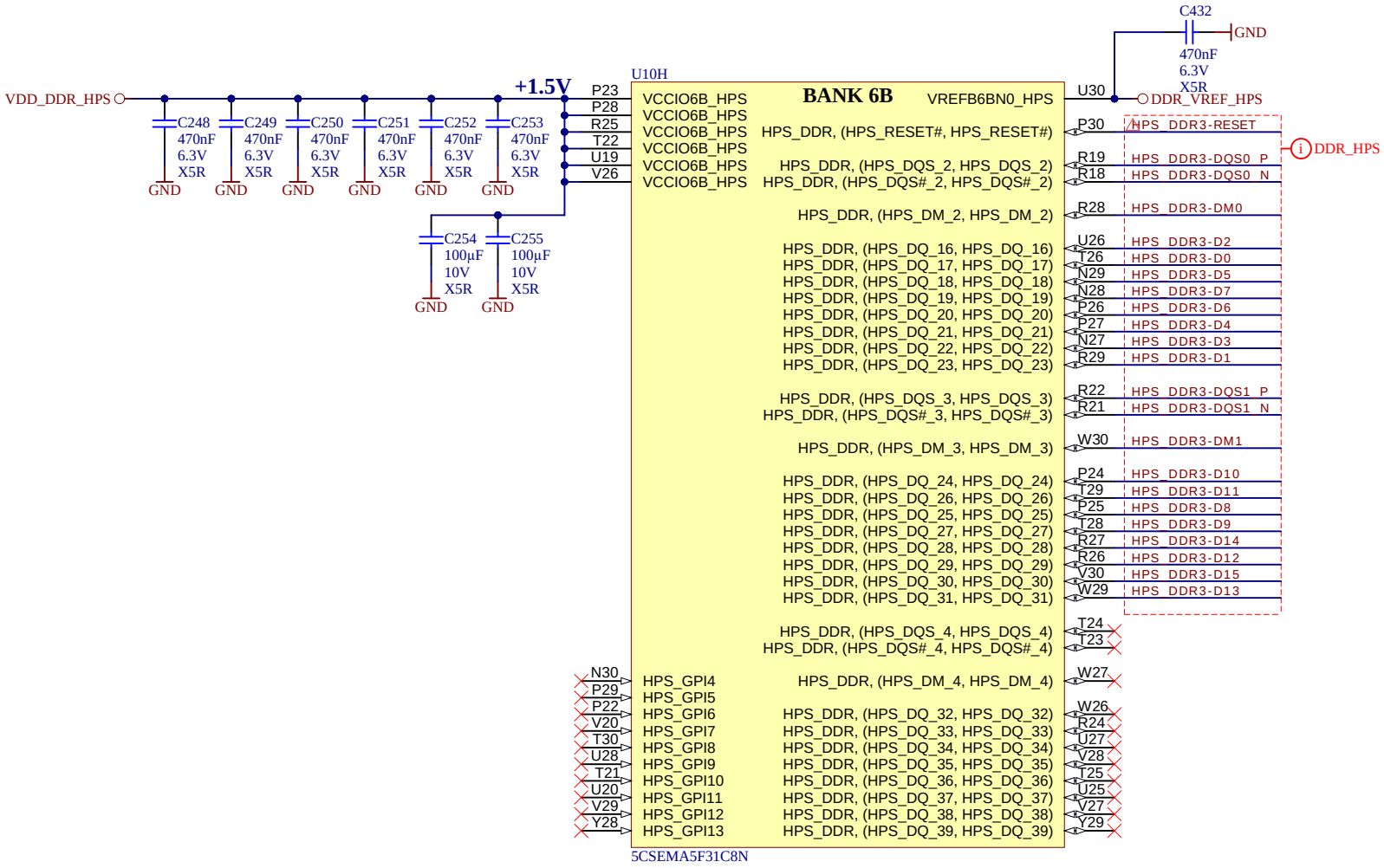
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 8 of 34
Drawn by: ED	Filename: FPGA_Bank_4A.SchDoc		



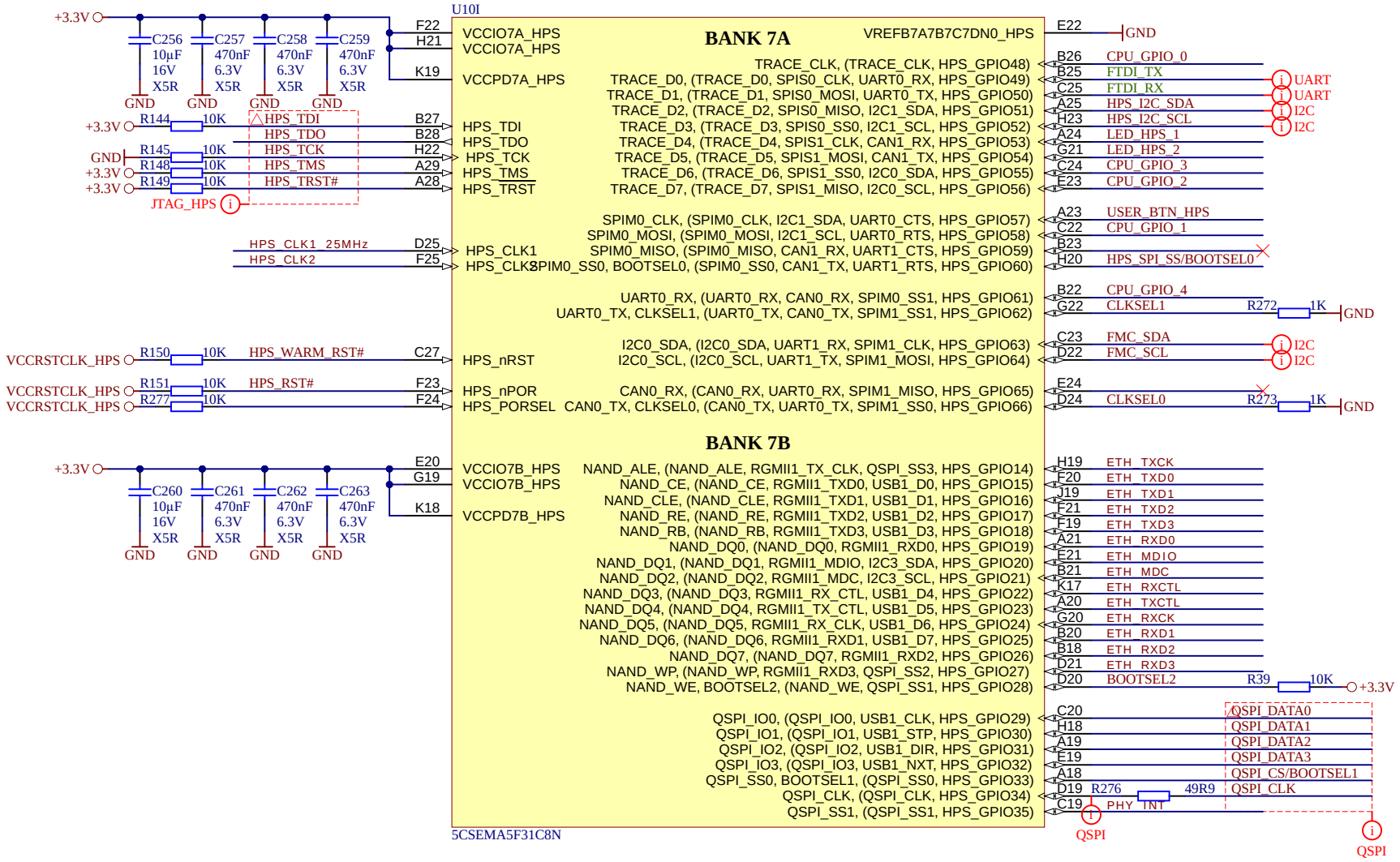
trenz electronic	Title: FPGA_Bank_5		
	A4	Number: TEI0022.PrjPCB Default	Rev. 03
	Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 9 of 34
	Drawn by: ED	Filename: FPGA_Bank_5.SchDoc	



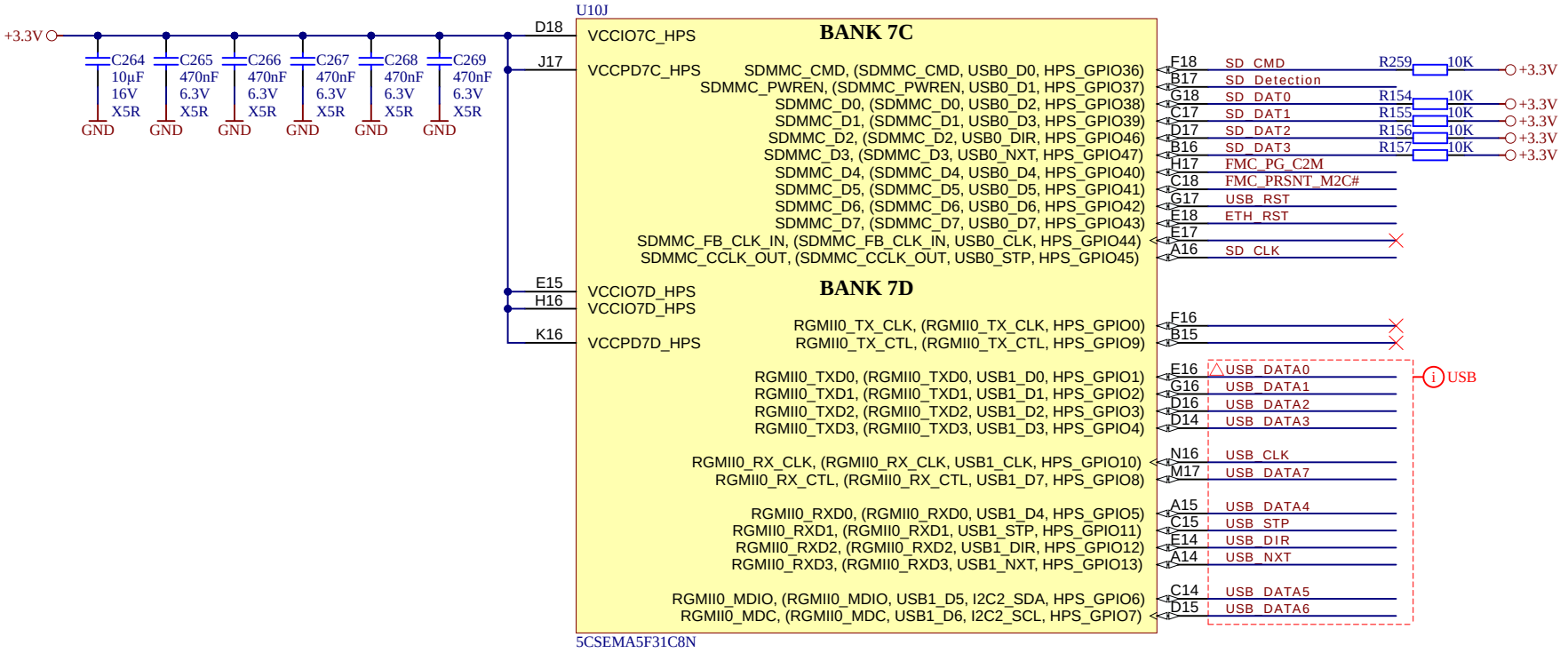
trenz electronic	Title: FPGA_Bank_6A		
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 10 of 34
Drawn by: ED	Filename: FPGA_Bank_6A.SchDoc		



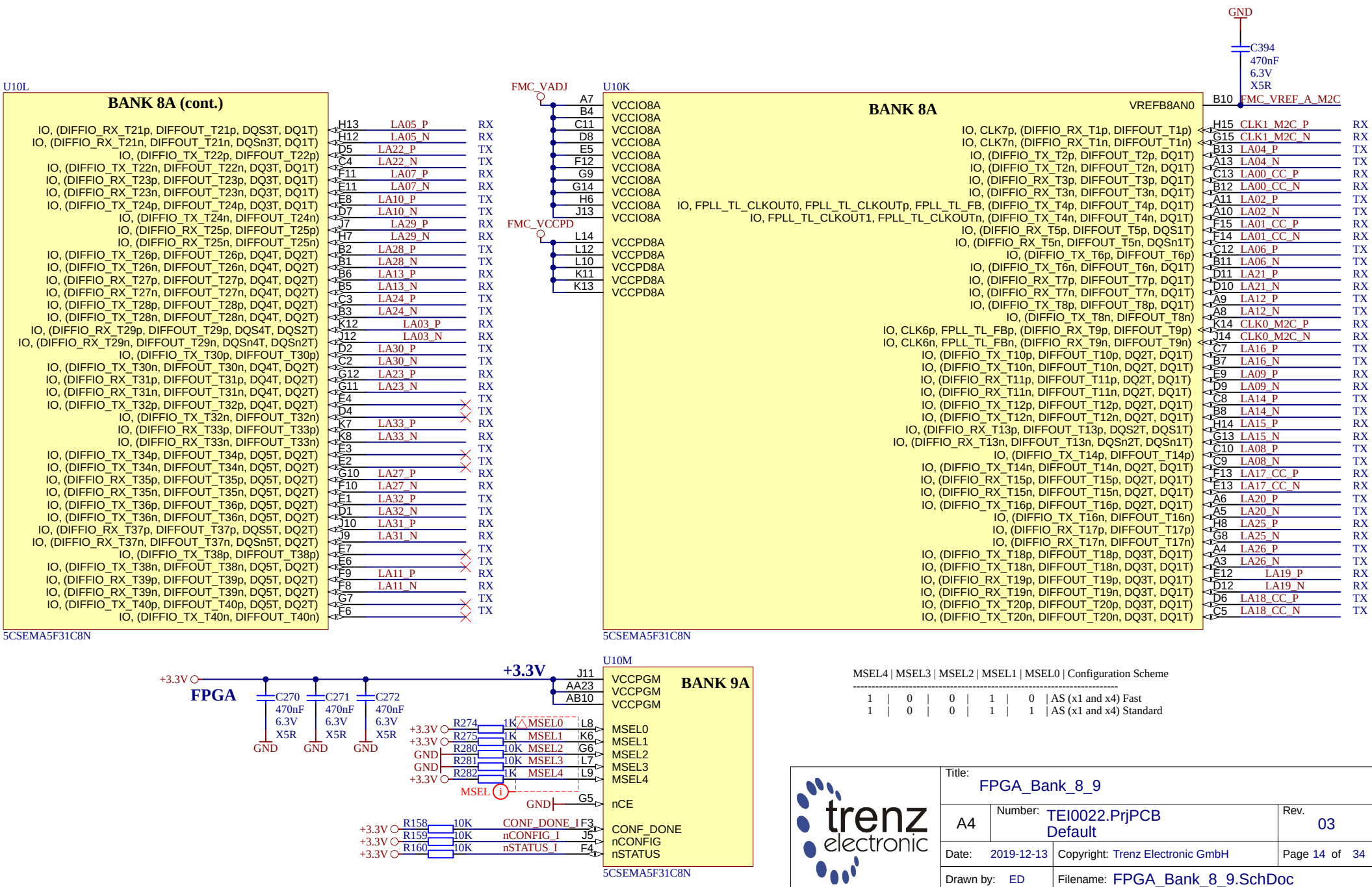
trenz electronic	Title: FPGA_Bank_6B		
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 11 of 34
Drawn by: ED	Filename: FPGA_Bank_6B.SchDoc		



trenz electronic	Title: FPGA_Bank_7A_7B		
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 12 of 34
Drawn by: ED	Filename: FPGA_Bank_7A_7B.SchDoc		



trenz electronic	Title: FPGA_Bank_7C_7D		
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 13 of 34
Drawn by: ED	Filename: FPGA_Bank_7C_7D.SchDoc		


U10L
BANK 8A (cont.)
IO, (DIFFIO_RX_T21p, DIFFOUT_T21p, DQS3T, DQ1T) H13 LA05_P RX
IO, (DIFFIO_RX_T21n, DIFFOUT_T21n, DQSn3T, DQ1T) H12 LA05_N RX
IO, (DIFFIO_TX_T22p, DIFFOUT_T22p) D5 LA22_P TX
IO, (DIFFIO_TX_T22n, DIFFOUT_T22n, DQ3T, DQ1T) C4 LA22_N TX
IO, (DIFFIO_RX_T23p, DIFFOUT_T23p, DQ3T, DQ1T) F11 LA07_P RX
IO, (DIFFIO_RX_T23n, DIFFOUT_T23n, DQ3T, DQ1T) E11 LA07_N RX
IO, (DIFFIO_TX_T24p, DIFFOUT_T24p, DQ3T, DQ1T) E8 LA10_P TX
IO, (DIFFIO_TX_T24n, DIFFOUT_T24n) D7 LA10_N TX
IO, (DIFFIO_RX_T25p, DIFFOUT_T25p) J7 LA29_P RX
IO, (DIFFIO_RX_T25n, DIFFOUT_T25n) H7 LA29_N RX
IO, (DIFFIO_TX_T26p, DIFFOUT_T26p, DQ4T, DQ2T) B2 LA28_P TX
IO, (DIFFIO_TX_T26n, DIFFOUT_T26n, DQ4T, DQ2T) B1 LA28_N TX
IO, (DIFFIO_RX_T27p, DIFFOUT_T27p, DQ4T, DQ2T) B6 LA13_P RX
IO, (DIFFIO_RX_T27n, DIFFOUT_T27n, DQ4T, DQ2T) B5 LA13_N RX
IO, (DIFFIO_TX_T28p, DIFFOUT_T28p, DQ4T, DQ2T) C3 LA24_P TX
IO, (DIFFIO_TX_T28n, DIFFOUT_T28n, DQ4T, DQ2T) B3 LA24_N TX
IO, (DIFFIO_RX_T29p, DIFFOUT_T29p, DQS4T, DQS2T) K12 LA03_P RX
IO, (DIFFIO_RX_T29n, DIFFOUT_T29n, DQSn4T, DQSn2T) J12 LA03_N RX
IO, (DIFFIO_TX_T30p, DIFFOUT_T30p) D2 LA30_P TX
IO, (DIFFIO_TX_T30n, DIFFOUT_T30n, DQ4T, DQ2T) C2 LA30_N TX
IO, (DIFFIO_RX_T31p, DIFFOUT_T31p, DQ4T, DQ2T) G12 LA23_P RX
IO, (DIFFIO_RX_T31n, DIFFOUT_T31n, DQ4T, DQ2T) G11 LA23_N RX
IO, (DIFFIO_TX_T32p, DIFFOUT_T32p, DQ4T, DQ2T) E4 TX
IO, (DIFFIO_TX_T32n, DIFFOUT_T32n) D4 TX
IO, (DIFFIO_RX_T33p, DIFFOUT_T33p) K7 LA33_P RX
IO, (DIFFIO_RX_T33n, DIFFOUT_T33n) K8 LA33_N RX
IO, (DIFFIO_TX_T34p, DIFFOUT_T34p, DQ5T, DQ2T) E3 TX
IO, (DIFFIO_TX_T34n, DIFFOUT_T34n, DQ5T, DQ2T) E2 TX
IO, (DIFFIO_TX_T35p, DIFFOUT_T35p, DQ5T, DQ2T) G10 LA27_P RX
IO, (DIFFIO_TX_T35n, DIFFOUT_T35n, DQ5T, DQ2T) F10 LA27_N RX
IO, (DIFFIO_TX_T36p, DIFFOUT_T36p, DQ5T, DQ2T) E1 LA32_P TX
IO, (DIFFIO_TX_T36n, DIFFOUT_T36n, DQ5T, DQ2T) D1 LA32_N TX
IO, (DIFFIO_RX_T37p, DIFFOUT_T37p, DQS5T, DQ2T) J10 LA31_P RX
IO, (DIFFIO_RX_T37n, DIFFOUT_T37n, DQSn5T, DQ2T) J9 LA31_N RX
IO, (DIFFIO_TX_T38p, DIFFOUT_T38p) E7 TX
IO, (DIFFIO_TX_T38n, DIFFOUT_T38n, DQ5T, DQ2T) E6 TX
IO, (DIFFIO_RX_T39p, DIFFOUT_T39p, DQ5T, DQ2T) F9 LA11_P RX
IO, (DIFFIO_RX_T39n, DIFFOUT_T39n, DQ5T, DQ2T) F8 LA11_N RX
IO, (DIFFIO_TX_T40p, DIFFOUT_T40p, DQ5T, DQ2T) G7 TX
IO, (DIFFIO_TX_T40n, DIFFOUT_T40n) F6 TX
5CSEMA5F31C8N
FMC_VADJ
A7 B4 C11 D8 E5 F12 G9 G14 H6 J13
VCCIO8A
FMC_VCCPD
L14 L12 L10 K11 K13
VCCPD8A
U10K
BANK 8A
VREFB8AN0 B10 FMC_VREF_A_M2C
IO, CLK7p, (DIFFIO_RX_T1p, DIFFOUT_T1p) H15 CLK1_M2C_P RX
IO, CLK7n, (DIFFIO_RX_T1n, DIFFOUT_T1n) G15 CLK1_M2C_N RX
IO, (DIFFIO_TX_T2p, DIFFOUT_T2p, DQ1T) B13 LA04_P TX
IO, (DIFFIO_TX_T2n, DIFFOUT_T2n, DQ1T) A13 LA04_N TX
IO, (DIFFIO_RX_T3p, DIFFOUT_T3p, DQ1T) C13 LA00_CC_P RX
IO, (DIFFIO_RX_T3n, DIFFOUT_T3n, DQ1T) B12 LA00_CC_N RX
IO, FPLL_TL_CLKOUT0, FPLL_TL_CLKOUTp, FPLL_TL_FB, (DIFFIO_TX_T4p, DIFFOUT_T4p, DQ1T) A11 LA02_P TX
IO, FPLL_TL_CLKOUT1, FPLL_TL_CLKOUTn, (DIFFIO_TX_T4n, DIFFOUT_T4n, DQ1T) A10 LA02_N TX
IO, (DIFFIO_RX_T5p, DIFFOUT_T5p, DQS1T) F15 LA01_CC_P RX
IO, (DIFFIO_RX_T5n, DIFFOUT_T5n, DQSn1T) F14 LA01_CC_N RX
IO, (DIFFIO_TX_T6p, DIFFOUT_T6p) C12 LA06_P TX
IO, (DIFFIO_TX_T6n, DIFFOUT_T6n, DQ1T) B11 LA06_N TX
IO, (DIFFIO_RX_T7p, DIFFOUT_T7p, DQ1T) D11 LA21_P RX
IO, (DIFFIO_RX_T7n, DIFFOUT_T7n, DQ1T) D10 LA21_N RX
IO, (DIFFIO_TX_T8p, DIFFOUT_T8p, DQ1T) A9 LA12_P TX
IO, (DIFFIO_TX_T8n, DIFFOUT_T8n) A8 LA12_N TX
IO, CLK6p, FPLL_TL_FBp, (DIFFIO_RX_T9p, DIFFOUT_T9p) K14 CLK0_M2C_P RX
IO, CLK6n, FPLL_TL_FBn, (DIFFIO_RX_T9n, DIFFOUT_T9n) J14 CLK0_M2C_N RX
IO, (DIFFIO_TX_T10p, DIFFOUT_T10p, DQ2T, DQ1T) C7 LA16_P TX
IO, (DIFFIO_TX_T10n, DIFFOUT_T10n, DQ2T, DQ1T) B7 LA16_N TX
IO, (DIFFIO_RX_T11p, DIFFOUT_T11p, DQ2T, DQ1T) E9 LA09_P RX
IO, (DIFFIO_RX_T11n, DIFFOUT_T11n, DQ2T, DQ1T) D9 LA09_N RX
IO, (DIFFIO_TX_T12p, DIFFOUT_T12p, DQ2T, DQ1T) C8 LA14_P TX
IO, (DIFFIO_TX_T12n, DIFFOUT_T12n, DQ2T, DQ1T) B8 LA14_N TX
IO, (DIFFIO_RX_T13p, DIFFOUT_T13p, DQS2T, DQS1T) H14 LA15_P RX
IO, (DIFFIO_RX_T13n, DIFFOUT_T13n, DQSn2T, DQSn1T) G13 LA15_N RX
IO, (DIFFIO_TX_T14p, DIFFOUT_T14p) C10 LA08_P TX
IO, (DIFFIO_TX_T14n, DIFFOUT_T14n, DQ2T, DQ1T) C9 LA08_N TX
IO, (DIFFIO_RX_T15p, DIFFOUT_T15p, DQ2T, DQ1T) F13 LA17_CC_P RX
IO, (DIFFIO_RX_T15n, DIFFOUT_T15n, DQ2T, DQ1T) E13 LA17_CC_N RX
IO, (DIFFIO_TX_T16p, DIFFOUT_T16p, DQ2T, DQ1T) A6 LA20_P TX
IO, (DIFFIO_TX_T16n, DIFFOUT_T16n) A5 LA20_N TX
IO, (DIFFIO_RX_T17p, DIFFOUT_T17p) H8 LA25_P RX
IO, (DIFFIO_RX_T17n, DIFFOUT_T17n) G8 LA25_N RX
IO, (DIFFIO_TX_T18p, DIFFOUT_T18p, DQ3T, DQ1T) A4 LA26_P TX
IO, (DIFFIO_TX_T18n, DIFFOUT_T18n, DQ3T, DQ1T) A3 LA26_N TX
IO, (DIFFIO_RX_T19p, DIFFOUT_T19p, DQ3T, DQ1T) E12 LA19_P RX
IO, (DIFFIO_RX_T19n, DIFFOUT_T19n, DQ3T, DQ1T) D12 LA19_N RX
IO, (DIFFIO_TX_T20p, DIFFOUT_T20p, DQ3T, DQ1T) D6 LA18_CC_P TX
IO, (DIFFIO_TX_T20n, DIFFOUT_T20n, DQ3T, DQ1T) C5 LA18_CC_N TX
5CSEMA5F31C8N
GND
C394 470nF 6.3V X5R
+3.3V
FPGA
C270 470nF 6.3V X5R
C271 470nF 6.3V X5R
C272 470nF 6.3V X5R
GND
U10M
BANK 9A
J11 AA23 AB10
VCCPGM
R274 1K MSEL0 L8
R275 1K MSEL1 K6
R280 10K MSEL2 G6
R281 10K MSEL3 L7
R282 1K MSEL4 L9
MSEL0 MSEL1 MSEL2 MSEL3 MSEL4
MSEL
G5
nCE
R158 10K CONF_DONE_I F3
R159 10K nCONFIG_I J5
R160 10K nSTATUS_I F4
CONF_DONE nCONFIG nSTATUS
5CSEMA5F31C8N
MSEL4 | MSEL3 | MSEL2 | MSEL1 | MSEL0 | Configuration Scheme
1 | 0 | 0 | 1 | 0 | AS (x1 and x4) Fast
1 | 0 | 0 | 1 | 1 | AS (x1 and x4) Standard
trenz electronic
Title: FPGA_Bank_8_9
A4
Number: TEI0022.PrjPCB Default
Rev. 03
Date: 2019-12-13
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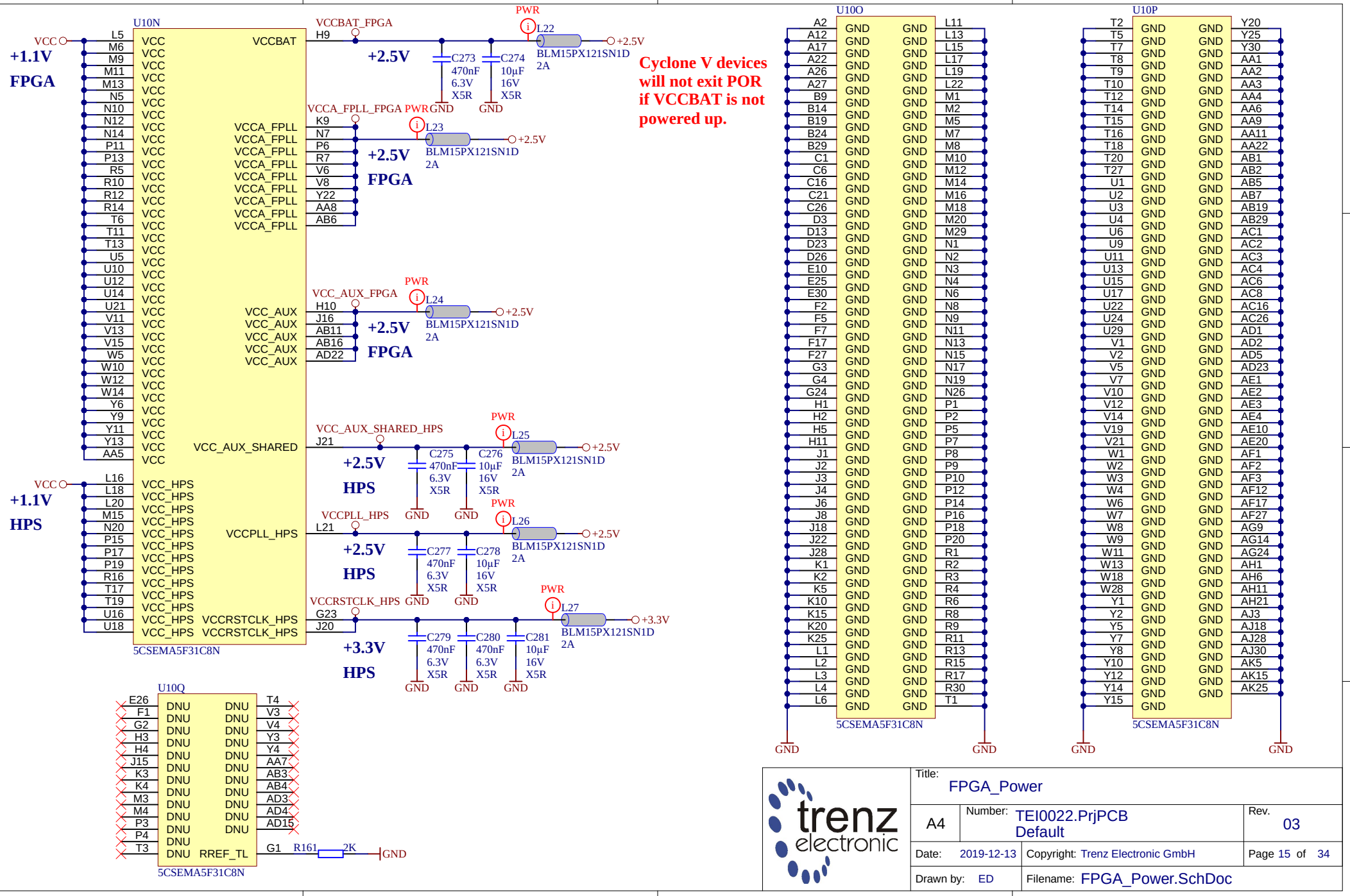
Drawn by: ED
Filename: FPGA_Bank_8_9.SchDoc


U10N
VCC
+1.1V
FPGA
VCCBAT
VCCBAT_FPGA
H9
PWR
L22
BLM15PX121SN1D
2A
+2.5V
C273
470nF
6.3V
X5R
C274
10µF
16V
X5R
GND
VCCA_FPLL
VCCA_FPLL_FPGA
K9
N7
P6
R7
V6
V8
Y22
AA8
AB6
L23
+2.5V
FPGA
VCC_AUX
VCC_AUX_FPGA
H10
J16
AB11
AB16
AD22
L24
VCC_AUX_SHARED
VCC_AUX_SHARED_HPS
J21
L25
C275
C276
+1.1V
HPS
VCC_HPS
VCCPLL_HPS
L21
L26
C277
C278
VCCRSTCLK_HPS
G23
J20
L27
+3.3V
C279
C280
C281
5CSEMA5F31C8N
U10Q
DNU
RREF_TL
G1
R161
2K
Cyclone V devices will not exit POR if VCCBAT is not powered up.
U10O
U10P
GND
trenz electronic
Title:
FPGA_Power
A4
Number:
TEI0022.PrjPCB
Default
Rev.
03
Date:
2019-12-13
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ED
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FPGA_Power.SchDoc

trenz electronic	Title: FPGA_Decoupling		
	A4	Number: TEI0022.PrjPCB Default	Rev. 03
	Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 16 of 34
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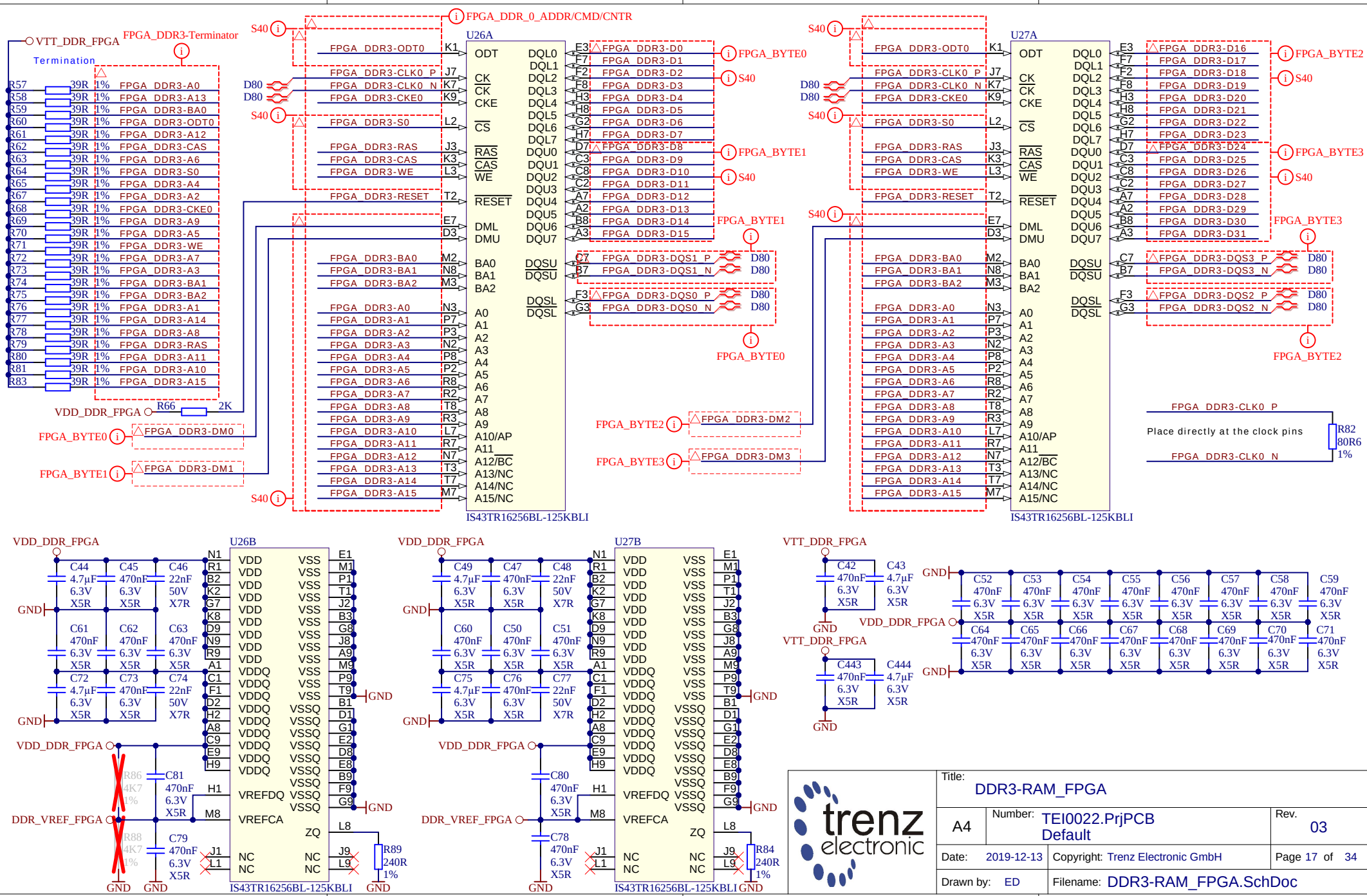
FPGA_DDR3-Terminator
VTT_DDR_FPGA
Termination
R57 39R 1% FPGA_DDR3-A0
R58 39R 1% FPGA_DDR3-A13
R59 39R 1% FPGA_DDR3-BA0
R60 39R 1% FPGA_DDR3-ODT0
R61 39R 1% FPGA_DDR3-A12
R62 39R 1% FPGA_DDR3-CAS
R63 39R 1% FPGA_DDR3-A6
R64 39R 1% FPGA_DDR3-S0
R65 39R 1% FPGA_DDR3-A4
R67 39R 1% FPGA_DDR3-A2
R68 39R 1% FPGA_DDR3-CKE0
R69 39R 1% FPGA_DDR3-A9
R70 39R 1% FPGA_DDR3-A5
R71 39R 1% FPGA_DDR3-WE
R72 39R 1% FPGA_DDR3-A7
R73 39R 1% FPGA_DDR3-A3
R74 39R 1% FPGA_DDR3-BA1
R75 39R 1% FPGA_DDR3-BA2
R76 39R 1% FPGA_DDR3-A1
R77 39R 1% FPGA_DDR3-A14
R78 39R 1% FPGA_DDR3-A8
R79 39R 1% FPGA_DDR3-RAS
R80 39R 1% FPGA_DDR3-A11
R81 39R 1% FPGA_DDR3-A10
R83 39R 1% FPGA_DDR3-A15
VDD_DDR_FPGA
R66 2K
FPGA_BYTE0
FPGA_DDR3-DM0
FPGA_BYTE1
FPGA_DDR3-DM1
FPGA_DDR_0_ADDR/CMD/CNTR
U26A
FPGA_DDR3-ODT0 K1 ODT
FPGA_DDR3-CLK0_P J7 CK
FPGA_DDR3-CLK0_N K7 CK
FPGA_DDR3-CKE0 K9 CKE
FPGA_DDR3-S0 L2 CS
FPGA_DDR3-RAS J3 RAS
FPGA_DDR3-CAS K3 CAS
FPGA_DDR3-WE L3 WE
FPGA_DDR3-RESET T2 RESET
E7 DML
D3 DMU
FPGA_DDR3-BA0 M2 BA0
FPGA_DDR3-BA1 N8 BA1
FPGA_DDR3-BA2 M3 BA2
FPGA_DDR3-A0 N3 A0
FPGA_DDR3-A1 P7 A1
FPGA_DDR3-A2 P3 A2
FPGA_DDR3-A3 N2 A3
FPGA_DDR3-A4 P8 A4
FPGA_DDR3-A5 P2 A5
FPGA_DDR3-A6 R8 A6
FPGA_DDR3-A7 R2 A7
FPGA_DDR3-A8 T8 A8
FPGA_DDR3-A9 R3 A9
FPGA_DDR3-A10 L7 A10/AP
FPGA_DDR3-A11 R7 A11
FPGA_DDR3-A12 N7 A12/BC
FPGA_DDR3-A13 T3 A13/NC
FPGA_DDR3-A14 T7 A14/NC
FPGA_DDR3-A15 M7 A15/NC
DQL0 E3 FPGA_DDR3-D0
DQL1 F7 FPGA_DDR3-D1
DQL2 F2 FPGA_DDR3-D2
DQL3 F8 FPGA_DDR3-D3
DQL4 H3 FPGA_DDR3-D4
DQL5 H8 FPGA_DDR3-D5
DQL6 G2 FPGA_DDR3-D6
DQL7 H7 FPGA_DDR3-D7
DQU0 D7 FPGA_DDR3-D8
DQU1 C3 FPGA_DDR3-D9
DQU2 C8 FPGA_DDR3-D10
DQU3 C2 FPGA_DDR3-D11
DQU4 A7 FPGA_DDR3-D12
DQU5 A2 FPGA_DDR3-D13
DQU6 B8 FPGA_DDR3-D14
DQU7 A3 FPGA_DDR3-D15
DQSU C7 FPGA_DDR3-DQS1_P
DQSU B7 FPGA_DDR3-DQS1_N
DQSL F3 FPGA_DDR3-DQS0_P
DQSL G3 FPGA_DDR3-DQS0_N
IS43TR16256BL-125KBLI
FPGA_BYTE0
FPGA_BYTE1
FPGA_BYTE2
FPGA_BYTE3
S40
D80
U27A
FPGA_DDR3-D16
FPGA_DDR3-D17
FPGA_DDR3-D18
FPGA_DDR3-D19
FPGA_DDR3-D20
FPGA_DDR3-D21
FPGA_DDR3-D22
FPGA_DDR3-D23
FPGA_DDR3-D24
FPGA_DDR3-D25
FPGA_DDR3-D26
FPGA_DDR3-D27
FPGA_DDR3-D28
FPGA_DDR3-D29
FPGA_DDR3-D30
FPGA_DDR3-D31
FPGA_DDR3-DQS3_P
FPGA_DDR3-DQS3_N
FPGA_DDR3-DQS2_P
FPGA_DDR3-DQS2_N
FPGA_DDR3-DM2
FPGA_DDR3-DM3
FPGA_DDR3-CLK0_P
Place directly at the clock pins
FPGA_DDR3-CLK0_N
R82 80R6 1%
U26B
U27B
VDD_DDR_FPGA
GND
C44 4.7µF 6.3V X5R
C45 470nF 6.3V X5R
C46 22nF 50V X7R
C61 470nF 6.3V X5R
C62 470nF 6.3V X5R
C63 470nF 6.3V X5R
C72 4.7µF 6.3V X5R
C73 470nF 6.3V X5R
C74 22nF 50V X7R
C49 4.7µF 6.3V X5R
C47 470nF 6.3V X5R
C48 22nF 50V X7R
C60 470nF 6.3V X5R
C50 470nF 6.3V X5R
C51 470nF 6.3V X5R
C75 4.7µF 6.3V X5R
C76 470nF 6.3V X5R
C77 22nF 50V X7R
VTT_DDR_FPGA
C42 470nF 6.3V X5R
C43 4.7µF 6.3V X5R
C52 470nF 6.3V X5R
C53 470nF 6.3V X5R
C54 470nF 6.3V X5R
C55 470nF 6.3V X5R
C56 470nF 6.3V X5R
C57 470nF 6.3V X5R
C58 470nF 6.3V X5R
C59 470nF 6.3V X5R
C64 470nF 6.3V X5R
C65 470nF 6.3V X5R
C66 470nF 6.3V X5R
C67 470nF 6.3V X5R
C68 470nF 6.3V X5R
C69 470nF 6.3V X5R
C70 470nF 6.3V X5R
C71 470nF 6.3V X5R
C443 470nF 6.3V X5R
C444 4.7µF 6.3V X5R
R86 4K7 1%
R88 4K7 1%
C81 470nF 6.3V X5R
C79 470nF 6.3V X5R
C80 470nF 6.3V X5R
C78 470nF 6.3V X5R
DDR_VREF_FPGA
R89 240R 1%
R84 240R 1%
trenz electronic
Title: DDR3-RAM_FPGA
A4
Number: TEI0022.PrjPCB Default
Rev. 03
Date: 2019-12-13
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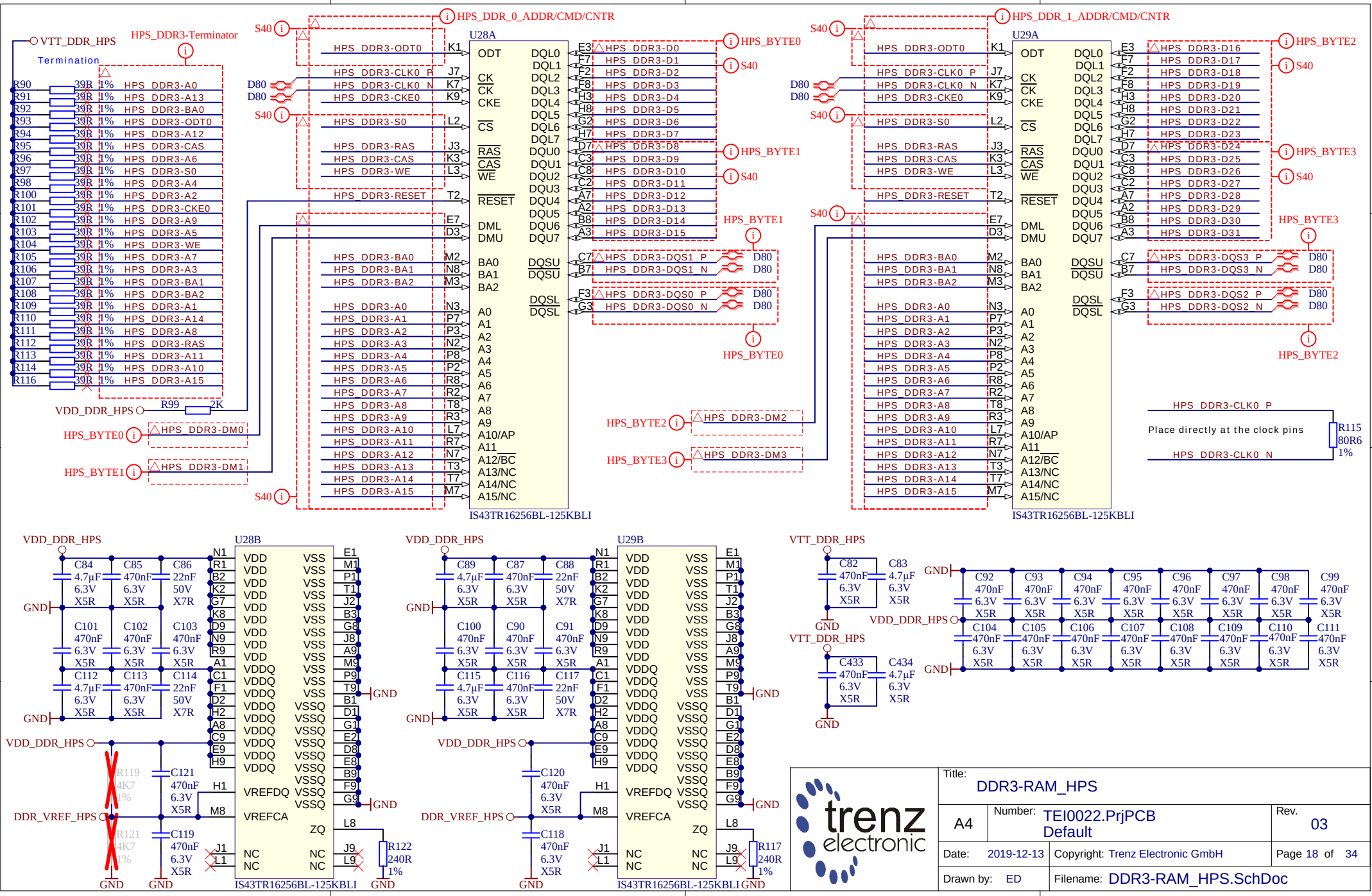
Filename: DDR3-RAM_FPGA.SchDoc


HPS_DDR_0_ADDR/CMD/CNTR
HPS_DDR_1_ADDR/CMD/CNTR
VTT_DDR_HPS
HPS_DDR3-Terminator
Termination
VDD_DDR_HPS
HPS_BYTE0
HPS_BYTE1
HPS_BYTE2
HPS_BYTE3
U28A
U29A
U28B
U29B
IS43TR16256BL-125KBLI
HPS_DDR3-DM0
HPS_DDR3-DM1
HPS_DDR3-DM2
HPS_DDR3-DM3
HPS_DDR3-RESET
DDR_VREF_HPS
HPS_DDR3-CLK0_P
HPS_DDR3-CLK0_N
Place directly at the clock pins
R115
80R6
1%
GND
Title: DDR3-RAM_HPS
A4
Number: TEI0022.PrjPCB Default
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Date: 2019-12-13
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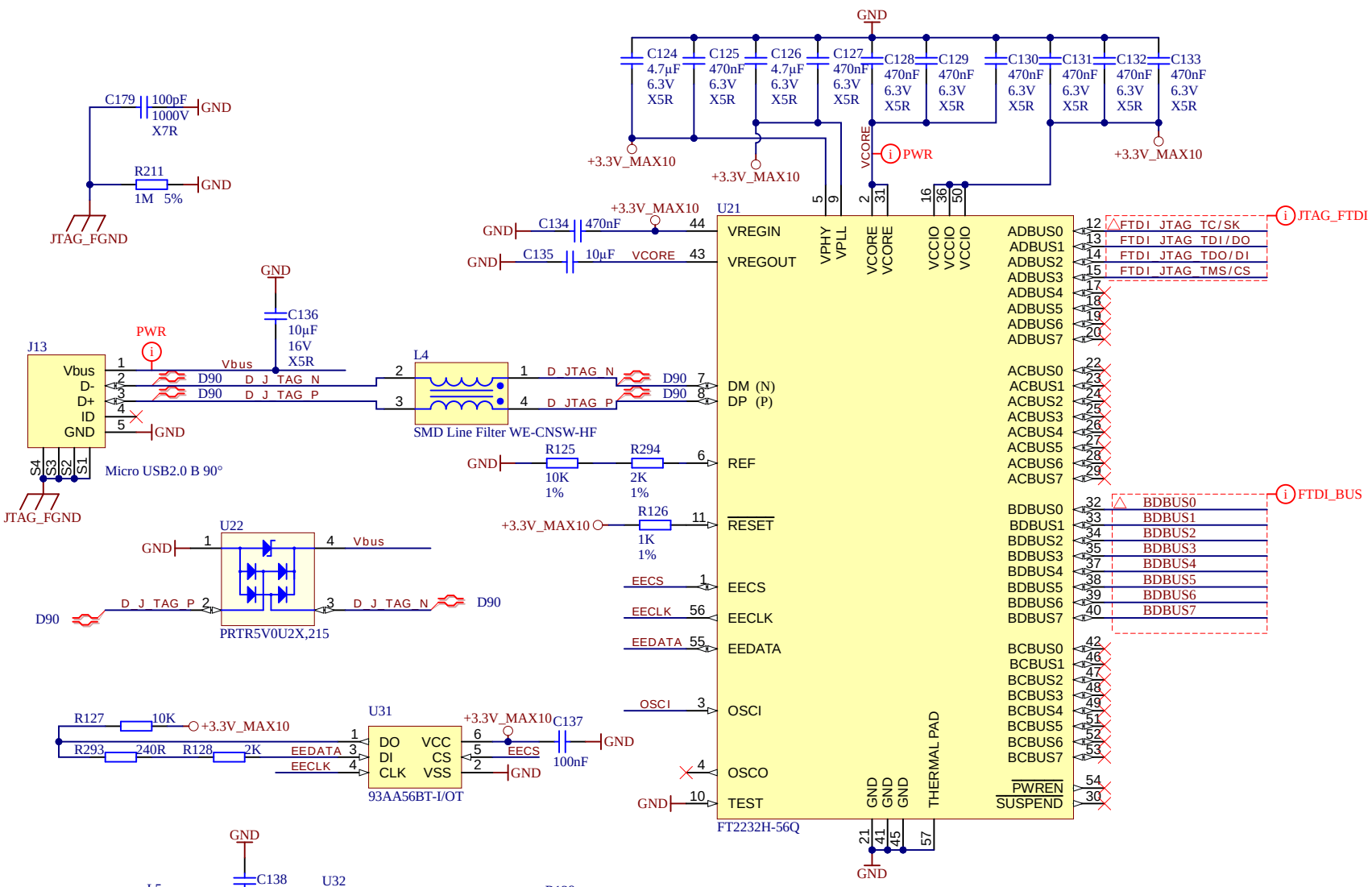

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	Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 19 of 34
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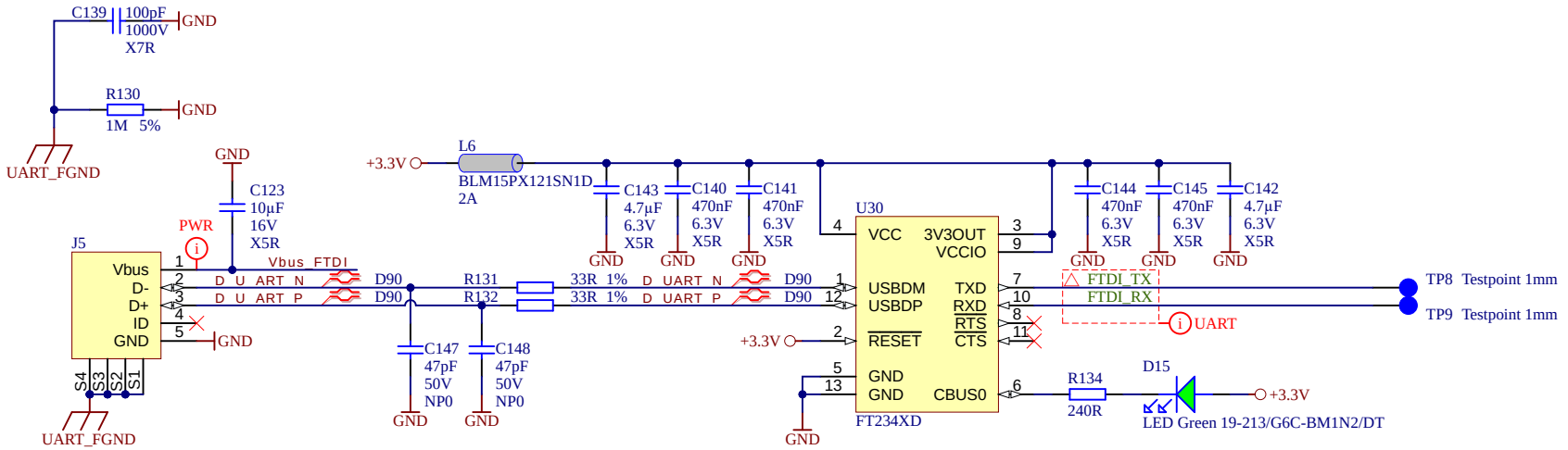
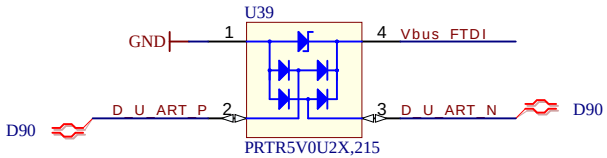
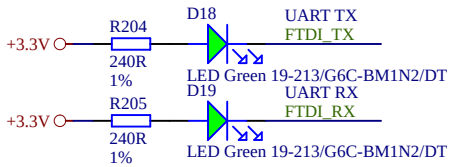
USB/UART Bridge

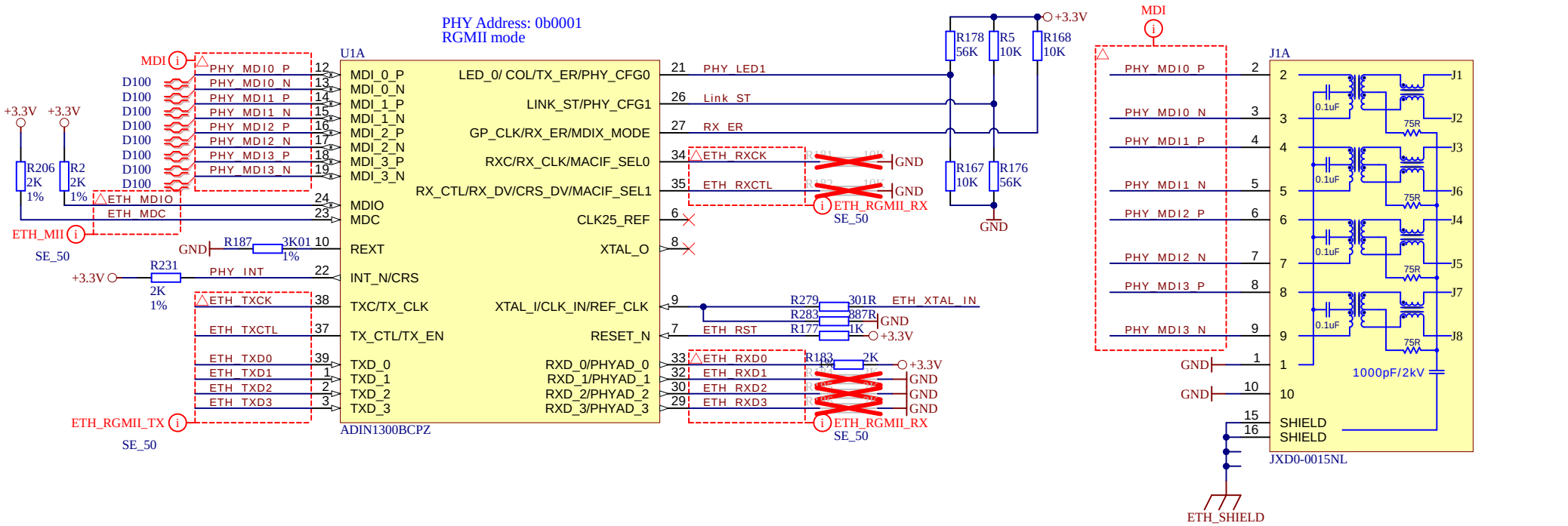


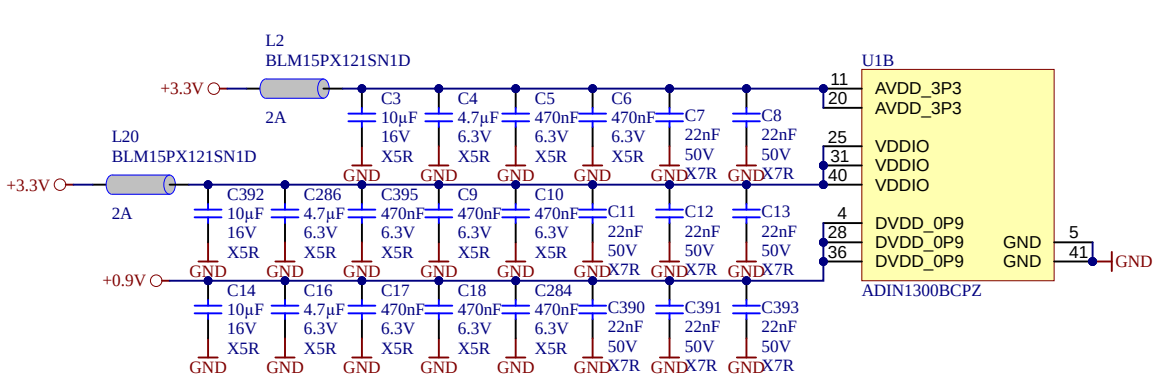
Micro USB2.0 B 90°

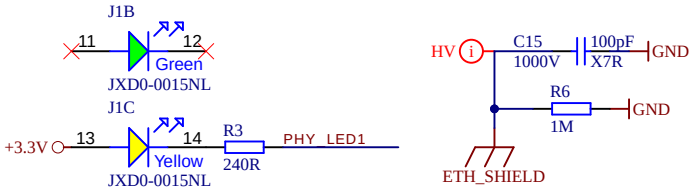




trenz electronic	Title: FTDI_UART		
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 20 of 34
Drawn by: ED	Filename: FTDI_UART.SchDoc		

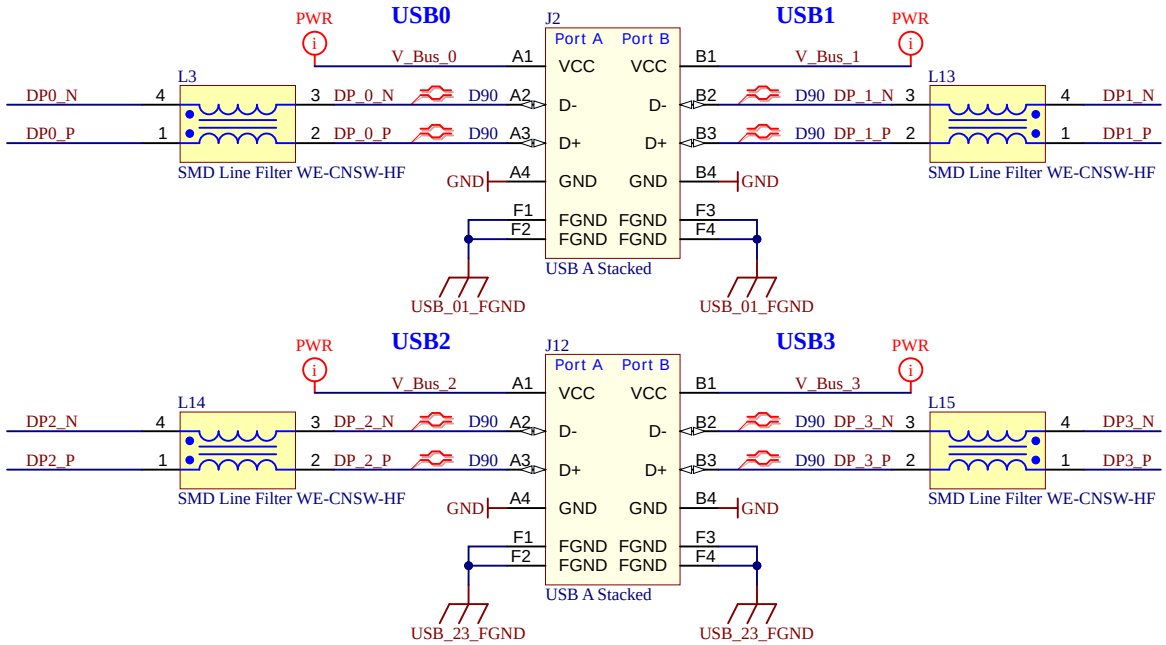


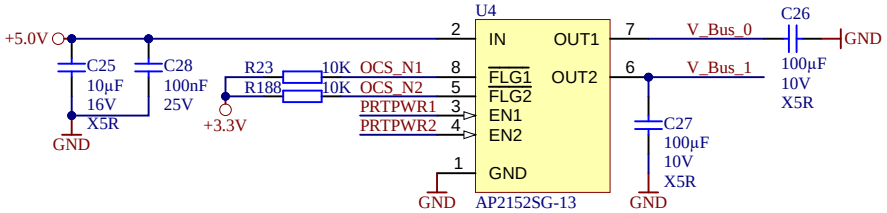


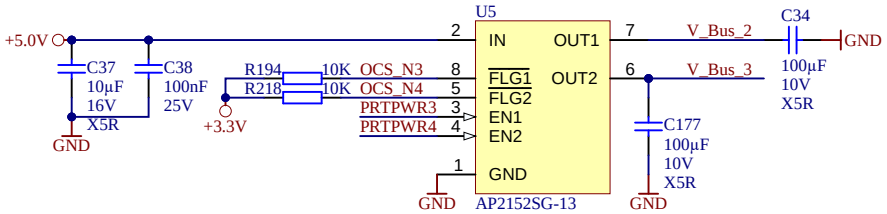


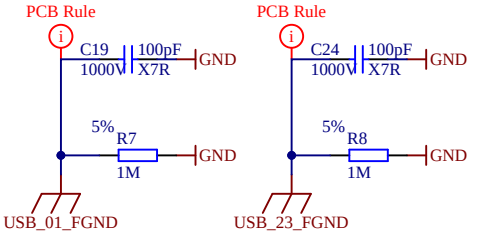
trenz electronic

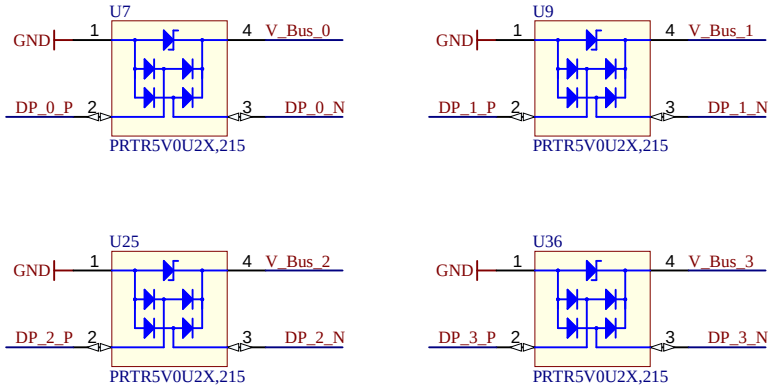
Title: Ethernet			
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 21 of 34
Drawn by: ED	Filename: Ethernet.SchDoc		



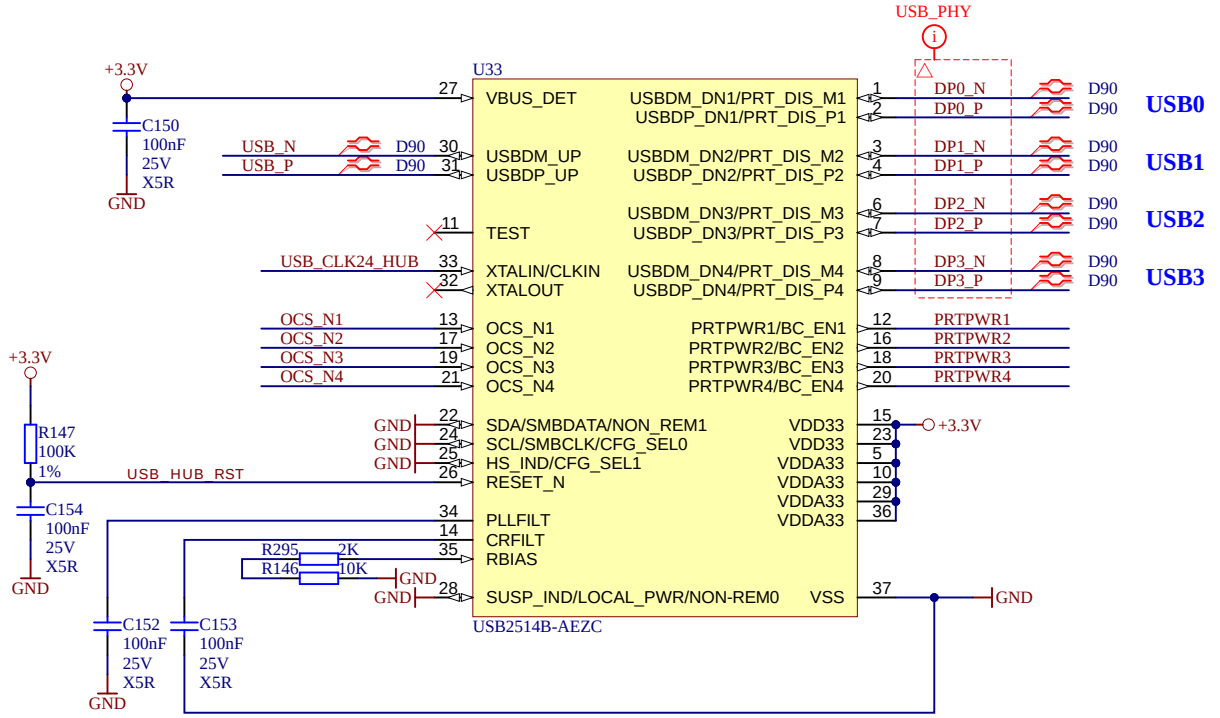








trenz electronic	Title: USB		
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 22 of 34
Drawn by: ED	Filename: USB.SchDoc		



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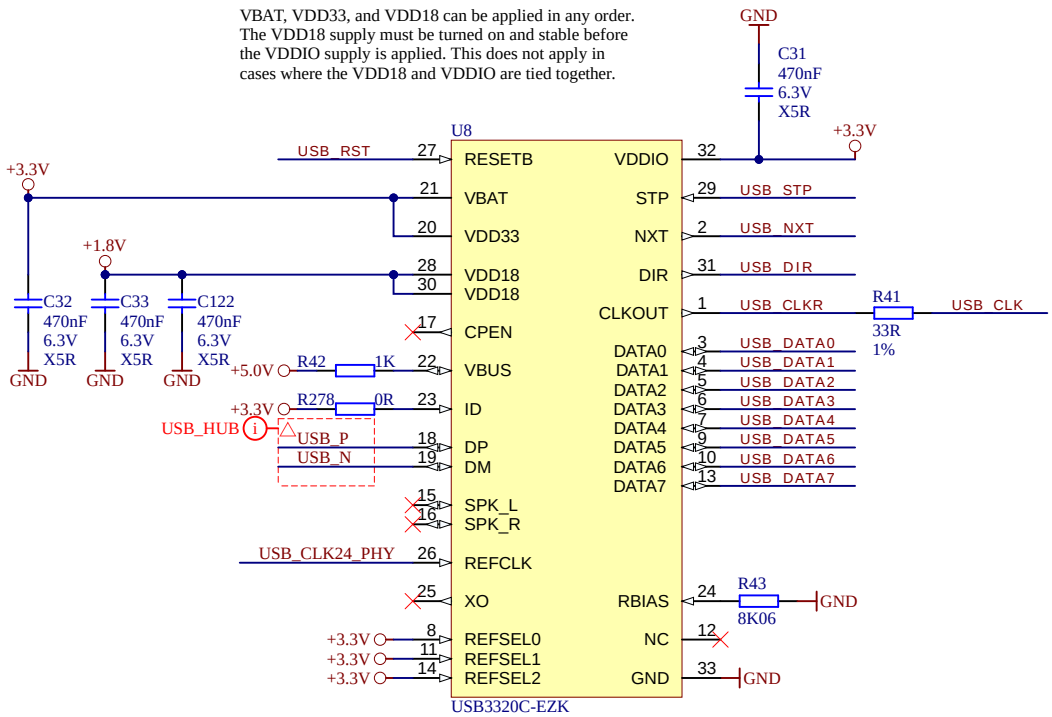
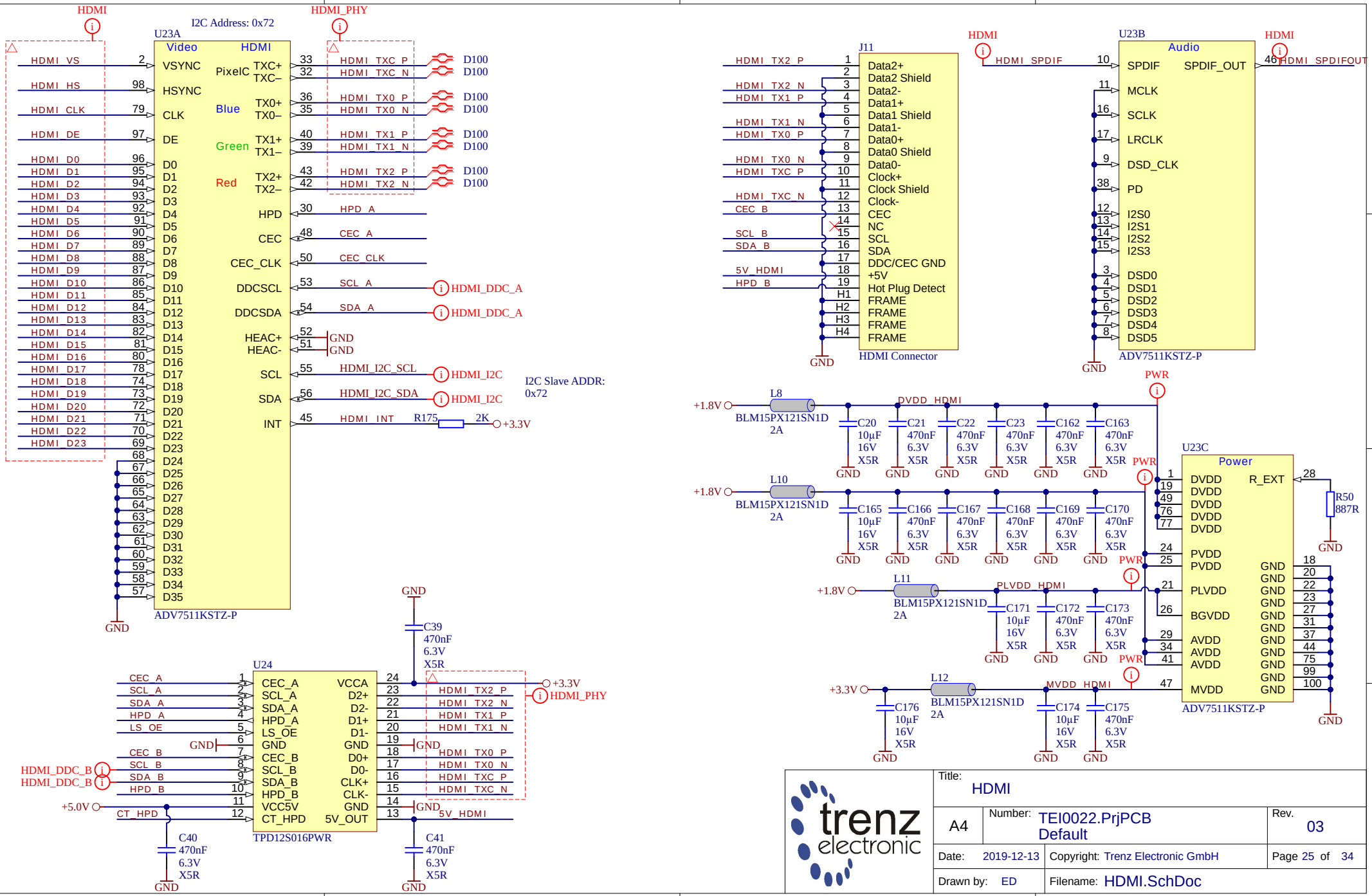
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 23 of 34
Drawn by: ED	Filename: USB-HUB.SchDoc		



trenz electronic	Title: USB-PHY		
A4	Number: TEI0022.PrjPCB Default		Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH		Page 24 of 34
Drawn by: ED	Filename: USB-PHY.SchDoc		


HDMI
HDMI_PHY
I2C Address: 0x72
U23A
Video
HDMI
HDMI_VS
HDMI_HS
HDMI_CLK
HDMI_DE
HDMI_D0
HDMI_D1
HDMI_D2
HDMI_D3
HDMI_D4
HDMI_D5
HDMI_D6
HDMI_D7
HDMI_D8
HDMI_D9
HDMI_D10
HDMI_D11
HDMI_D12
HDMI_D13
HDMI_D14
HDMI_D15
HDMI_D16
HDMI_D17
HDMI_D18
HDMI_D19
HDMI_D20
HDMI_D21
HDMI_D22
HDMI_D23
VSYNC
HSYNC
CLK
DE
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
D32
D33
D34
D35
PixelC
Blue
Green
Red
TXC+
TXC–
TX0+
TX0–
TX1+
TX1–
TX2+
TX2–
HPD
CEC
CEC_CLK
DDCSCL
DDCSDA
HEAC+
HEAC-
SCL
SDA
INT
HDMI_TXC_P
HDMI_TXC_N
HDMI_TX0_P
HDMI_TX0_N
HDMI_TX1_P
HDMI_TX1_N
HDMI_TX2_P
HDMI_TX2_N
D100
HPD_A
CEC_A
CEC_CLK
SCL_A
SDA_A
HDMI_DDC_A
GND
HDMI_I2C_SCL
HDMI_I2C_SDA
HDMI_I2C
HDMI_INT
R175
2K
+3.3V
I2C Slave ADDR:
0x72
ADV7511KSTZ-P
U24
CEC_A
SCL_A
SDA_A
HPD_A
LS_OE
CEC_B
SCL_B
SDA_B
HPD_B
VCC5V
CT_HPD
VCCA
D2+
D2-
D1+
D1-
D0+
D0-
CLK+
CLK-
5V_OUT
HDMI_DDC_B
+5.0V
C39
470nF
6.3V
X5R
C40
C41
TPD12S016PWR
J11
Data2+
Data2 Shield
Data2-
Data1+
Data1 Shield
Data1-
Data0+
Data0 Shield
Data0-
Clock+
Clock Shield
Clock-
CEC
NC
SCL
SDA
DDC/CEC GND
+5V
Hot Plug Detect
FRAME
HDMI Connector
5V_HDMI
HPD_B
U23B
Audio
HDMI_SPDIF
SPDIF
SPDIF_OUT
HDMI_SPDIFOUT
MCLK
SCLK
LRCLK
DSD_CLK
PD
I2S0
I2S1
I2S2
I2S3
DSD0
DSD1
DSD2
DSD3
DSD4
DSD5
PWR
+1.8V
L8
L10
L11
L12
BLM15PX121SN1D
2A
DVDD_HDMI
PLVDD_HDMI
MVDD_HDMI
C20
C21
C22
C23
C162
C163
C165
C166
C167
C168
C169
C170
C171
C172
C173
C174
C175
C176
10µF
16V
X5R
470nF
6.3V
X5R
U23C
Power
DVDD
R_EXT
PVDD
PLVDD
BGVDD
AVDD
MVDD
GND
R50
887R
ADV7511KSTZ-P
Title:
HDMI
A4
Number:
TEI0022.PrjPCB
Default
Rev.
03
Date:
2019-12-13
Copyright:
Trenz Electronic GmbH
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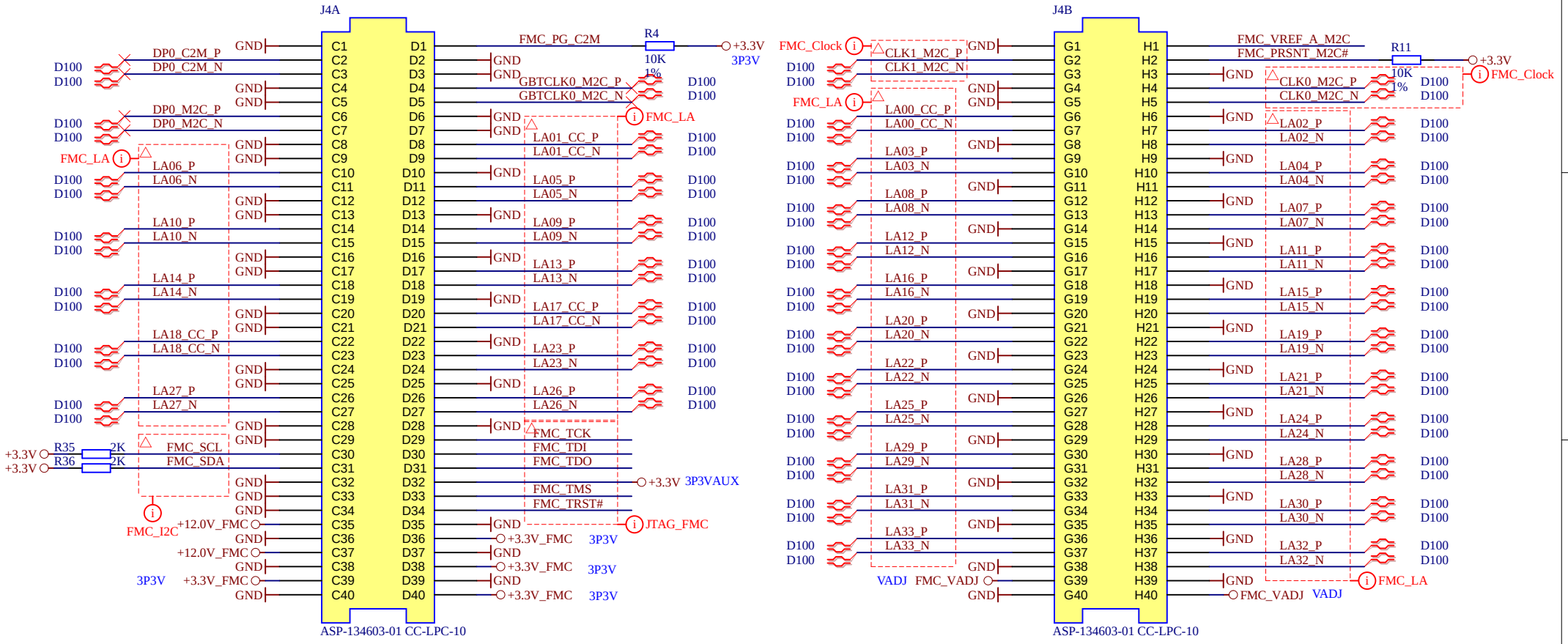
Drawn by:
ED
Filename:
HDMI.SchDoc
trenz
electronic

I2C Address: 0x50
Pin C34: GA[0]=0
Pin D35: GA[1]=0



FMC_VADJ	**2 A**	**FMC_VADJ**	**FPGA**
FMC_VREF_A_M2C	**1 mA**		
3P3VAUX	**20 mA**	**+3.3 V**	**FPGA**
3P3V	**3 A**	**+3.3V_FMC**	**FPGA**
+12.0V	**1 A**	**+12.0V_FMC**	

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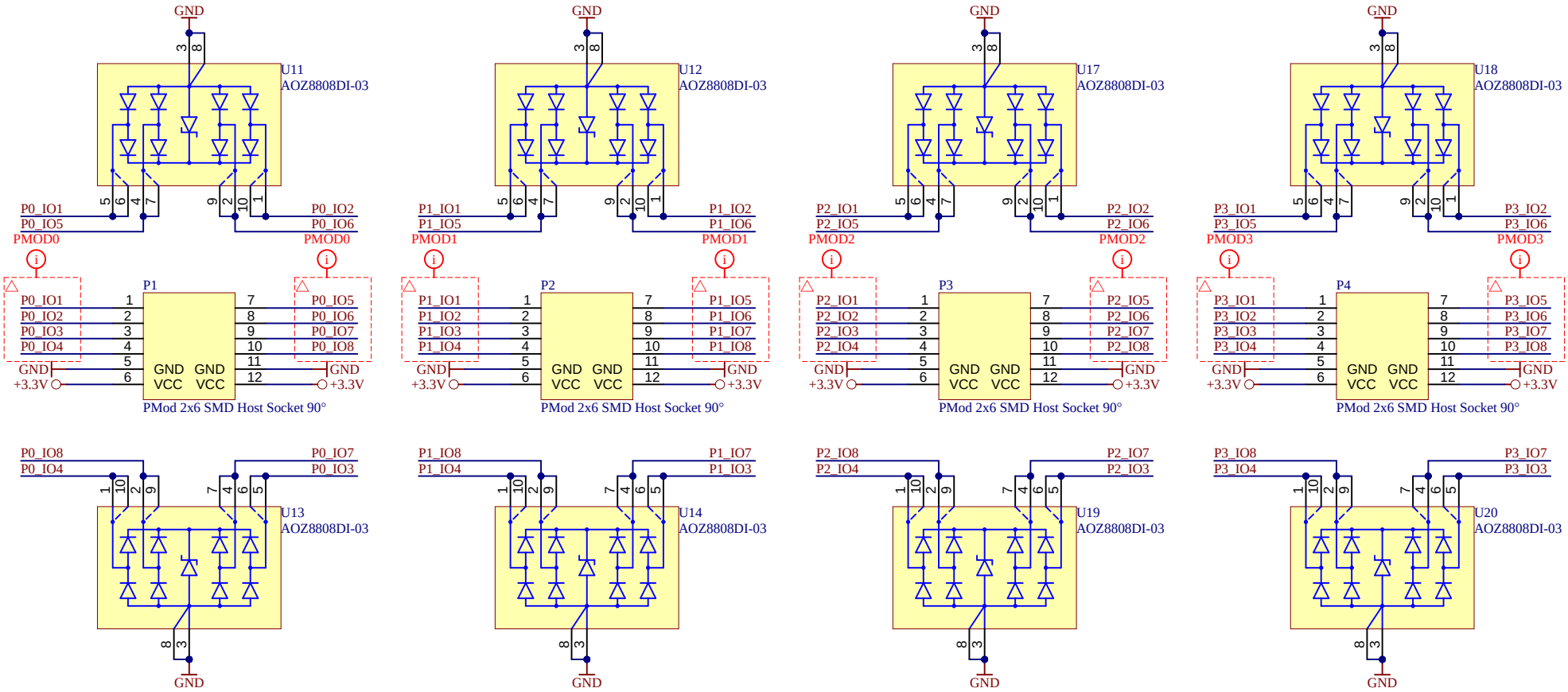
Title: FMC		
A4	Number: TEI0022.PrjPCB Default	Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 26 of 34
Drawn by: ED	Filename: FMC.SchDoc	



trenz electronic	Title: PMOD		
	A4	Number: TEI0022.PrjPCB Default	Rev. 03
	Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 27 of 34
	Drawn by: ED	Filename: PMOD.SchDoc	

Power1
Power1.SchDoc

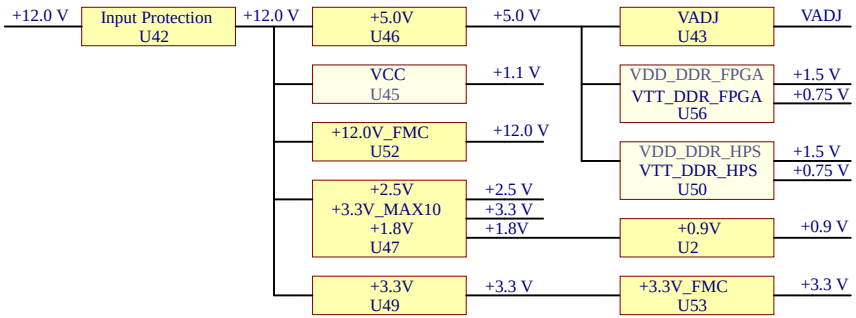
Power2
Power2.SchDoc

Power3
Power3.SchDoc

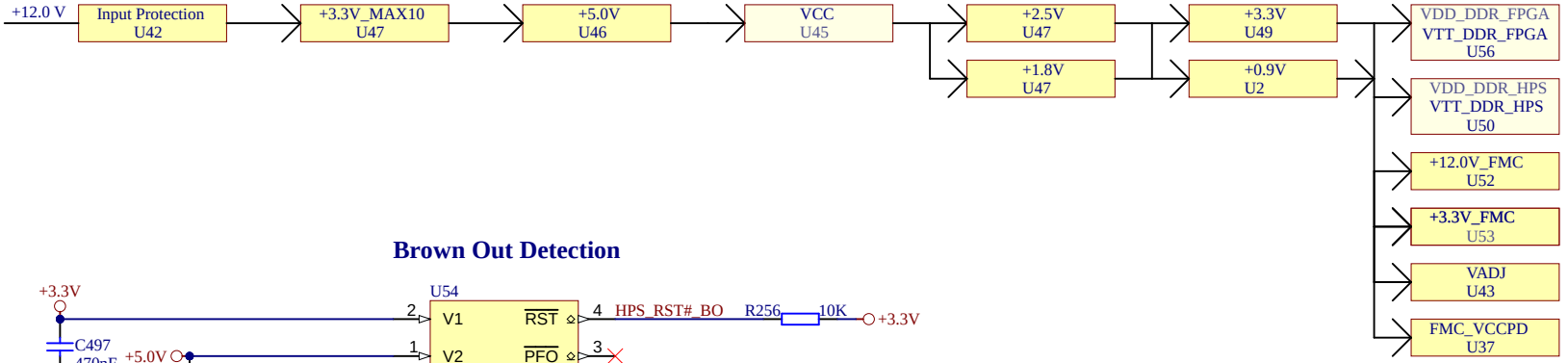
Power4
Power4.SchDoc

Power5
Power5.SchDoc

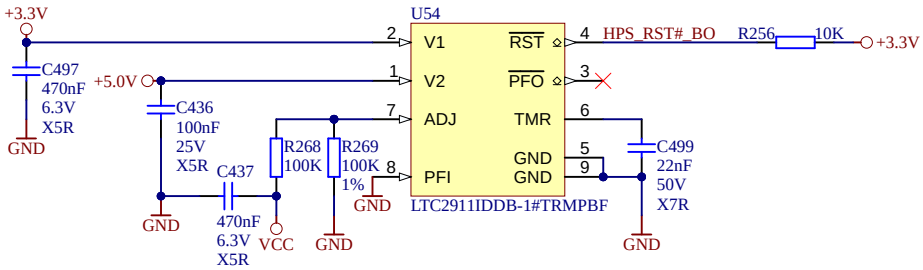
Power Supply Structure



Power Supply Sequencing

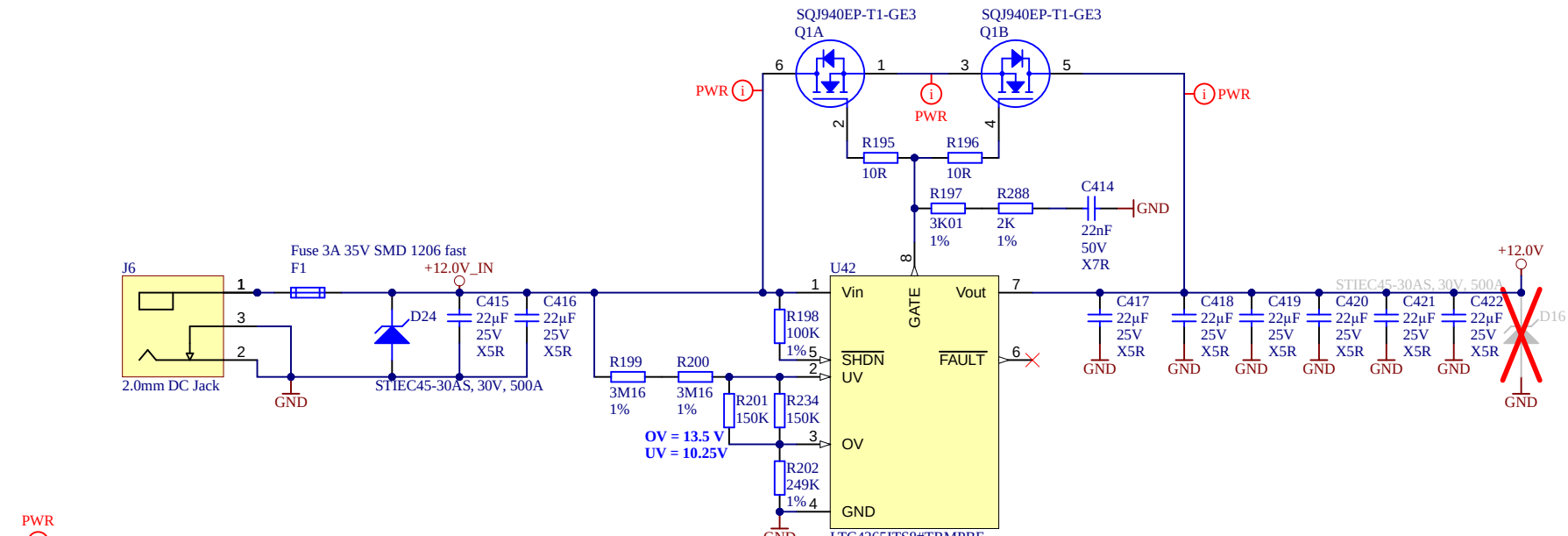


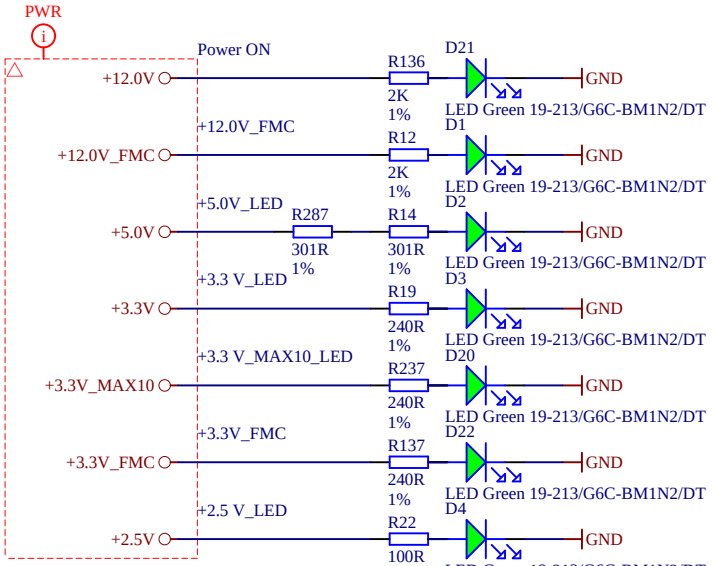
Brown Out Detection



VADJ-Threshold: 1.0 V

trenz electronic	Title: TEB0911		
	A4	Number: TEI0022.PrjPCB Default	Rev. 03
	Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 28 of 34
	Drawn by: ED	Filename: Power.SchDoc	

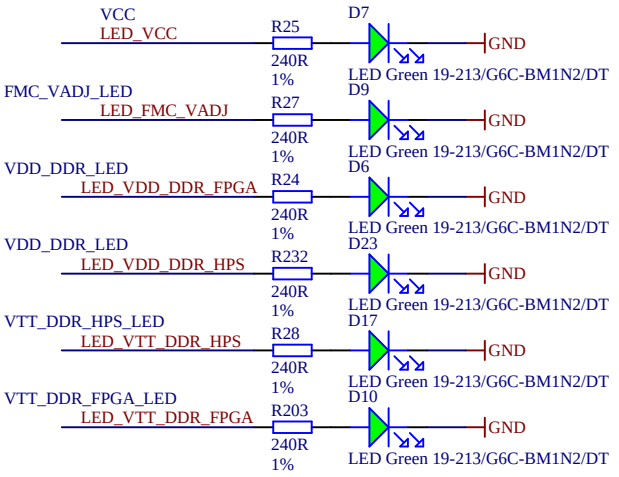




For 12 V input mode:

R52 = 6M32
R54 = 75k
R55 = 249k

OV = 10.25 V
UV = 13.5 V



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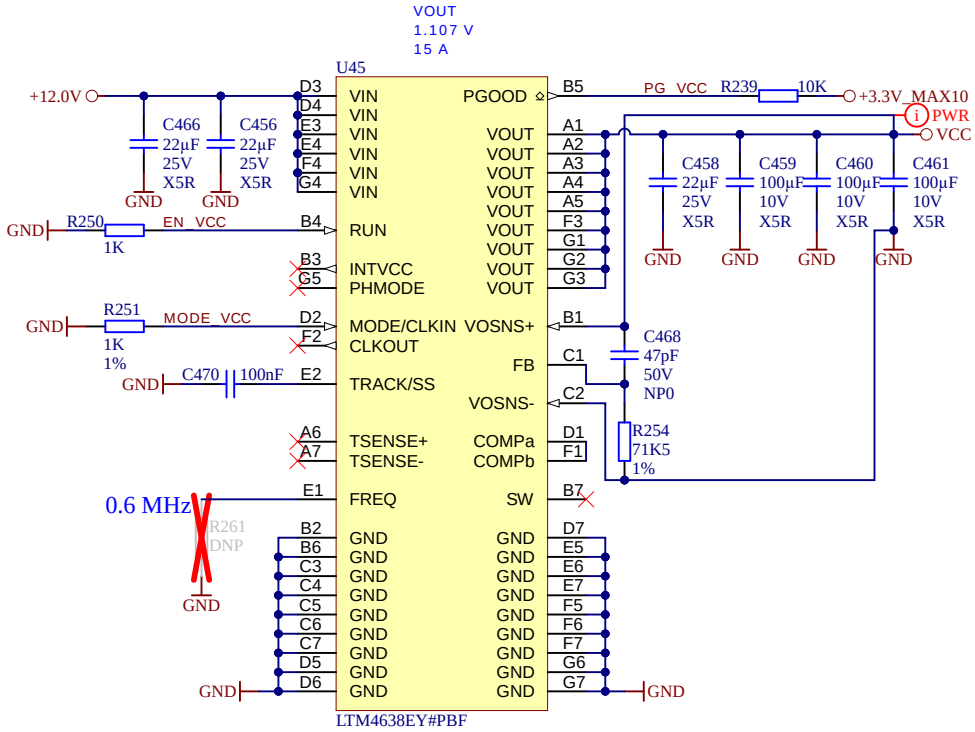
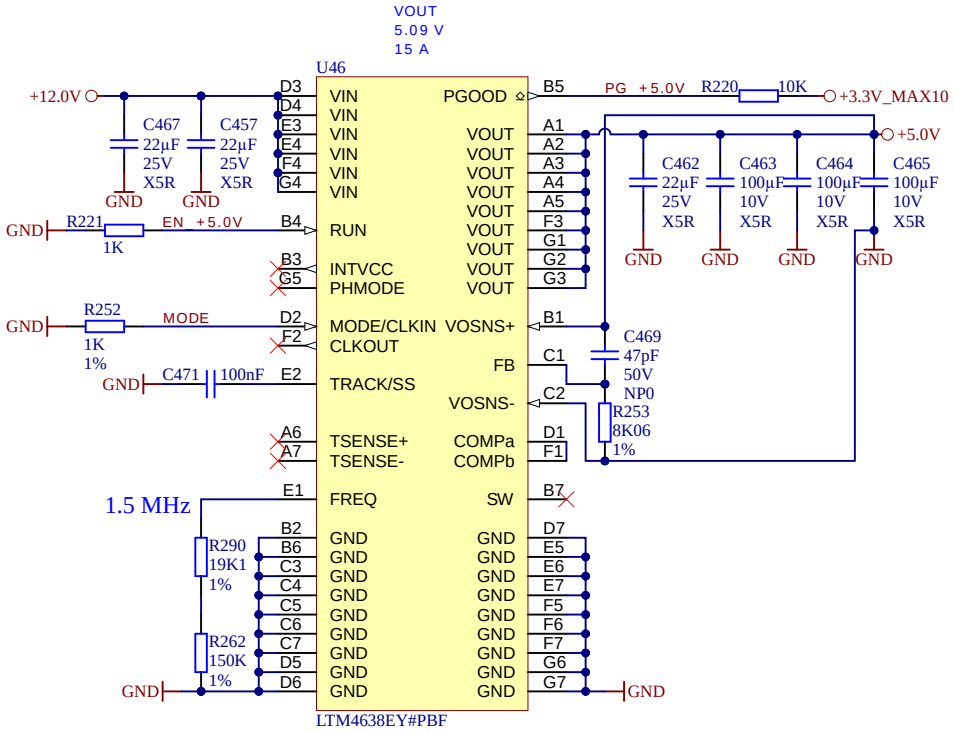
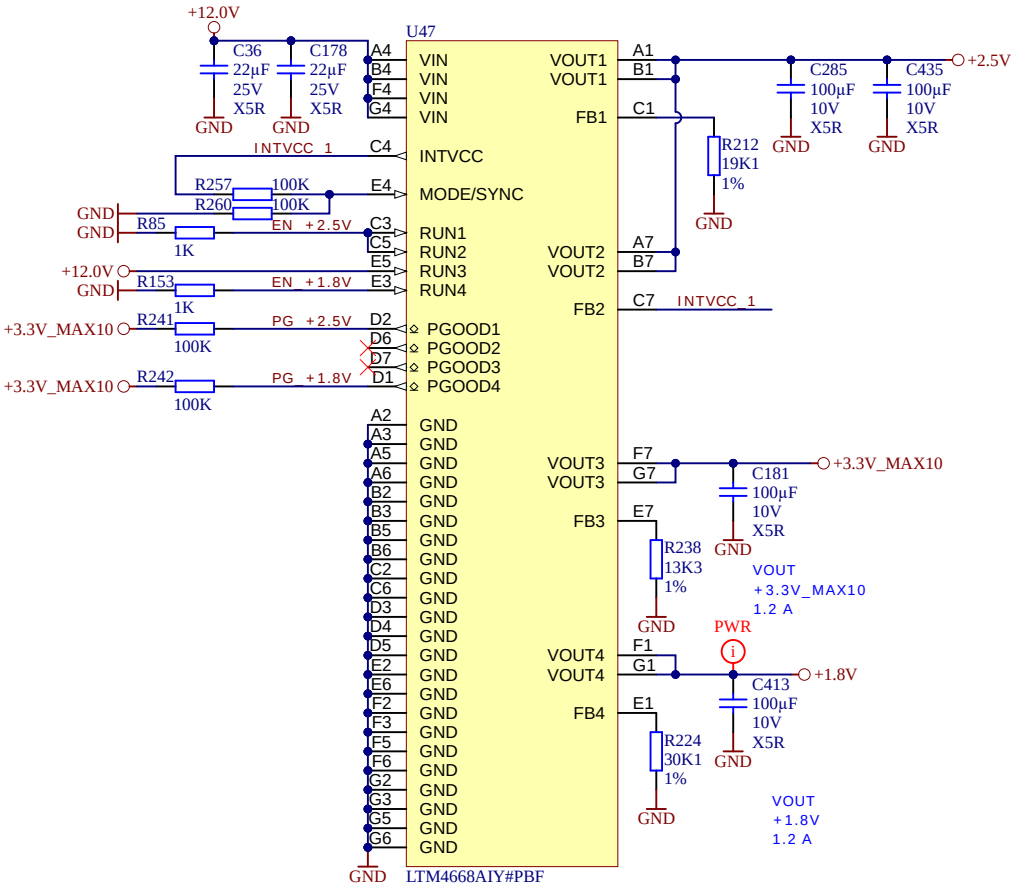
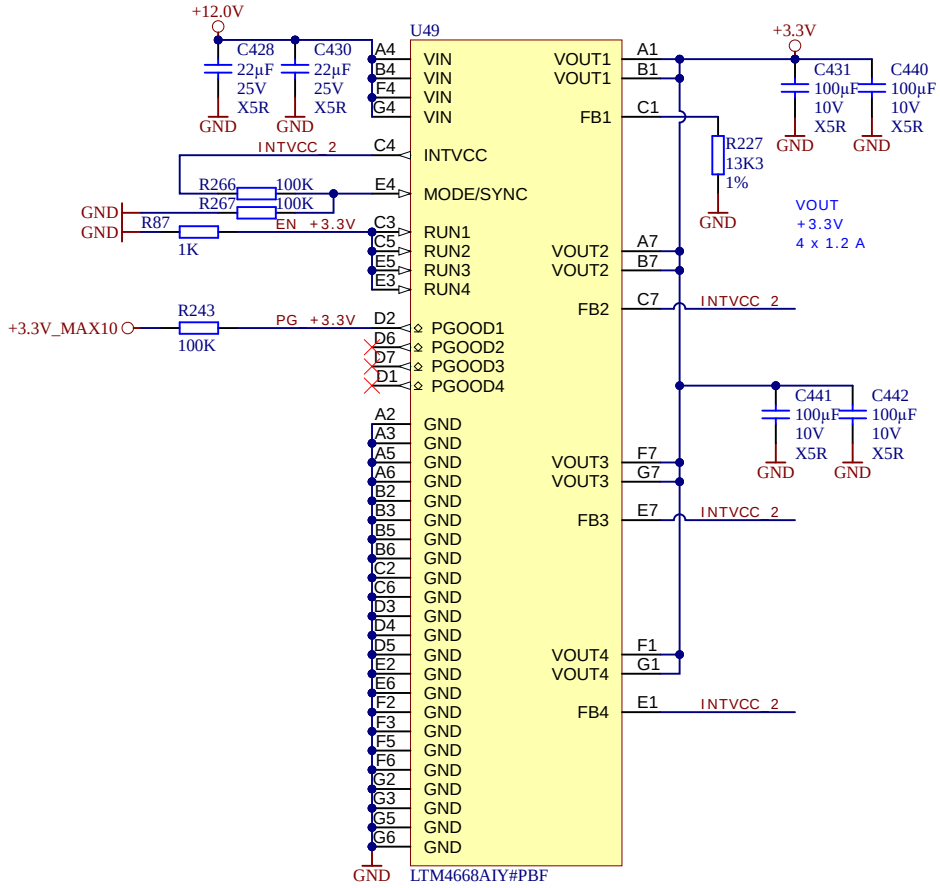
Title: Power1		
A4	Number: TEI0022.PrjPCB Default	Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 29 of 34
Drawn by: ED	Filename: Power1.SchDoc	



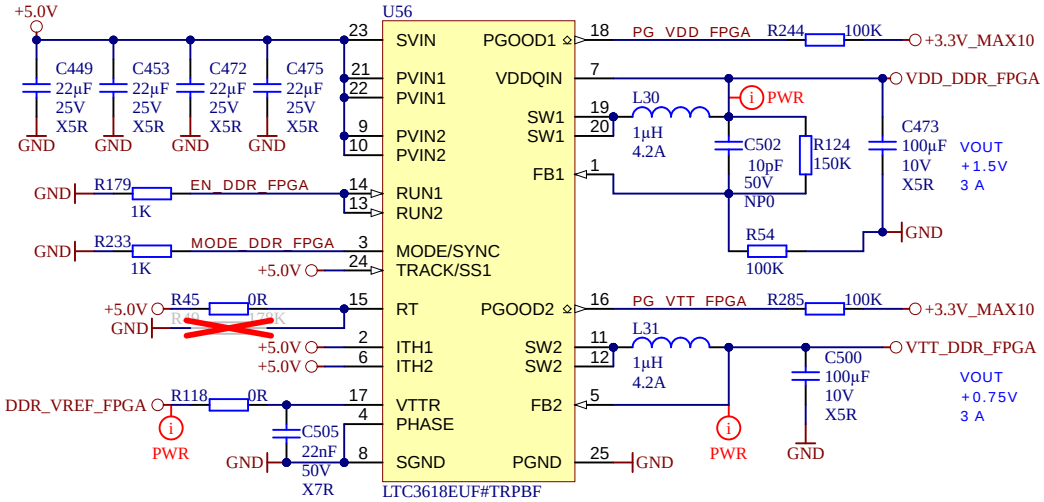


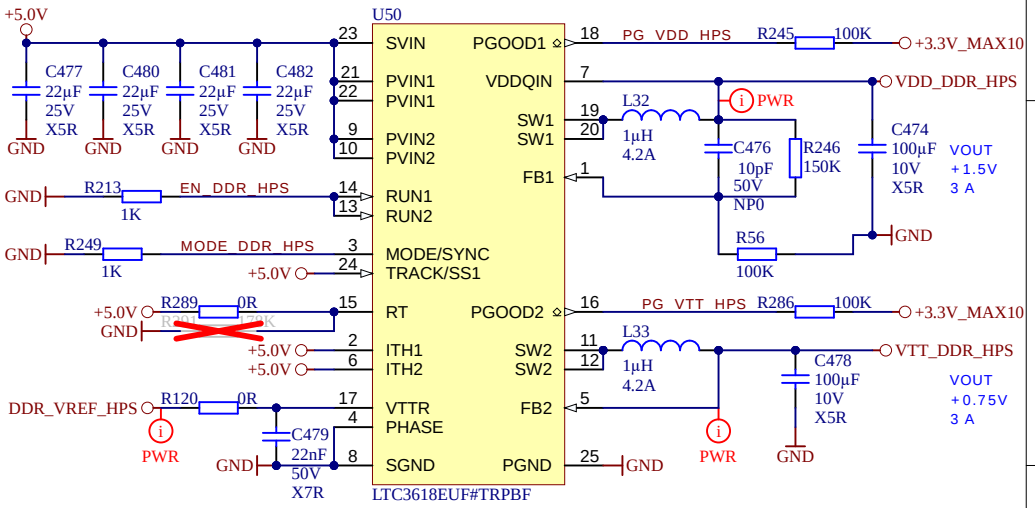
trenz electronic	Title: Power2		
	A4	Number: TEI0022.PrjPCB Default	Rev. 03
	Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 30 of 34
	Drawn by: ED	Filename: Power2.SchDoc	

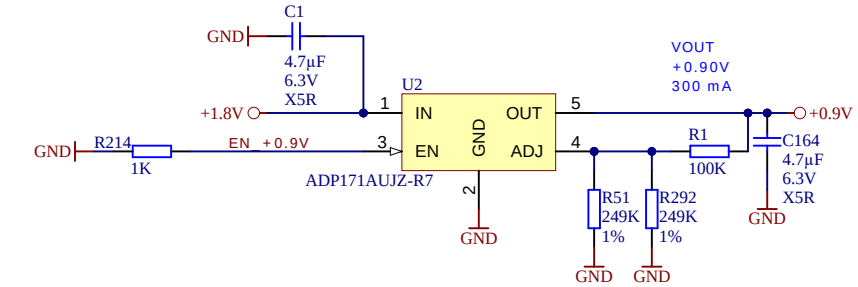




trenz electronic	Title: Power3		
	A4	Number: TEI0022.PrjPCB Default	Rev. 03
	Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 31 of 34
	Drawn by: ED	Filename: Power3.SchDoc	

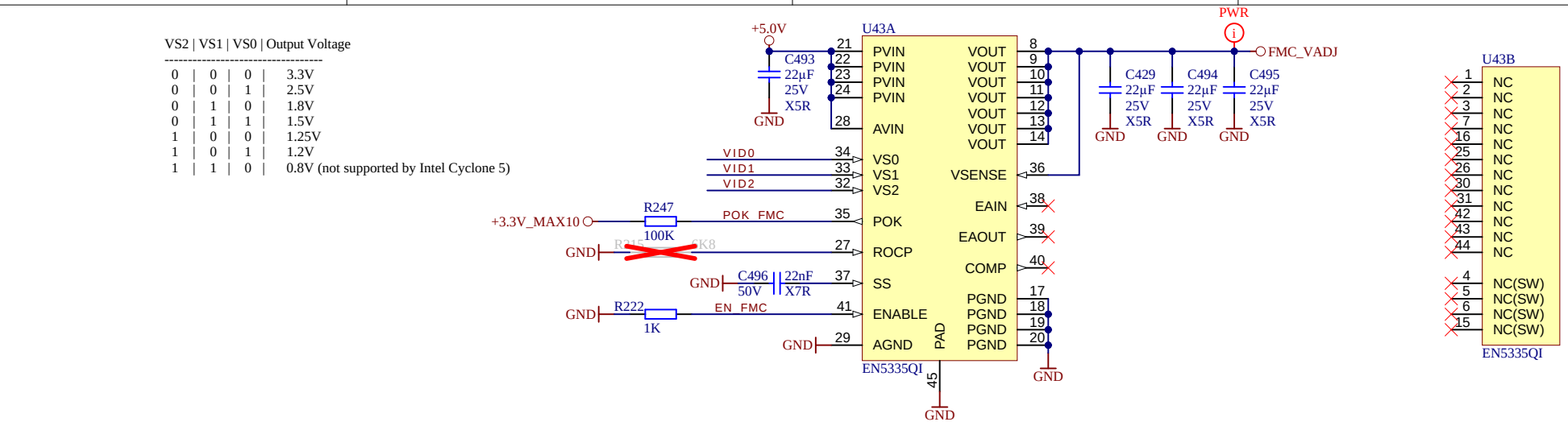


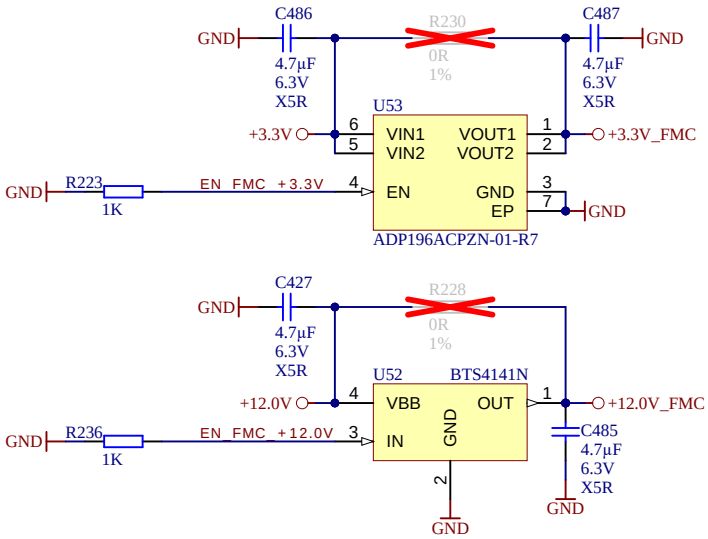


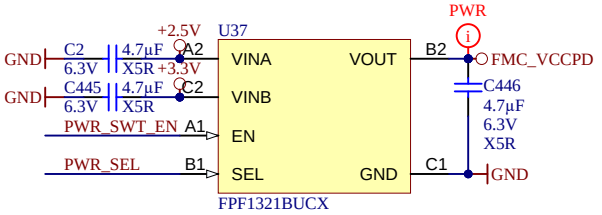


trenz electronic	Title: Power4		
	A4	Number: TEI0022.PrjPCB Default	Rev. 03
	Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 32 of 34
	Drawn by: ED	Filename: Power4.SchDoc	

VS2	VS1	VS0	Output Voltage
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V (not supported by Intel Cyclone 5)







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Title: Power5		
A4	Number: TEI0022.PrjPCB Default	Rev. 03
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 33 of 34
Drawn by: ED	Filename: Power5.SchDoc	

CHANGES REV01 to REV02

- Added "Revision_Changes.SchDoc"
- Swapped FTDI_JTAG_TMS/CS and FTDI_JTAG_TDI/DO at MAX10 (JIRA GT-1064)
- Added "+12 V" comment in PCB
- Added power in symbol and attention symbol in PCB
- LED circuits changed (JIRA GT-1062)
- FTDI LED polarity and resistors changed
- Added pull-ups at OCS_N1...4 to "+3.3V"
- Changed net name CLK_50MHz_MAX10 to CLK_MAX10
- Changed net name HPS_CLK2_25MHz to HPS_CLK2
- Changed C468 and C469 from 33 pF to 47 pF
- Connected PG from U46 to MAX10
- Pulled the MODE pins from U45, U46, U50, and U56 down
- Changed net name "INTVCC_+5.0V" to "MODE"
- Deleted nets "INTVCC_+5.0V"
- Disconnect nets "Link_ST", and "RX_ER" from Cyclone V
- Inserted net "EN_+5.0V" for controlling DCDC U46
- Changed the Power Supply Sequencing
- Changed resistors for LEDs
- Changed MODE pin circuit from U47 and U49 (JIRA GT-1077)
- Added pull up for net "HPS_RST#_BO"
- Added pull downs for net "MODE_DDR_HPS" and "MODE_DDR_FPGA"
- Change pull down of net "FPGA_DDR-RESET" to pull up to "VDD_DDR_FPGA"
- Change pull down of net "HPS_DDR-RESET" to pull up to "VDD_DDR_FPGA"
- Deleted 100 Ohm resistor between nets "SMA_CLK_OUT_p" and "SMA_CLK_OUT_n"
- Added zero Ohm resistor at U3 pin 2.
- Added pull up for U2 pin HPS_PORSEL
- Changed resistor values from signals CONF_DONE_I, nCONFIG_I, and nSTATUS from 12k to 10k
- Changed voltage divider resistor values of R268 and R269
- Connected ID of U8 to +3.3V via a 0 Ohm resistor
- Changed R42 from 8k06 Ohm to 1k Ohm
- Added resistor divider (R279 and R283) for Ethernet clock input
- Connected Ethernet reset to Intel MAX10
- Added cooler attachment (JIRA GT-1070)
- Changed transistor T3 circuit to component U37
- Swapped HDMI pins (JIRA GT-1079)
- Changed programmable clock (U3) to project specific clock
- Connected net "QSPI_RST" from Cyclone V to "+3.3V" via pull-up resistor
- Connected net "AS_RST" from Cyclone V to "+3.3V" via pull-up resistor
- Added pull-up resistor for net "ETH_MDC"
- Connect nets "GPIO2", "GPIO3", and "GPIO4" between MAX10 and Cyclone V
- Connect nets "THERM_N" and "ALERT_N" to Cyclone V bank 6A and changed pull-up to net "VDD_DDR_HPS"
- Connect nets "FPGA_RST#_SW" and "USER_BTN_SW" to MAX10 bank 8 and changed pull-up to net "+3.3V_MAX10"
- Delete nets "BCBUS4", "BCBUS5", "BCBUS6", and "BCBUS7"
- Connect USB HUB reset to MAX10 with net "USB_HUB_RST"
- Increased size of "ARROW" logo on PCB
- Add boxes for LEDs on PCB
- Change address on PCB
- Change revision on PCB
- Changed RJ45 connector
- Changed assembly option of C35, C80, C81, C120, C121, C426, D26, D29, D32, R210, R228, R230, R255, R264, R225, R239, R193, R265, R241, R242, R243, R244, R245, and R226
- Changed D11, D12, D13, D14, D18, D19, and D25 from active-low to active-high
- Change resistor value of R41from 0 Ohm to 33 Ohm
- Connect net "USB_RST" to MAX10
- Insert resistors R207, R208, R209, and R284 to connect I2C HDMI with I2C HPS optionally
- Change net "PG_VDD_HPS" to "PG_DDR_HPS" and "PG_VDD_HPS"
- Insert R286 as pull-up for net "PG_VDD_HPS"
- Change net "PG_VDD_FPGA" to "PG_DDR_FPGA" and "PG_VDD_FPGA"
- Insert R285 as pull-up for net "PG_VDD_FPGA"
- Delete nets "BCBUS0" and "BCBUS3"
- Changed C436 to higher voltage range
- Library update
- Pull-up for I2C bus set to 2K2
- Deleted "BCBUS1" and "BCBUS2"

CHANGES REV02 to REV03

- Changed PGOOD connection for DCDC U47 (+2.5V)
- Changed PGOOD connection for DCDC U49 (+3.3V)
- Swapped TX and RX labels for FTDI_RX and FTDI_TX
- Added R287 and changed R14 and R279 to 301R
- Changed R13, R15...18, R20, R141, R169, R171...174 from 12K1 to 10K
- Changed R283 from 820R to 887R
- Changed R197 from 5K1 to 3K01 and added R288 with 2K
- Changed R2, R206, and R231 from 1K5 to 2K
- Changed R35 R36, R40, R52, R163, R164, from 2K2 to 2K
- Changed R128 from 2K2 to 2K and added R293 with 240R
- Change R262 from 174K to 150K and add R290 with 19K1
- Change R1 from 150K to 100K, R51 from 187K to 249K and add R292 with 249K in parallel to R51
- Changed R253 from 8K2 to 8K06
- Changed C46, C48, C74, C77, C86, C88, C114, C117 from 47nF to 22nF
- Changed R4, R11, R34, R37, R39, R44, R46, R165, R166, R190, R280, R281 from 12K to 10K
- Changed R125 from 12K to 10K and added R294 with 2K
- Changed R146 from 12K to 10K and added R295 with 2K
- Changed DDR U26, U27, U28, U29 from IS43TR16512BL-125KBLI (1 GByte) to IS43TR16256BL-125KBLI (512 MByte)

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