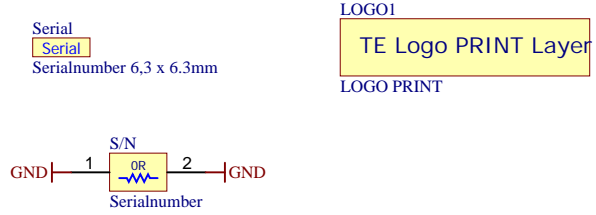
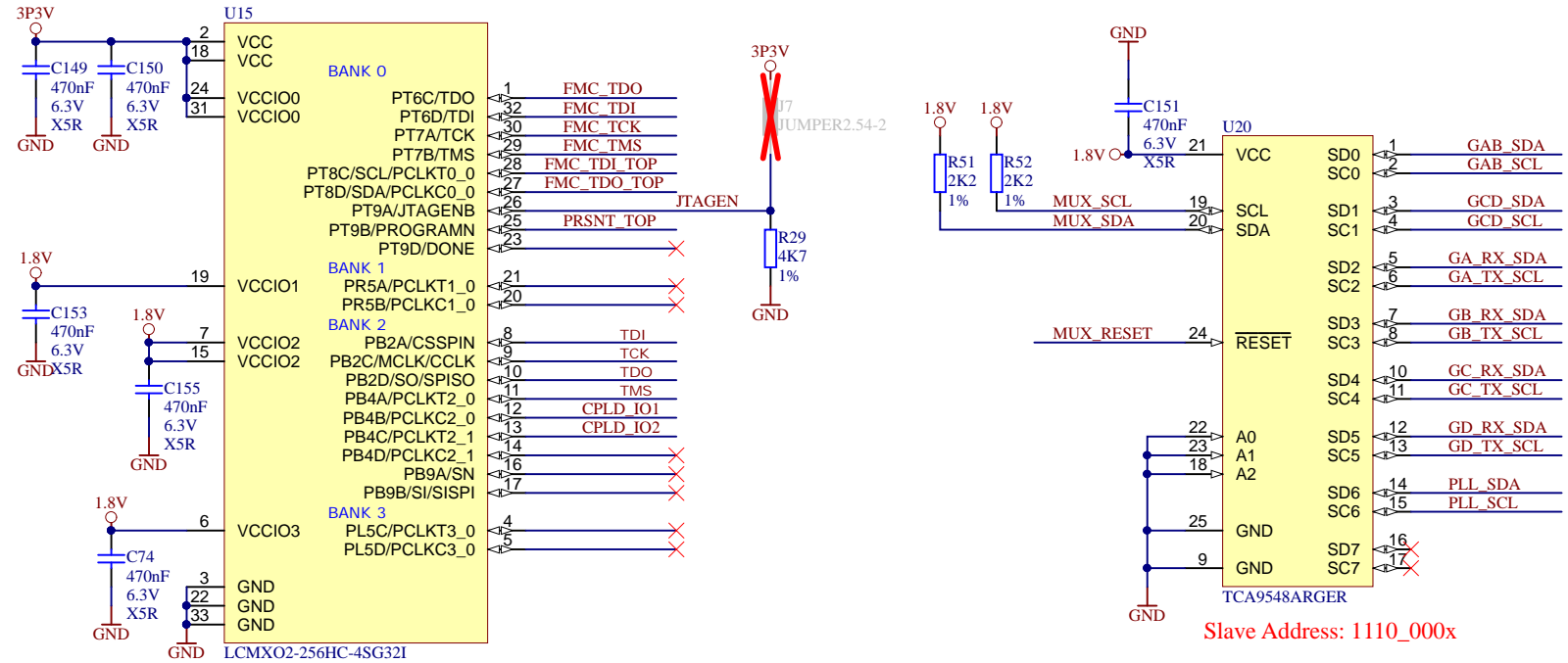
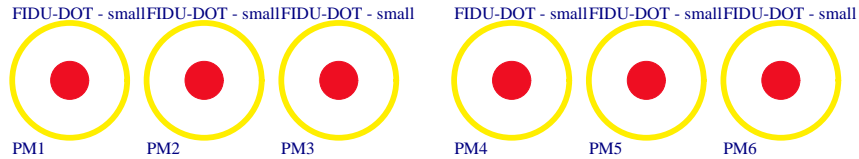


- FMC
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- FMC_TOP
FMC_TOP.SchDoc
- FRONT
FRONT.SchDoc
- GMSL_A
GMSL_A.SchDoc
- GMSL_B
GMSL_B.SchDoc
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GMSL_C.SchDoc
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FPGA_MGT.SchDoc
- FPGA-PWR
FPGA-PWR.SchDoc
- PWR
PWR.SchDoc
- Clock
Clock.SchDoc



Assembly variant	PROTO
Created by	VT
Modified by	VT
Modified at	2019-07-29
SVN Revision	8596

Title: TEF0003		
A4	Number: TEF0003 PROTO	Rev. 01
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Filename: TEF0003.SchDoc		

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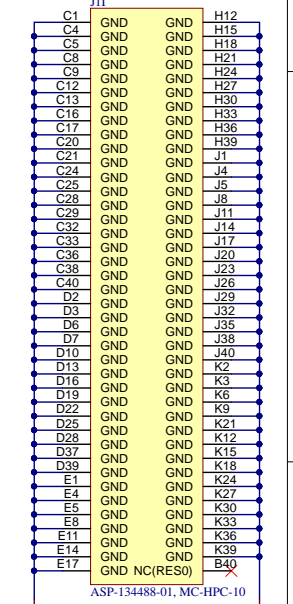
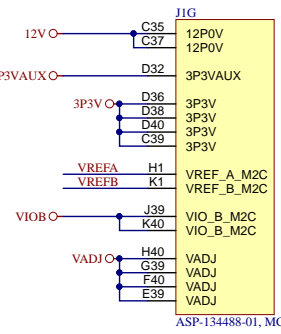
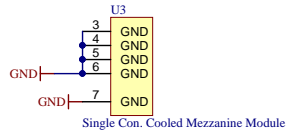
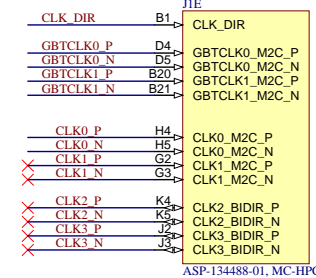
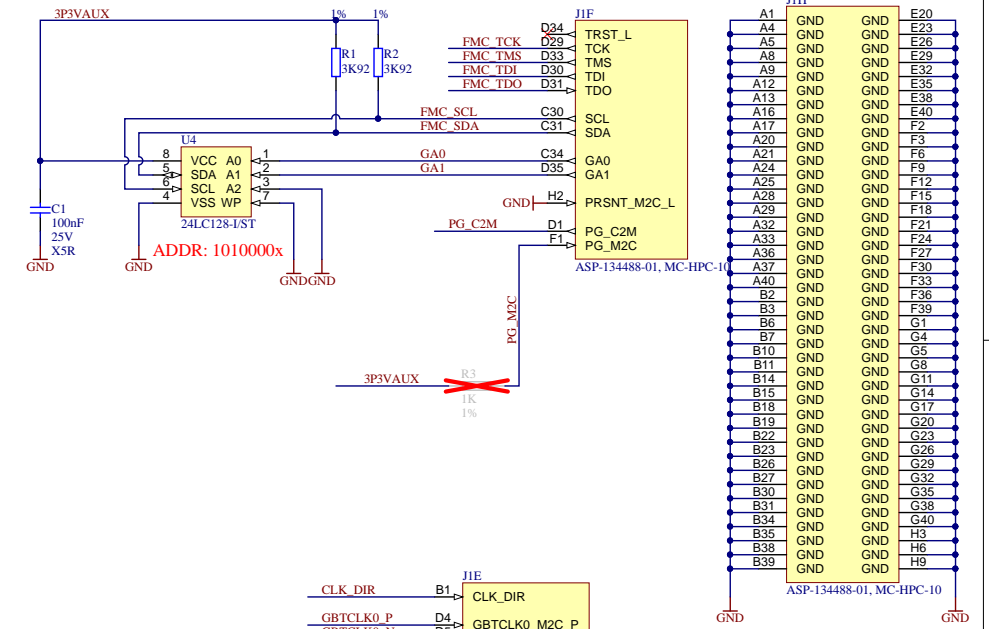
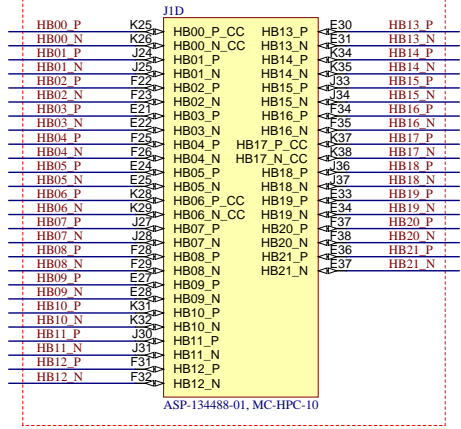
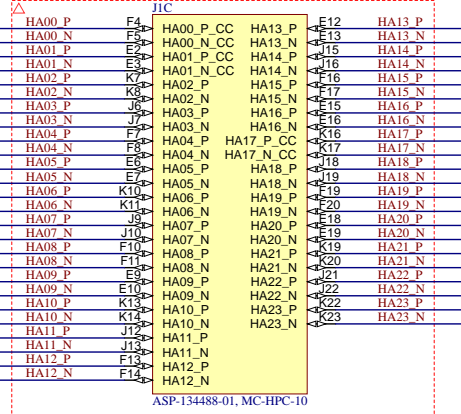
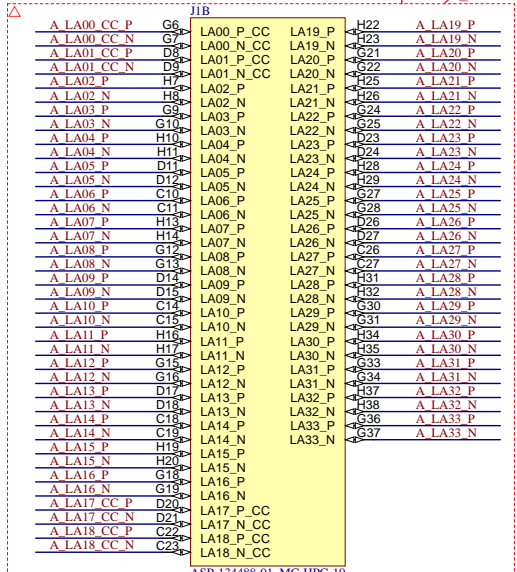
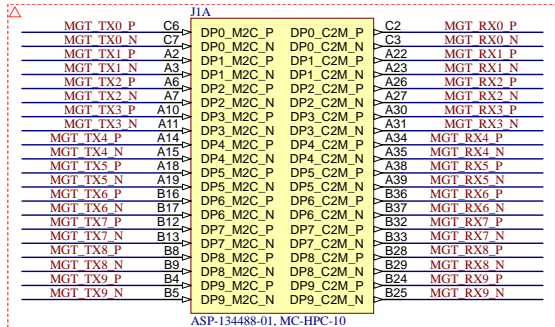
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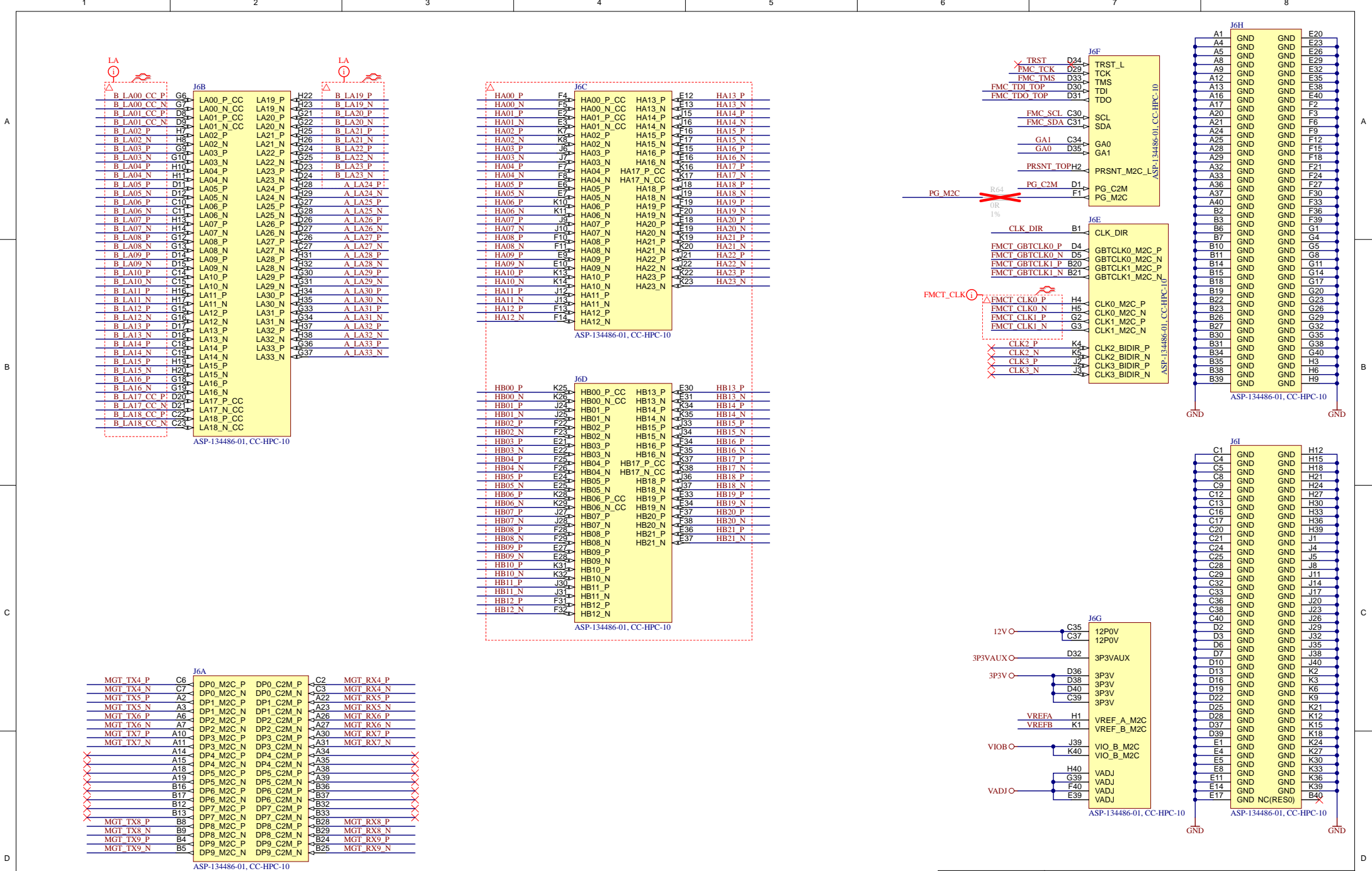
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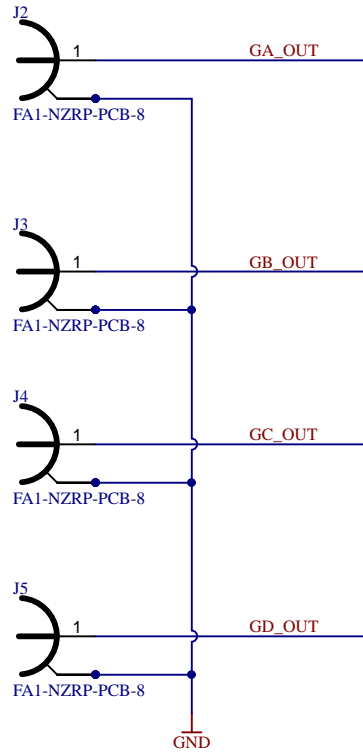
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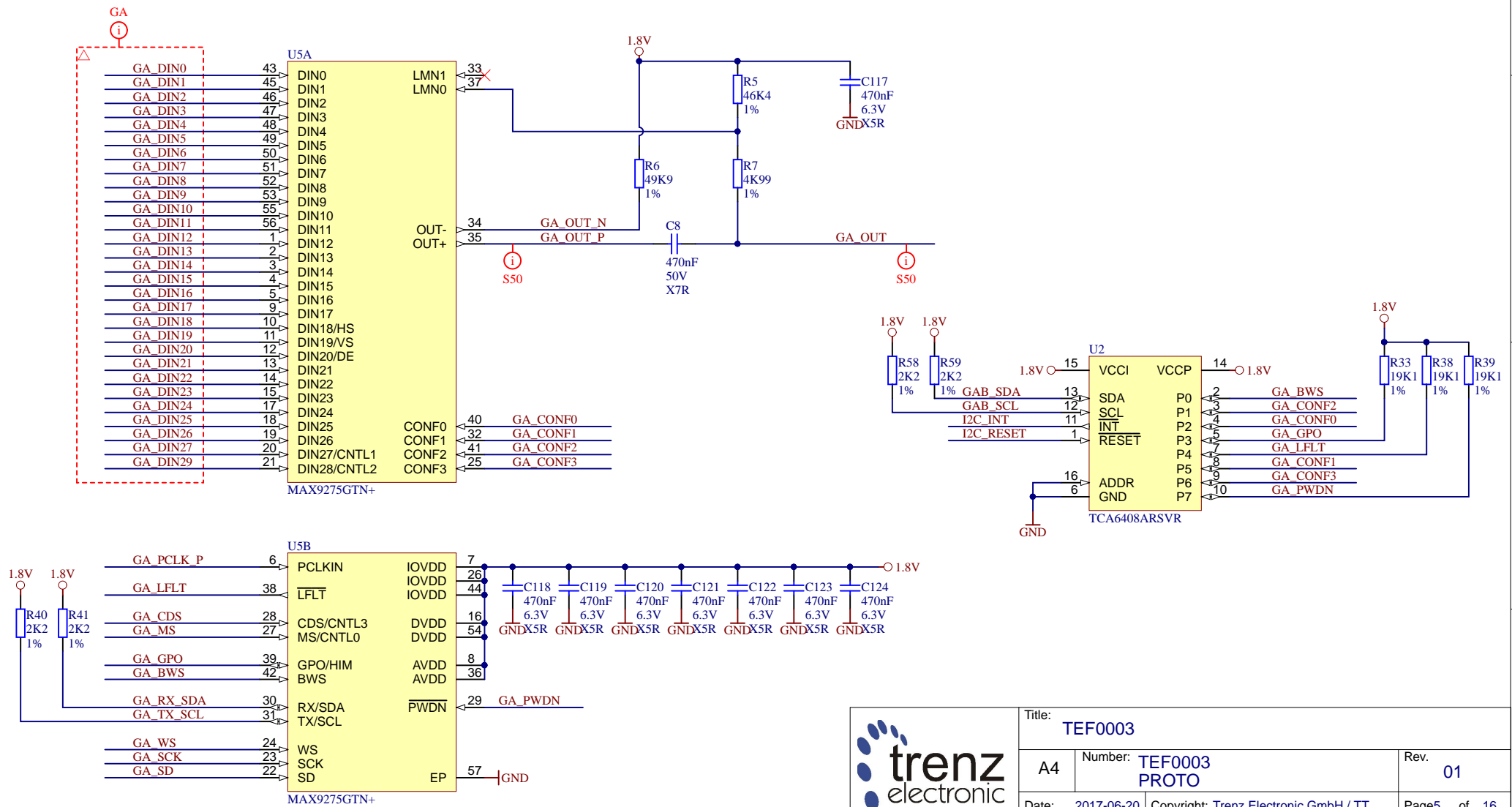
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Date: 2017-06-20		Copyright: Trenz Electronic GmbH / TT	
Filename: FRONT.SchDoc		Page 4 of 16	

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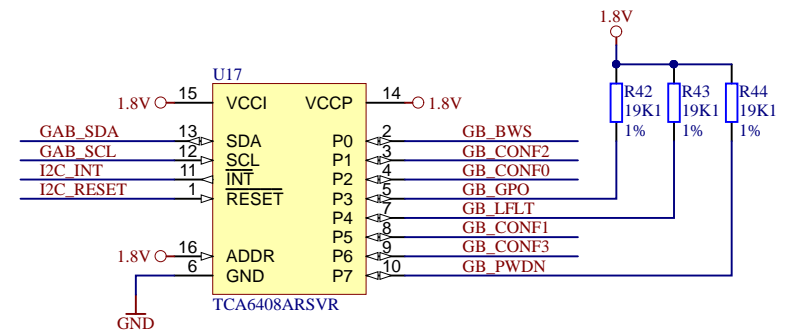
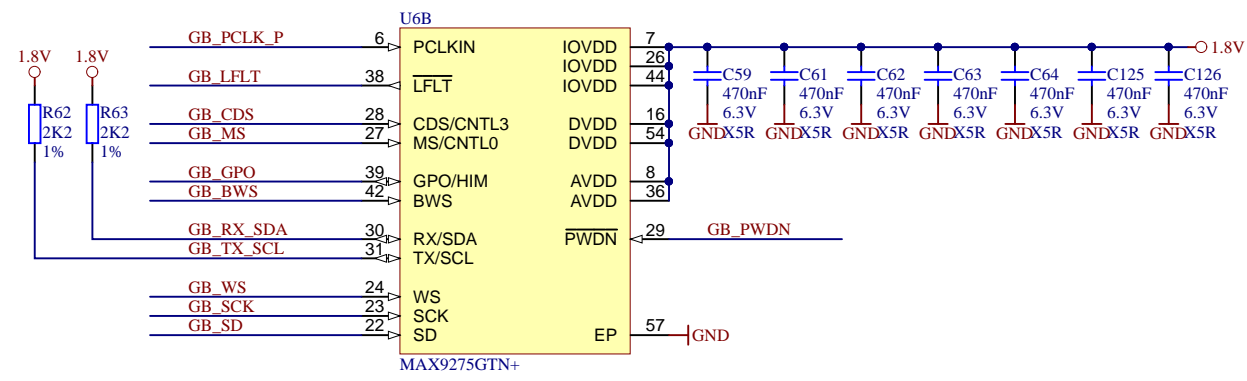
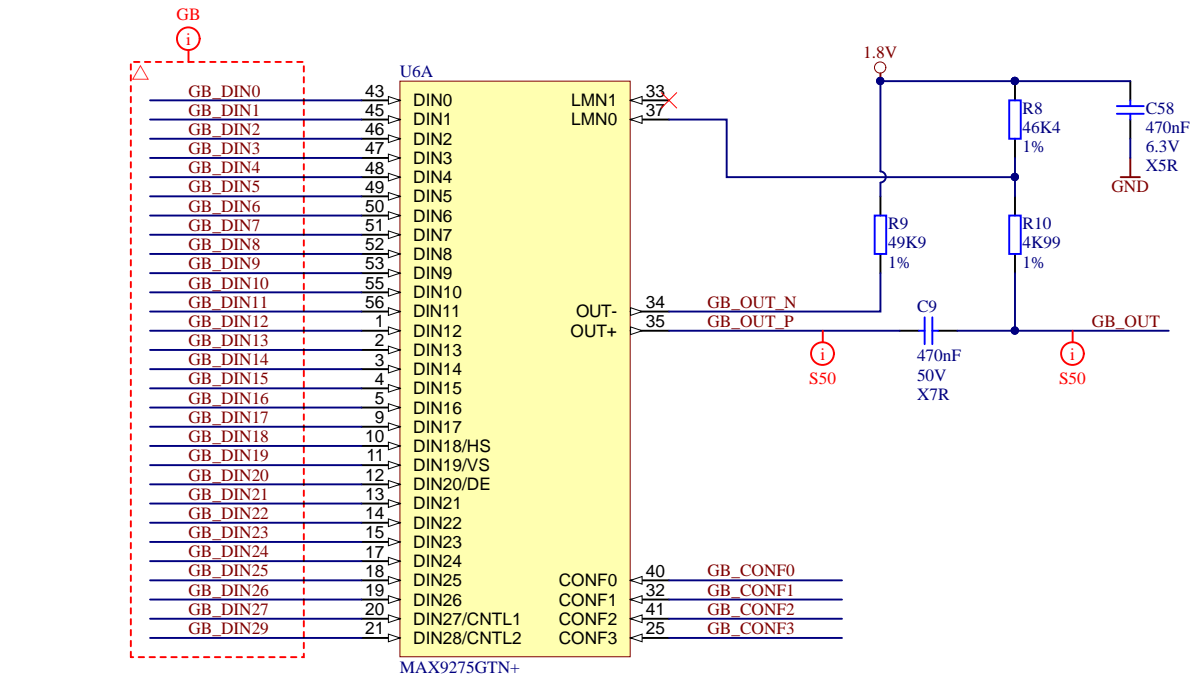
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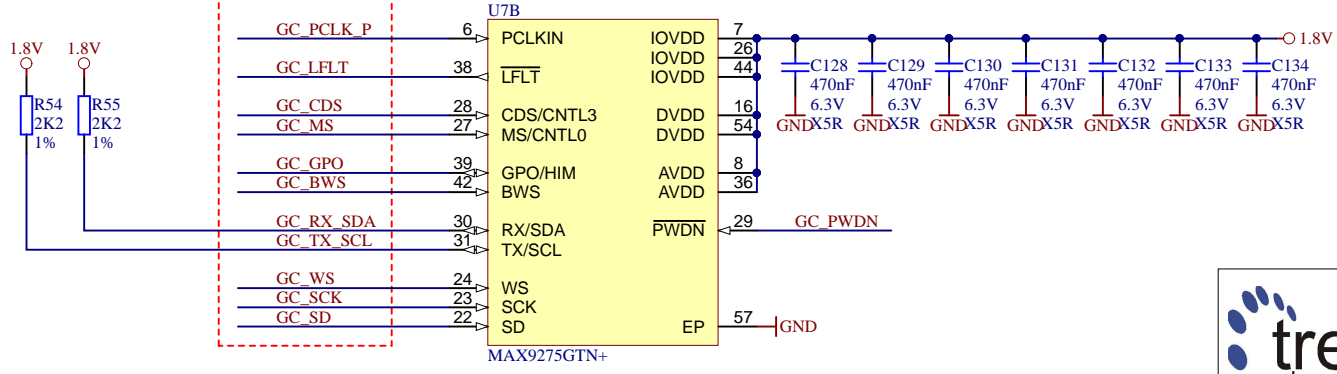
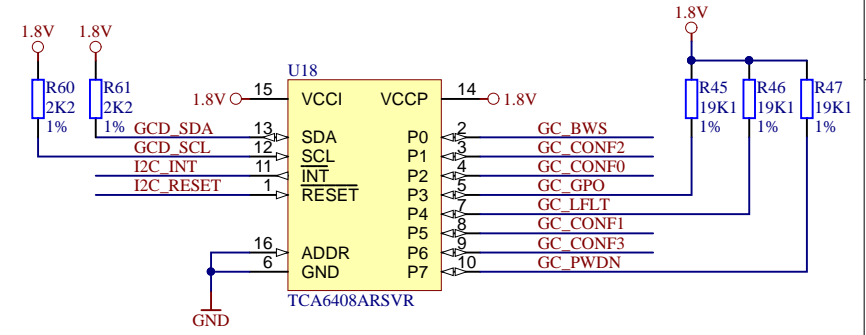
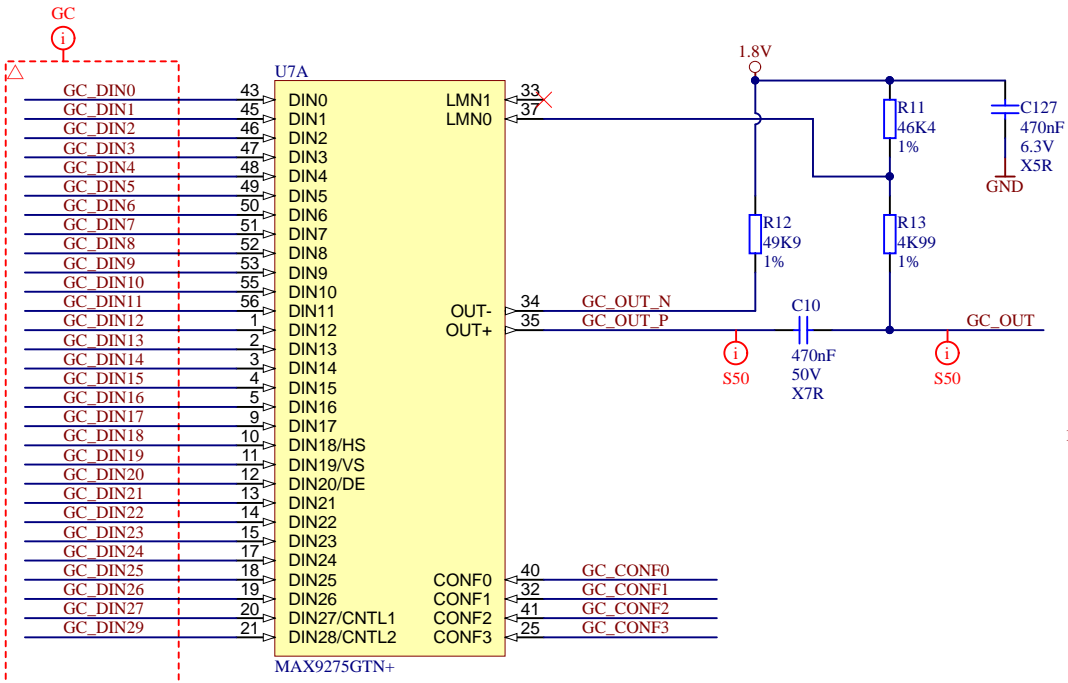
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A4	Number: TEF0003 PROTO	Rev. 01
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A4	Number: TEF0003 PROTO	Rev. 01
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Filename: GMSL_C.SchDoc		

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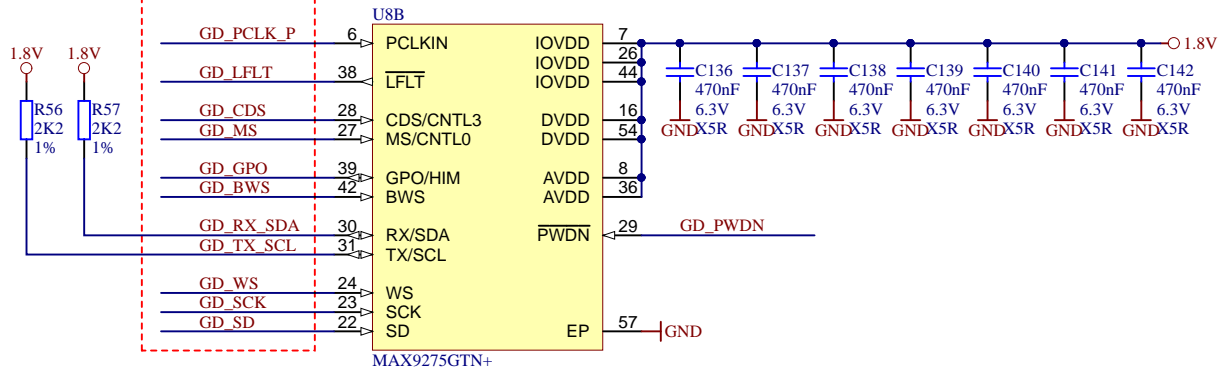
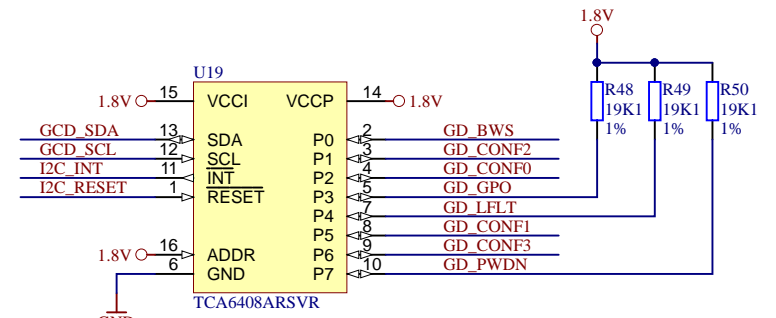
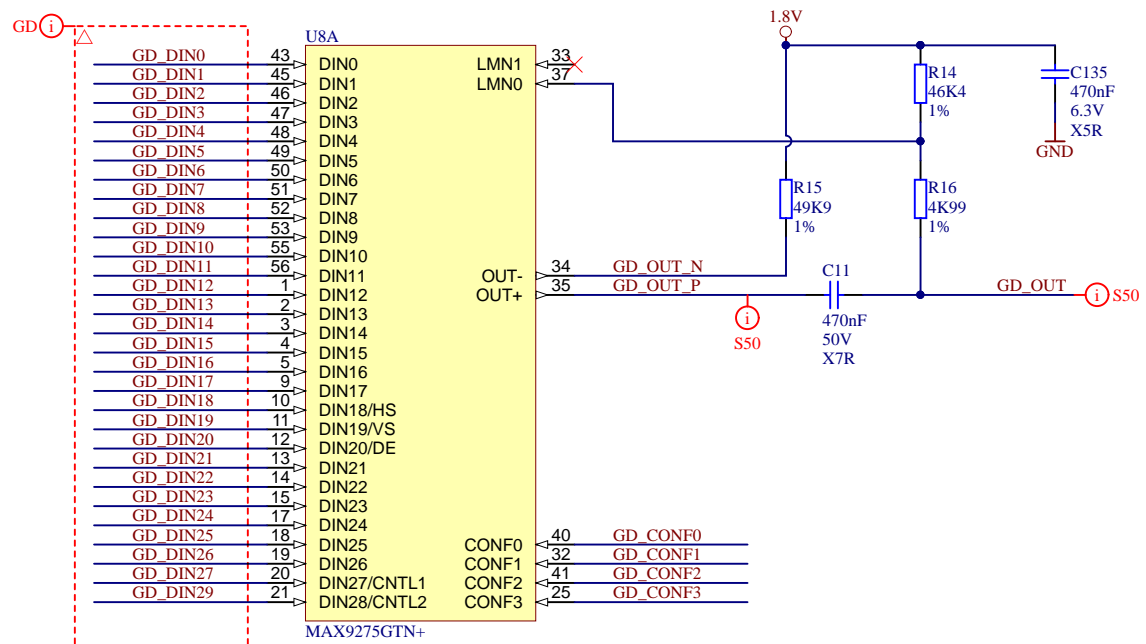
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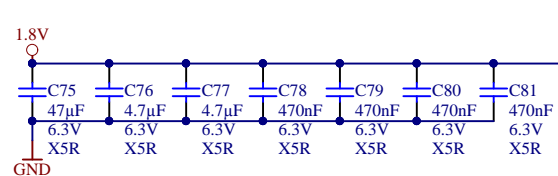
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UIB

		BANK 14			
	M14	VCCO_14	IO_L10P_T1_D14_14	AB21	GB_GPO
	F18	VCCO_14	IO_L10N_T1_D15_14	AB22	GB_TX_SCL
	F15	VCCO_14	IO_L11P_T1_SRCC_14	U20	GB_PCLK_N
	T22	VCCO_14	IO_L11N_T1_SRCC_14	V20	GB_DIN21
	U19	VCCO_14	IO_L12P_T1_MRCC_14	W19	GB_DIN1
	Y20	VCCO_14	IO_L12N_T1_MRCC_14	W20	GB_DIN14
			IO_L13P_T2_MRCC_14	Y18	GB_DIN10
			IO_L13N_T2_MRCC_14	Y19	GB_DIN5
			IO_L14P_T2_SRCC_14	V18	GB_DIN7
			IO_L14N_T2_SRCC_14	V19	GB_DIN13
			IO_L15P_T2_DQS_RDWR_B_14	AA19	GC_RX_SDA
			IO_L15N_T2_DQS_DOUT_CSO_B_14	AB20	GB_DIN2
			IO_L16P_T2_CSI_B_14	V17	GB_DIN11
			IO_L16N_T2_A15_D31_14	W17	GB_DIN9
			IO_L17P_T2_A14_D30_14	AA18	GC_PWDN
			IO_L17N_T2_A13_D29_14	AB18	GC_TX_SCL
			IO_L18P_T2_A12_D28_14	U17	GB_DIN6
			IO_L18N_T2_A11_D27_14	U18	GB_DIN15
			IO_L19P_T3_A10_D26_14	P14	GB_DIN0
			IO_L19N_T3_A09_D25_VREF_14	R14	GB_DIN4
			IO_L20P_T3_A08_D24_14	R18	GB_DIN19
			IO_L20N_T3_A07_D23_14	T18	GB_DIN18
			IO_L21P_T3_DQS_14	N17	GB_DIN29
			IO_L21N_T3_DQS_A06_D22_14	P17	GB_DIN23
			IO_L22P_T3_A05_D21_14	P15	GB_DIN20
			IO_L22N_T3_A04_D20_14	R16	GB_DIN8
			IO_L23P_T3_A03_D19_14	N13	GB_DIN3
			IO_L23N_T3_A02_D18_14	N14	GB_DIN12
			IO_L24P_T3_A01_D17_14	P16	GB_DIN27
			IO_L24N_T3_A00_D16_14	R17	GB_DIN16

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- SPI-DQ0
- SPI-DQ1
- SPI-DQ2
- SPI-DQ3

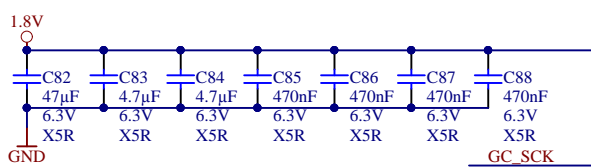
- GB_DIN26
- GB_DIN17
- P22
- R22
- P21
- R21
- U21
- V21
- T21
- U21
- P19
- R19
- T19
- T20
- W21
- W21
- W21
- AA21
- AA21
- Y21
- Y22

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UIA

		BANK 13			
	V16	VCCO_13	IO_L7P_T1_13	AB11	GC_DIN18
	W13	VCCO_13	IO_L7N_T1_13	AB12	GC_DIN20
	Y10	VCCO_13	IO_L8P_T1_13	AA9	GC_DIN4
	AA17	VCCO_13	IO_L8N_T1_13	AB10	
	AB14	VCCO_13	IO_L9P_T1_DQS_13	AA10	GC_DIN2
			IO_L9N_T1_DQS_13	AA11	GC_DIN19
			IO_L10P_T1_13	V10	GC_DIN12
			IO_L10N_T1_13	W10	GC_DIN13
			IO_L11P_T1_SRCC_13	Y11	GC_WS
			IO_L11N_T1_SRCC_13	Y12	GC_DIN10
			IO_L12P_T1_MRCC_13	W11	GC_PCLK_N
			IO_L12N_T1_MRCC_13	W12	GC_DIN14
			IO_L13P_T2_MRCC_13	V13	GC_DIN11
			IO_L13N_T2_MRCC_13	V14	GC_DIN3
			IO_L14P_T2_SRCC_13	U15	GC_DIN1
			IO_L14N_T2_SRCC_13	V15	GC_DIN6
			IO_L15P_T2_DQS_13	T14	GC_DIN17
			IO_L15N_T2_DQS_13	T15	GC_DIN7
			IO_L16P_T2_13	W15	GC_DIN0
			IO_L16N_T2_13	W16	
			IO_L17P_T2_13	T16	GC_DIN15
			IO_L17N_T2_13	U16	GC_DIN16

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- GC_SCK
- Y16
- AA16
- AB16
- AB17
- AA13
- AB13
- AA15
- AB15
- Y13
- AA14
- W14
- Y14

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Date: 2017-06-20	Copyright: Trenz Electronic GmbH	Page9 of 16
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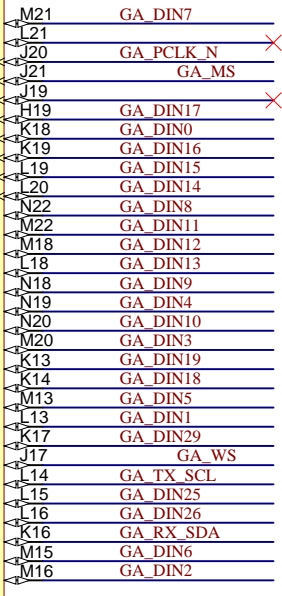
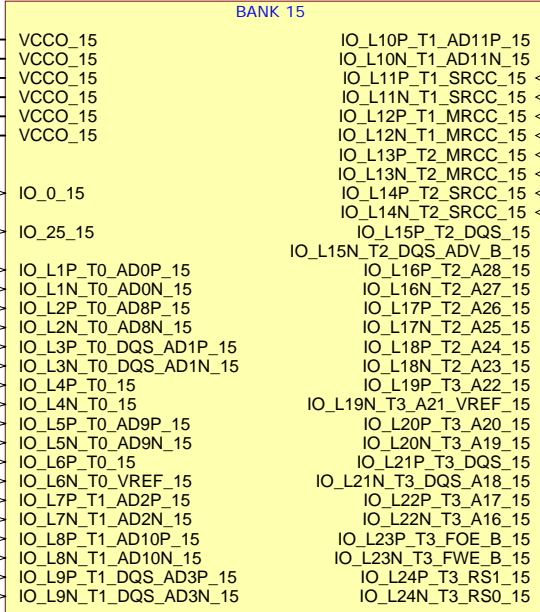
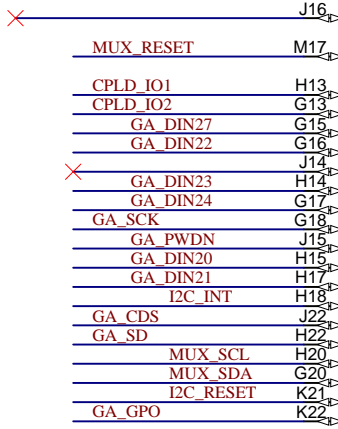
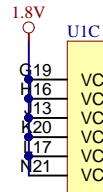
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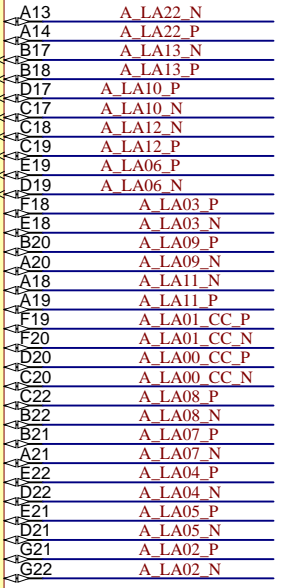
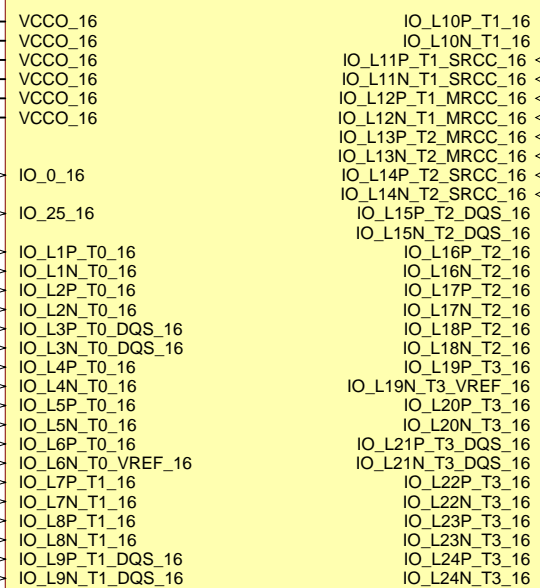
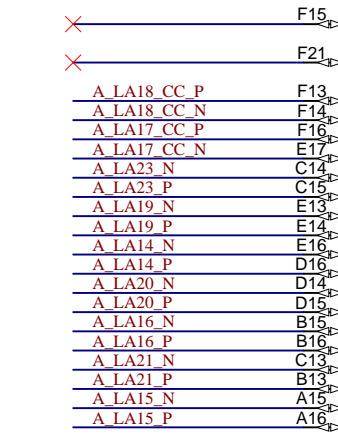
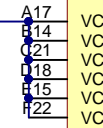
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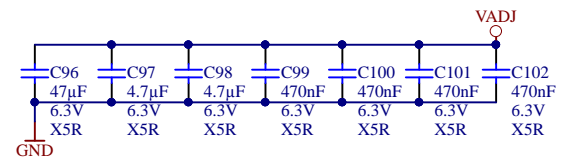
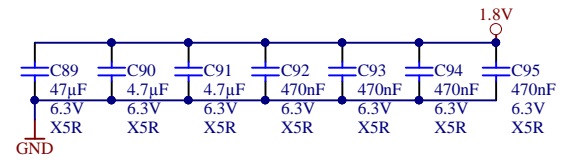


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UID



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Date: 2017-06-20	Copyright: Trenz Electronic GmbH	Page 10 of 16
Filename: B16.SchDoc		

A

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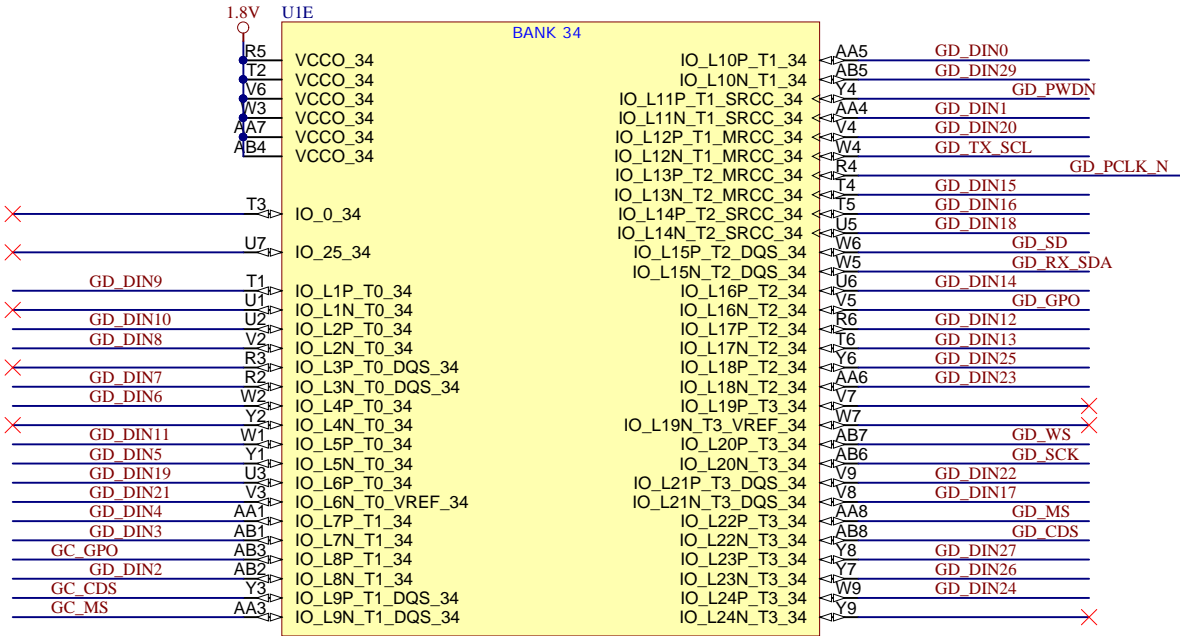
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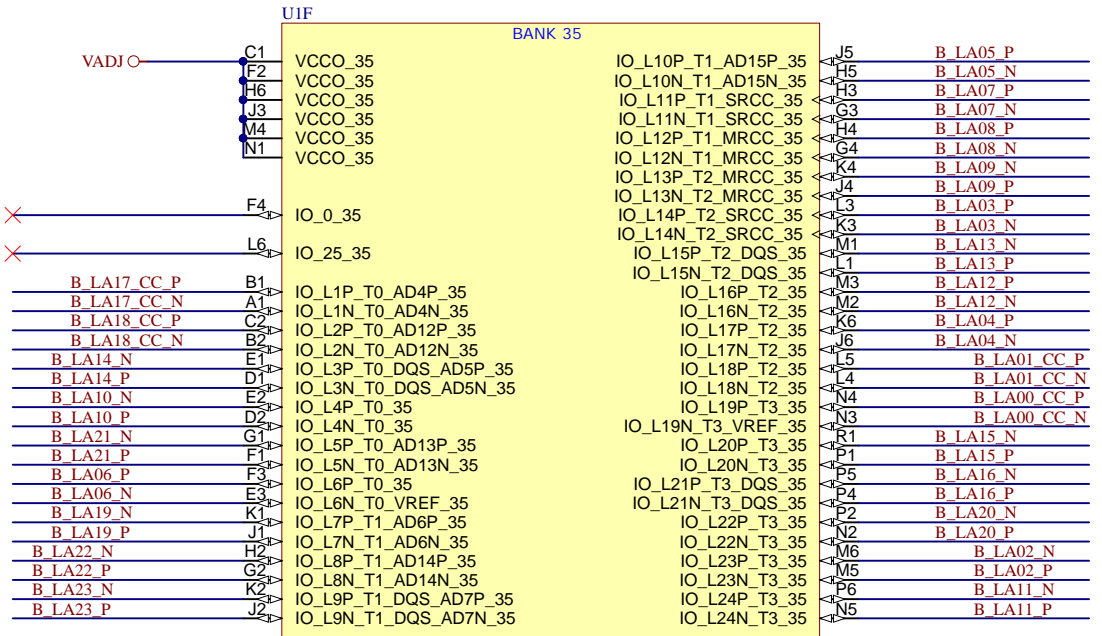
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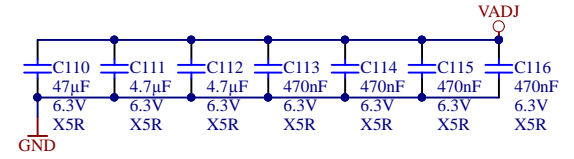
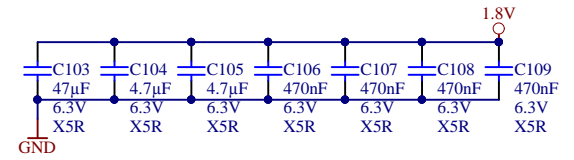
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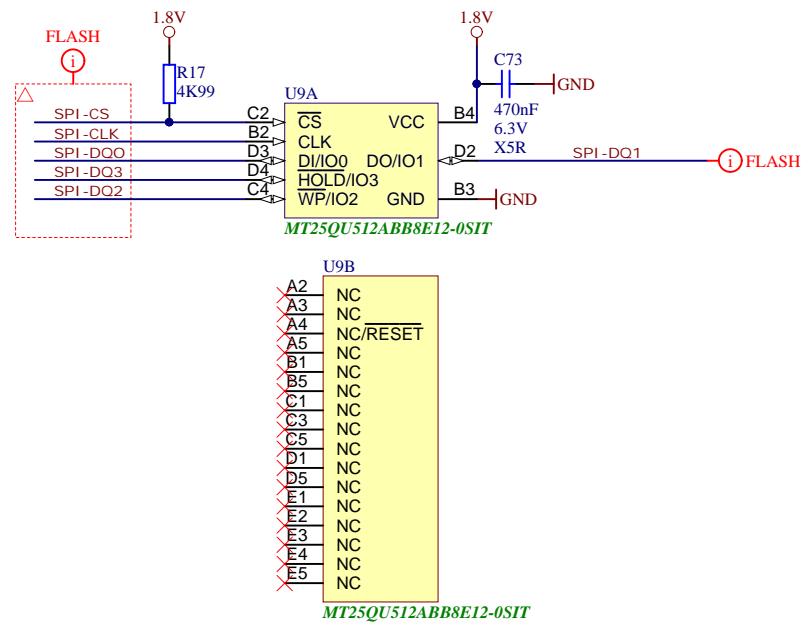
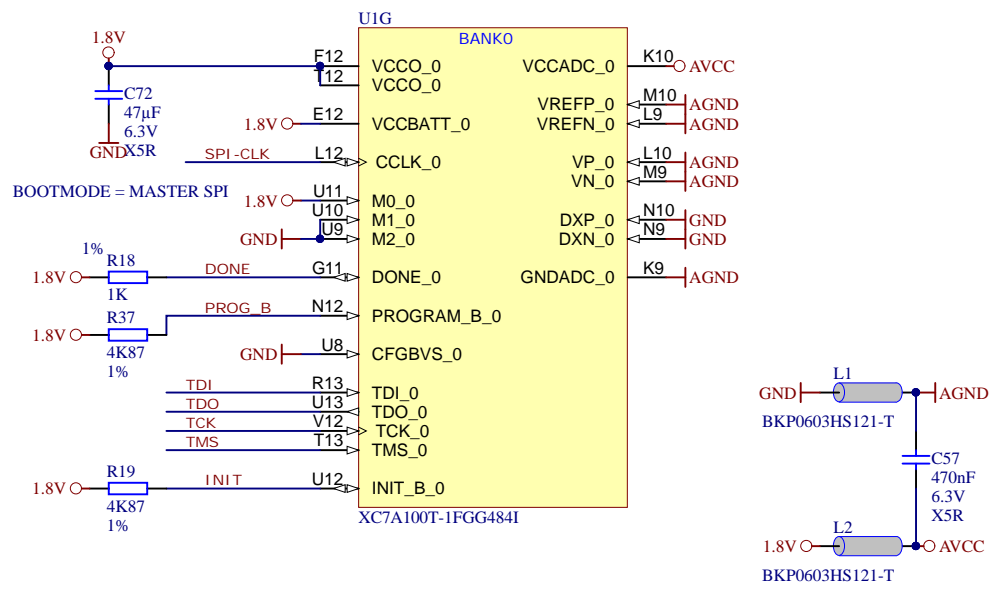
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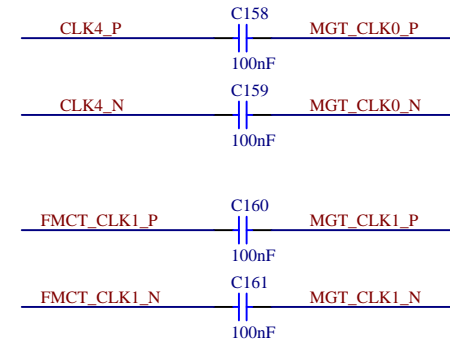
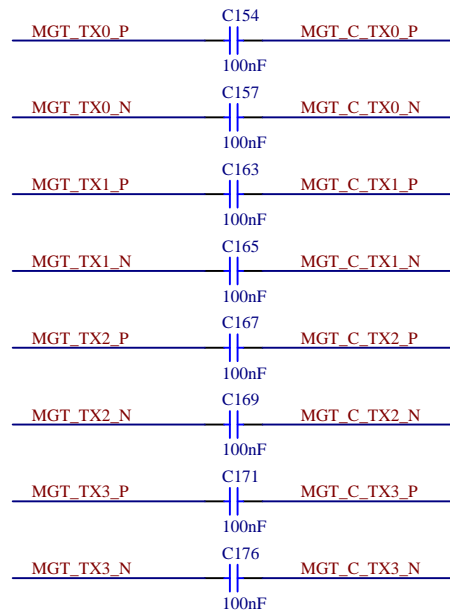
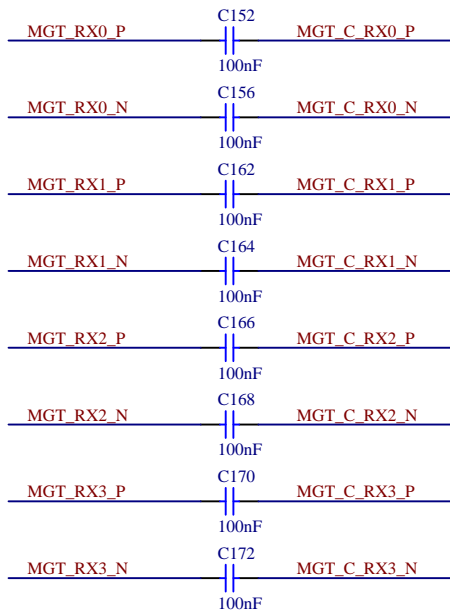
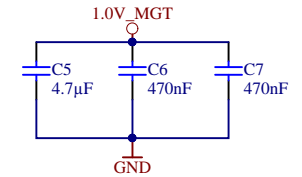
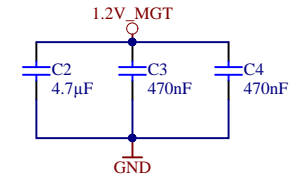
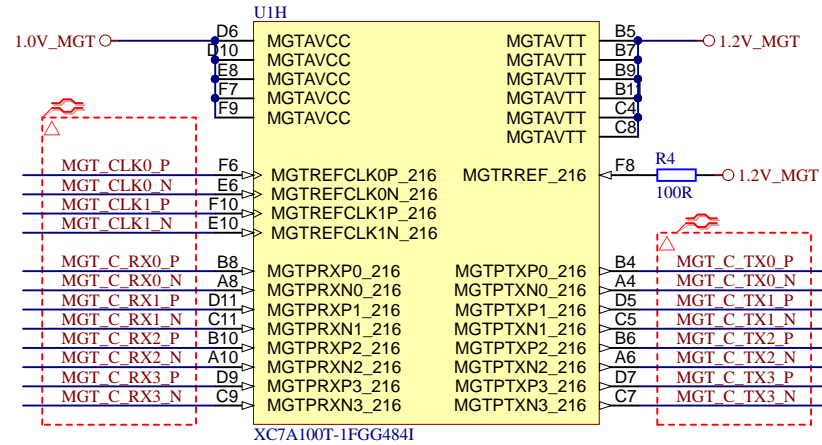
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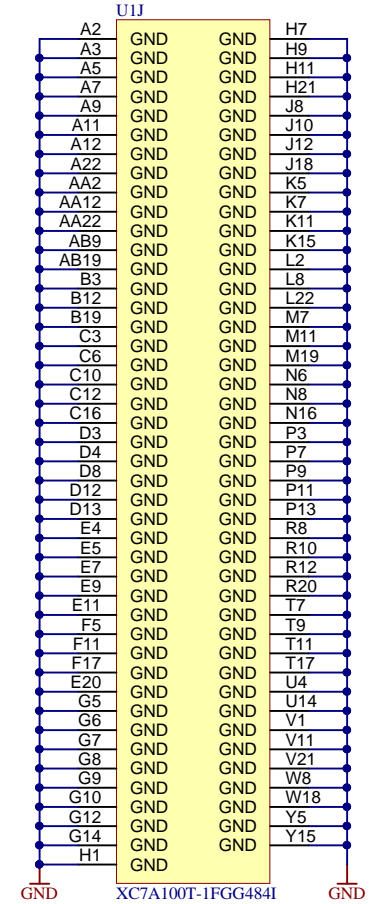
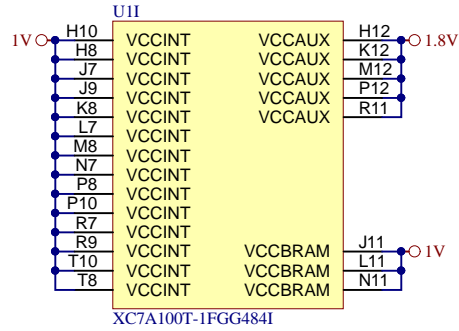
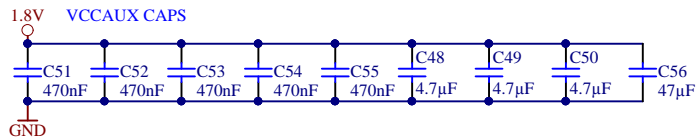
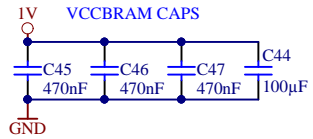
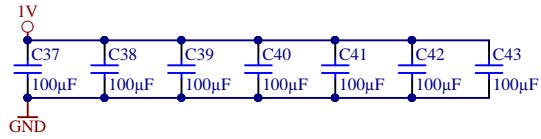
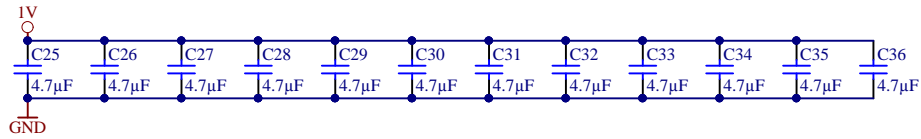
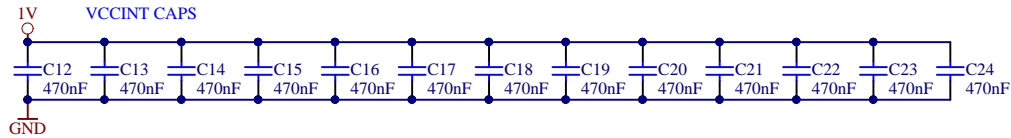
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Filename: B34.SchDoc		



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Filename: FPGA_MISC.SchDoc		



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	A4	Number: TEF0003 PROTO	Rev. 01
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	Filename: FPGA_MGT.SchDoc		



Title: TEF0003		
A4	Number: TEF0003 PROTO	Rev. 01
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Filename: FPGA-PWR.SchDoc		

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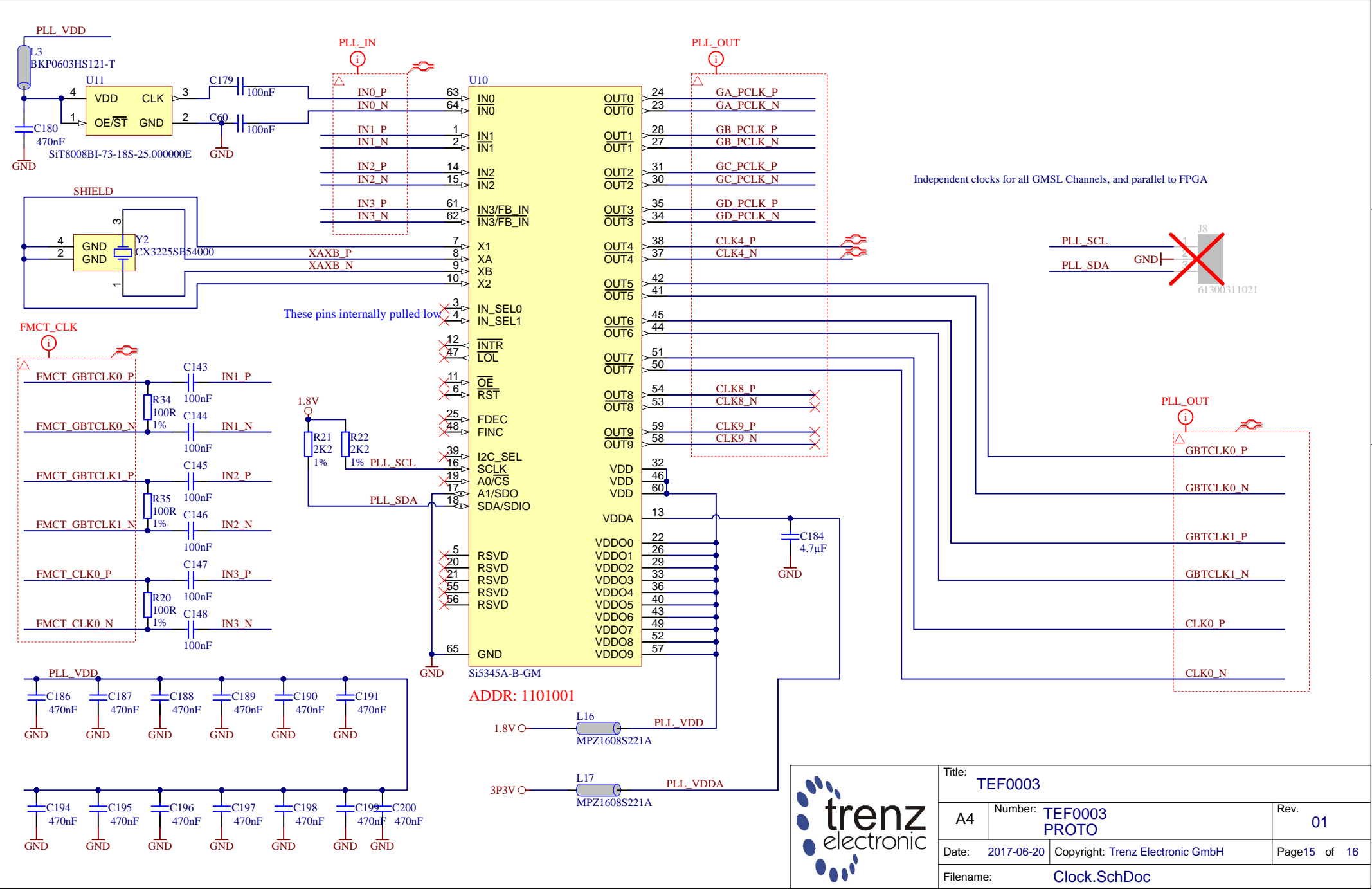
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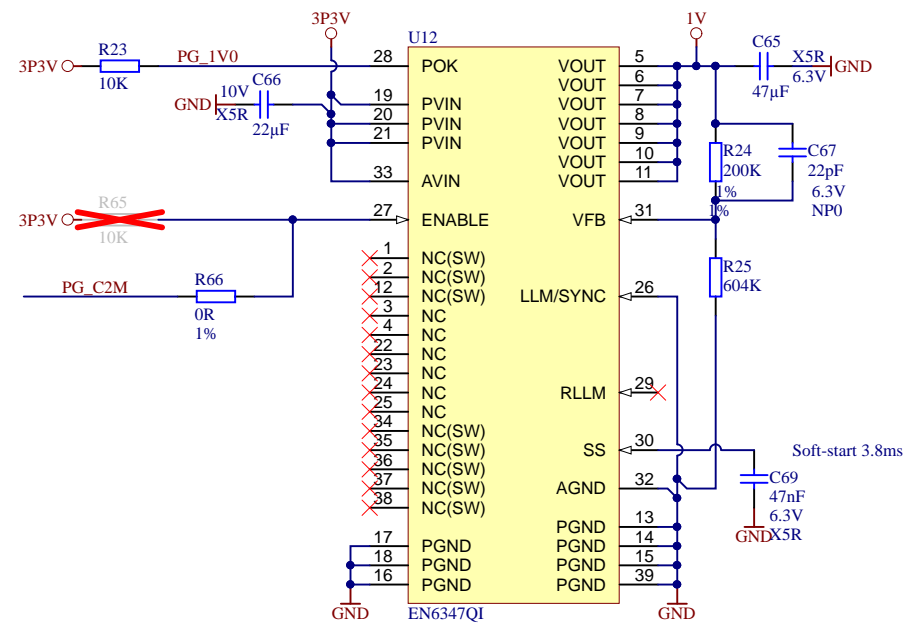
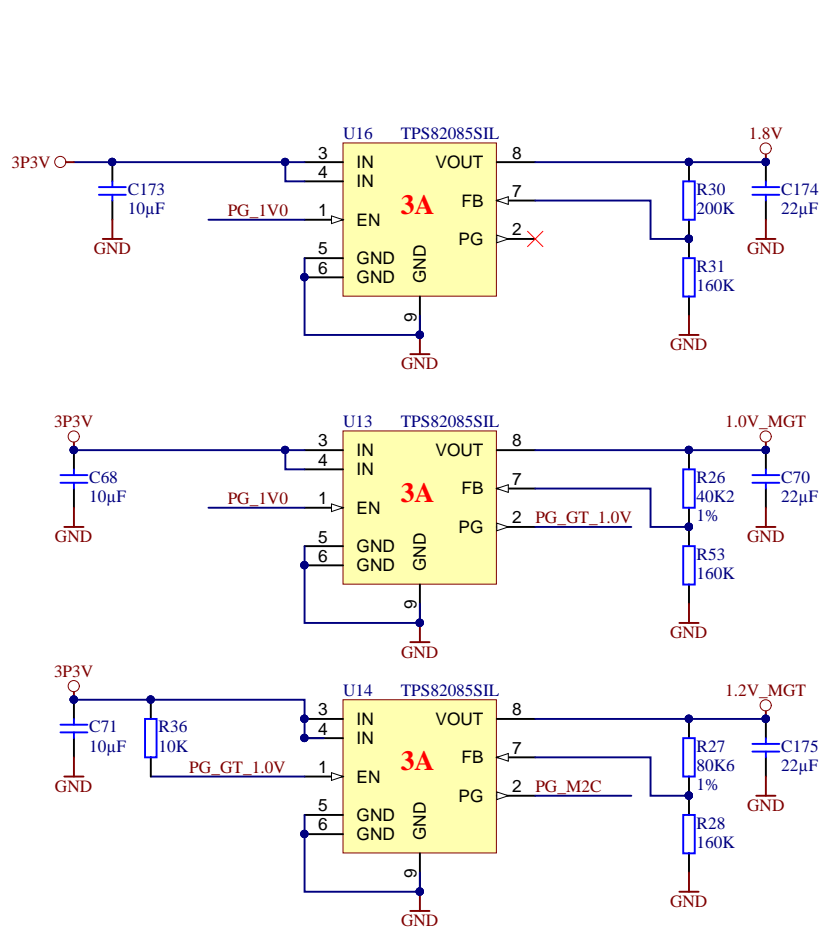
Independent clocks for all GMSL Channels, and parallel to FPGA


These pins internally pulled low

ADDR: 1101001



Title: TEF0003		
A4	Number: TEF0003 PROTO	Rev. 01
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		A4	Number: TEF0003 PROTO
Date: 2017-06-20		Copyright: Trenz Electronic GmbH	
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