FMC
FMC.SchDoc

DP_IC_SourceSide
DP_IC_SourceSide.SchDoc

DP_IC_SinkSide
DP_IC_SinkSide.SchDoc

MISC
MISC.SchDoc

MGT_CAPS
MGT_CAPS.SchDoc

PWR
PWR.SchDoc

CLOCK
Clock.SchDoc

PWR1
PWR1.SchDoc

B12
B12.SchDoc

B13
B13.SchDoc

B14
B14.SchDoc

B15
B15.SchDoc

B16
B16.SchDoc

B33
B33.SchDoc

B34
B34.SchDoc

FPGA-CFG
FPGA-CFG.SchDoc

FPGA-MGT
FPGA-MGT.SchDoc

FPGA-PWR
FPGA-PWR.SchDoc

LOGO1

TE Logo PRINT Layer

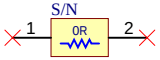
LOGO PRINT

Serial

Serial

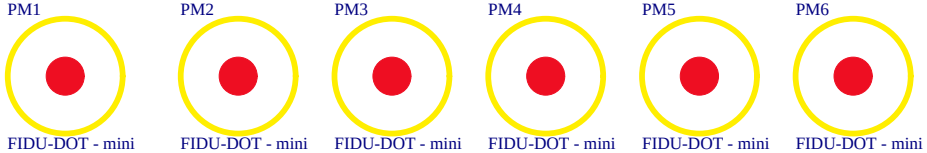
Serialnumber 6,3 x 6.3mm

S/N



Serialnumber

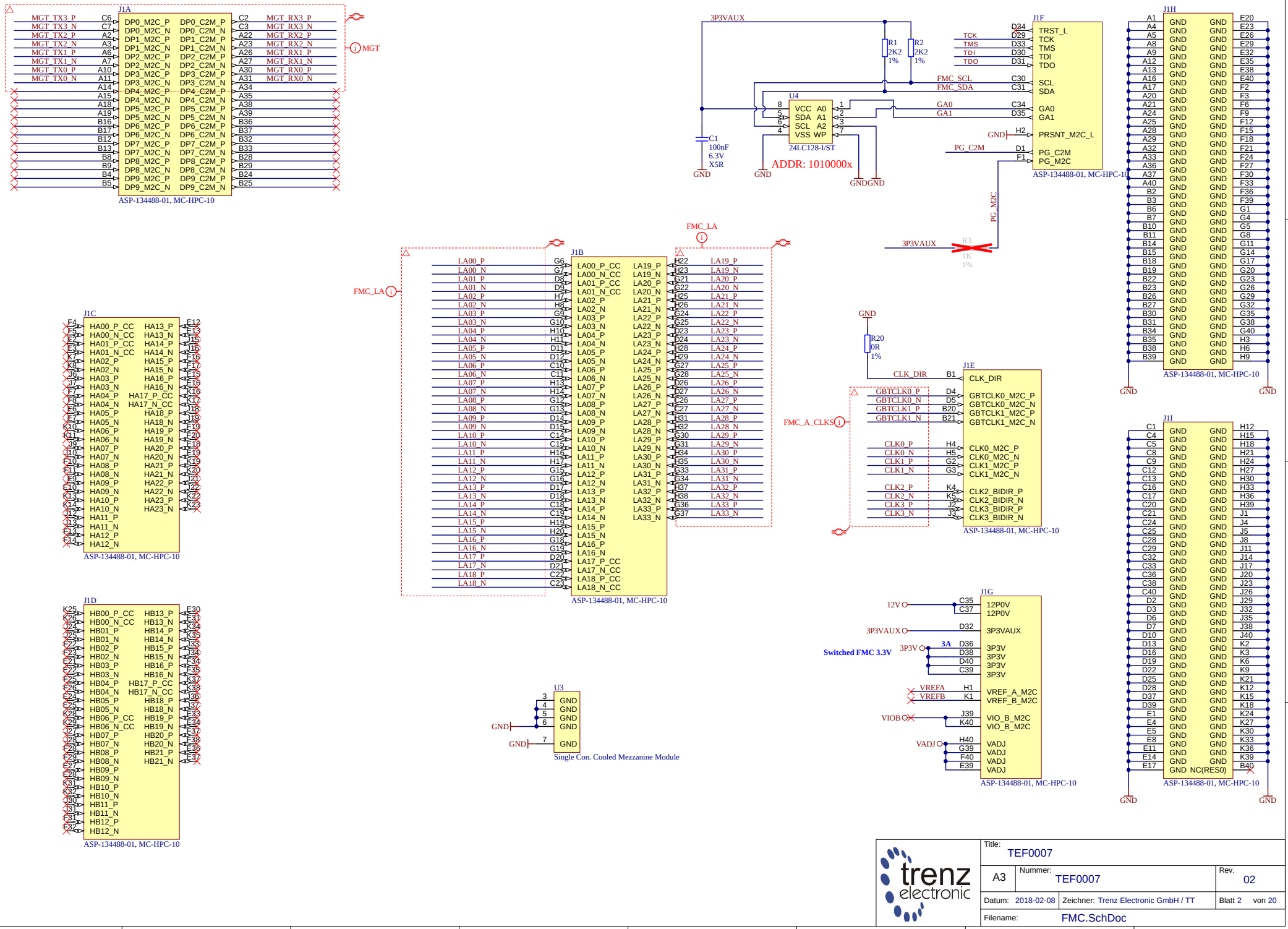
PM1 PM2 PM3 PM4 PM5 PM6



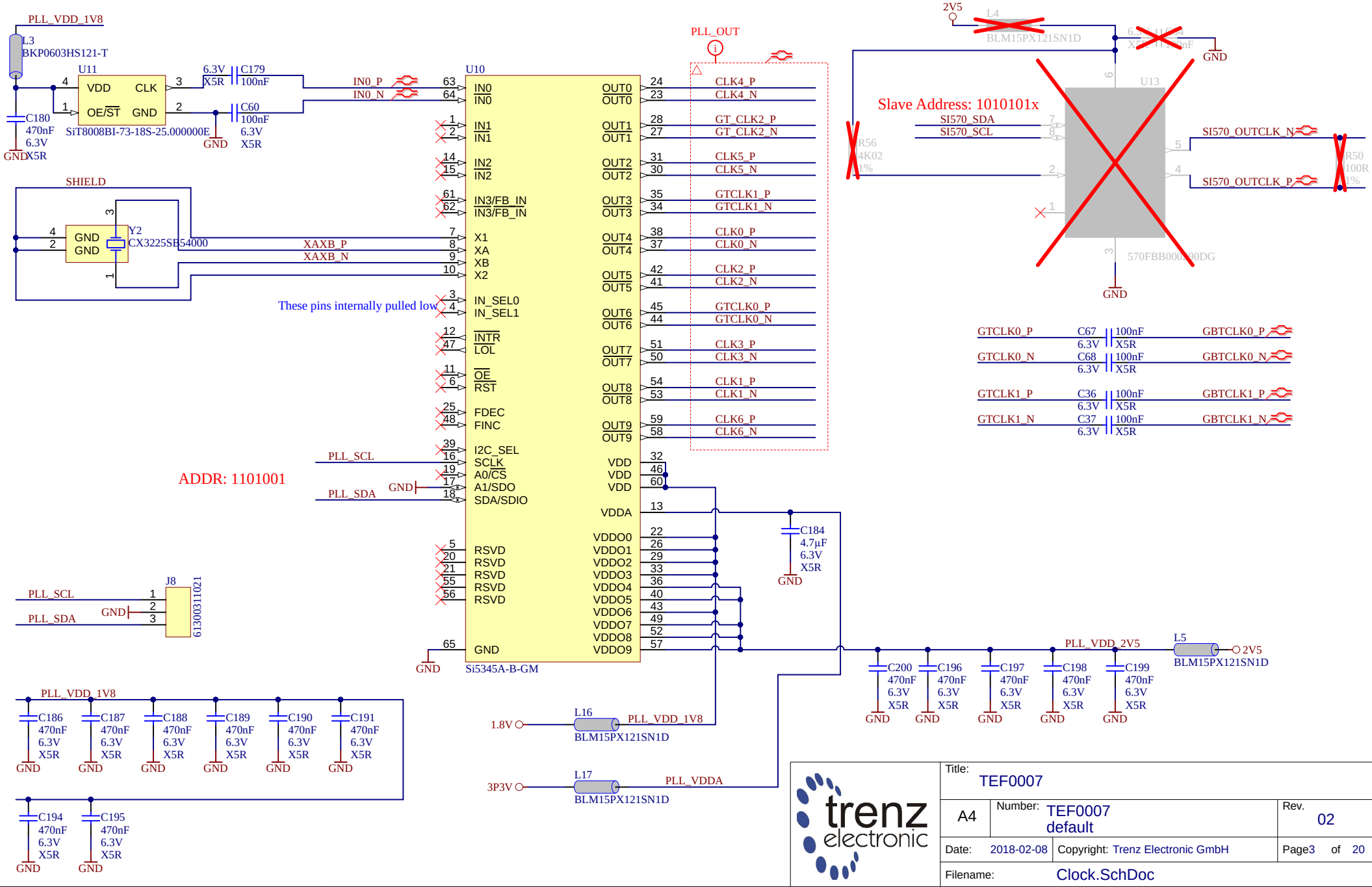
FIDU-DOT - mini FIDU-DOT - mini FIDU-DOT - mini FIDU-DOT - mini FIDU-DOT - mini FIDU-DOT - mini

trenz electronic

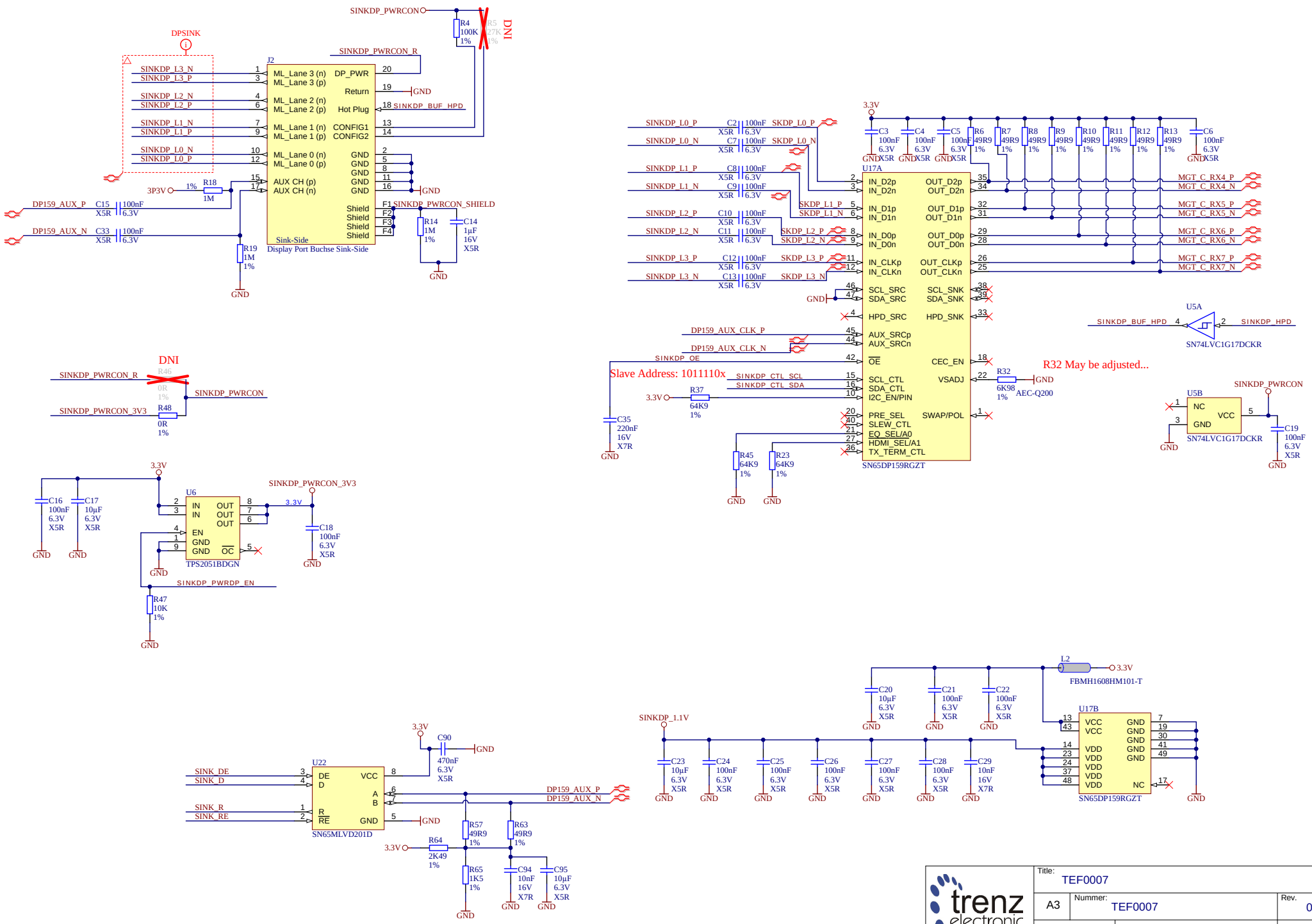
Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: Trenz Electronic GmbH / TT		Page1 of 20
Filename: TEF0007-01.SchDoc			



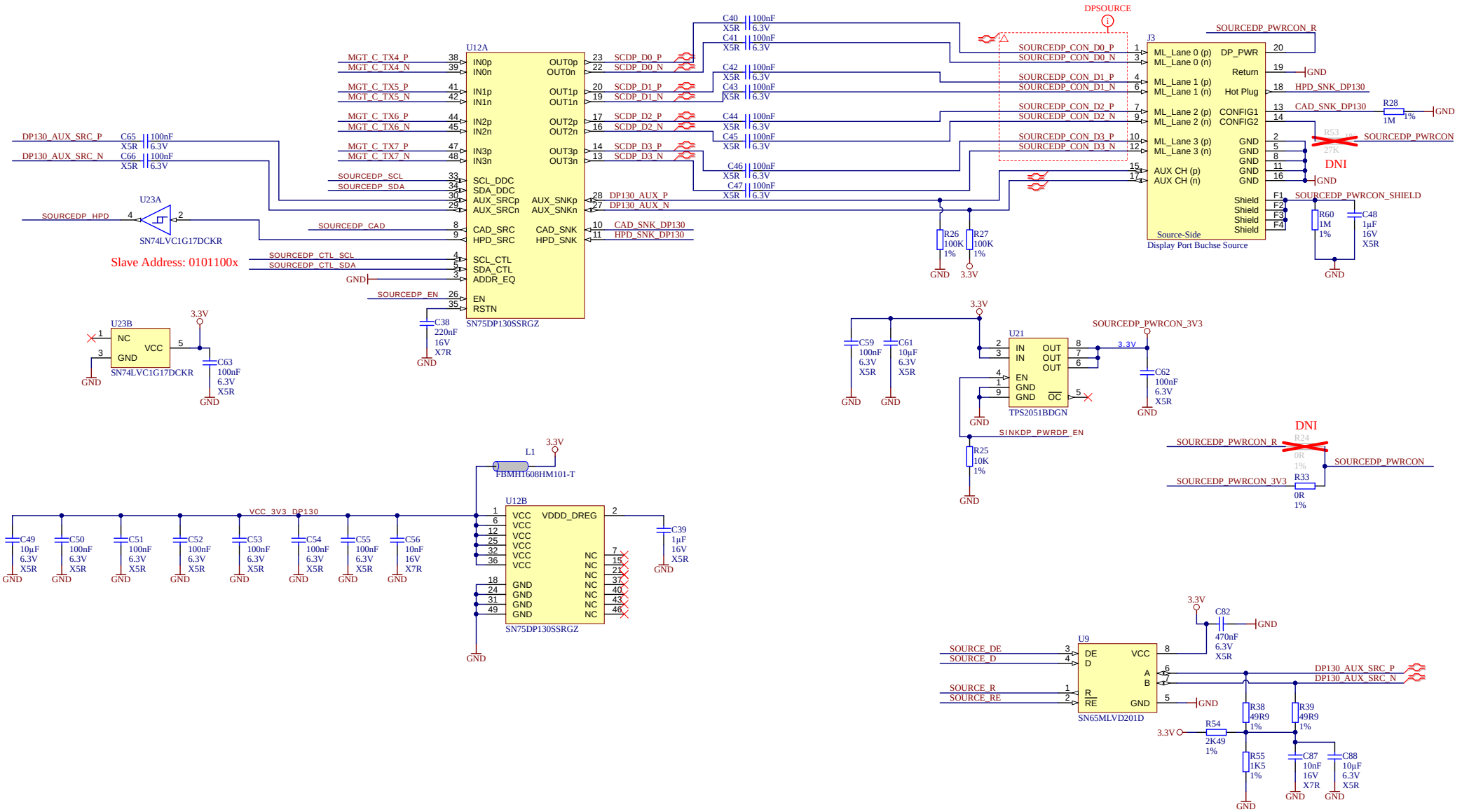
Title:	TEF0007		
A3	Nummer: TEF0007		Rev. 02
Datum: 2018-02-08	Zeichner: Trenz Electronic GmbH / TT		Blatt 2 von 20
Filename:	FMC.SchDoc		

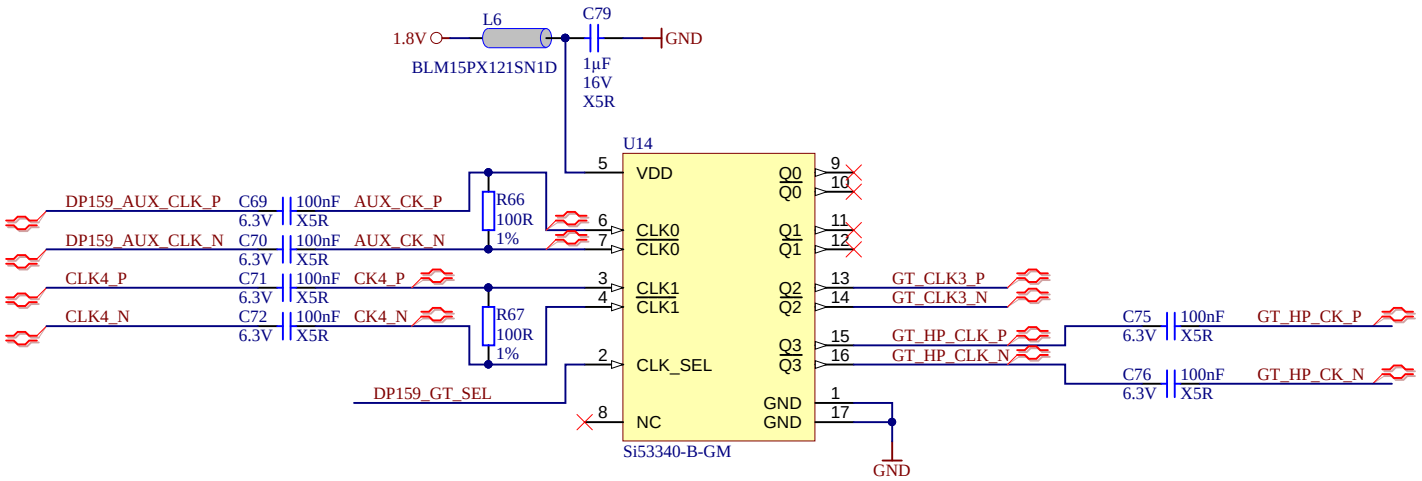


Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: Trenz Electronic GmbH		Page3 of 20
Filename: Clock.SchDoc			

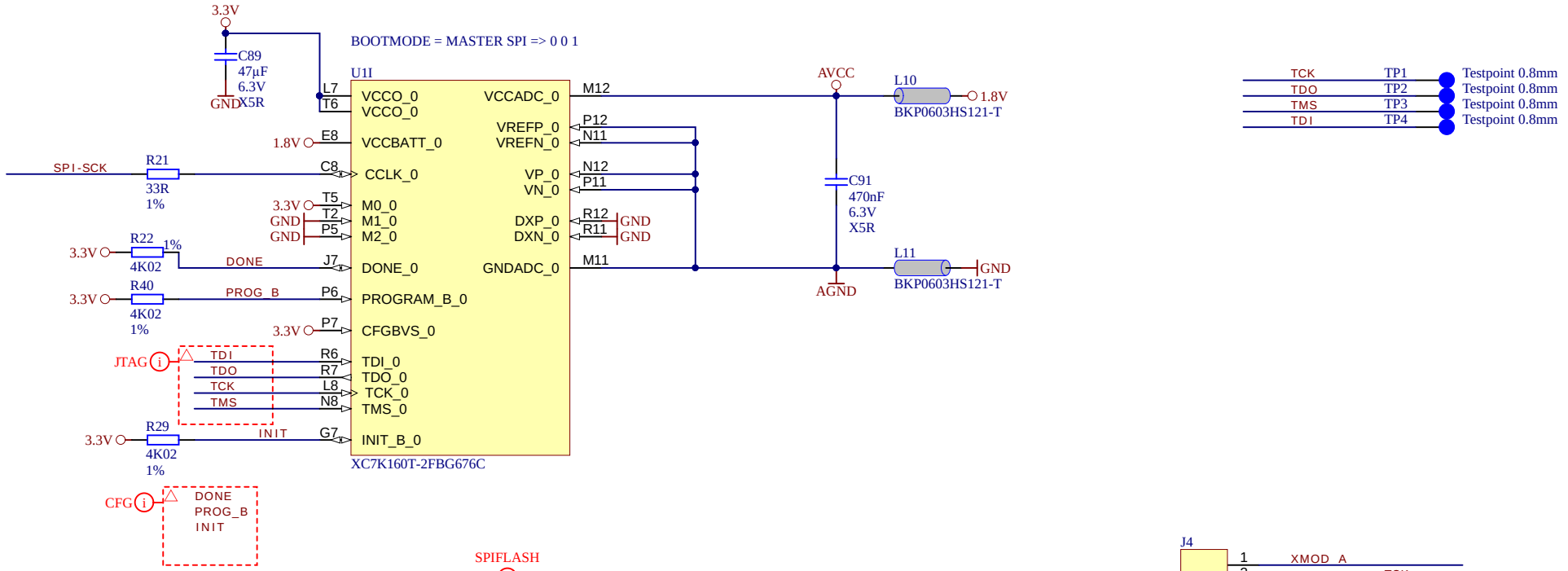


Title:	TEF0007		
A3	Nummer: TEF0007		Rev. 02
Datum: 2018-02-08	Zeichner: Trenz Electronic GmbH / TT		Blatt 4 von 20
Filename:	DP_IC_SinkSide.SchDoc		


U12A
SN75DP130SSRGZ
MGT_C_TX4_P
MGT_C_TX4_N
MGT_C_TX5_P
MGT_C_TX5_N
MGT_C_TX6_P
MGT_C_TX6_N
MGT_C_TX7_P
MGT_C_TX7_N
SCDP_D0_P
SCDP_D0_N
SCDP_D1_P
SCDP_D1_N
SCDP_D2_P
SCDP_D2_N
SCDP_D3_P
SCDP_D3_N
SOURCEDP_SCL
SOURCEDP_SDA
SOURCEDP_CTL_SCL
SOURCEDP_CTL_SDA
SOURCEDP_EN
SOURCEDP_CAD
DP130_AUX_P
DP130_AUX_N
CAD_SNK_DP130
HPD_SNK_DP130
DP130_AUX_SRC_P
DP130_AUX_SRC_N
U23A
SN74LVC1G17DCKR
SOURCEDP_HPD
Slave Address: 0101100x
U23B
SN74LVC1G17DCKR
DPSOURCE
J3
Source-Side
Display Port Buchse Source
SOURCEDP_CON_D0_P
SOURCEDP_CON_D0_N
SOURCEDP_CON_D1_P
SOURCEDP_CON_D1_N
SOURCEDP_CON_D2_P
SOURCEDP_CON_D2_N
SOURCEDP_CON_D3_P
SOURCEDP_CON_D3_N
SOURCEDP_PWRCON_R
SOURCEDP_PWRCON
SOURCEDP_PWRCON_SHIELD
DNI
U21
TPS2051BDGN
SOURCEDP_PWRCON_3V3
SINKDP_PWRDP_EN
L1
FBMH1608HM101-T
U12B
SN75DP130SSRGZ
VCC_3V3_DP130
U9
SN65MLVD201D
SOURCE_DE
SOURCE_D
SOURCE_R
SOURCE_RE
trenz electronic
Title: TEF0007
A3
Nummer: TEF0007
Rev. 02
Datum: 2018-02-08
Zeichner: Trenz Electronic GmbH / TT
Blatt 5 von 20
Filename: DP_IC_SourceSide.SchDoc

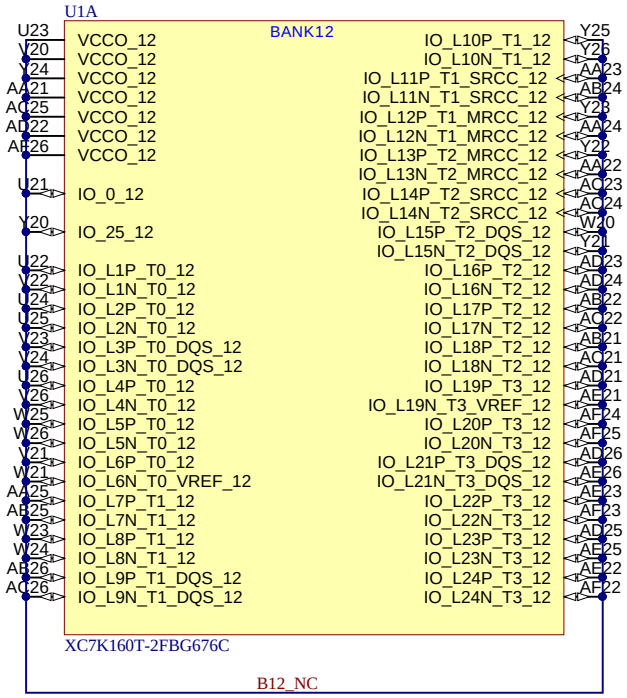


Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: Trenz Electronic GmbH / TT		Page6 of 20
Filename: MISC.SchDoc			



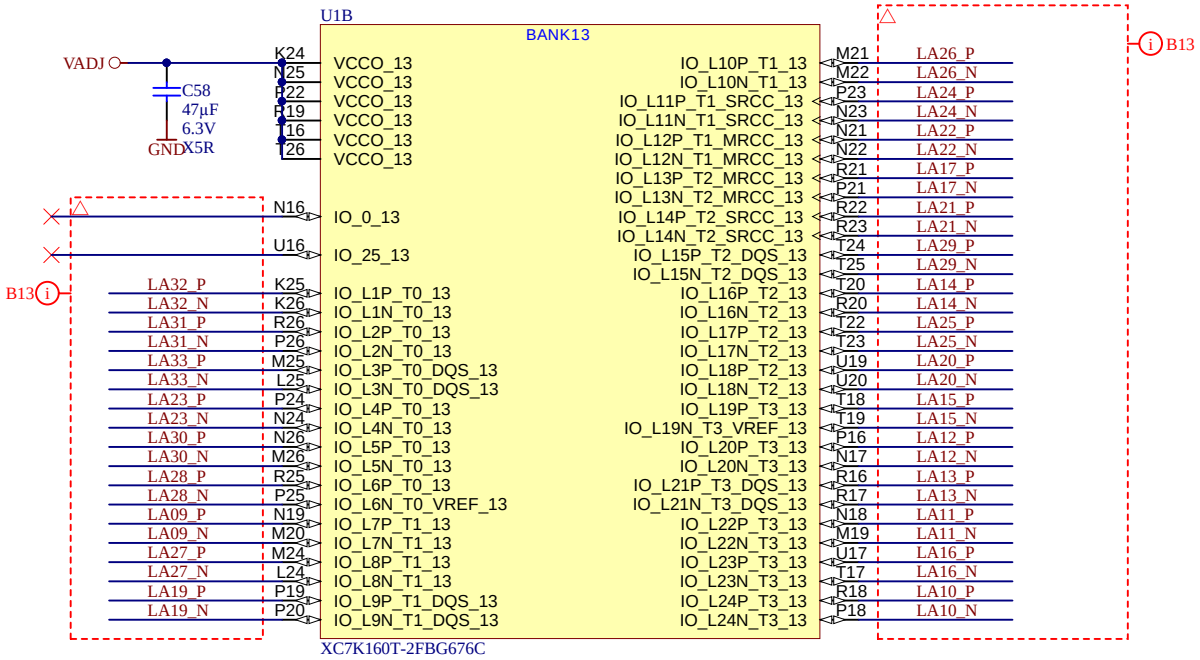
Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: 2013 Trenz Electronic GmbH		Page7 of 20
Filename: FPGA-CFG.SchDoc			

K70T version does not have this bank!

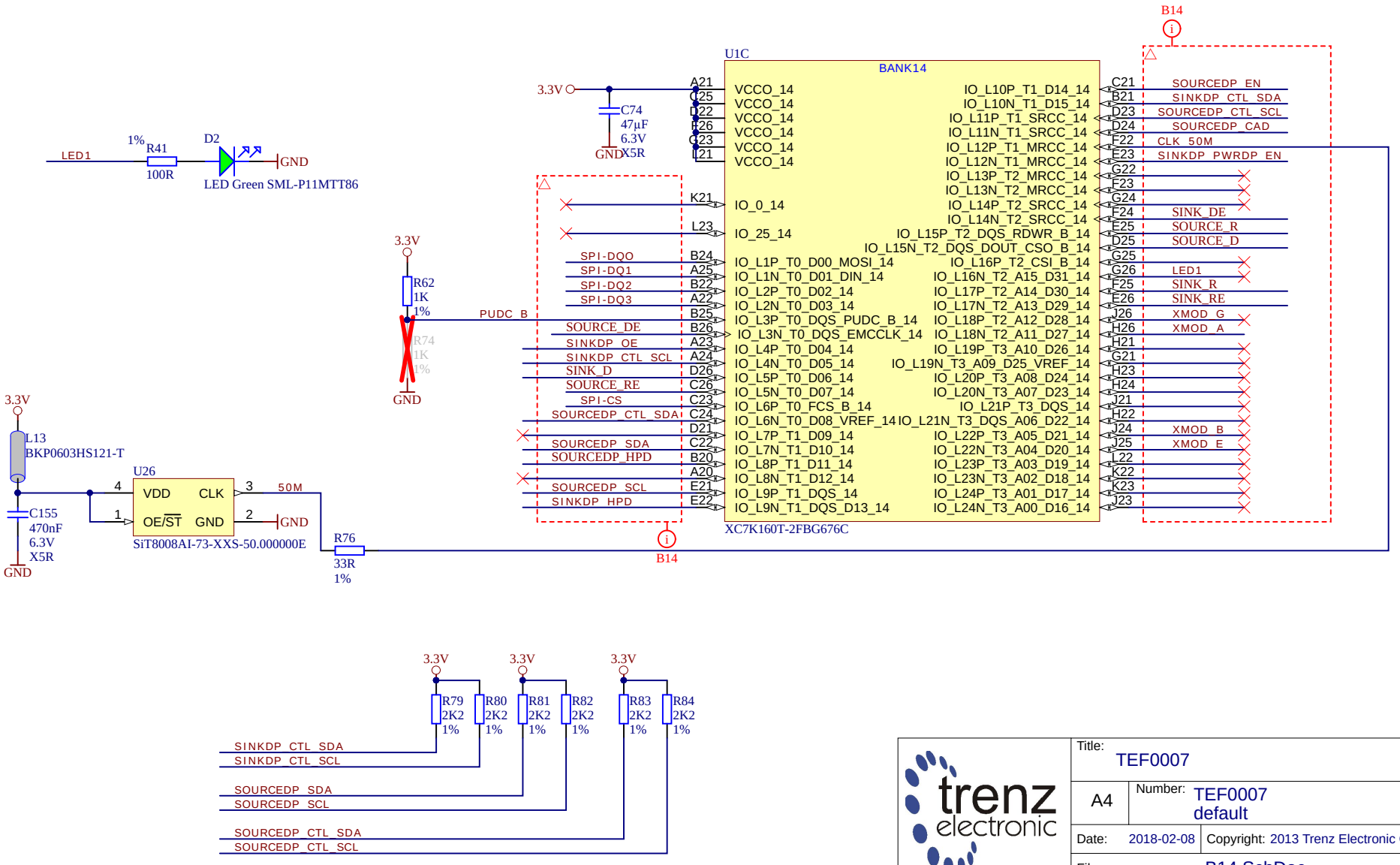


trenz electronic

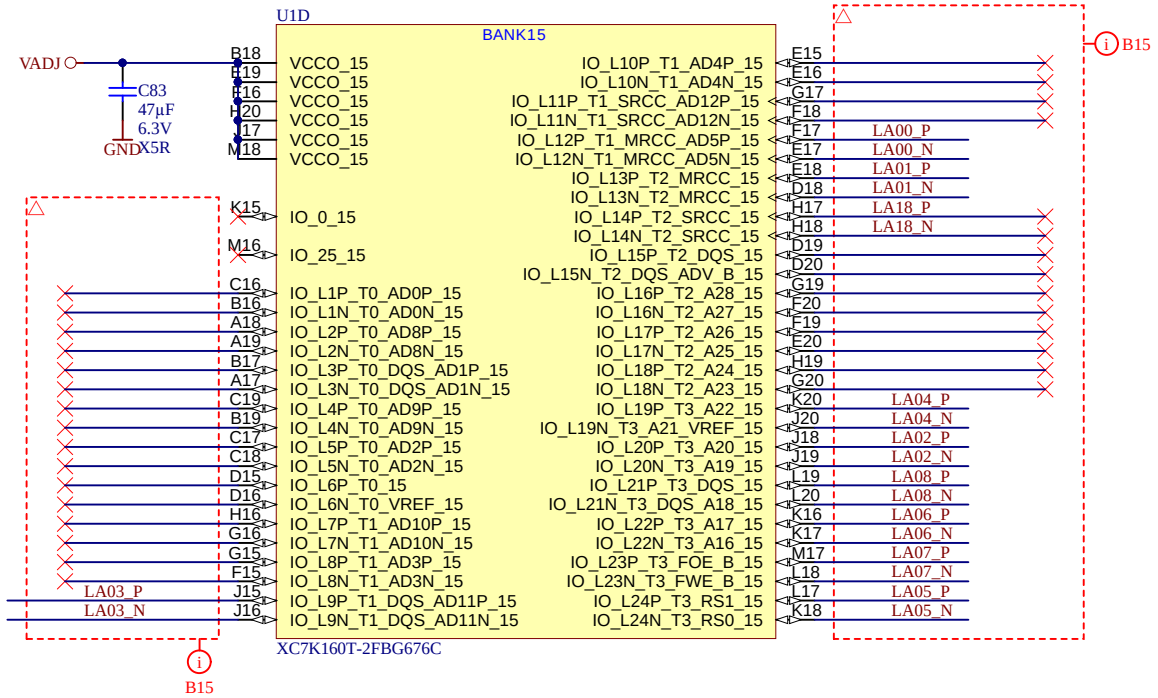
Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: 2013 Trenz Electronic GmbH		Page 8 of 20
Filename: B12.SchDoc			



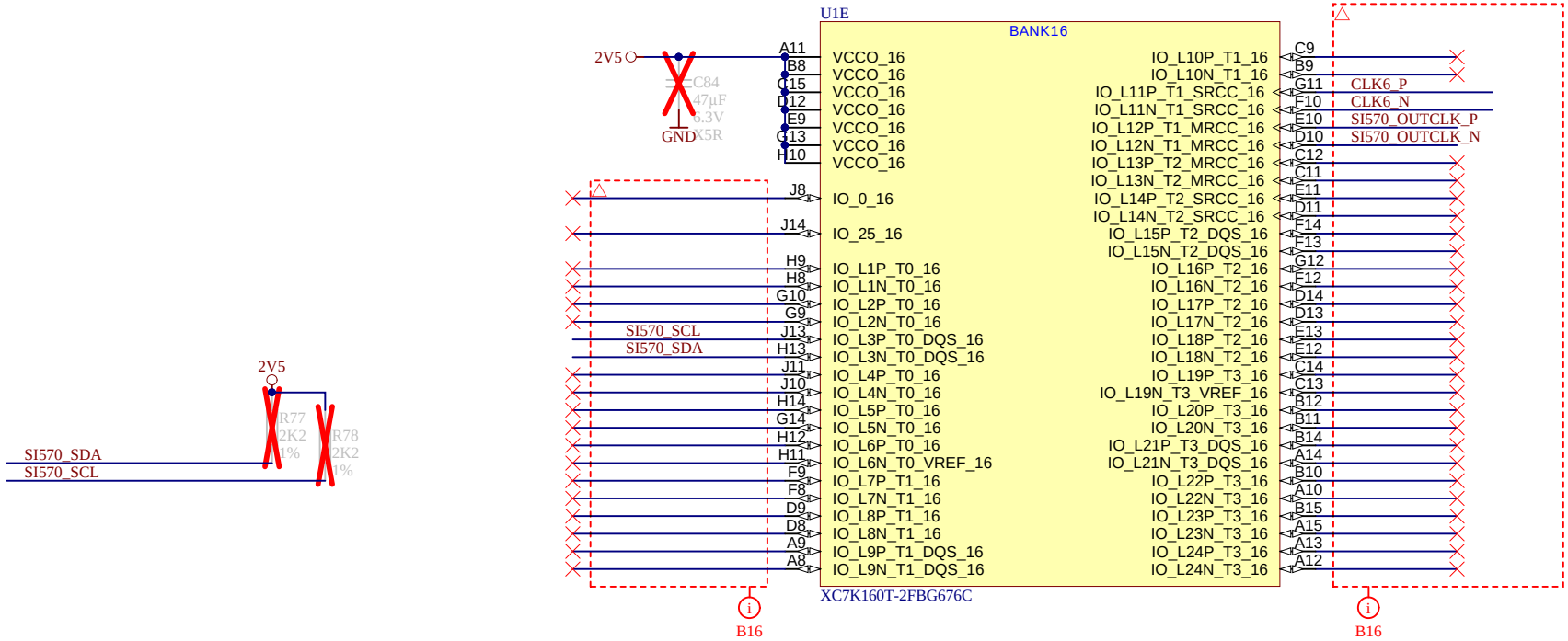
trenz electronic	Title: TEF0007		
	A4	Number: TEF0007 default	Rev. 02
	Date: 2018-02-08	Copyright: 2013 Trenz Electronic GmbH	Page9 of 20
	Filename: B13.SchDoc		



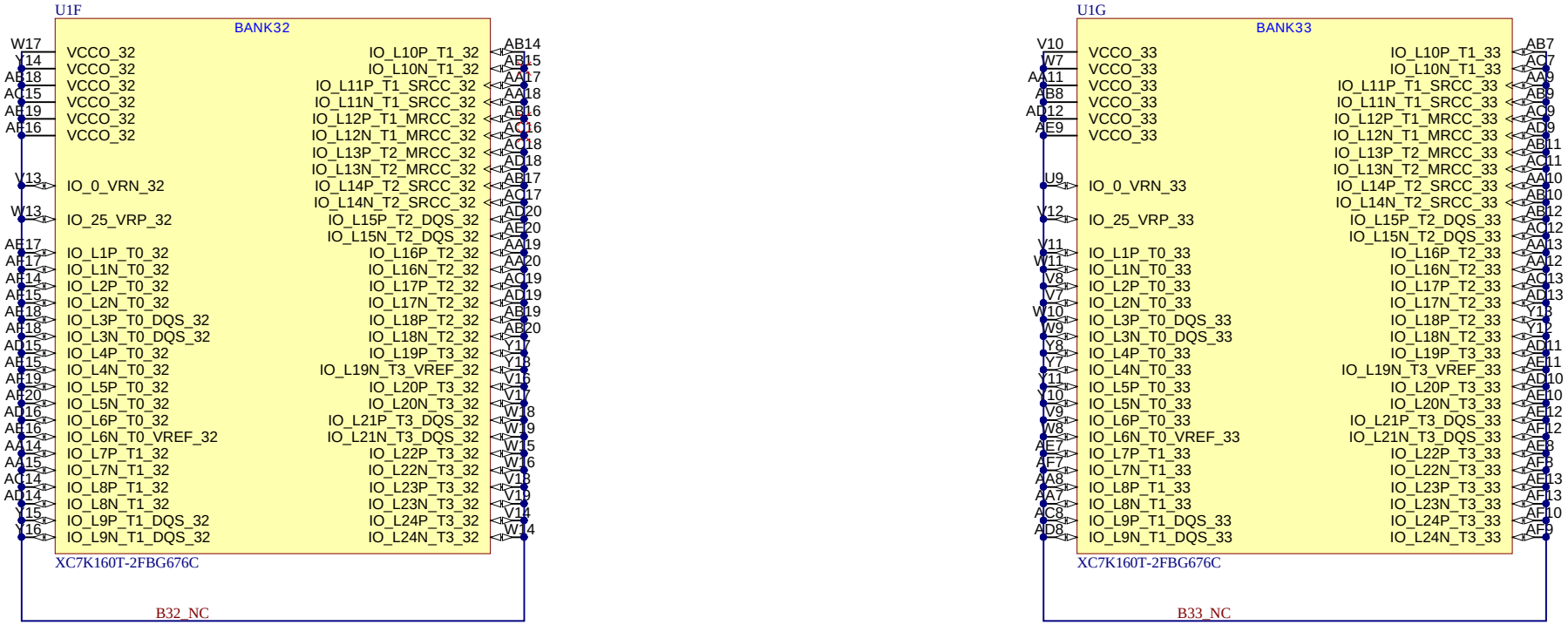
Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: 2013 Trenz Electronic GmbH		Page10 of 20
Filename: B14.SchDoc			



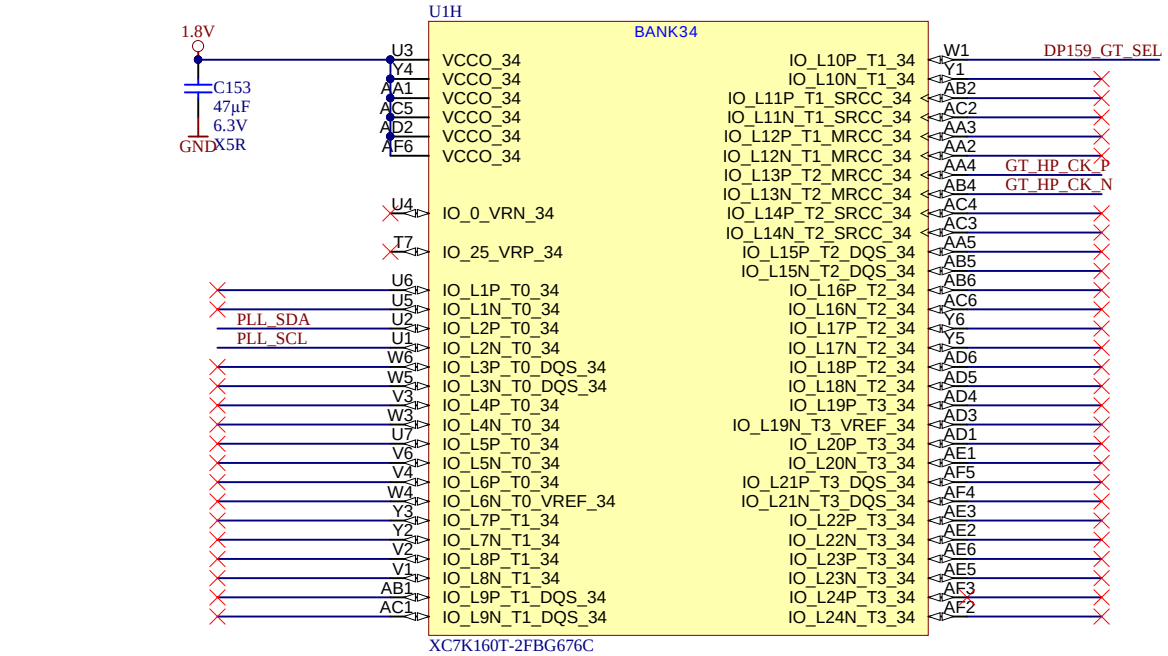
trenz electronic	Title: TEF0007		
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: 2013 Trenz Electronic GmbH		Page11 of 20
Filename: B15.SchDoc			



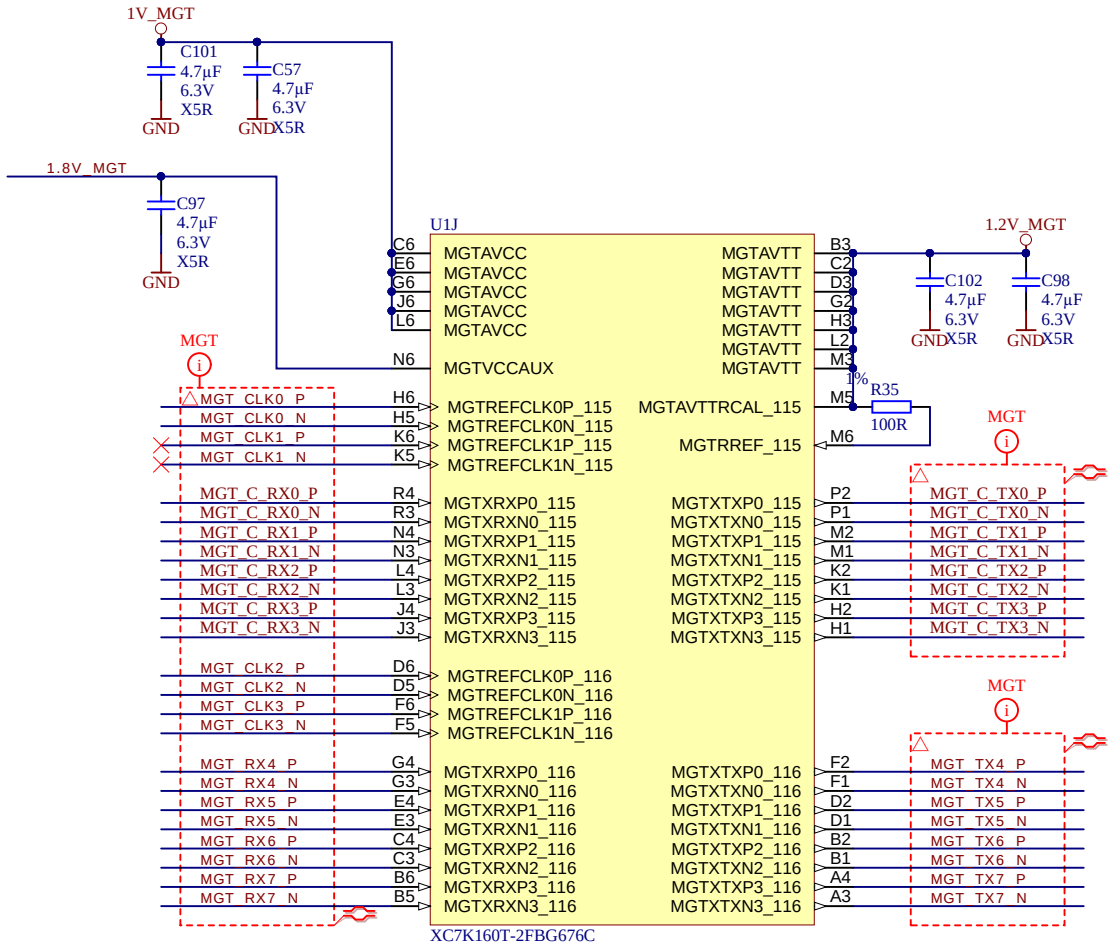
trenz electronic	Title: TEF0007		
	A4	Number: TEF0007 default	Rev. 02
	Date: 2018-02-08	Copyright: 2013 Trenz Electronic GmbH	Page12 of 20
	Filename: B16.SchDoc		



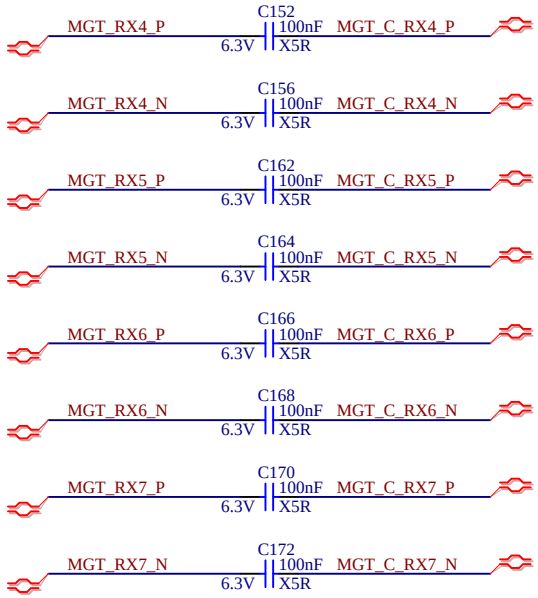
trenz electronic	Title: TEF0007		
	A4	Number: TEF0007 default	Rev. 02
	Date: 2018-02-08	Copyright: 2013 Trenz Electronic GmbH	Page13 of 20
	Filename: B33.SchDoc		

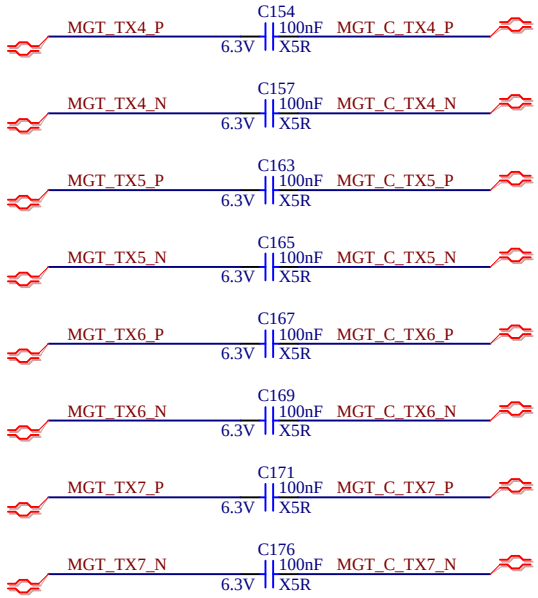


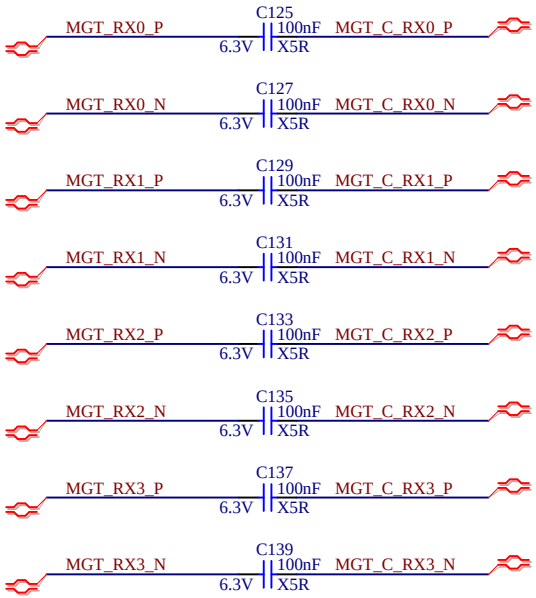
Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: 2013 Trenz Electronic GmbH		Page14 of 20
Filename: B34.SchDoc			

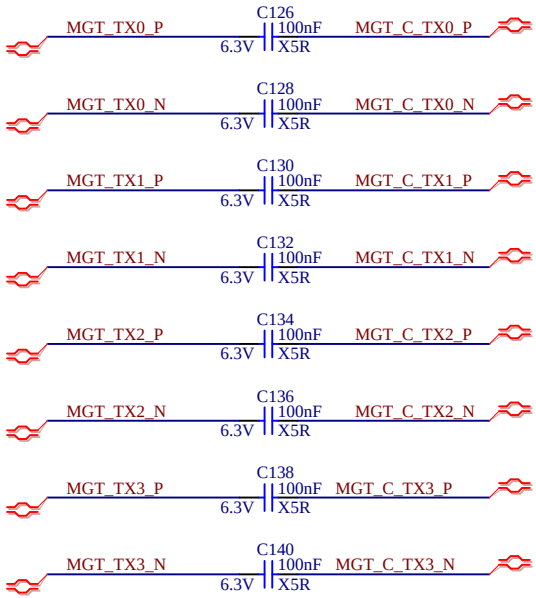


Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: 2013 Trenz Electronic GmbH		Page15 of 20
Filename: FPGA-MGT.SchDoc			



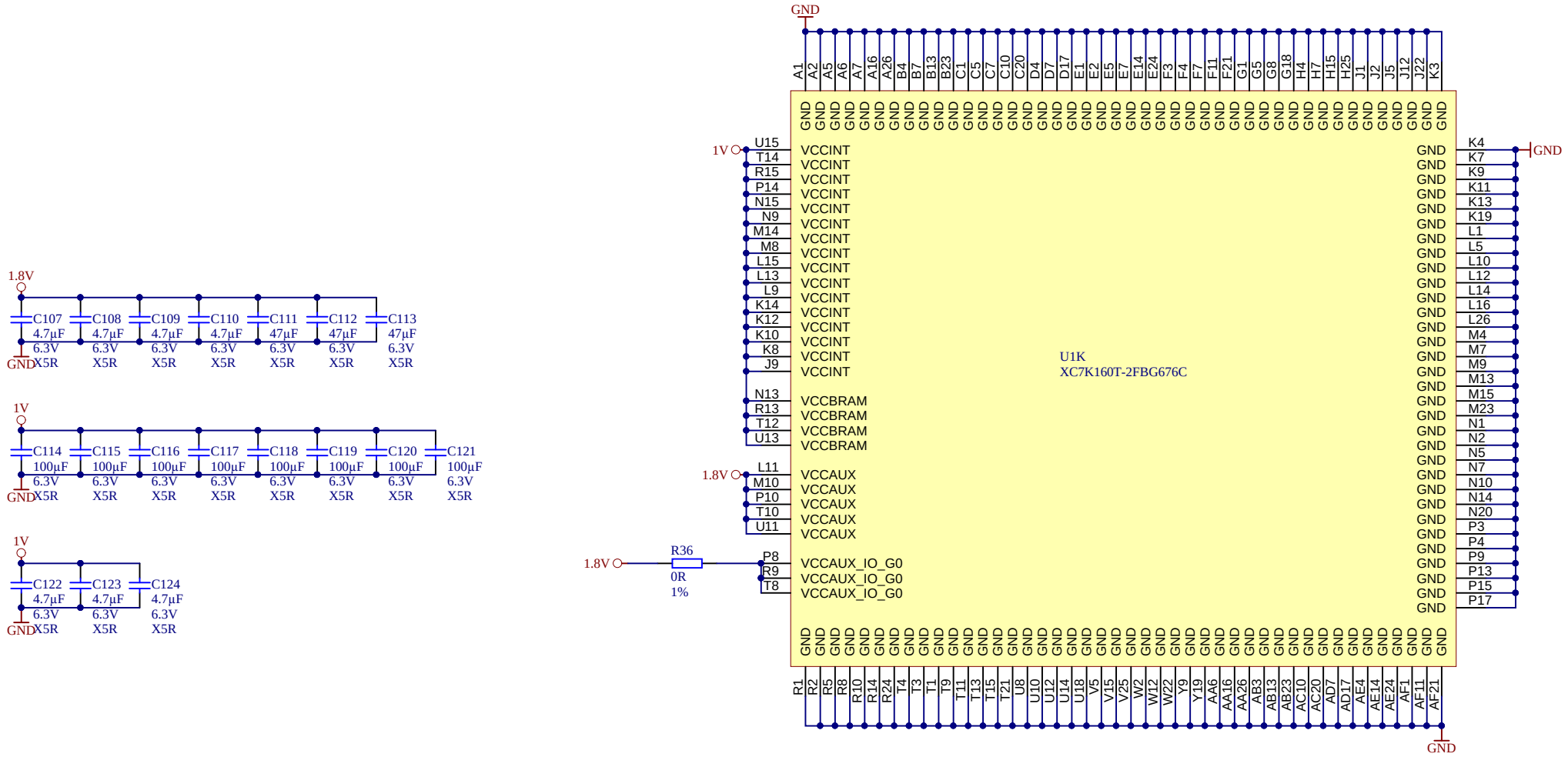




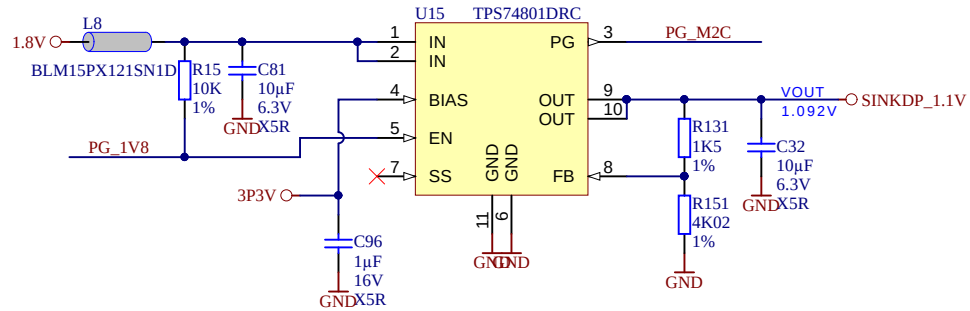


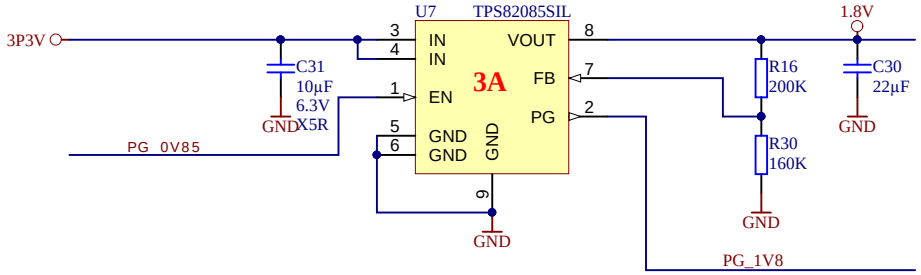
trenz electronic

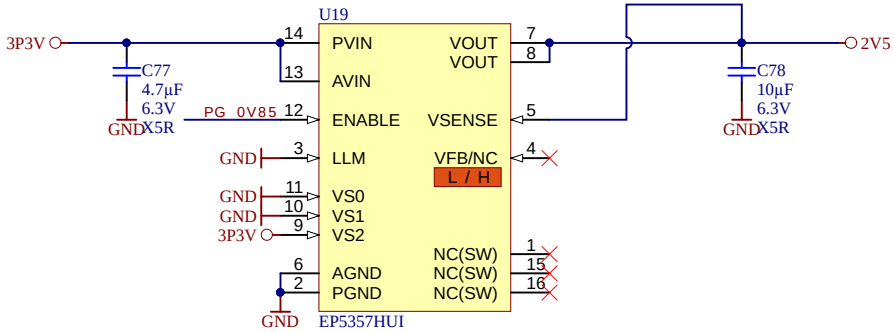
Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: Trenz Electronic GmbH / TT		Page16 of 20
Filename: MGT_CAPS.SchDoc			



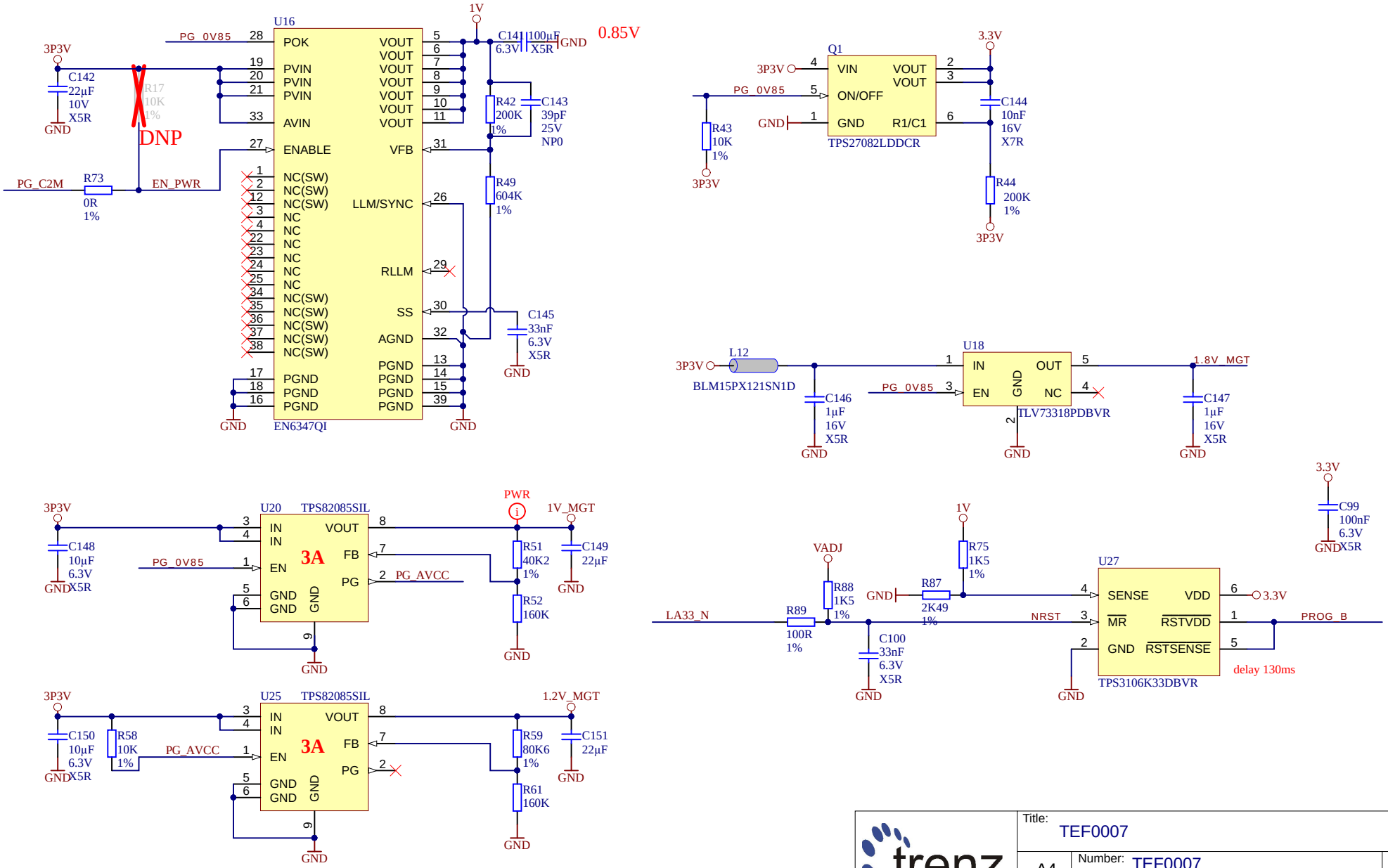
trenz electronic	Title: TEF0007		
	A4	Number: TEF0007 default	Rev. 02
	Date: 2018-02-08	Copyright: 2013 Trenz Electronic GmbH	Page17 of 20
	Filename: FPGA-PWR.SchDoc		



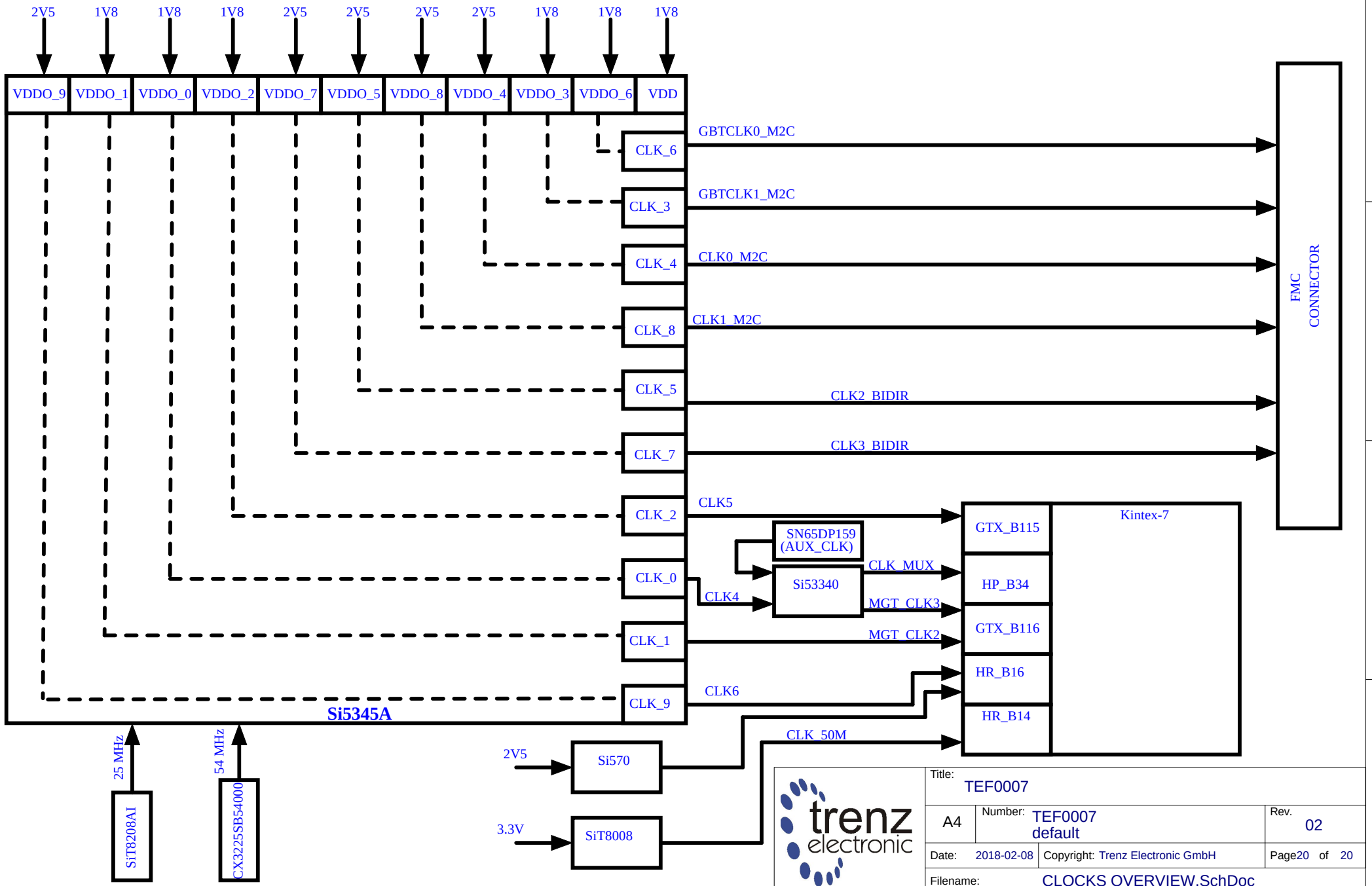




trenz electronic	Title: TEF0007		
	A4	Number: TEF0007 default	Rev. 02
	Date: 2018-02-08	Copyright: Trenz Electronic GmbH	Page18 of 20
	Filename: PWR.SchDoc		



Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02
Date: 2018-02-08	Copyright: Trenz Electronic GmbH		Page19 of 20
Filename: PWR1.SchDoc			


2V5
1V8
1V8
1V8
2V5
2V5
2V5
2V5
1V8
1V8
1V8
VDDO_9
VDDO_1
VDDO_0
VDDO_2
VDDO_7
VDDO_5
VDDO_8
VDDO_4
VDDO_3
VDDO_6
VDD
CLK_6
CLK_3
CLK_4
CLK_8
CLK_5
CLK_7
CLK_2
CLK_0
CLK_1
CLK_9
Si5345A
GBTCLK0_M2C
GBTCLK1_M2C
CLK0_M2C
CLK1_M2C
CLK2_BIDIR
CLK3_BIDIR
CLK5
CLK4
CLK6
FMC
CONNECTOR
SN65DP159
(AUX_CLK)
Si53340
CLK_MUX
MGT_CLK3
MGT_CLK2
Kintex-7
GTX_B115
HP_B34
GTX_B116
HR_B16
HR_B14
25 MHz
SiT8208AI
54 MHz
CX3225SB54000
2V5
Si570
CLK_50M
3.3V
SiT8008
trenz
electronic
Title:
TEF0007
A4
Number:
TEF0007
default
Rev.
02
Date:
2018-02-08
Copyright: Trenz Electronic GmbH
Page20 of 20
Filename:
CLOCKS OVERVIEW.SchDoc