FMC
FMC.SchDoc

DP_IC_SourceSide
DP_IC_SourceSide.SchDoc

DP_IC_SinkSide
DP_IC_SinkSide.SchDoc

MISC
MISC.SchDoc

MGT_CAPS
MGT_CAPS.SchDoc

PWR
PWR.SchDoc

CLOCK
Clock.SchDoc

PWR1
PWR1.SchDoc

B12
B12.SchDoc

B13
B13.SchDoc

B14
B14.SchDoc

B15
B15.SchDoc

B16
B16.SchDoc

B33
B33.SchDoc

B34
B34.SchDoc

FPGA-CFG
FPGA-CFG.SchDoc

FPGA-MGT
FPGA-MGT.SchDoc

FPGA-PWR
FPGA-PWR.SchDoc

LOGO1

TE Logo PRINT Layer

LOGO PRINT

Serial

Serial

Serialnumber 6,3 x 6.3mm

S/N

Serialnumber

PM1 FIDU-DOT - mini

PM2 FIDU-DOT - mini

PM3 FIDU-DOT - mini

PM4 FIDU-DOT - mini

PM5 FIDU-DOT - mini

PM6 FIDU-DOT - mini

Assembly variant	default
Created by	VT
Modified by	VT
Modified at	04.05.2022
SVN Revision	

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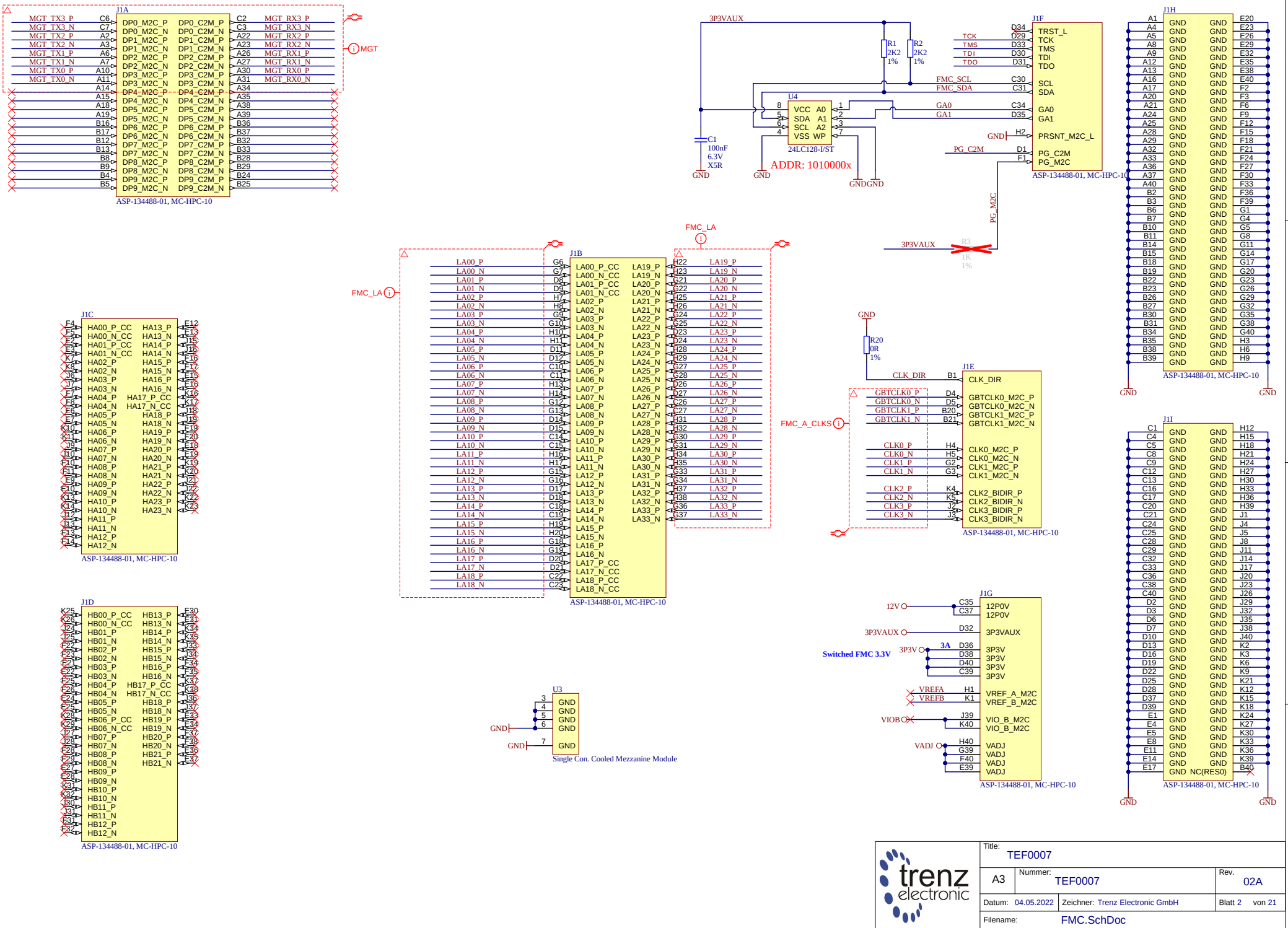
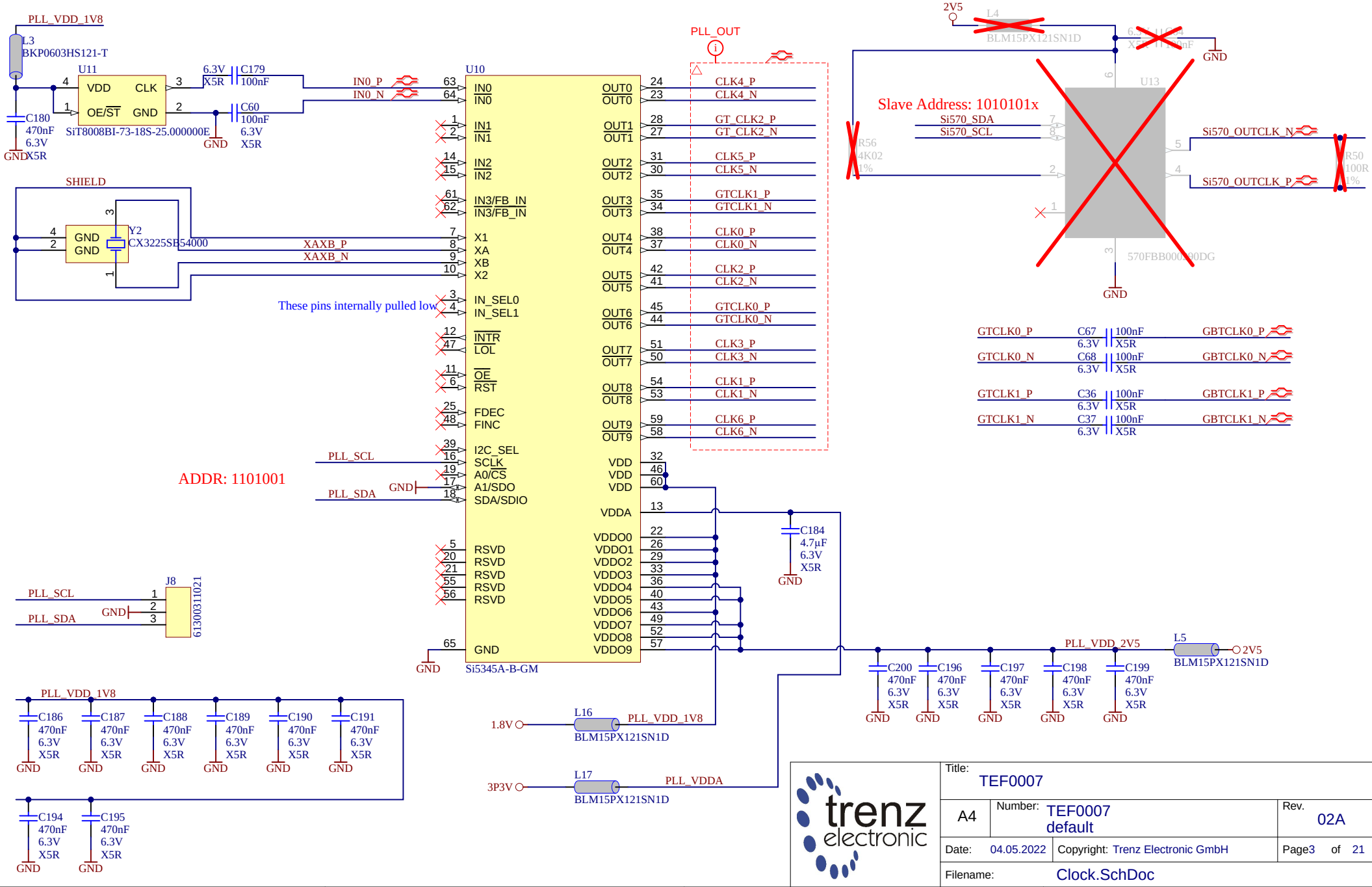
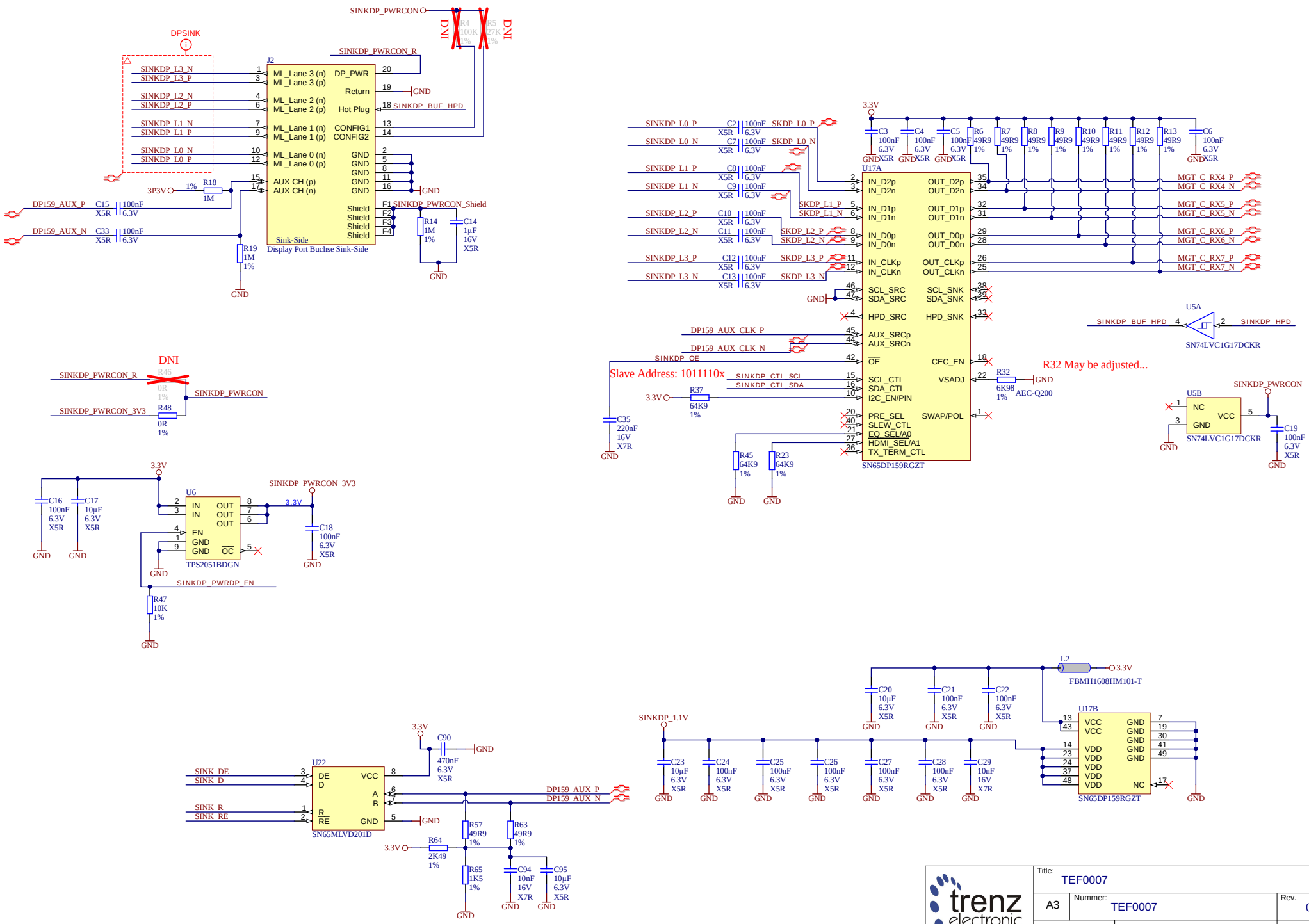
Title: TEF0007		
A4	Number: TEF0007 default	Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH	Page1 of 21
Filename: TEF0007-01.SchDoc		



Title:	TEF0007		
A3	Nummer: TEF0007		Rev. 02A
Datum: 04.05.2022	Zeichner: Trenz Electronic GmbH		Blatt 2 von 21
Filename:	FMC.SchDoc		



Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH		Page3 of 21
Filename: Clock.SchDoc			



Title:	TEF0007
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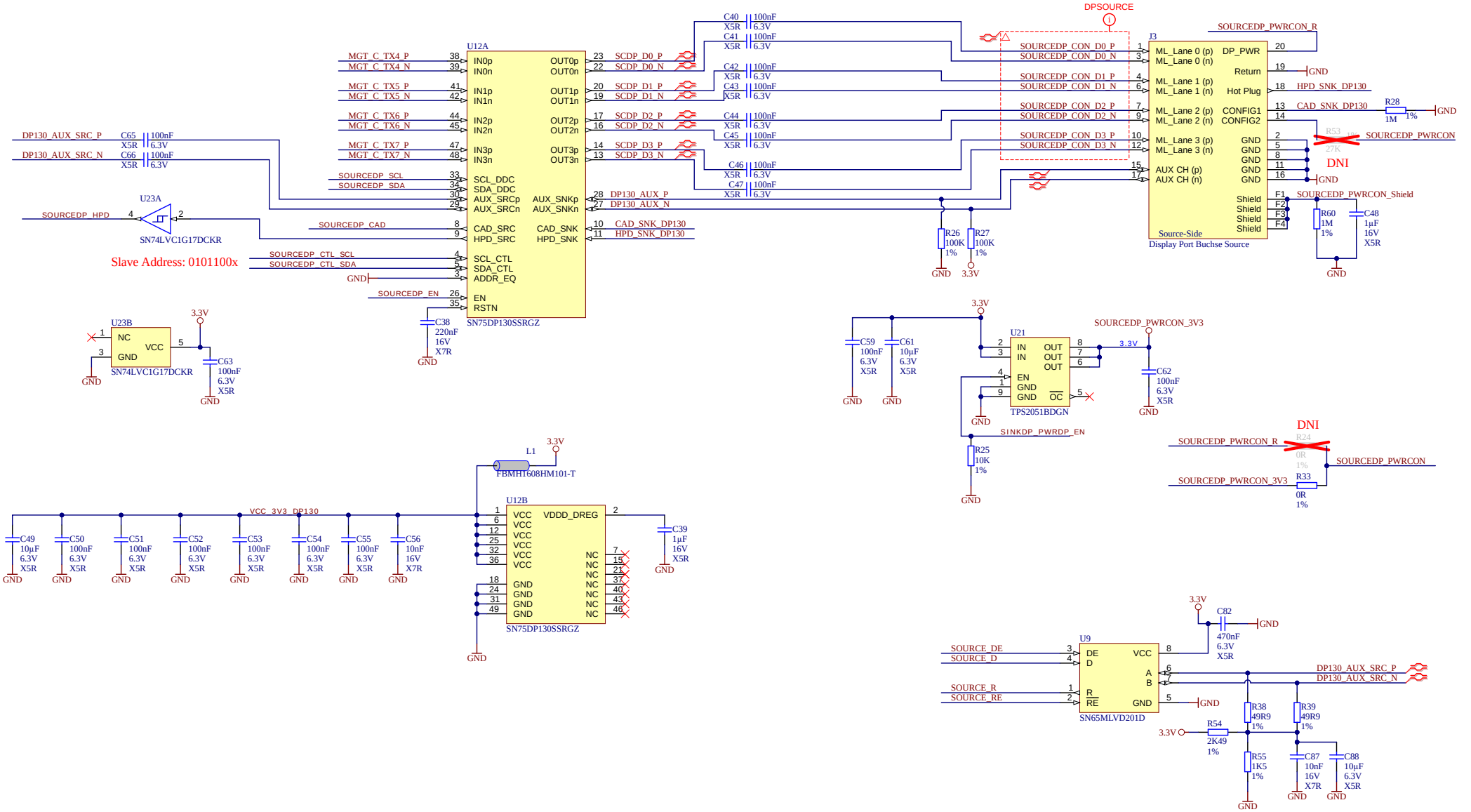
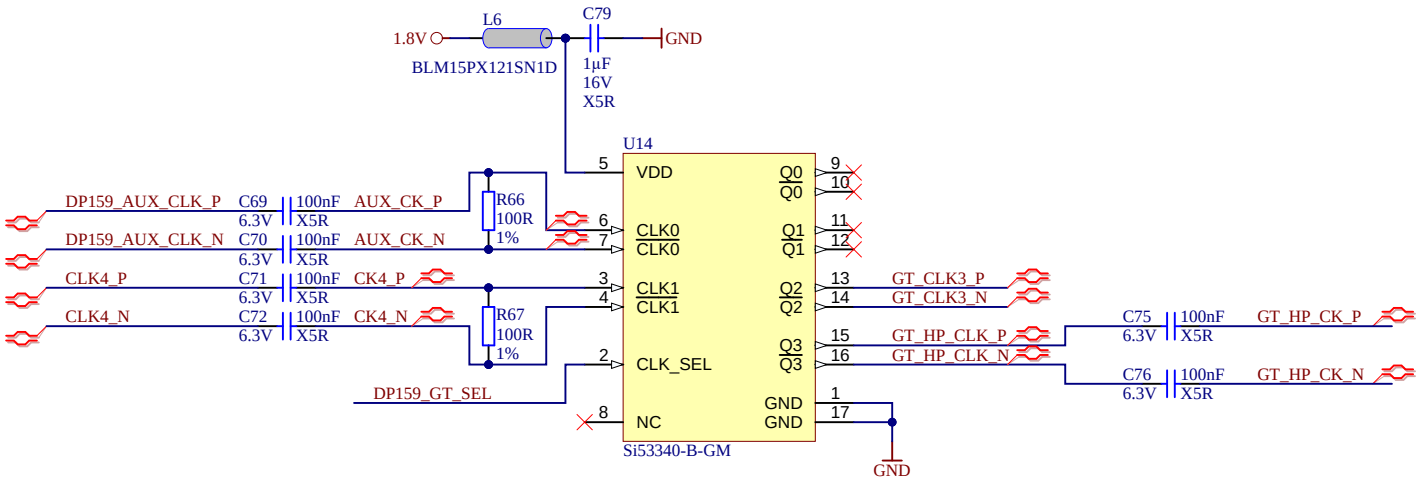
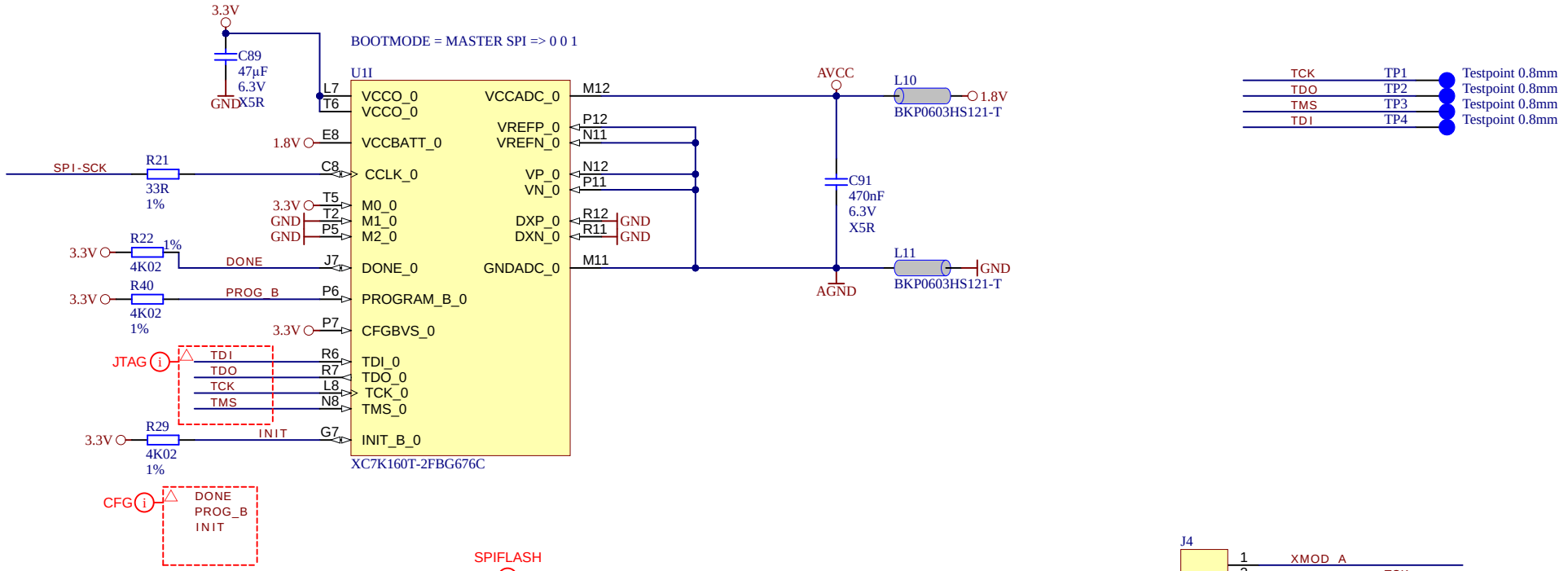
Datum: 04.05.2022	Zeichner: Trenz Electronic GmbH — Blatt 4 von 21
Filename:	DP_IC_SinkSide.SchDoc



Title:	TEF0007
A3	Nummer: TEF0007
	Rev. 02A
Datum: 04.05.2022	Zeichner: Trenz Electronic GmbH
	Blatt 5 von 21
Filename:	DP_IC_SourceSide.SchDoc

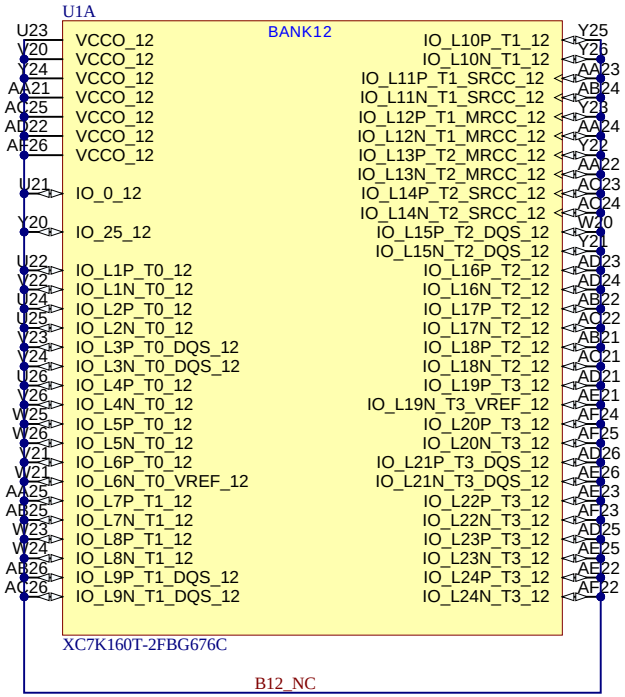


Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH		Page6 of 21
Filename: MISC.SchDoc			



trenz electronic	Title: TEF0007		
	A4	Number: TEF0007 default	Rev. 02A
	Date: 04.05.2022	Copyright: Trenz Electronic GmbH	Page7 of 21
	Filename: FPGA-CFG.SchDoc		

K70T version does not have this bank!



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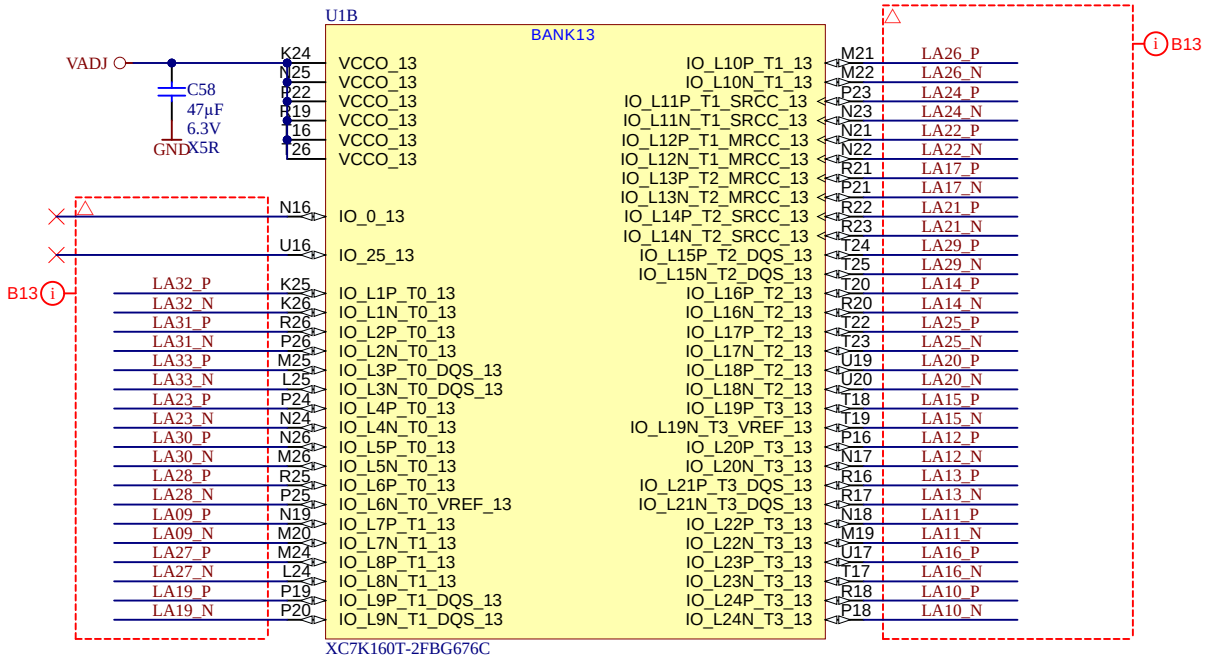
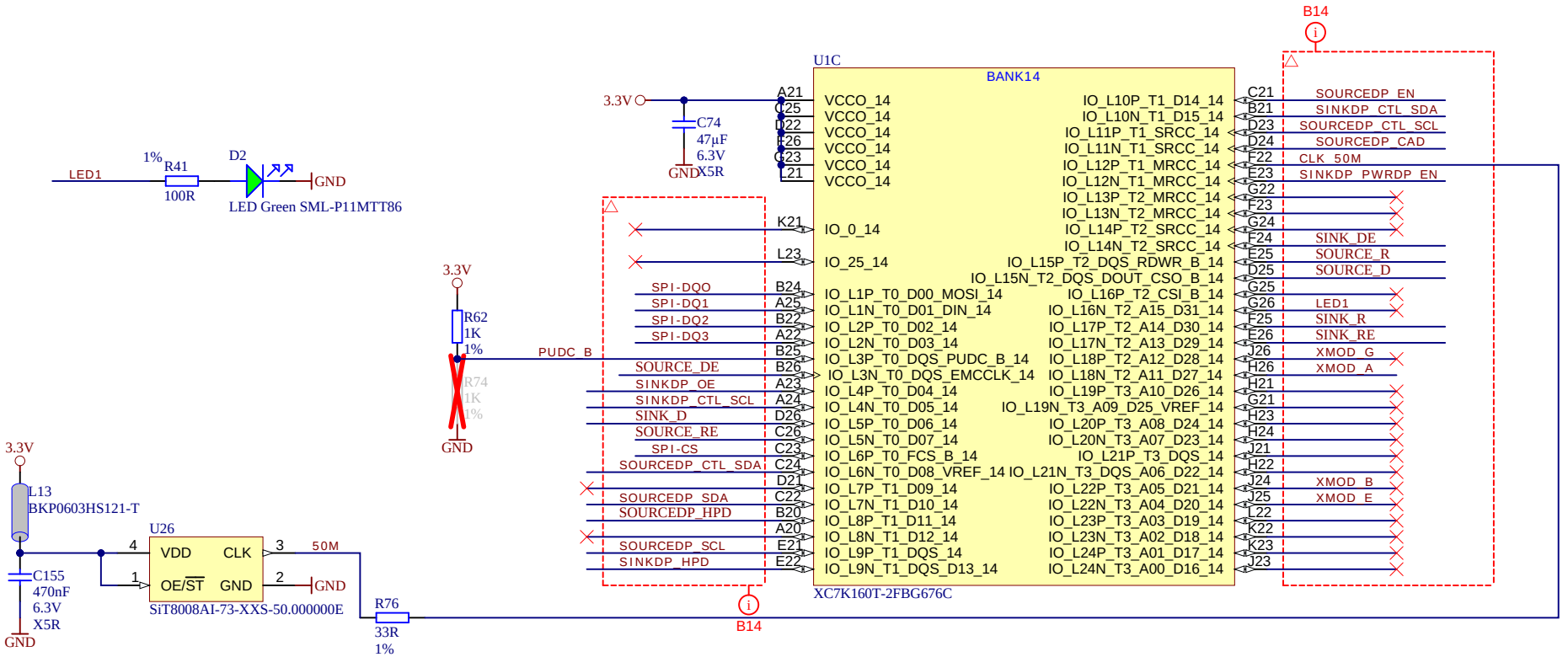
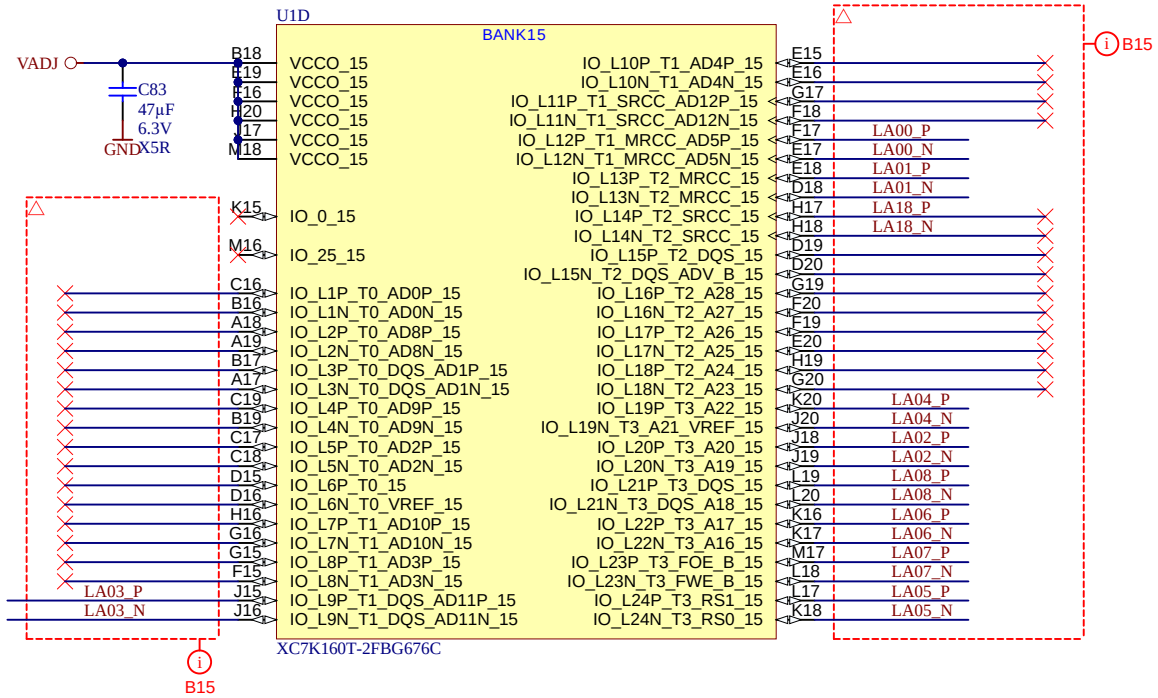
Title: TEF0007		
A4	Number: TEF0007 default	Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH	Page 8 of 21
Filename: B12.SchDoc		



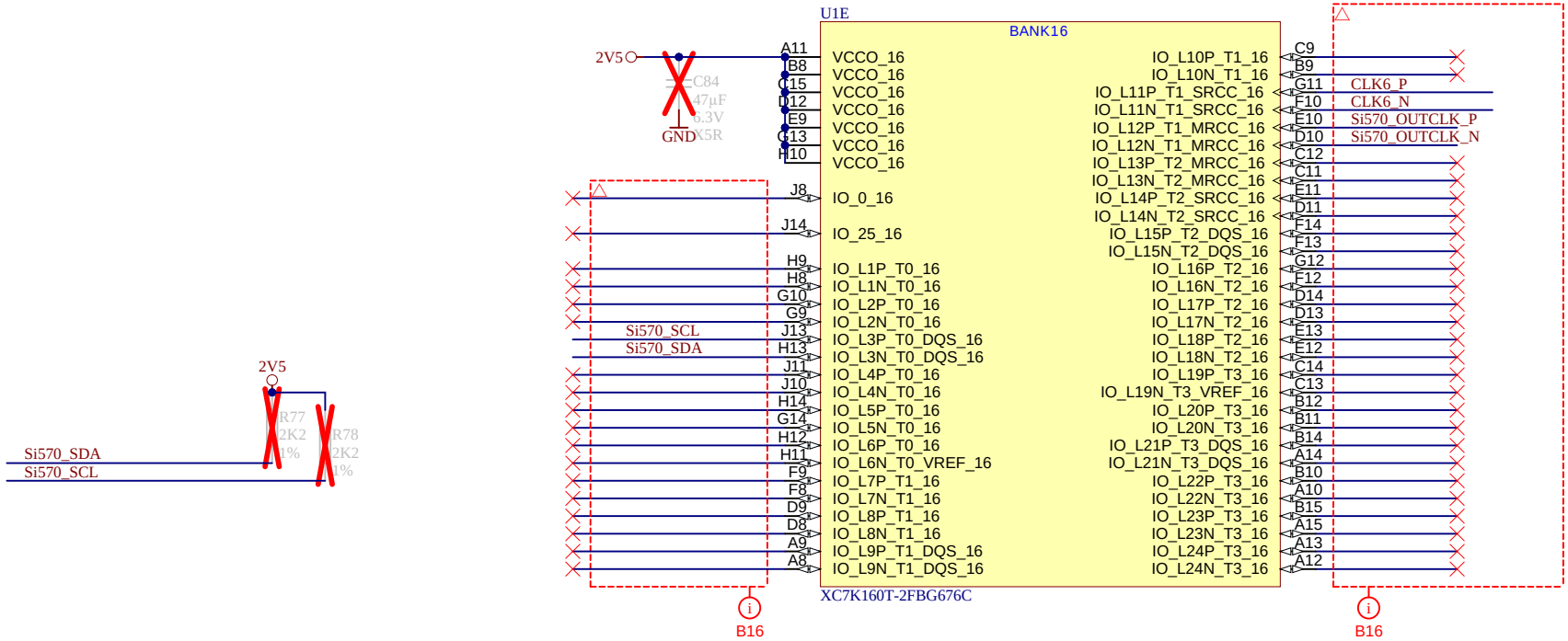
trenz electronic	Title: TEF0007		
	A4	Number: TEF0007 default	Rev. 02A
	Date: 04.05.2022	Copyright: Trenz Electronic GmbH	Page9 of 21
	Filename: B13.SchDoc		



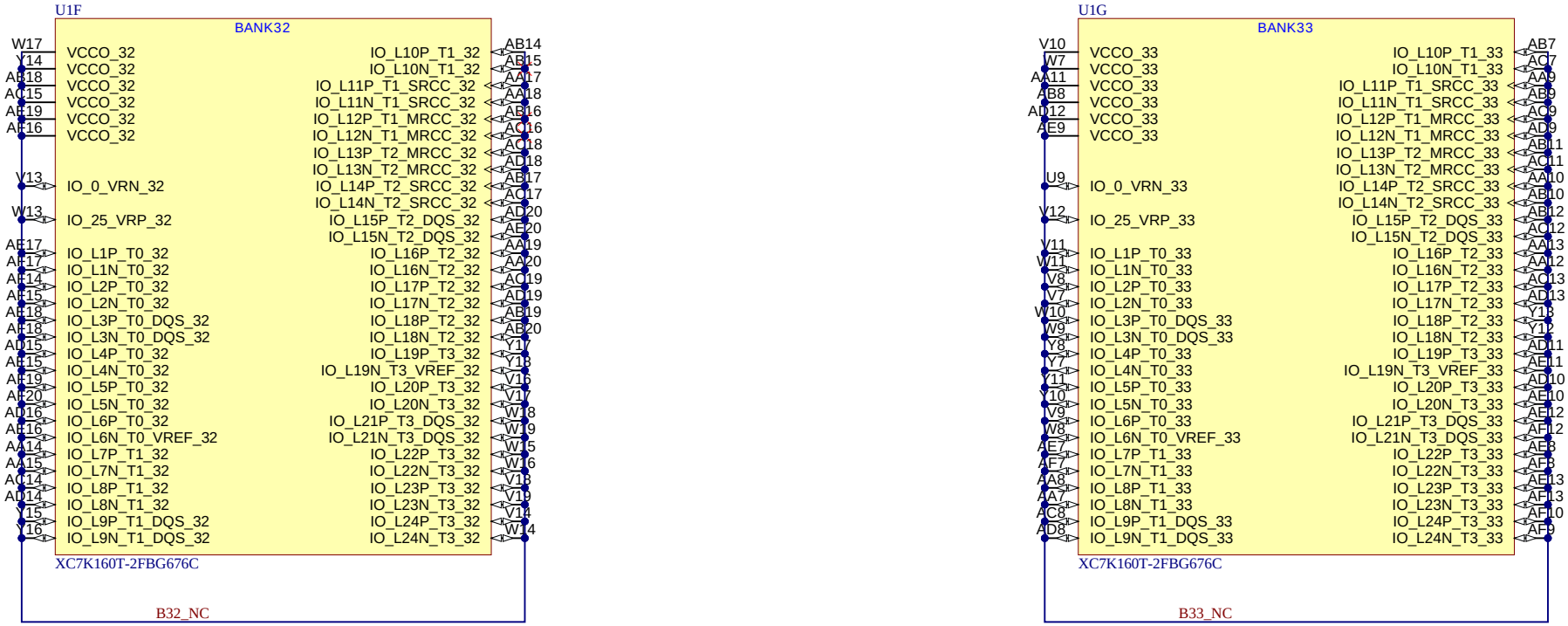
trenz electronic	Title: TEF0007		
	A4	Number: TEF0007 default	Rev. 02A
	Date: 04.05.2022	Copyright: Trenz Electronic GmbH	Page10 of 21
	Filename: B14.SchDoc		



trenz electronic	Title: TEF0007		
A4	Number: TEF0007 default		Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH		Page 11 of 21
Filename: B15.SchDoc			



trenz electronic	Title: TEF0007		
A4	Number: TEF0007 default		Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH		Page12 of 21
Filename: B16.SchDoc			



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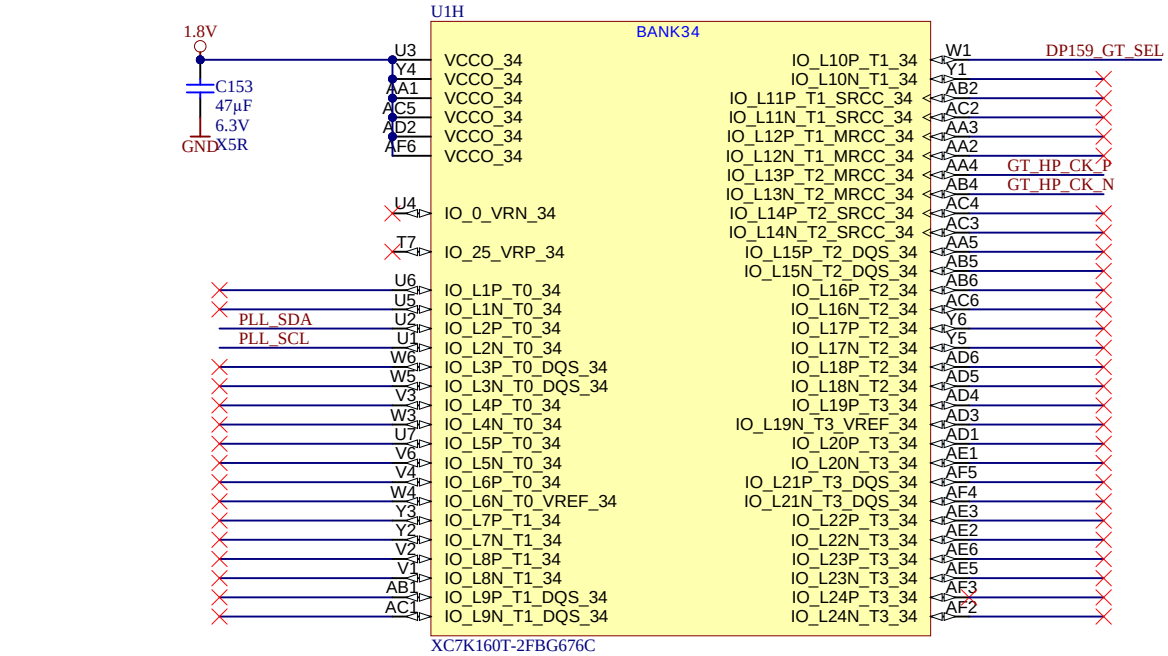
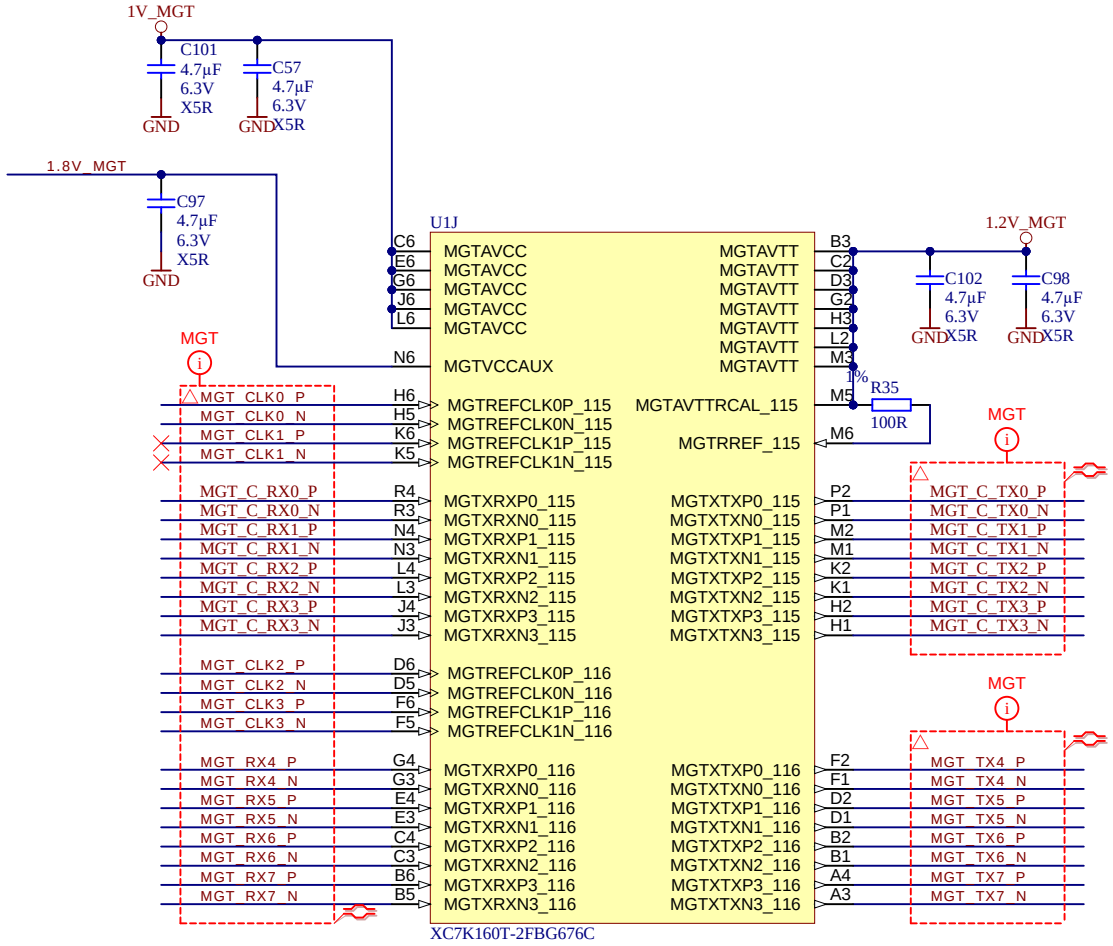
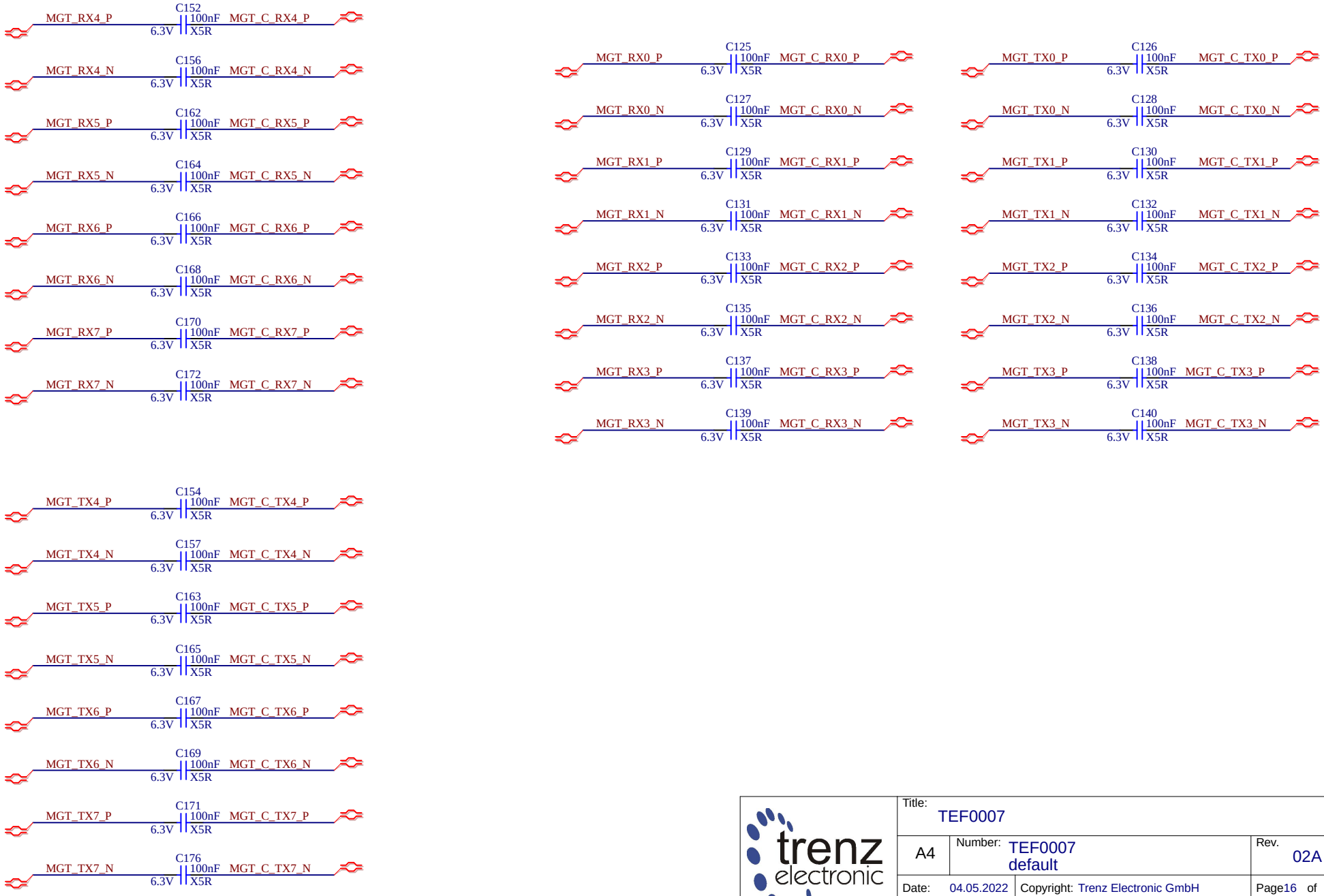
Title: TEF0007		
A4	Number: TEF0007 default	Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH	Page13 of 21
Filename: B33.SchDoc		



Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH		Page14 of 21
Filename: B34.SchDoc			



Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH		Page15 of 21
Filename: FPGA-MGT.SchDoc			


MGT_RX4_P
C152
100nF
6.3V
X5R
MGT_C_RX4_P
MGT_RX4_N
C156
MGT_C_RX4_N
MGT_RX5_P
C162
MGT_C_RX5_P
MGT_RX5_N
C164
MGT_C_RX5_N
MGT_RX6_P
C166
MGT_C_RX6_P
MGT_RX6_N
C168
MGT_C_RX6_N
MGT_RX7_P
C170
MGT_C_RX7_P
MGT_RX7_N
C172
MGT_C_RX7_N
MGT_TX4_P
C154
MGT_C_TX4_P
MGT_TX4_N
C157
MGT_C_TX4_N
MGT_TX5_P
C163
MGT_C_TX5_P
MGT_TX5_N
C165
MGT_C_TX5_N
MGT_TX6_P
C167
MGT_C_TX6_P
MGT_TX6_N
C169
MGT_C_TX6_N
MGT_TX7_P
C171
MGT_C_TX7_P
MGT_TX7_N
C176
MGT_C_TX7_N
MGT_RX0_P
C125
MGT_C_RX0_P
MGT_RX0_N
C127
MGT_C_RX0_N
MGT_RX1_P
C129
MGT_C_RX1_P
MGT_RX1_N
C131
MGT_C_RX1_N
MGT_RX2_P
C133
MGT_C_RX2_P
MGT_RX2_N
C135
MGT_C_RX2_N
MGT_RX3_P
C137
MGT_C_RX3_P
MGT_RX3_N
C139
MGT_C_RX3_N
MGT_TX0_P
C126
MGT_C_TX0_P
MGT_TX0_N
C128
MGT_C_TX0_N
MGT_TX1_P
C130
MGT_C_TX1_P
MGT_TX1_N
C132
MGT_C_TX1_N
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MGT_TX2_N
C136
MGT_C_TX2_N
MGT_TX3_P
C138
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C140
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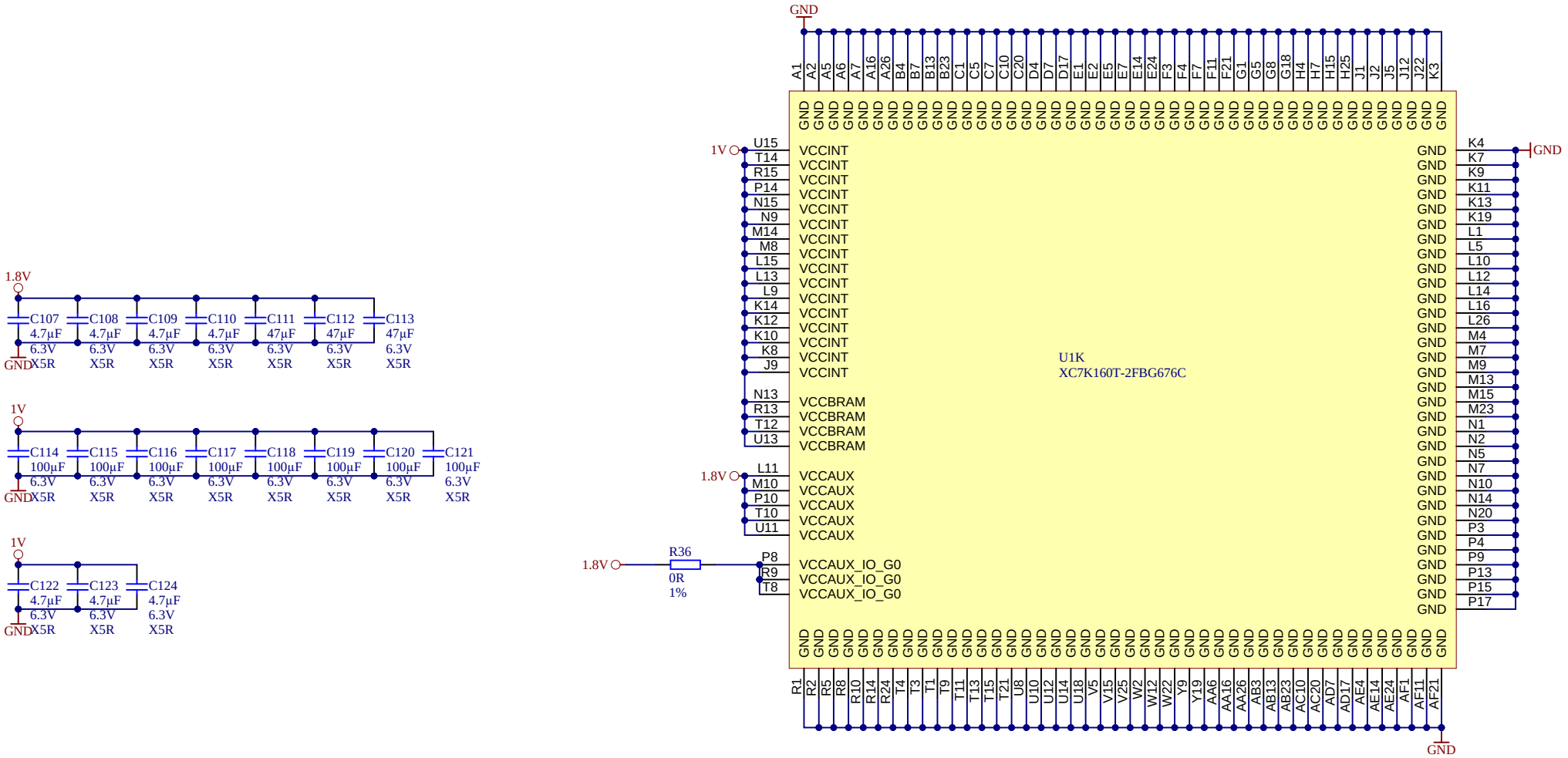
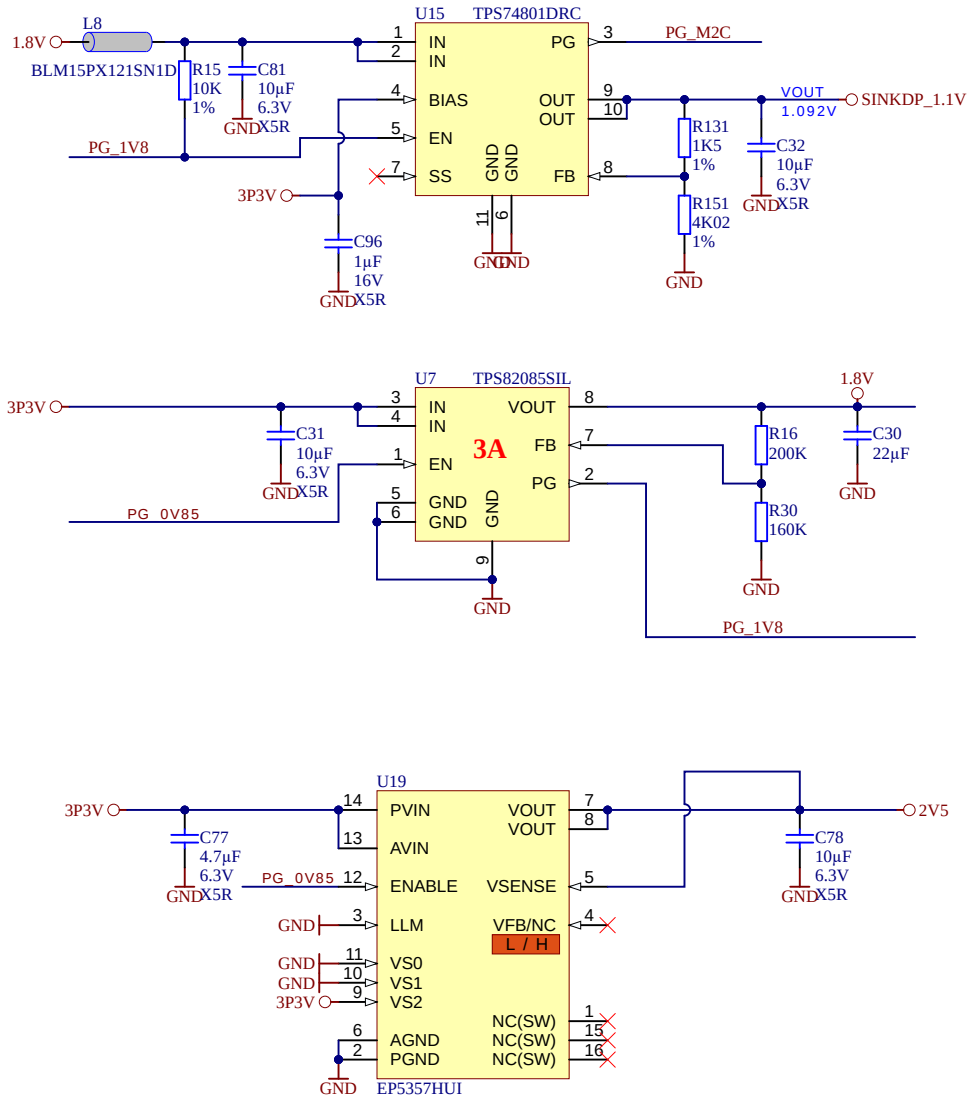
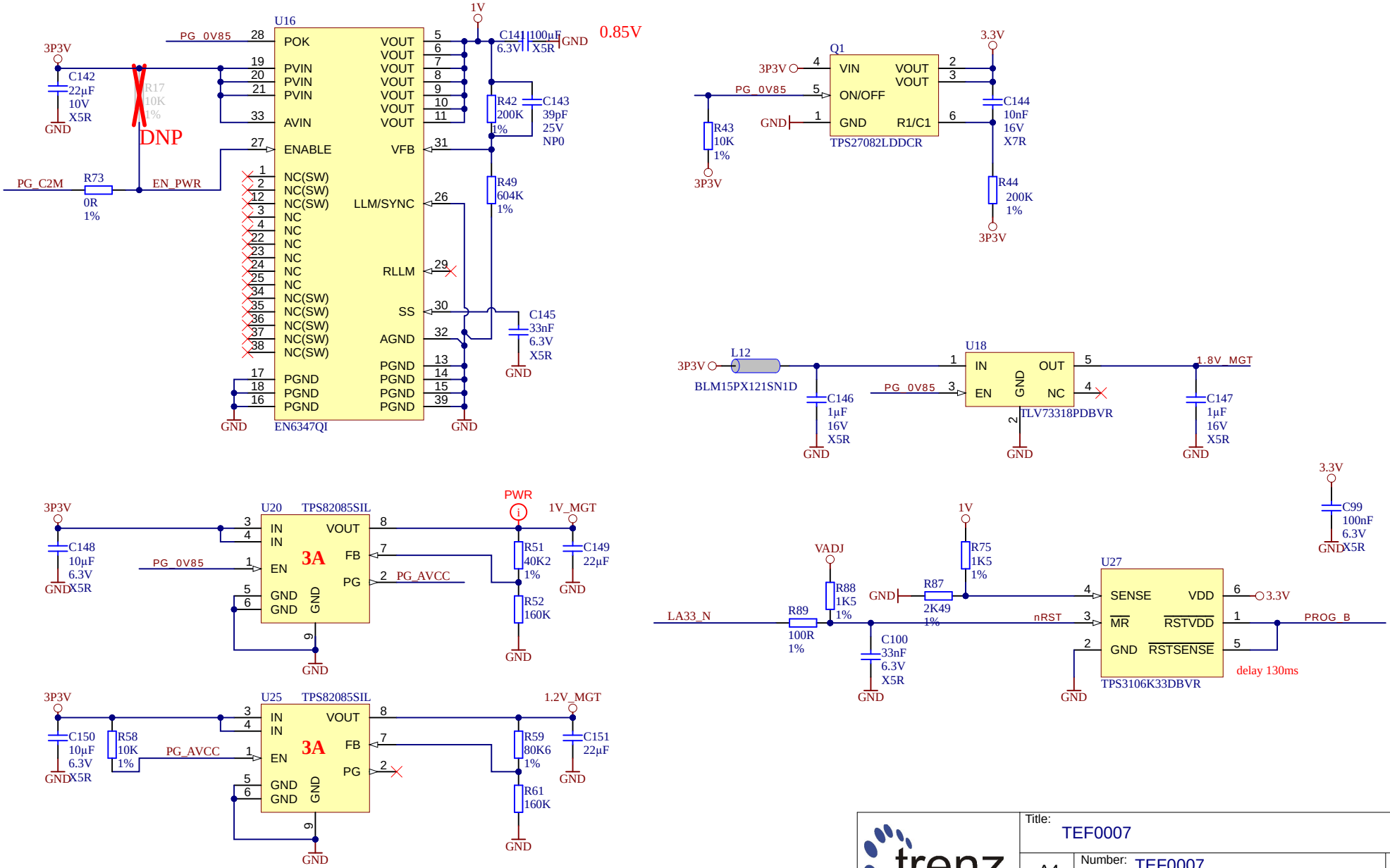
trenz
electronic
Title:
TEF0007
A4
Number:
TEF0007
default
Rev.
02A
Date:
04.05.2022
Copyright:
Trenz Electronic GmbH
Page16
of
21
Filename:
MGT_CAPS.SchDoc



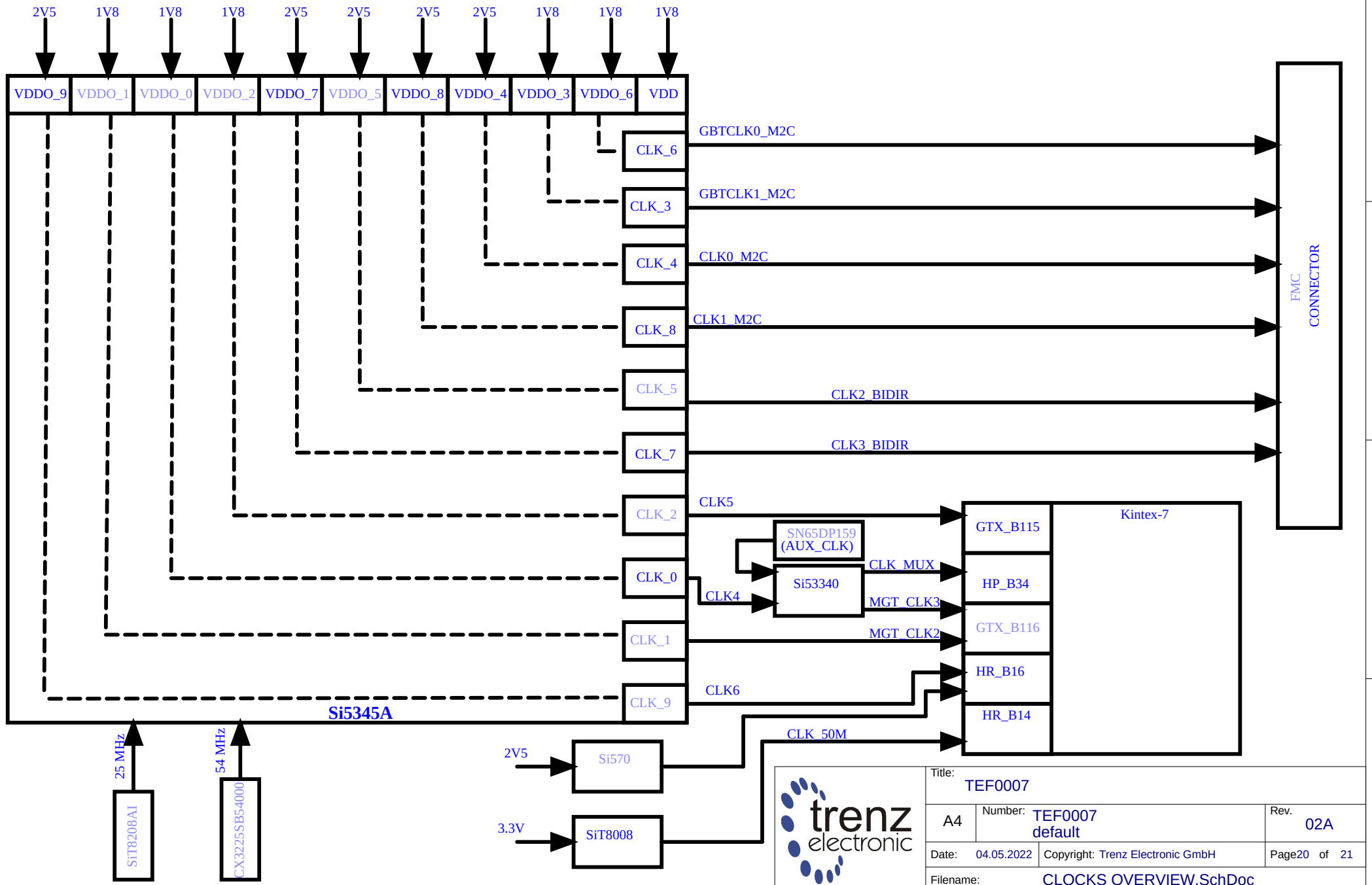
Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH		Page17 of 21
Filename: FPGA-PWR.SchDoc			



trenz electronic	Title: TEF0007		
	A4	Number: TEF0007 default	Rev. 02A
	Date: 04.05.2022	Copyright: Trenz Electronic GmbH	Page18 of 21
	Filename: PWR.SchDoc		



Title: TEF0007			
A4	Number: TEF0007 default		Rev. 02A
Date: 04.05.2022	Copyright: Trenz Electronic GmbH		Page19 of 21
Filename: PWR1.SchDoc			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1V8
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1V8
2V5
2V5
2V5
2V5
1V8
1V8
1V8
VDDO_9
VDDO_1
VDDO_0
VDDO_2
VDDO_7
VDDO_5
VDDO_8
VDDO_4
VDDO_3
VDDO_6
VDD
CLK_6
CLK_3
CLK_4
CLK_8
CLK_5
CLK_7
CLK_2
CLK_0
CLK_1
CLK_9
GBTCLK0_M2C
GBTCLK1_M2C
CLK0_M2C
CLK1_M2C
CLK2_BIDIR
CLK3_BIDIR
CLK5
CLK4
CLK6
FMC
CONNECTOR
SN65DP159
(AUX_CLK)
Si53340
CLK_MUX
MGT_CLK3
MGT_CLK2
CLK_50M
GTX_B115
HP_B34
GTX_B116
HR_B16
HR_B14
Kintex-7
Si5345A
25 MHz
54 MHz
SiT8208AI
CX3225SB54000
2V5
Si570
3.3V
SiT8008
trenz
electronic
Title:
TEF0007
A4
Number:
TEF0007
default
Rev.
02A
Date:
04.05.2022
Copyright:
Trenz Electronic GmbH
Page20
of
21
Filename:
CLOCKS OVERVIEW.SchDoc