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U_A-Headers
A-Headers.SchDoc



U_FPGA
FPGA.SchDoc



U_ADC
ADC.SchDoc



U_FTDI
FTDI.SchDoc



U_SENSOR_Flash_RAM
SENSOR_Flash_RAM.SchDoc



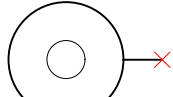
U_FPGA_MISC
FPGA_MISC.SchDoc



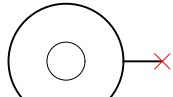
U_PowerSupply
PowerSupply.SchDoc



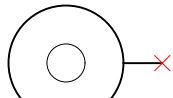
U_A_POWER
Analog_power.SchDoc



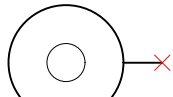
Mount.Hole 2mm (unplated)



Mount.Hole 2mm (unplated)

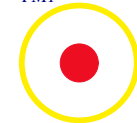


Mount.Hole 2mm (unplated)



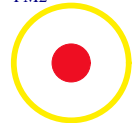
Mount.Hole 2mm (unplated)

PM1



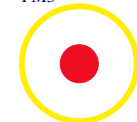
FIDU-DOT - mini

PM2



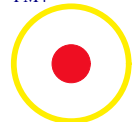
FIDU-DOT - mini

PM3



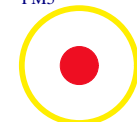
FIDU-DOT - mini

PM4



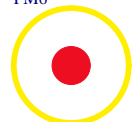
FIDU-DOT - mini

PM5



FIDU-DOT - mini

PM6



FIDU-DOT - mini

Assembly variant	08-C8A
Created by	IG
Modified by	VT
Modified at	2019-07-26
SVN Revision	11295

Serial
Serial
Serialnumber 6,3 x 6.3mm



Title: TEI0015		
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Drawn by: VY	Filename: TEI0015.SchDoc	

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A

A

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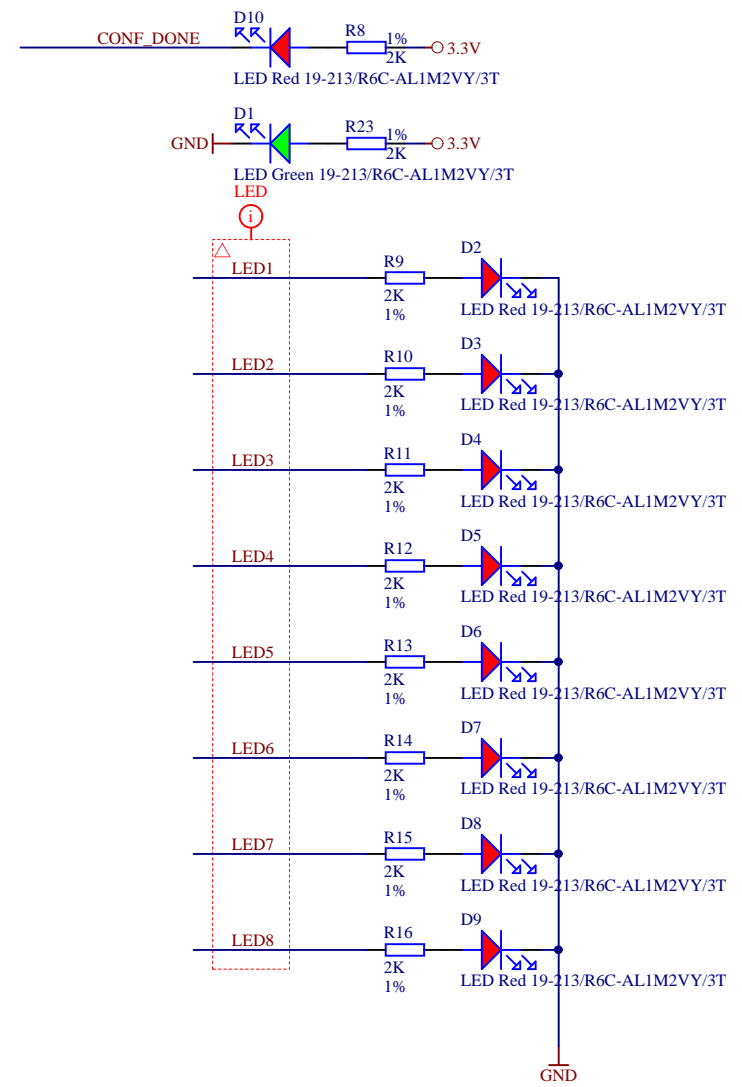
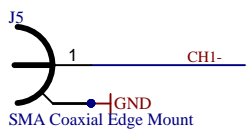
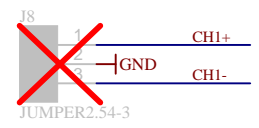
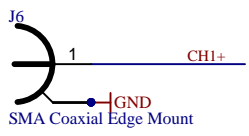
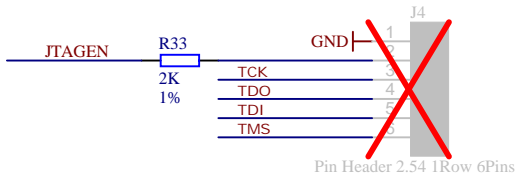
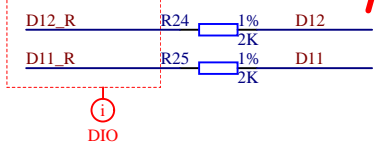
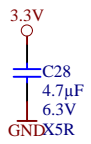
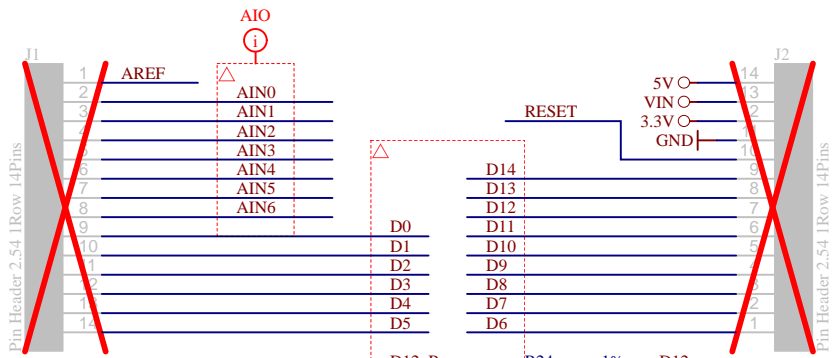
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C

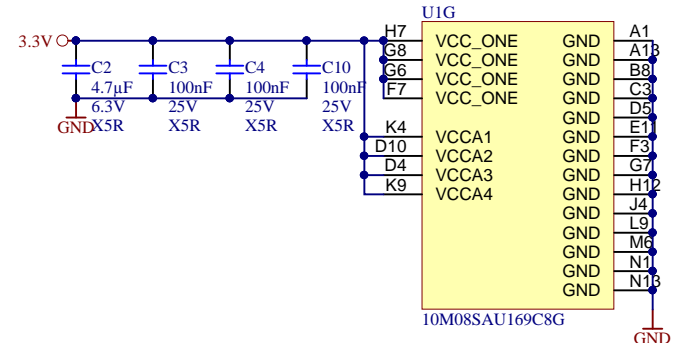
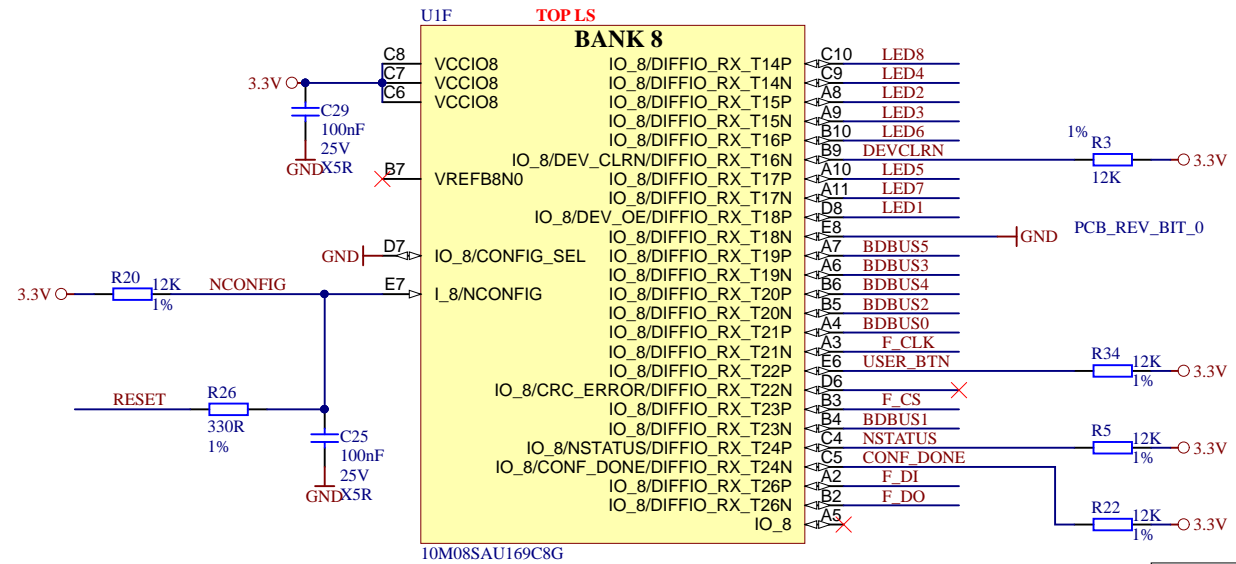
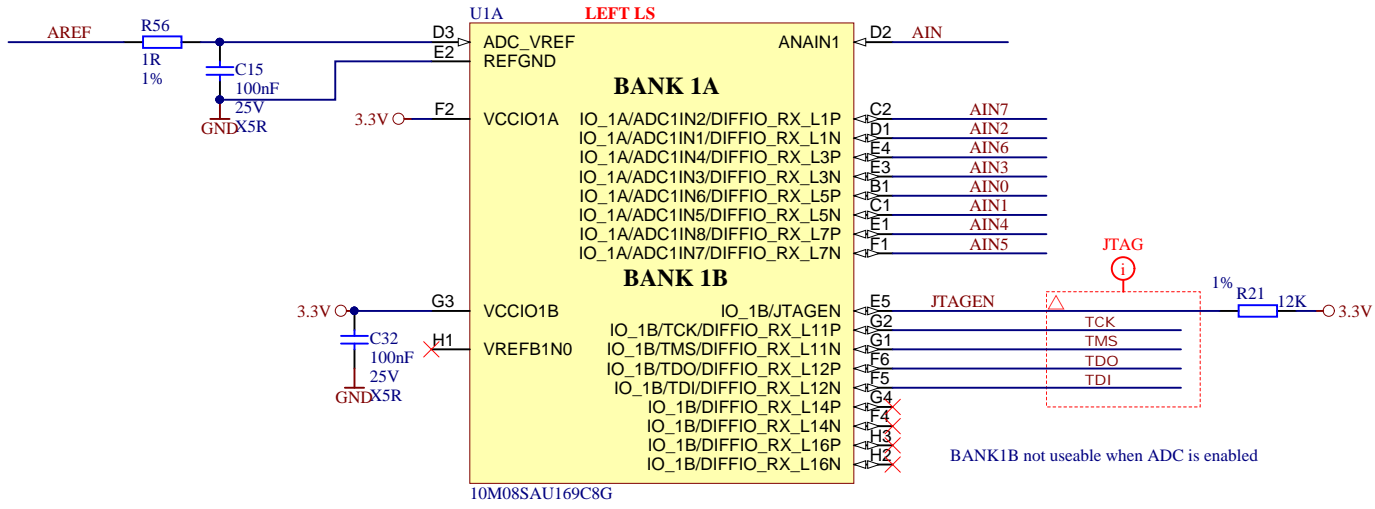
C

D

D



Title: Headers		
A4	Number: TEI0015 08-C8A	Rev. 03
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Title: FPGA MISC		
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Drawn by: VY	Filename: FPGA_MISC.SchDoc	

A

B

C

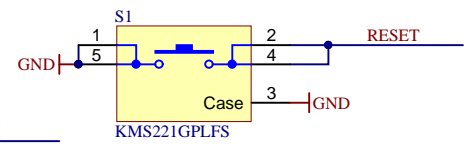
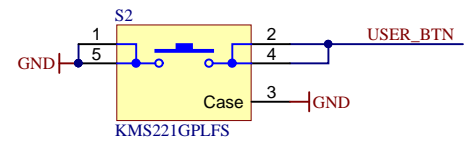
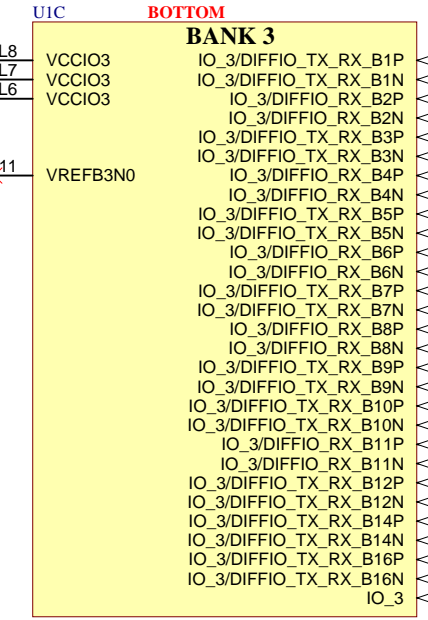
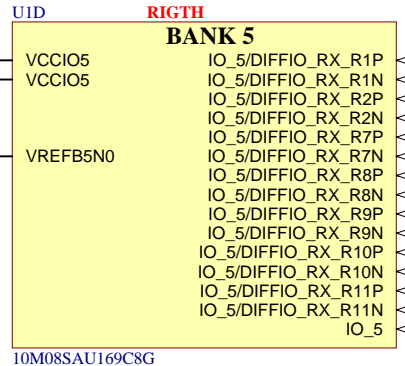
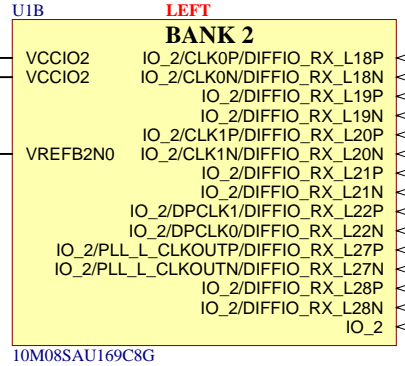
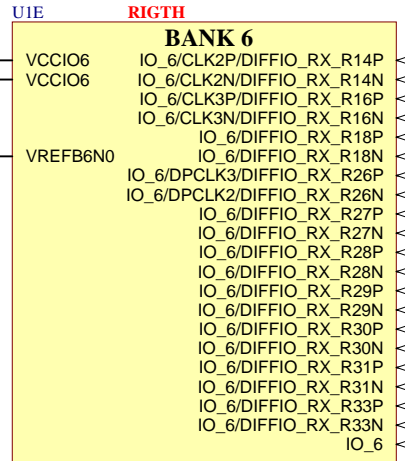
D

A

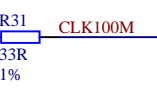
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C

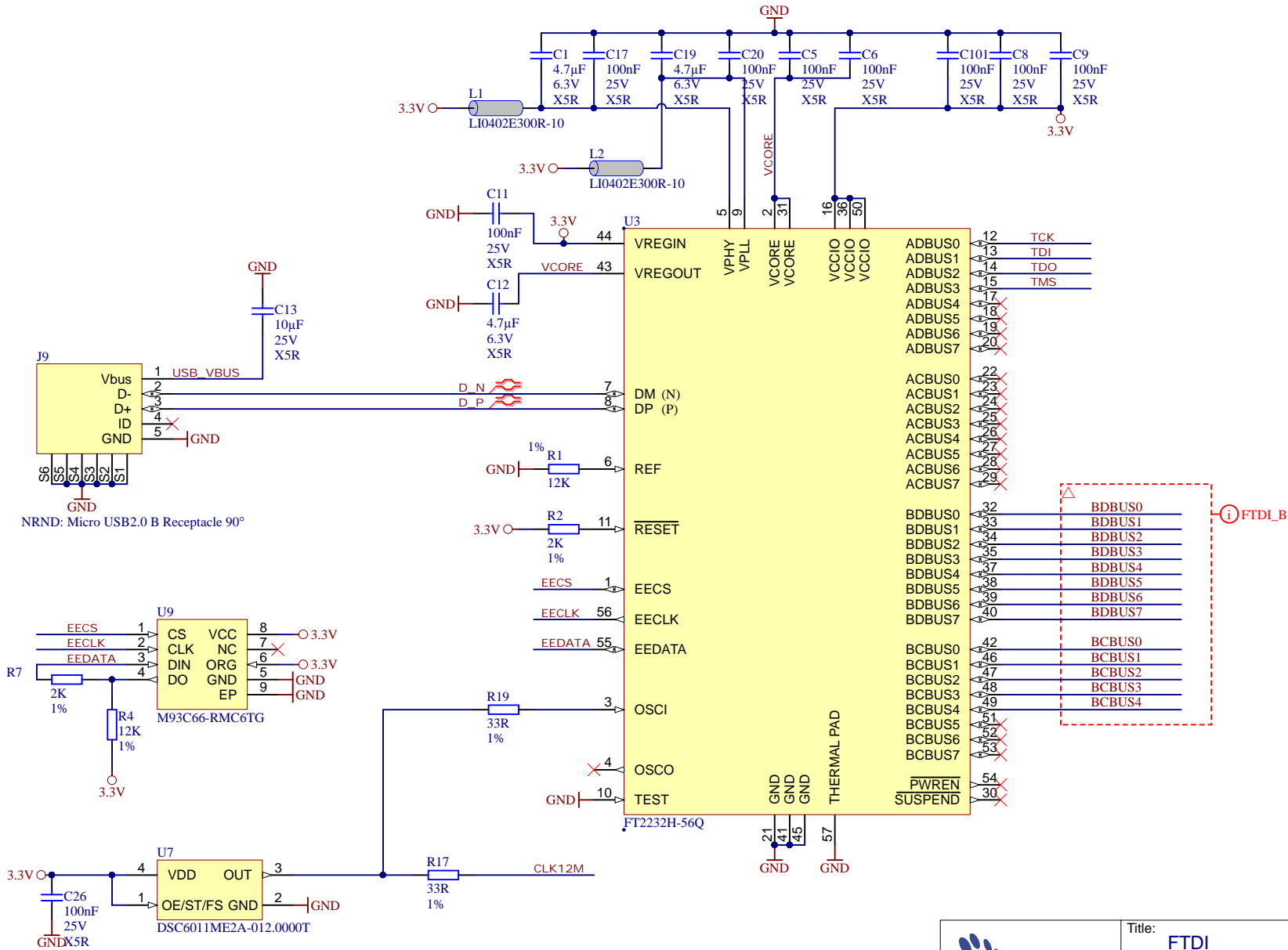
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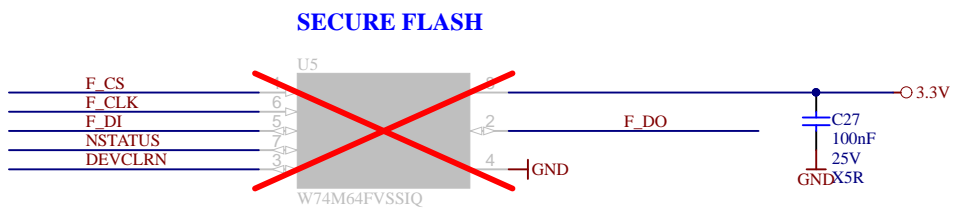
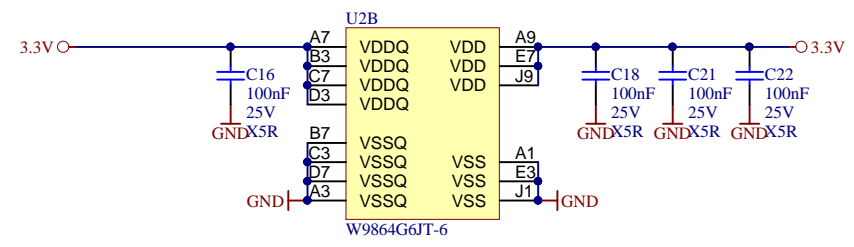
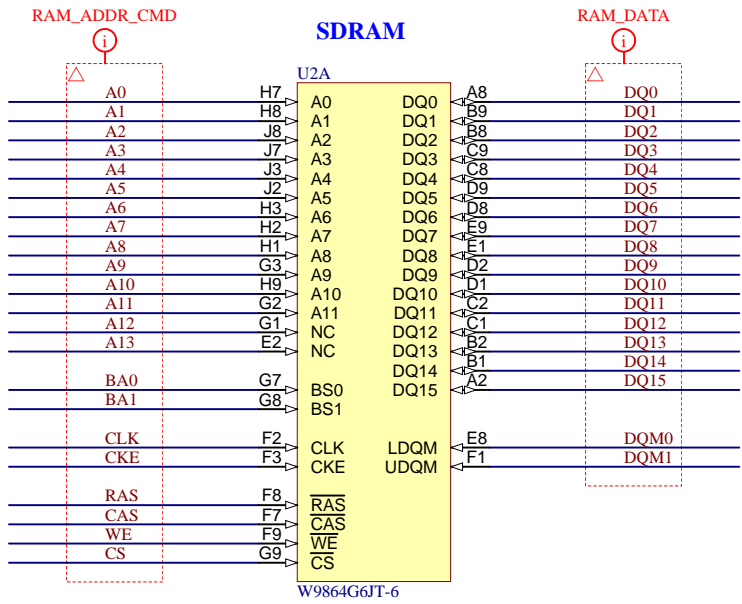
D11_R



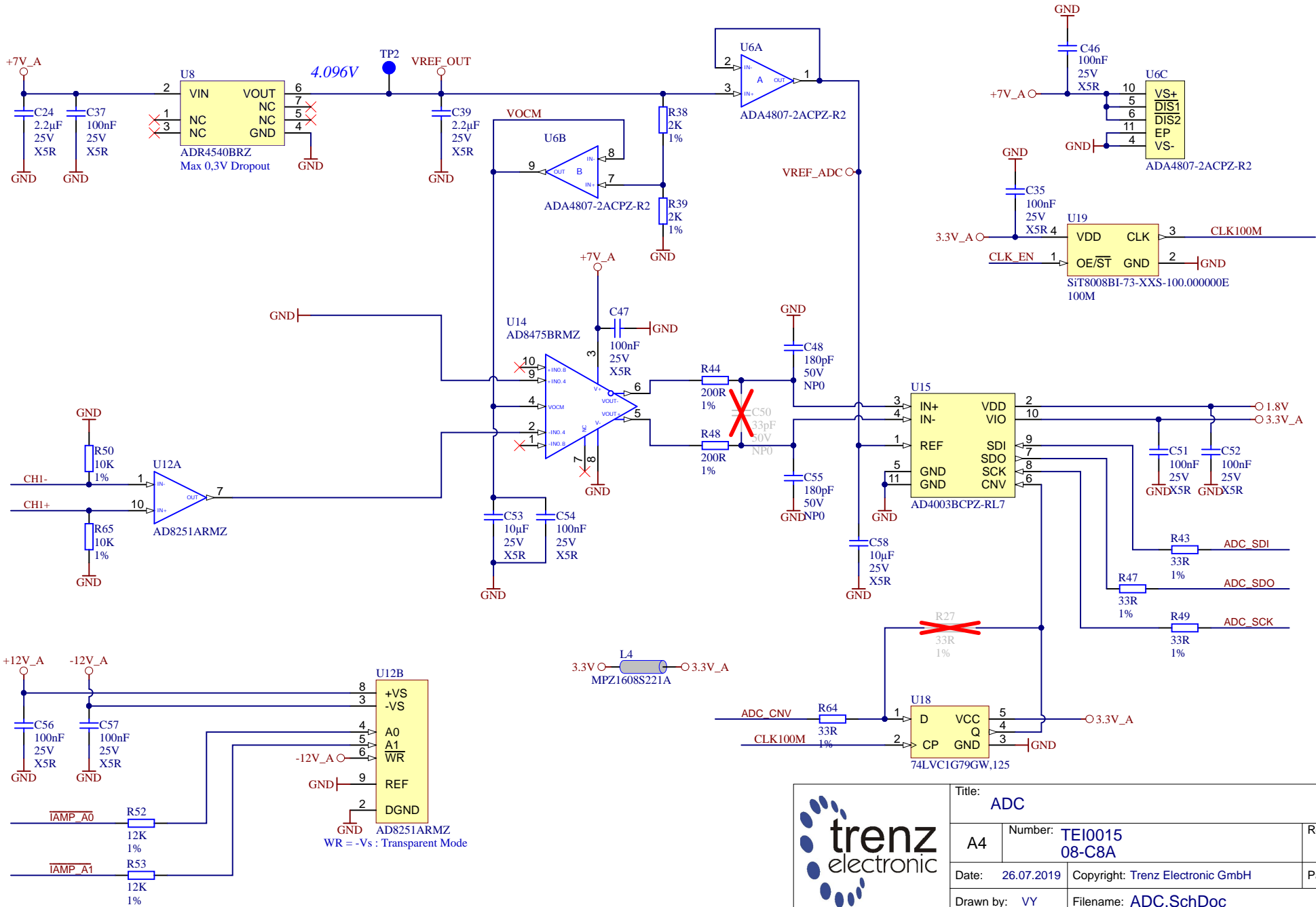
Title: FPGA		
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Date: 26.07.2019	Copyright: Trenz Electronic GmbH	Page 4 of 10
Drawn by: VY	Filename: FPGA.SchDoc	



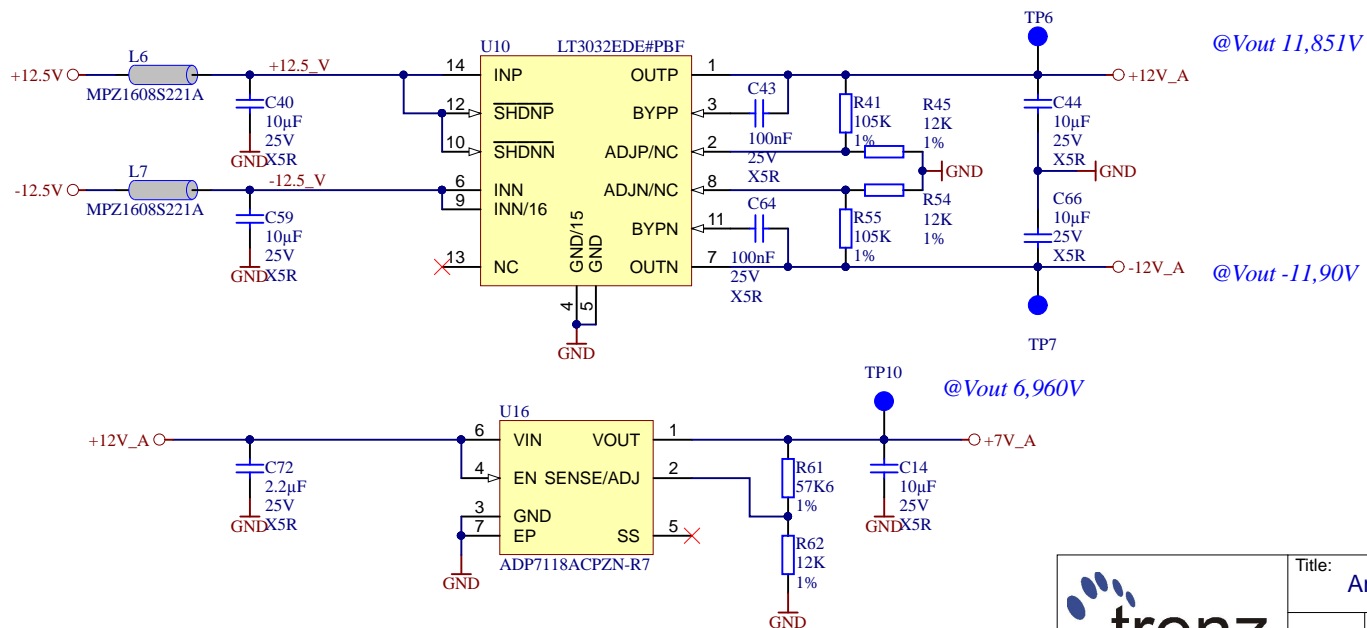
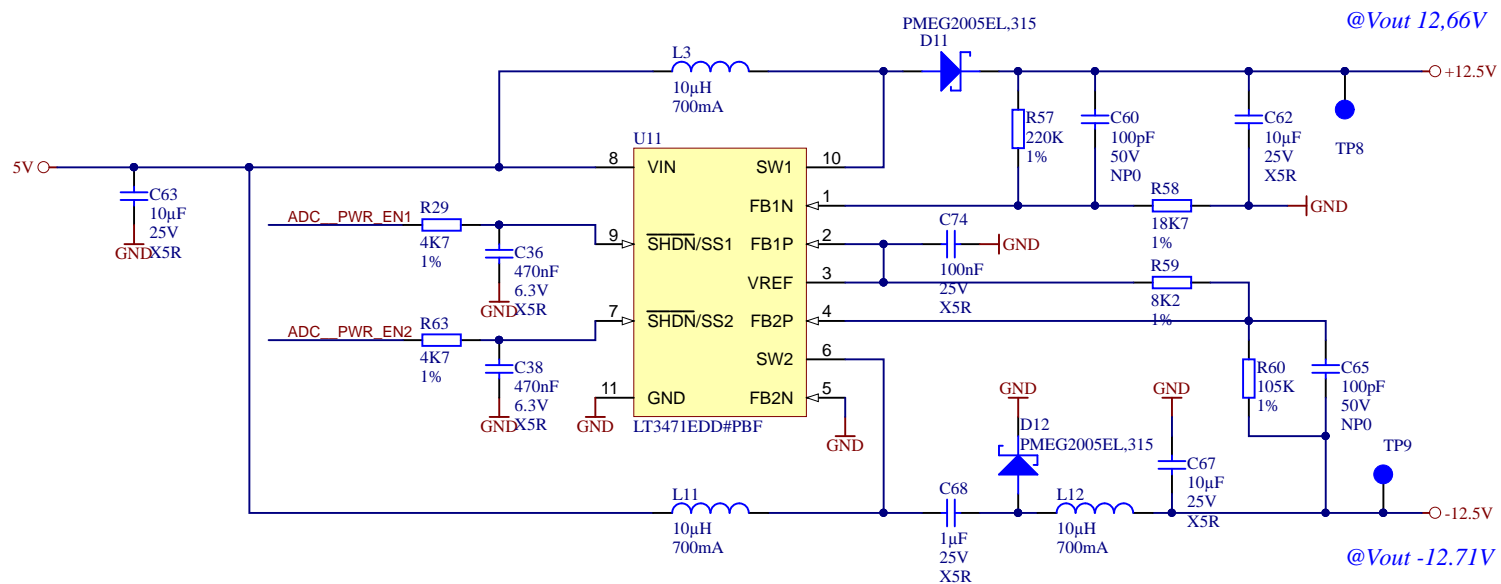
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			A4	Number: TEI0015 08-C8A
Date: 26.07.2019		Copyright: Trenz Electronic GmbH		Page 5 of 10
Drawn by: VY		Filename: FTDI.SchDoc		



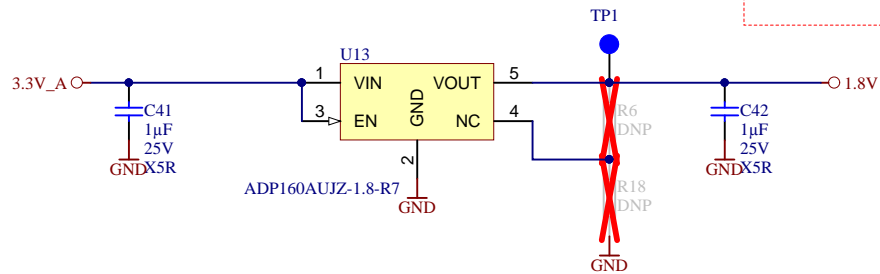
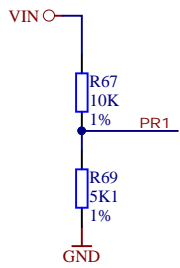
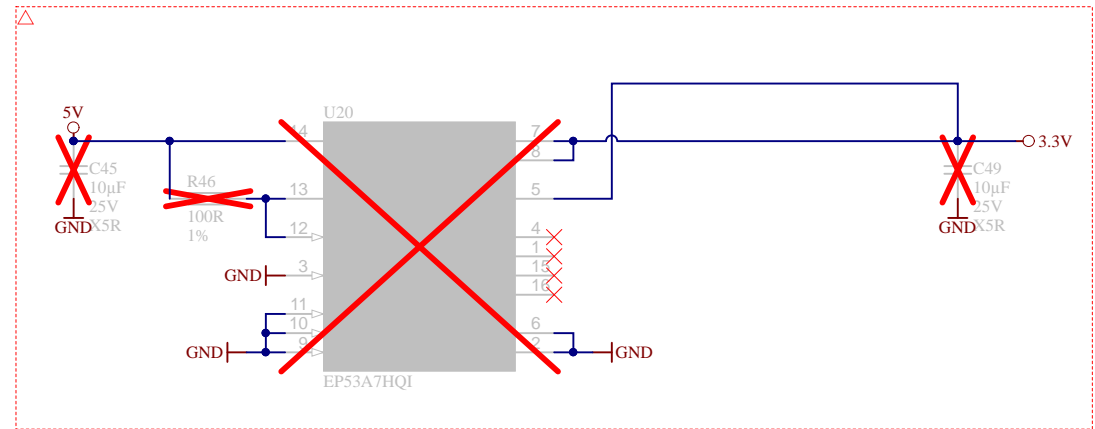
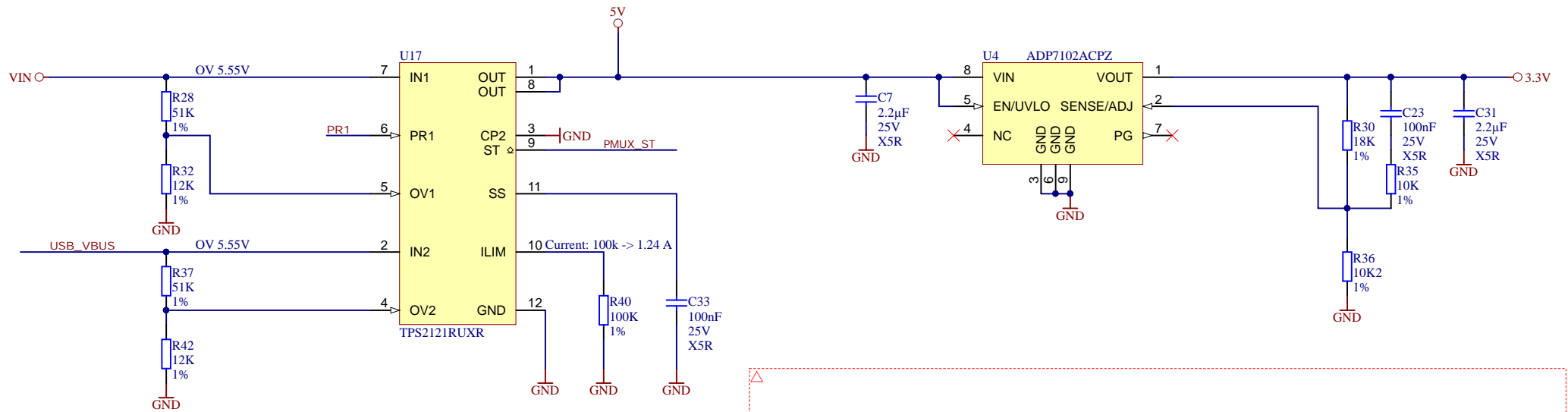
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	A4	Number: TEI0015 08-C8A	Rev. 03
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	Drawn by: VY	Filename: SENSOR_Flash_RAM.SchDoc	



Title: ADC		
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Title: Analog power		
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Title: PowerSupply		
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Revision 02:

- 1) VY: Replaced inductors L4, L5, L8 to 10µH L0603B100MDWFT
- 2) VY: Replaced diodes D11, D12 to PMEG2005EL,315
- 3) VY: Net ADC_EN renamed to ADC_PWR_EN
- 4) ED: Deleted T1A, T1B, T2A, T2B, T3A, T3B, R27, R28, R29, R30, R31, R32, R40 and C7
- 5) ED: Inserted power mux (U17) instead
- 6) ED: Changed U4 to LDO (ADP7102ACPZ)
- 7) ED: Inserted D-Flipflop (U18)
- 8) ED: Inserted oscillator (U19)
- 9) ED: Replaced inductors L3, L11, L12 to 10 µH MLP2520S100ST0S1

Revision 03:

- 1) VT: Added optional DCDC (U20, C45,C49,R46)

A

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D

	Title: Revision Changes		
	A4	Number: TEI0015 08-C8A	Rev. 03
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	Filename: Revision_Changes.SchDoc		

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