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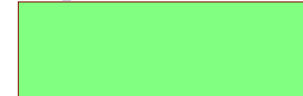
U_RPi-Headers
RPi-Headers.SchDoc



U_FPGA_B34
FPGA_B34.SchDoc



U_FPGA_B35
FPGA_B35.SchDoc



U_FPGA_MIO
FPGA_MIO.SchDoc



U_FPGA_RAM
FPGA_RAM.SchDoc



U_FPGA_PWR
FPGA_PWR.SchDoc



U_DDR3-RAM
DDR3-RAM.SchDoc



U_USB-PHY
USB-PHY.SchDoc



U_PowerSupply
PowerSupply.SchDoc



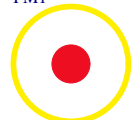
U_FTDI
FTDI.SchDoc



U_RPI_CAM_LCD
RPi-CAM-LCD.SchDoc



PM1



FIDU-DOT - mini
PM3

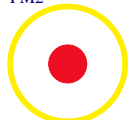


FIDU-DOT - mini
PM5



FIDU-DOT - mini

PM2



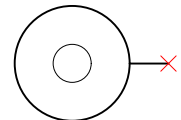
FIDU-DOT - mini
PM4



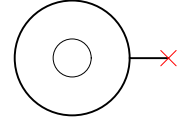
FIDU-DOT - mini
PM6



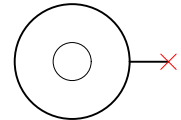
FIDU-DOT - mini



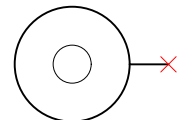
Mount.Hole 2.7mm (unplated)



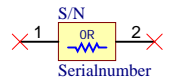
Mount.Hole 2.7mm (unplated)



Mount.Hole 2.7mm (unplated)



Mount.Hole 2.7mm (unplated)



Serial
Serial
Serialnumber 6,3 x 6.3mm

Assembly variant	010-1C
Created by	VT
Modified by	VT
Modified at	2019-11-21
SVN Revision	652



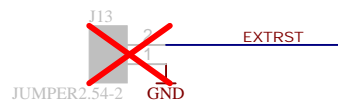
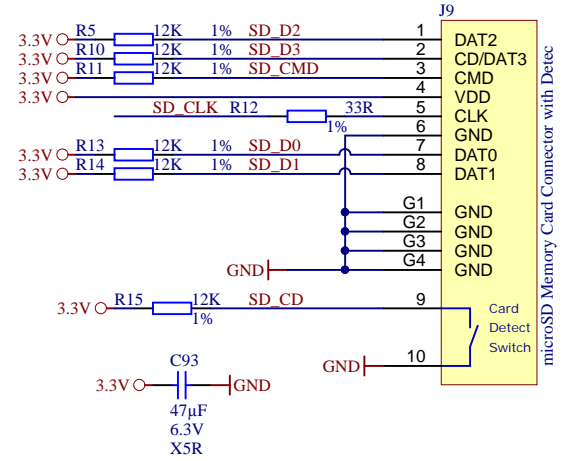
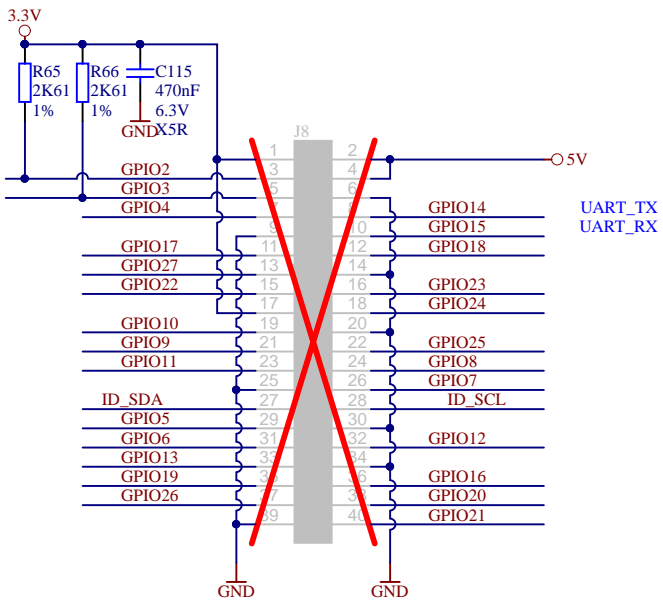
Title: TE0727		
A4	Number: TE0727 010-1C	Rev. 01
Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page1 of 12
Filename: TE0727.SchDoc		

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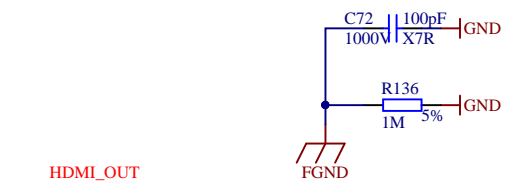
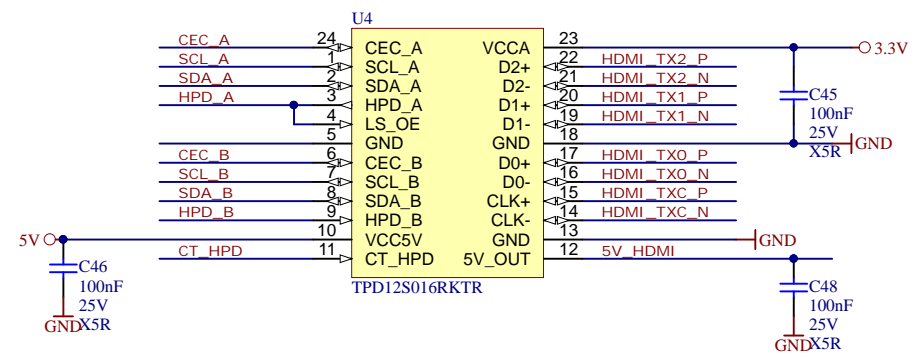
Title: TE0727 - Connectors		
A4	Number: TE0727 010-1C	Rev. 01
Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page2 of 12
Filename: RPi-Headers.SchDoc		

1

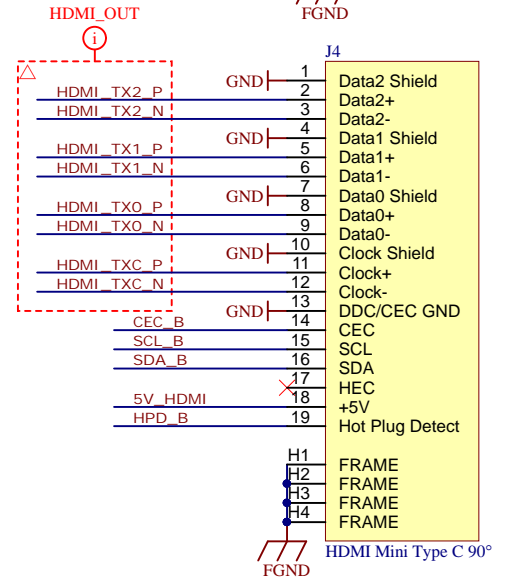
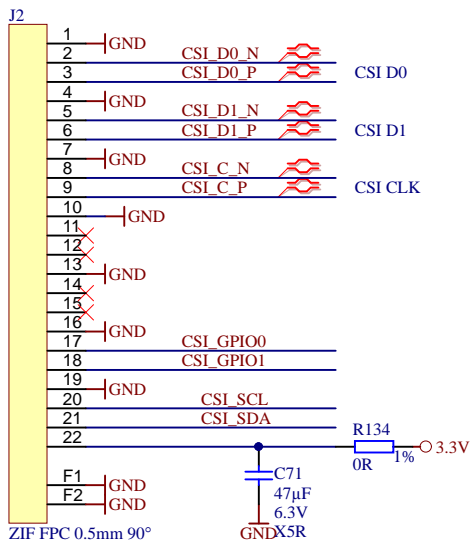
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CSI-2 Camera



Title: TE0727 - Connectors		
A4	Number: TE0727 010-1C	Rev. 01
Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page3 of 12
Filename: RPi-CAM-LCD.SchDoc		

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A

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D

U1A

BANK 34	
IO_L1P_T0_34	G11
IO_L1N_T0_34	H12
IO_L2P_T0_34	G12
IO_L2N_T0_34	H13
IO_L3P_T0_DQS_PUDC_B_34	G14
IO_L3N_T0_DQS_34	H14
IO_L4P_T0_34	J15
IO_L4N_T0_34	K15
IO_L5P_T0_34	J13
IO_L5N_T0_34	J14
IO_L6P_T0_34	H11
IO_L6N_T0_VREF_34	J11
IO_L7P_T1_34	N13
IO_L7N_T1_34	N14
IO_L8P_T1_34	L15
IO_L8N_T1_34	M15
IO_L9P_T1_DQS_34	L14
IO_L9N_T1_DQS_34	M14
IO_L10P_T1_34	K13
IO_L10N_T1_34	L13
IO_L11P_T1_SRCC_34	K11
IO_L11N_T1_SRCC_34	K12
IO_L12P_T1_MRCC_34	L12
IO_L12N_T1_MRCC_34	M12
IO_L13P_T2_MRCC_34	N11
IO_L13N_T2_MRCC_34	N12
IO_L15P_T2_DQS_34	P15
IO_L15N_T2_DQS_34	R15
IO_L16P_T2_34	P11
IO_L16N_T2_34	R11
IO_L17P_T2_34	R12
IO_L17N_T2_34	R13
IO_L18P_T2_34	P13
IO_L18N_T2_34	P14
IO_L19P_T3_34	M9
IO_L19N_T3_VREF_34	N9
IO_L20P_T3_34	R7
IO_L20N_T3_34	R8
IO_L21P_T3_DQS_34	M10
IO_L21N_T3_DQS_34	M11
IO_L22P_T3_34	N7
IO_L22N_T3_34	N8
IO_L23P_T3_34	P8
IO_L23N_T3_34	P9
IO_L24P_T3_34	P10
IO_L24N_T3_34	R10

XC7Z010-1CLG225C

B34



CEC_A

SDA_A

SCL_A

HPD_A

GPIO21

GPIO2

GPIO11

GPIO20

GPIO16

GPIO4

GPIO17

GPIO3

GPIO15

GPIO14

GPIO23

GPIO26

GPIO13

GPIO18

CT_HP

GPIO7

GPIO25

GPIO24

GPIO27

GPIO12

GPIO19

GPIO6

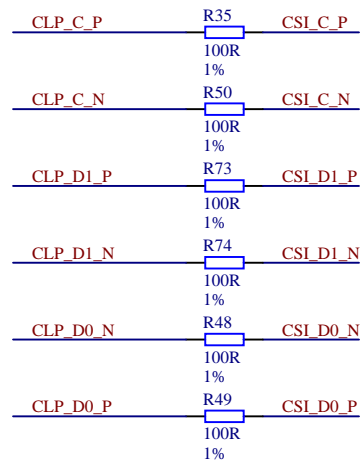
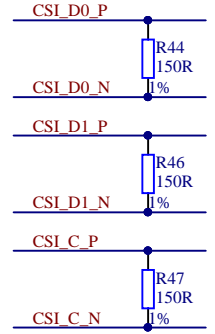
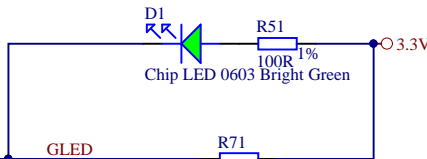
GPIO8

GPIO5

GPIO10

GPIO9

GPIO22



Title: TE0727 - FPGA B34			
A4	Number: TE0727 010-1C	Rev. 01	
Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page 4 of 12	
Filename: FPGA_B34.SchDoc			

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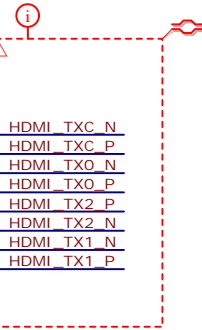
UIB


BANK 35	IO_L1P_T0_AD0P_35	F12
	IO_L1N_T0_AD0N_35	E13
	IO_L2P_T0_AD8P_35	E11
	IO_L2N_T0_AD8N_35	F12
	IO_L3P_T0_DQS_AD1P_35	F13
	IO_L3N_T0_DQS_AD1N_35	F14
	IO_L5P_T0_AD9P_35	G15
	IO_L5N_T0_AD9N_35	F15

XC7Z010-1CLG225C

HDMI_TXC_N
HDMI_TXC_P
HDMI_TX0_N
HDMI_TX0_P
HDMI_TX2_P
HDMI_TX2_N
HDMI_TX1_N
HDMI_TX1_P

B35



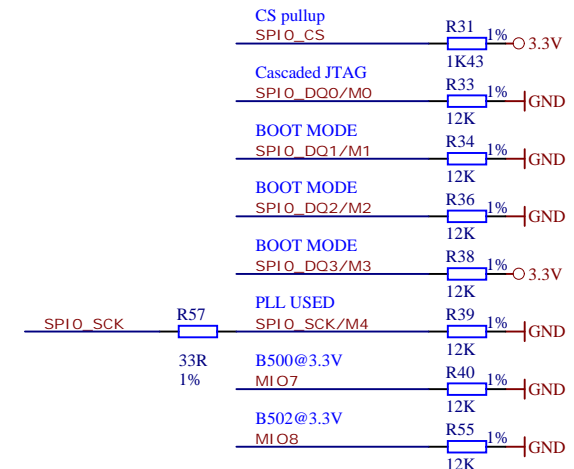
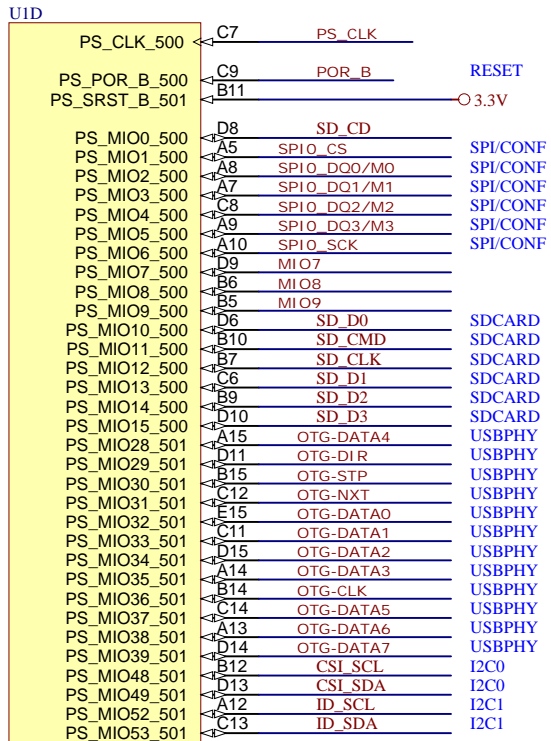
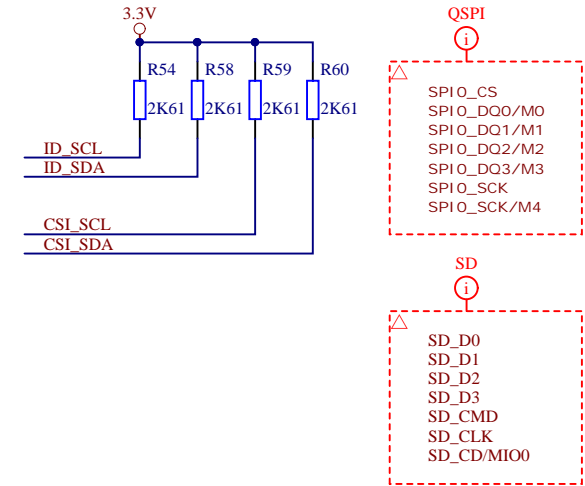
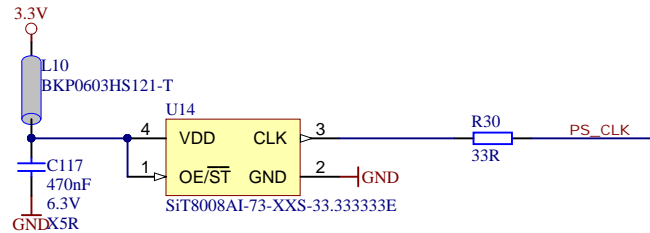
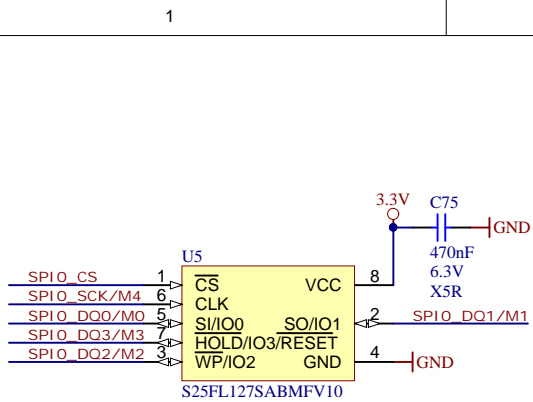
	Title: TE0727 - FPGA B35		
	A4	Number: TE0727 010-1C	Rev. 01
	Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page 5 of 12
	Filename: FPGA_B35.SchDoc		

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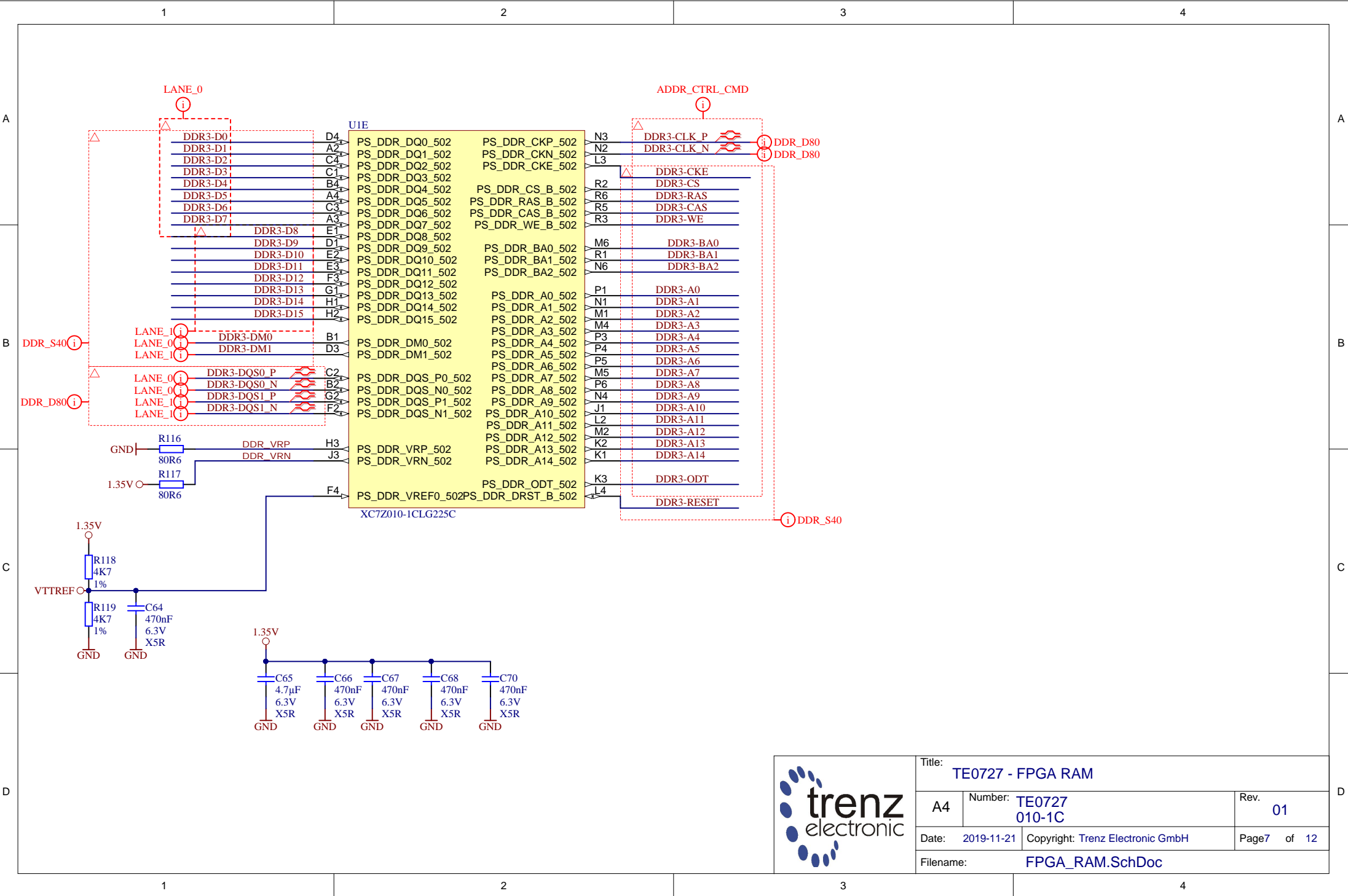

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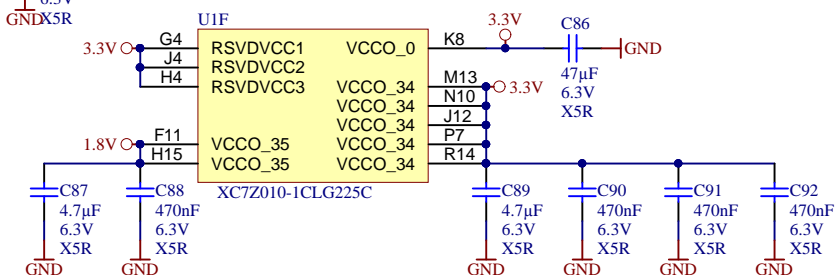
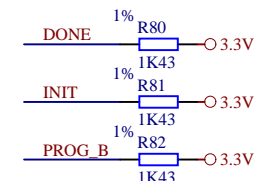
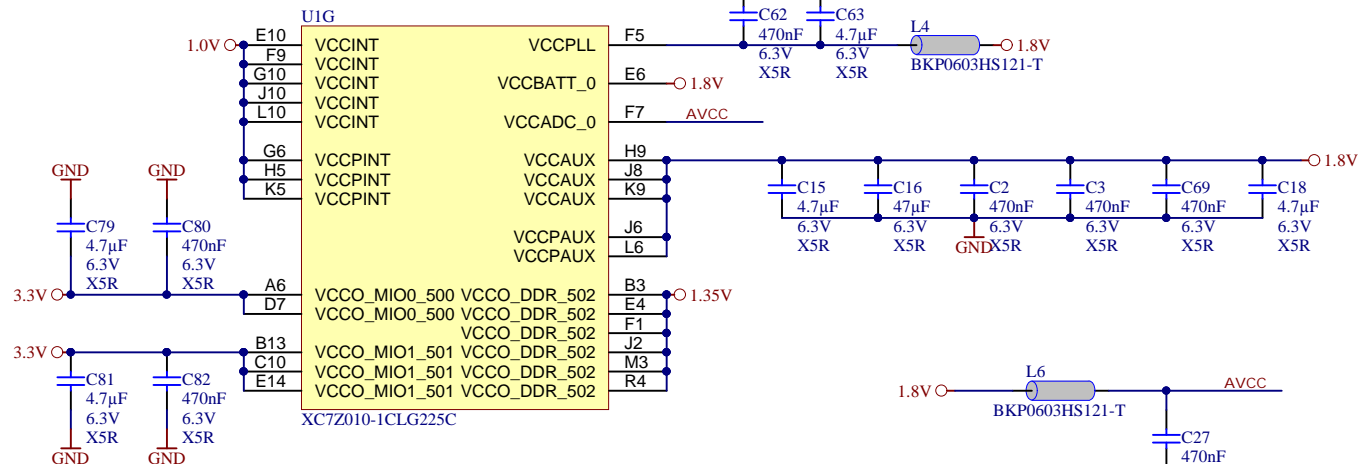
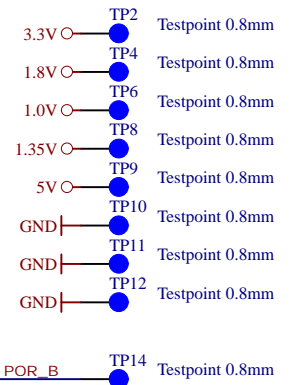
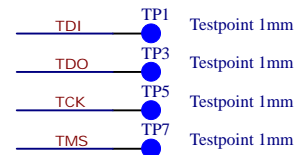
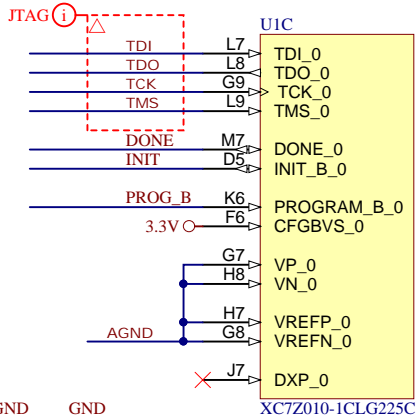
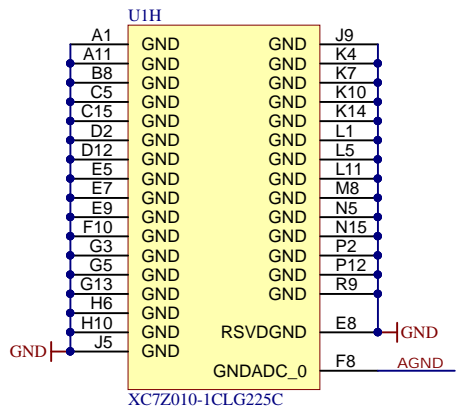
4



Title: TE0727 - FPGA MIO		
A4	Number: TE0727 010-1C	Rev. 01
Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page6 of 12
Filename: FPGA_MIO.SchDoc		

Title: TE0727 - FPGA RAM		
A4	Number: TE0727 010-1C	Rev. 01
Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page 7 of 12
Filename: FPGA_RAM.SchDoc		



Title: TE0727 - FPGA PWR		
A4	Number: TE0727 010-1C	Rev. 01
Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page 8 of 12
Filename: FPGA_PWR.SchDoc		

A

A

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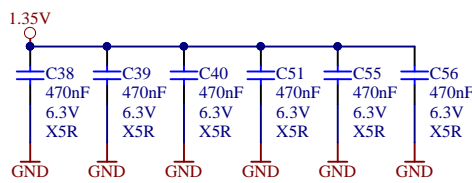
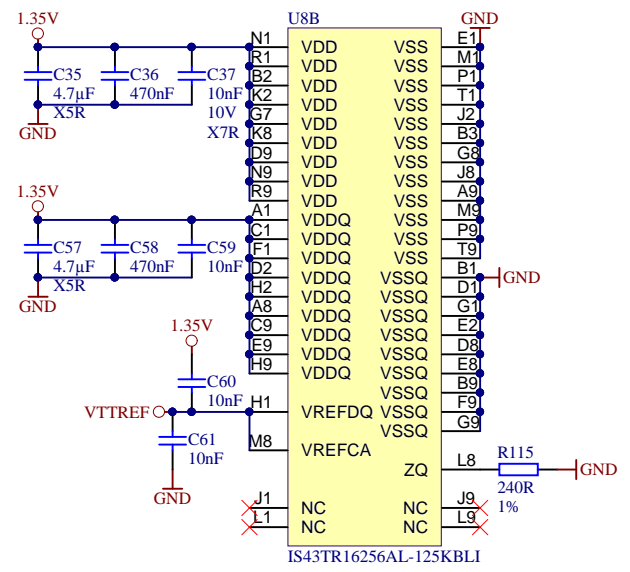
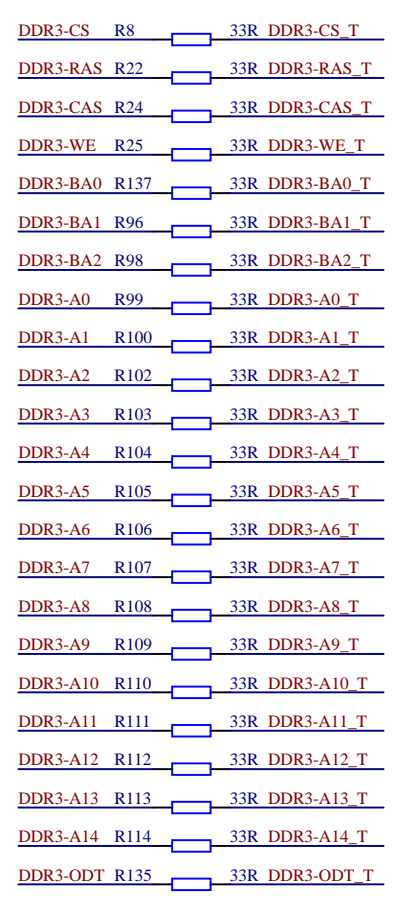
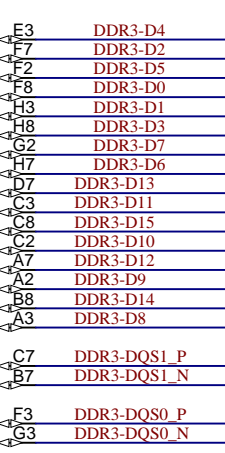
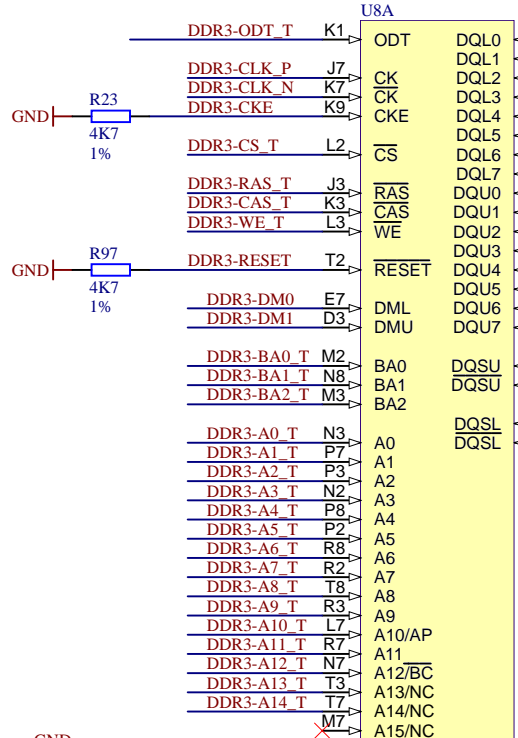
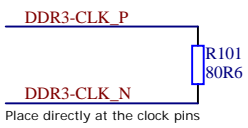
B

C

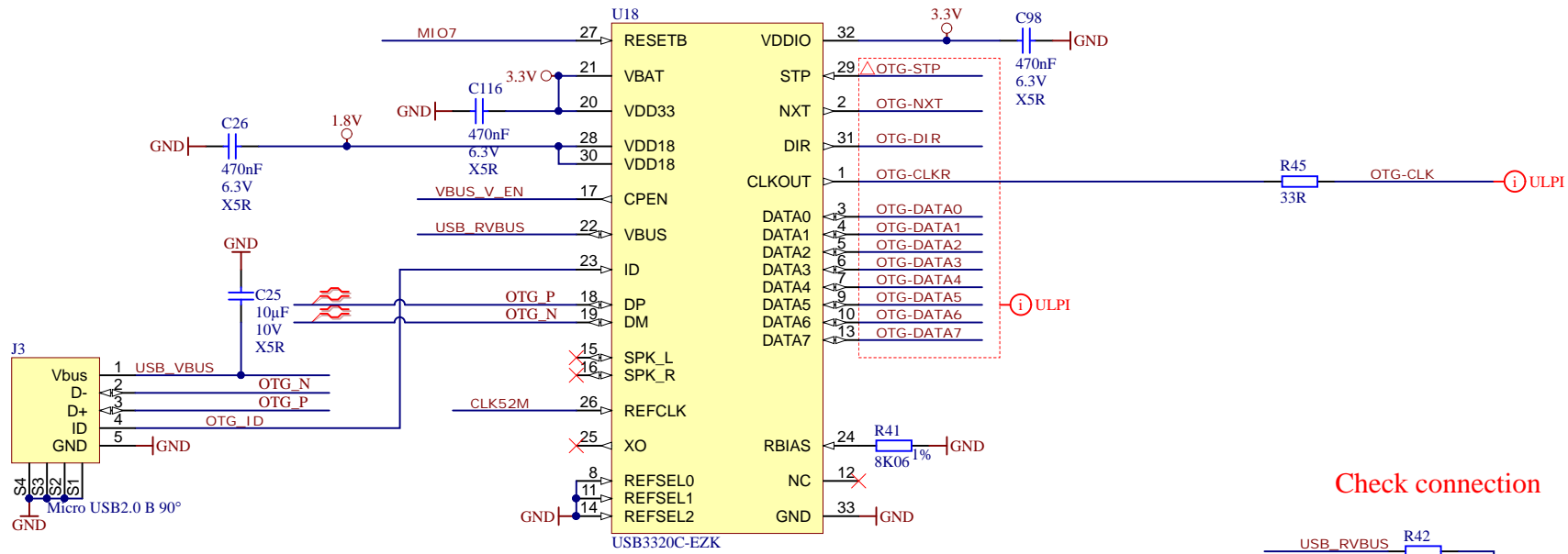
C

D

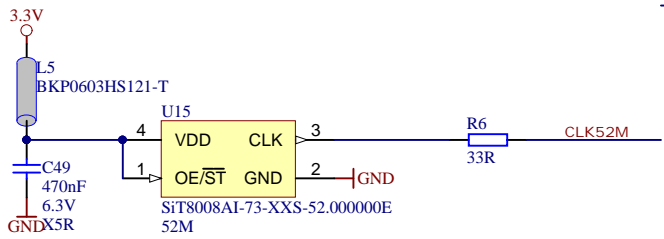
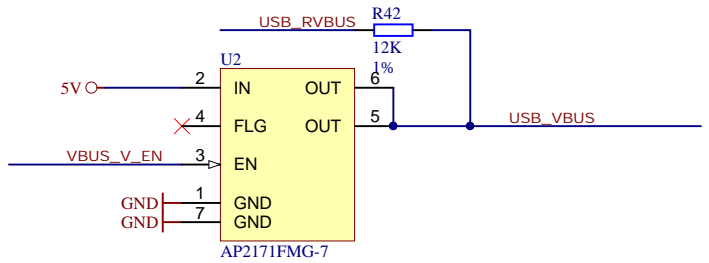
D



Title: TE0727 - DDR Memory		
A4	Number: TE0727 010-1C	Rev. 01
Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page 9 of 12
Filename: DDR3-RAM.SchDoc		



Check connection



Title: TE0727 - USB		
A4	Number: TE0727 010-1C	Rev. 01
Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page 10 of 12
Filename: USB-PHY.SchDoc		

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A

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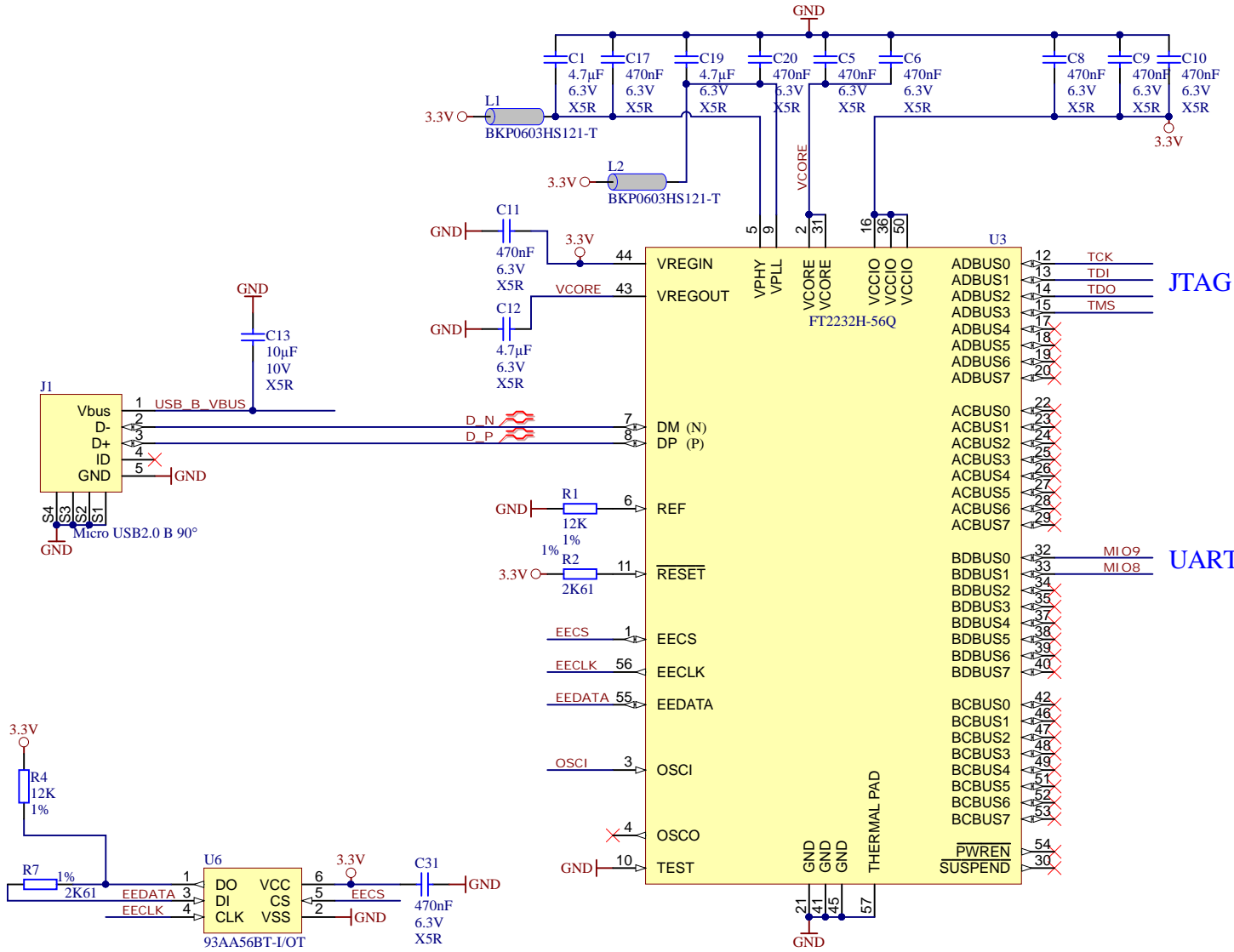
B

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D



JTAG

UART



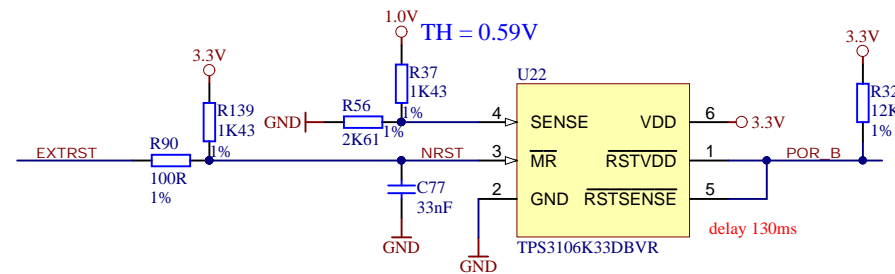
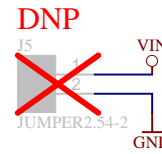
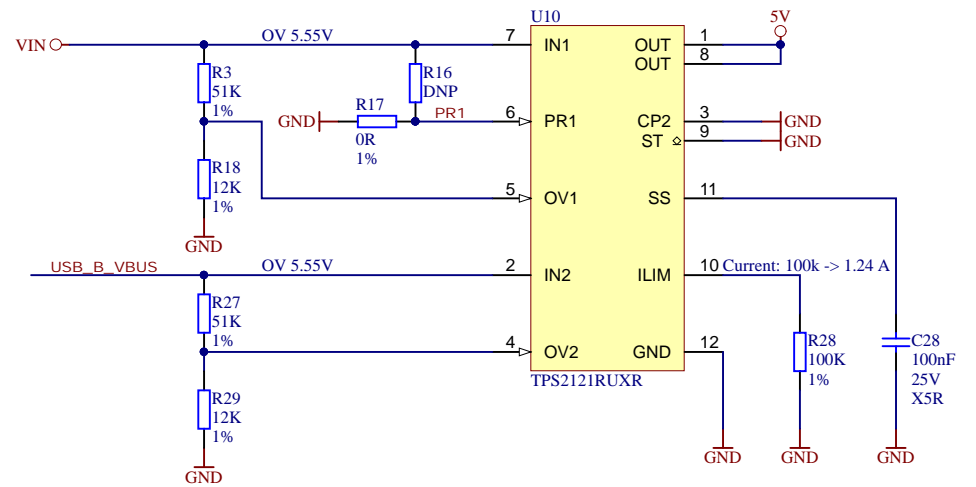
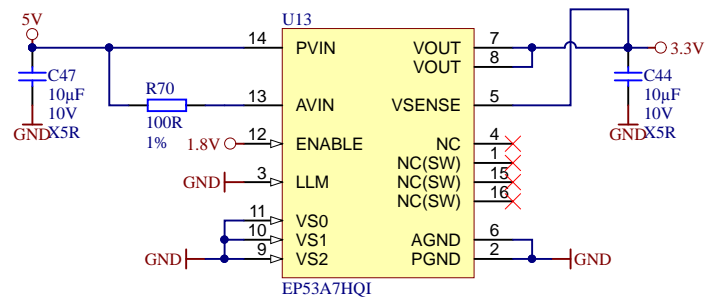
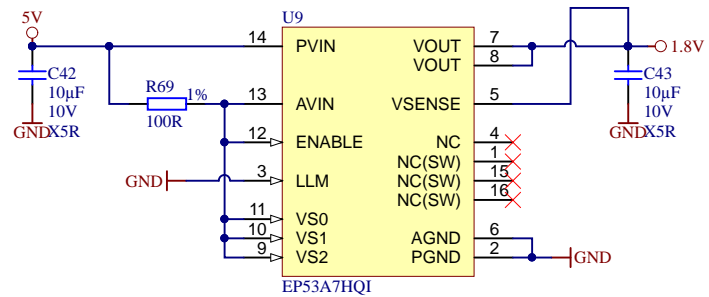
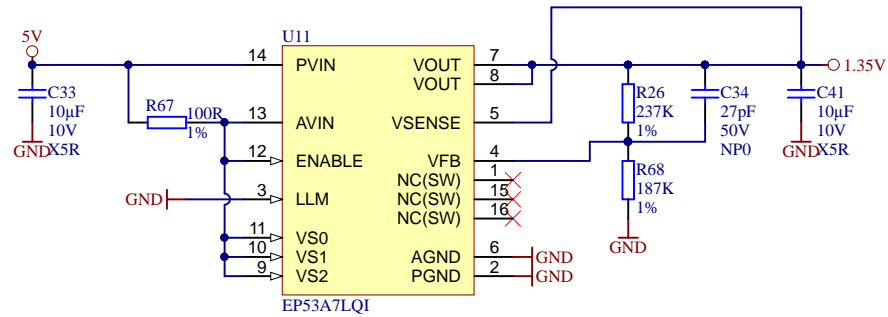
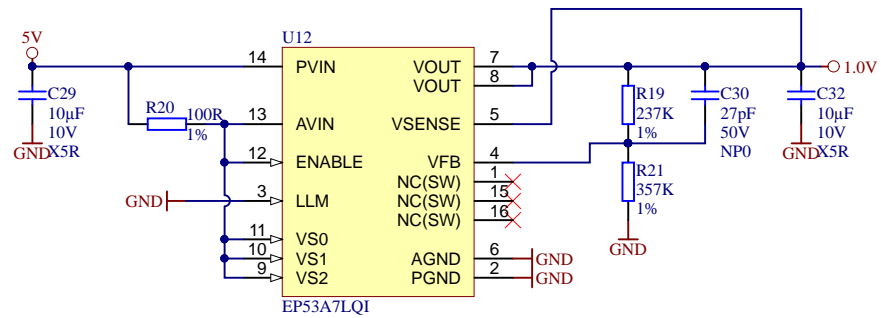
Title: TE0727 - FTDI		
A4	Number: TE0727 010-1C	Rev. 01
Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page 11 of 12
Filename: FTDI.SchDoc		

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	Title: TE0727 - PowerSupply		
	A4	Number: TE0727 010-1C	Rev. 01
	Date: 2019-11-21	Copyright: Trenz Electronic GmbH	Page 12 of 12
	Filename: PowerSupply.SchDoc		