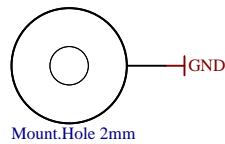
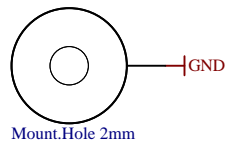
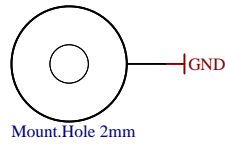
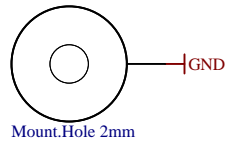
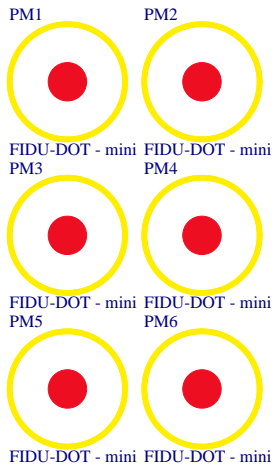
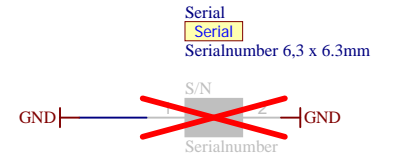


- U\_J1  
J1.SchDoc
- U\_Soc\_1  
Soc\_1.SchDoc
- U\_Soc\_2  
Soc\_2.SchDoc
- U\_Soc\_3  
Soc\_3.SchDoc
- U\_DDR3  
DDR3-RAM.SchDoc
- U\_ETH  
ETH.SchDoc
- U\_PowerSupply  
PowerSupply.SchDoc



Assembly variant	010I
Created by	VT
Modified by	VY
Modified at	2022-12-05
SVN Revision	Unknown revision

Title: TEM0005		
A4	Number: TEM0005 010I	Rev. 02
Date: 2020-01-22	Copyright: Trenz Electronic GmbH / TT	Page1 of 9
Filename: TEM0005.SchDoc		



1

2

3

4

A

A

B

B

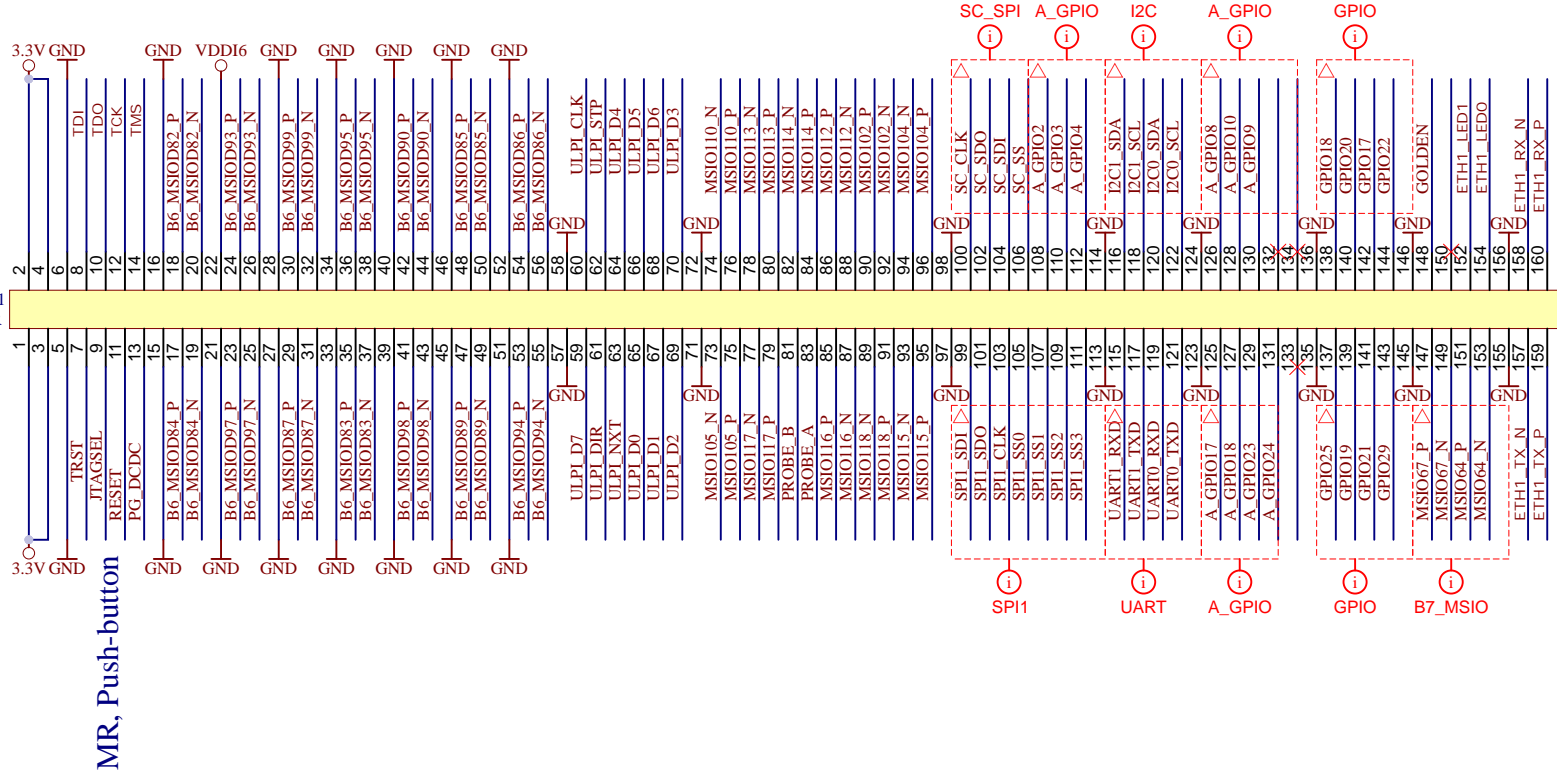
C

C


D

D

J1  
ST5-80-1.50-L-D-P-TR



MR, Push-button

			Title: TEM0005 - B2B_connector J1	
			A4	Number: TEM0005 010I
Date: 2020-01-22		Copyright: Trenz Electronic GmbH / TT		Page2 of 9
Filename: J1.SchDoc				

1

2

3

4

A

A

B

B

C

C

D

D

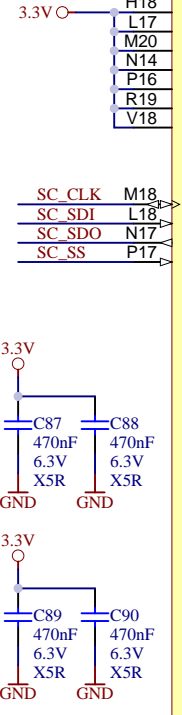
U2A

**BANK 0**

VDDIO A7  
VDDIO A17  
VDDIO B10  
VDDIO C3  
VDDIO C13  
VDDIO D6  
VDDIO D16  
VDDIO E9  
VDDIO G8  
VDDIO G10  
VDDIO G12

DDRIO29PB0/MDDR\_ADDR14  
DDRIO29NB0/MDDR\_ADDR15  
DDRIO30PB0/MDDR\_ADDR12  
DDRIO30NB0/MDDR\_ADDR13  
DDRIO31PB0/MDDR\_ADDR10  
DDRIO31NB0/MDDR\_ADDR11  
DDRIO32PB0/MDDR\_ADDR8  
DDRIO32NB0/MDDR\_ADDR9  
DDRIO33PB0/MDDR\_ODT  
DDRIO33NB0/MDDR\_ADDR7  
DDRIO34PB0/MDDR\_ADDR5  
DDRIO34NB0/MDDR\_ADDR6  
DDRIO35PB0/MDDR\_ADDR3  
DDRIO35NB0/MDDR\_ADDR4  
DDRIO36PB0/MDDR\_ADDR1  
DDRIO36NB0/MDDR\_ADDR2  
DDRIO37PB0/MDDR\_BA2  
DDRIO37NB0/MDDR\_ADDR0  
DDRIO38PB0/MDDR\_BA0  
DDRIO38NB0/MDDR\_BA1  
DDRIO39PB0/MDDR\_CLK  
DDRIO39NB0/MDDR\_CLK\_N  
DDRIO40PB0/MDDR\_RESET\_N  
DDRIO40NB0/MDDR\_CAS\_N  
DDRIO41PB0/MDDR\_CKE  
DDRIO41NB0/MDDR\_CS\_N  
DDRIO42PB0/MDDR\_RAS\_N  
DDRIO42NB0/MDDR\_WE\_N  
\*DDRIO43PB0/MDDR\_DQ14  
DDRIO43NB0/MDDR\_DQ15  
\*DDRIO44PB0/MDDR\_DQ12  
DDRIO44NB0/MDDR\_DQ13  
DDRIO45PB0/MDDR\_TMATCH\_0\_IN  
DDRIO45NB0/MDDR\_DM\_RDQS1  
\*DDRIO46PB0/MDDR\_DQS1  
DDRIO46NB0/MDDR\_DQS1\_N  
\*DDRIO47PB0/MDDR\_DQ10  
DDRIO47NB0/MDDR\_DQ11  
DDRIO48PB0/MDDR\_DQ8  
DDRIO48NB0/MDDR\_DQ9  
DDRIO49PB0/MDDR\_DQ7  
DDRIO49NB0/MDDR\_TMATCH\_0\_OUT  
DDRIO50PB0/MDDR\_DQ5  
DDRIO50NB0/MDDR\_DQ6  
DDRIO51PB0/MDDR\_DM\_RDQS0  
DDRIO51NB0/MDDR\_DQ4  
DDRIO52PB0/MDDR\_DQS0  
DDRIO52NB0/MDDR\_DQS0\_N  
DDRIO53PB0/MDDR\_DQ2  
DDRIO53NB0/MDDR\_DQ3  
DDRIO54PB0/MDDR\_DQ0  
DDRIO54NB0/MDDR\_DQ1  
DDRIO55PB0/CCC\_NE0\_CLKI3  
DDRIO55NB0  
DDRIO56PB0/MDDR\_DQ\_ECC1  
DDRIO56NB0/MDDR\_DQ\_ECC0  
DDRIO57PB0/MDDR\_TMATCH\_ECC\_IN  
DDRIO57NB0/MDDR\_DM\_RDQS\_ECC  
DDRIO58PB0/MDDR\_DQS\_ECC  
DDRIO58NB0/MDDR\_DQS\_ECC\_N  
DDRIO59PB0/GB0  
DDRIO59NB0/GB4  
DDRIO60PB0/MDDR\_TMATCH\_ECC\_OUT  
DDRIO60NB0/CCC\_NE1\_CLKI3

A18 DDR3-A14  
B18 DDR3-A15  
D17 DDR3-A12  
C17 DDR3-A13  
D15 DDR3-A10  
E15 DDR3-A11  
A16 DDR3-A8  
B17 DDR3-A9  
B16 DDR3-ODT  
C16 DDR3-A7  
B14 DDR3-A5  
A15 DDR3-A6  
C14 DDR3-A3  
C15 DDR3-A4  
A13 DDR3-A1  
A14 DDR3-A2  
D13 DDR3-BA2  
D14 DDR3-A0  
E13 DDR3-BA0  
F13 DDR3-BA1  
B13 DDR3-CLK\_P  
B12 DDR3-CLK\_N  
F11 DDR3-RESET  
E12 DDR3-CAS  
C12 DDR3-CKE  
C11 DDR3-CS  
D12 DDR3-RAS  
E11 DDR3-WE  
A11 DDR3-D14  
B11 DDR3-D15  
D10 DDR3-D12  
E10 DDR3-D13  
E8 TMATCH  
F9 DDR3-DM1  
C9 DDR3-DQS1\_P  
B9 DDR3-DQS1\_N  
D9 DDR3-D10  
C10 DDR3-D11  
A9 DDR3-D8  
A10 DDR3-D9  
D7 DDR3-D7  
D8  
A8 DDR3-D5  
B8 DDR3-D6  
B6 DDR3-DM0  
B7 DDR3-D4  
C6 DDR3-DQS0\_P  
C7 DDR3-DQS0\_N  
A5 DDR3-D2  
A6 DDR3-D3  
E7 DDR3-D0  
F8 DDR3-D1  
E6 NC  
D5 NC  
A3 NC  
A4 NC  
D4 TMATCH\_ECC  
C5 NC  
B3 NC  
B4 NC  
A1 NC  
B1 NC  
C4 NC  
D3 NC



\*clock input in M25025/50/60  
M2S010-VFG4001

U2C

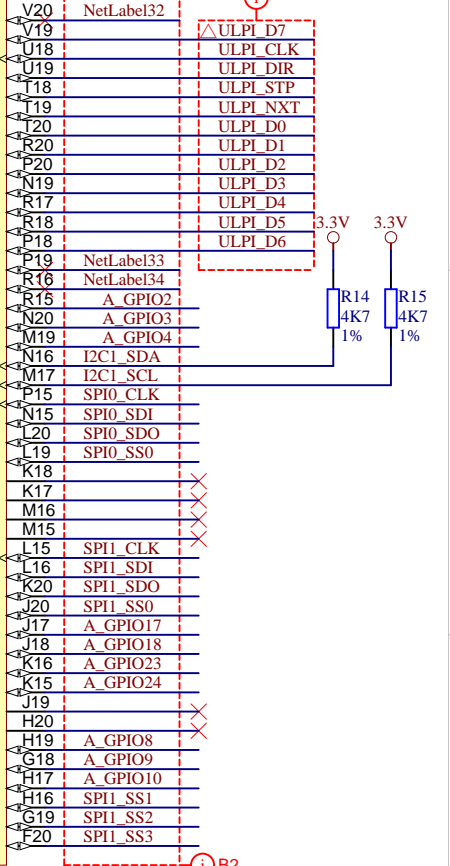
**BANK 2**

VDDI2 H18  
VDDI2 L17  
VDDI2 M20  
VDDI2 N14  
VDDI2 P16  
VDDI2 R19  
VDDI2 V18

SC\_CLK M18  
SC\_SDI L18  
SC\_SDO N17  
SC\_SS P17

VDDI2 V20  
VDDI2 V19  
VDDI2 U18  
VDDI2 U19  
VDDI2 T18  
VDDI2 T19  
VDDI2 T20  
VDDI2 R20  
VDDI2 P20  
VDDI2 N19  
VDDI2 R17  
VDDI2 R18  
VDDI2 P18  
VDDI2 P19  
VDDI2 R16  
VDDI2 R15  
VDDI2 M20  
VDDI2 N19  
VDDI2 M17  
VDDI2 P15  
VDDI2 N15  
VDDI2 L20  
VDDI2 K19  
VDDI2 K18  
VDDI2 K17  
VDDI2 M16  
VDDI2 NC  
VDDI2 M15  
VDDI2 L15  
VDDI2 L16  
VDDI2 K20  
VDDI2 J17  
VDDI2 J20  
VDDI2 K16  
VDDI2 K15  
VDDI2 J19  
VDDI2 H20  
VDDI2 H19  
VDDI2 G18  
VDDI2 H17  
VDDI2 H16  
VDDI2 G19  
VDDI2 F20

MSIO0PB2  
MSIO0NB2/USB\_DATA7\_B  
MSIO1PB2/USB\_XCLK\_B  
MSIO1NB2/USB\_DIR\_B  
MSIO2PB2/USB\_STP\_B  
MSIO2NB2/USB\_NXT\_B  
MSIO3PB2/USB\_DATA0\_B  
MSIO3NB2/USB\_DATA1\_B  
MSIO4PB2/USB\_DATA2\_B  
MSIO4NB2/USB\_DATA3\_B  
MSIO5PB2/USB\_DATA4\_B  
MSIO5NB2/USB\_DATA5\_B  
MSIO6PB2/USB\_DATA6\_B  
MSIO6NB2  
MSIO7PB2  
MSIO7NB2/CAN\_TX/GPIO\_2\_A/USB\_DATA0\_A  
MSIO8PB2/CAN\_RX/GPIO\_3\_A/USB\_DATA1\_A  
MSIO8NB2/CAN\_TX\_EN\_N/GPIO\_4\_A/USB\_DATA2\_A  
MSIO11PB2/CCC\_NE0\_CLKI1/I2C\_1\_SDA/GPIO\_0\_A/USB\_DATA3\_A  
MSIO11NB2/CCC\_NE0\_CLKI2/I2C\_1\_SCL/GPIO\_1\_A/USB\_DATA4\_A  
MSIO12PB2/SPI\_0\_CLK/USB\_XCLK\_A  
MSIO12NB2/SPI\_0\_SDI/GPIO\_5\_A/USB\_DIR\_A  
MSIO13PB2/SPI\_0\_SDO/GPIO\_6\_A/USB\_STP\_A  
MSIO13NB2/SPI\_0\_SS0/GPIO\_7\_A/USB\_NXT\_A  
MSIO14PB2/SPI\_1\_CLK  
MSIO14NB2/SPI\_1\_SDI/GPIO\_11\_A  
MSIO15PB2/SPI\_1\_SDO/GPIO\_12\_A  
MSIO15NB2/SPI\_1\_SS0/GPIO\_13\_A  
MSIO16PB2/SPI\_1\_SS4/GPIO\_17\_A  
MSIO16NB2/SPI\_1\_SS5/GPIO\_18\_A  
MSIO17PB2/SPI\_1\_SS6/GPIO\_23\_A  
MSIO17NB2/SPI\_1\_SS7/GPIO\_24\_A  
\*NC  
\*NC  
MSIO18PB2/SPI\_0\_SS1/GPIO\_8\_A/USB\_DATA5\_A  
MSIO18NB2/SPI\_0\_SS2/GPIO\_9\_A/USB\_DATA6\_A  
MSIO19PB2/SPI\_0\_SS3/GPIO\_10\_A/USB\_DATA7\_A  
MSIO19NB2/SPI\_1\_SS1/GPIO\_14\_A  
MSIO20PB2/SPI\_1\_SS2/GPIO\_15\_A  
MSIO20NB2/SPI\_1\_SS3/GPIO\_16\_A



Title: TEM005 - SoC_1		
A4	Number: TEM005 010I	Rev. 02
Date: 2020-01-22	Copyright: Trenz Electronic GmbH	Page3 of 9
Filename: Soc_1.SchDoc		

A

B

C

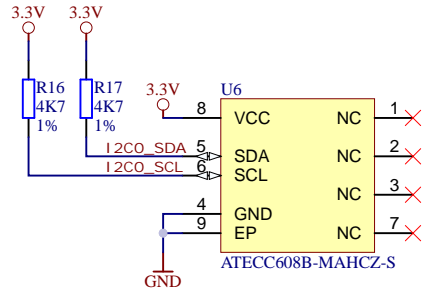
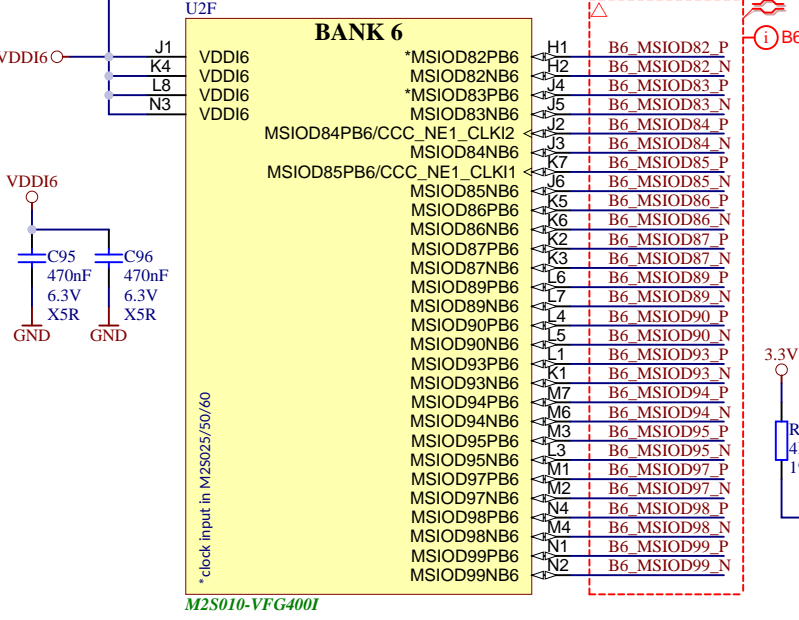
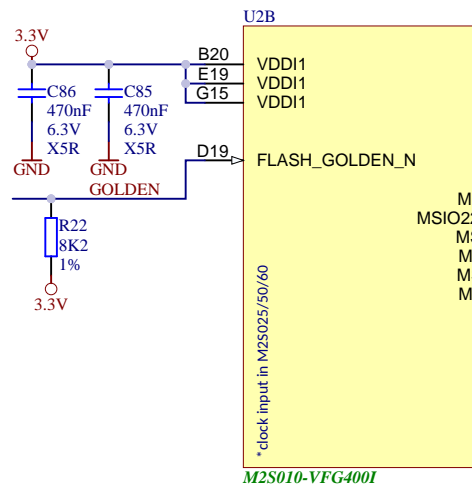
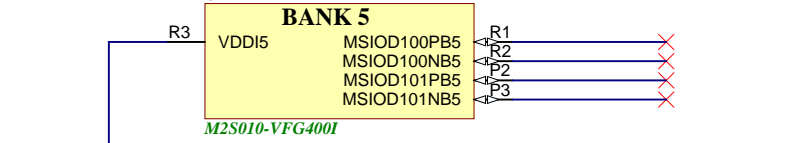
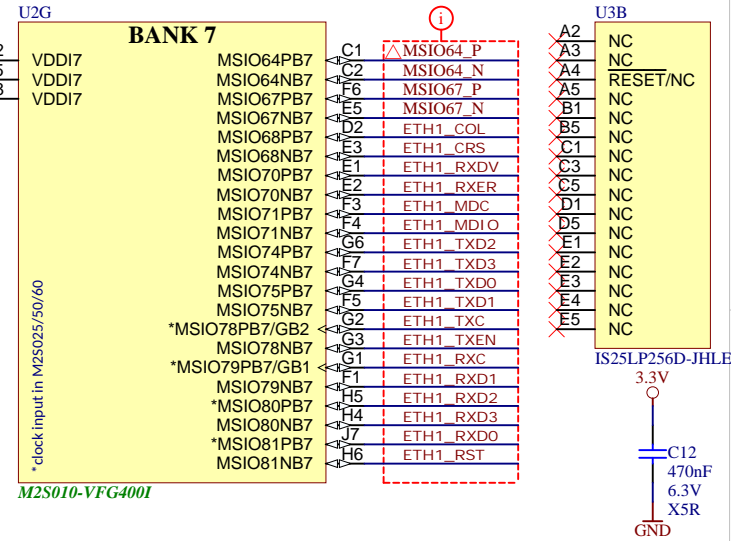
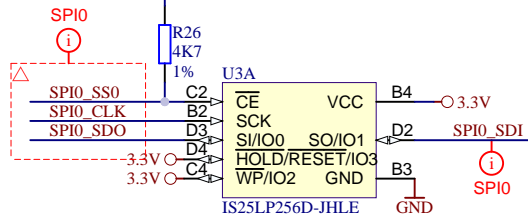
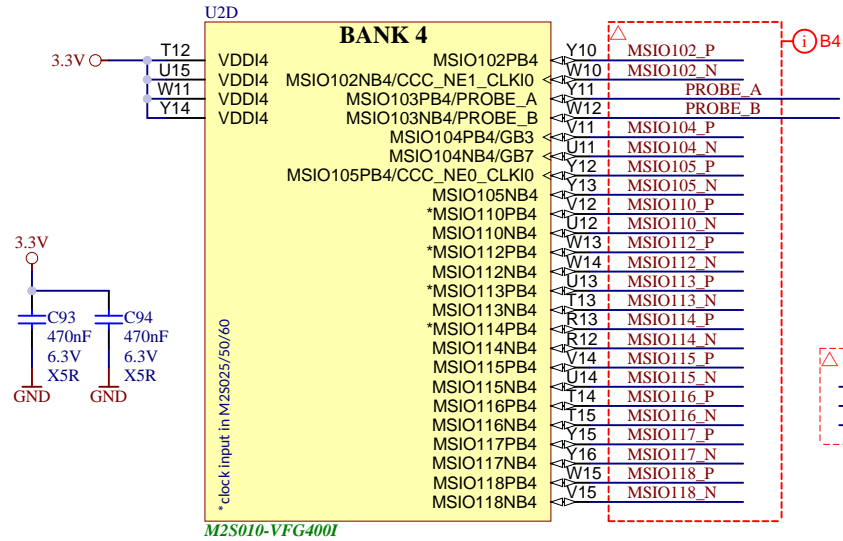
D

A

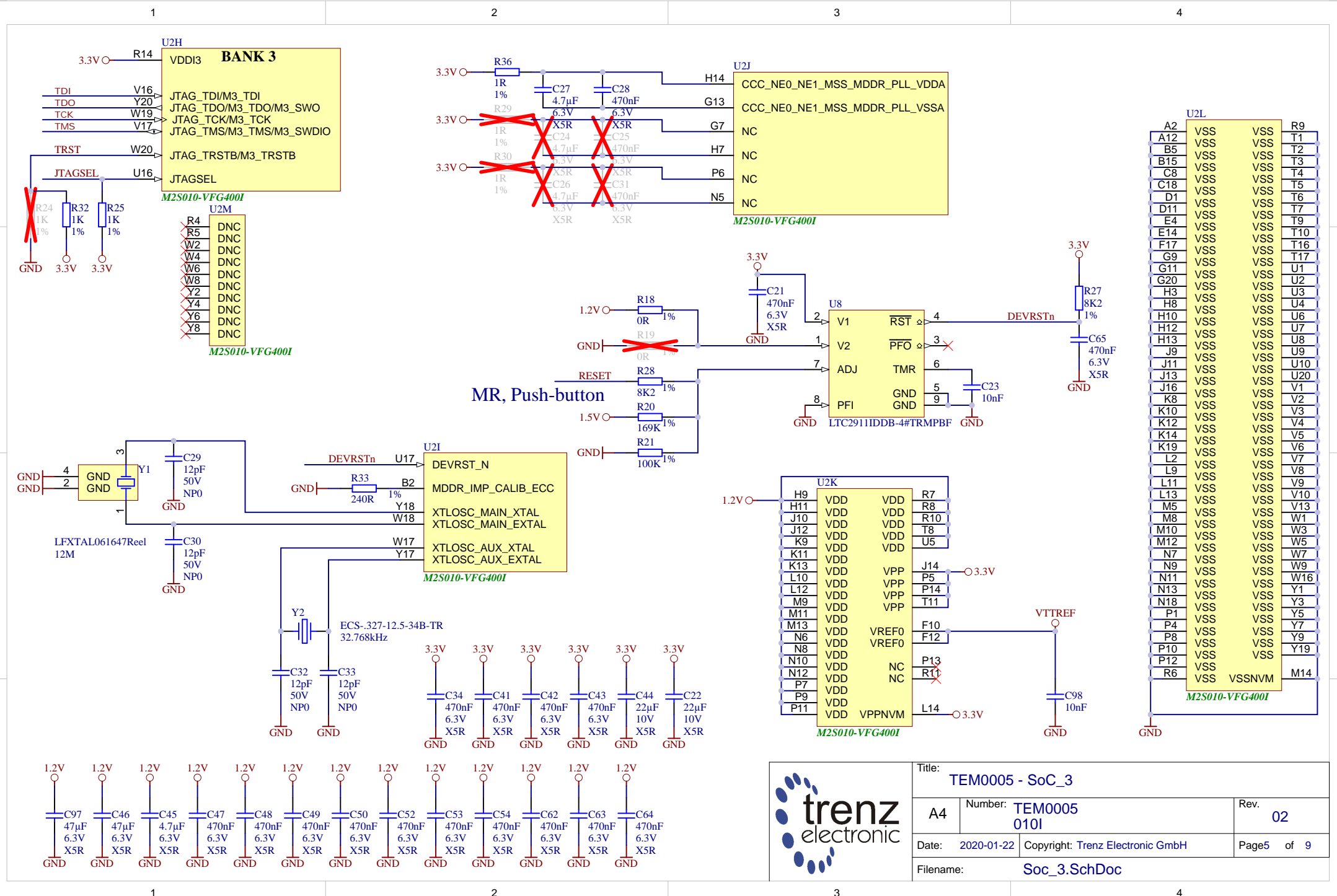
B

C

D



Title: TEM005 - SoC_2		Rev. 02	
A4	Number: TEM005 010I	Page 4 of 9	
Date: 2020-01-22	Copyright: Trenz Electronic GmbH	Page 4 of 9	
Filename: Soc_2.SchDoc			



Title: <b>TEM0005 - SoC_3</b>		
A4	Number: <b>TEM0005 010I</b>	Rev. <b>02</b>
Date: 2020-01-22	Copyright: Trenz Electronic GmbH	Page5 of 9
Filename: <b>Soc_3.SchDoc</b>		

A

A

B

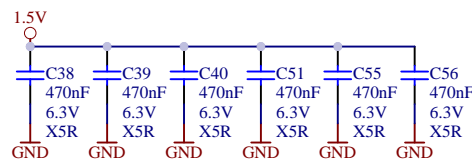
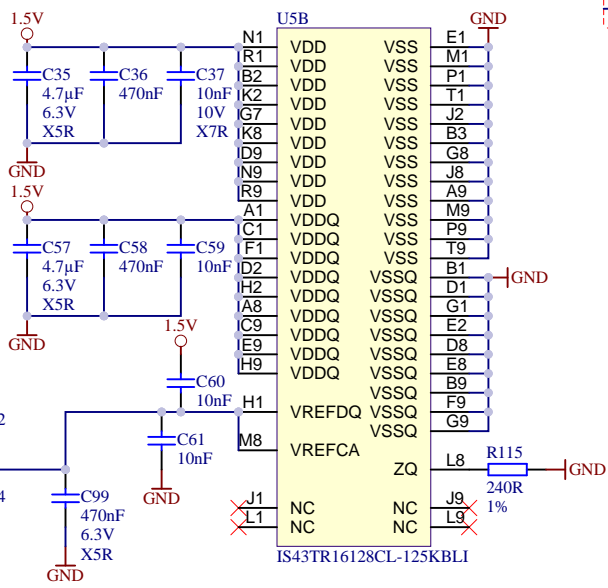
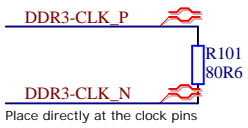
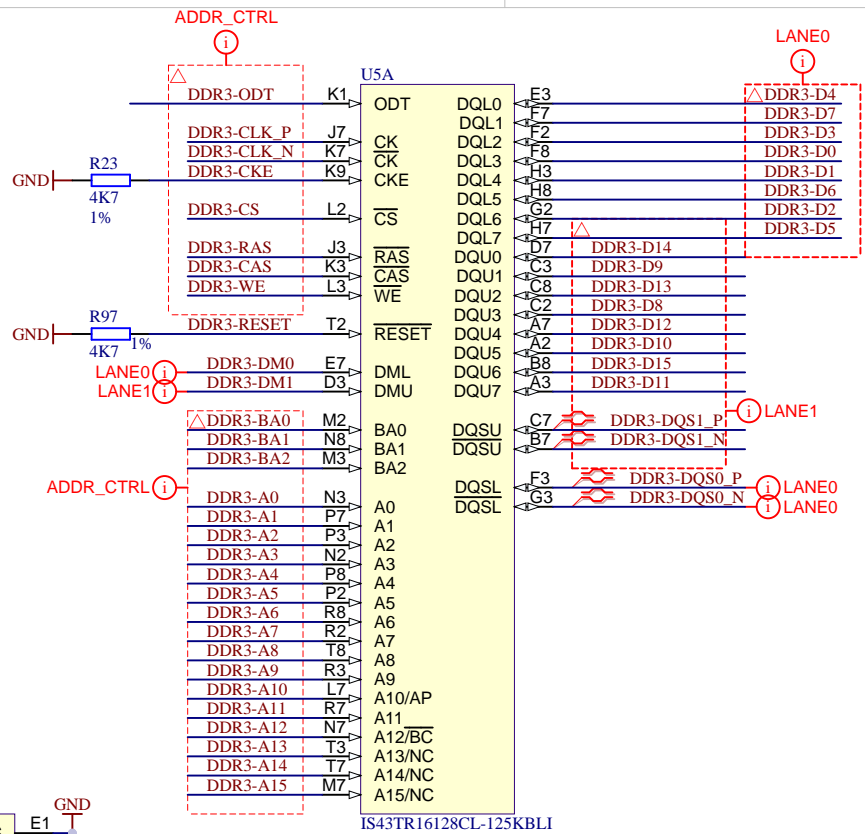
B

C

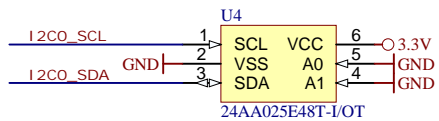
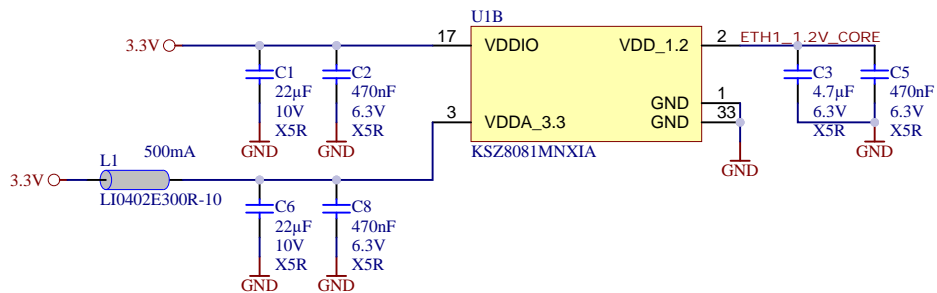
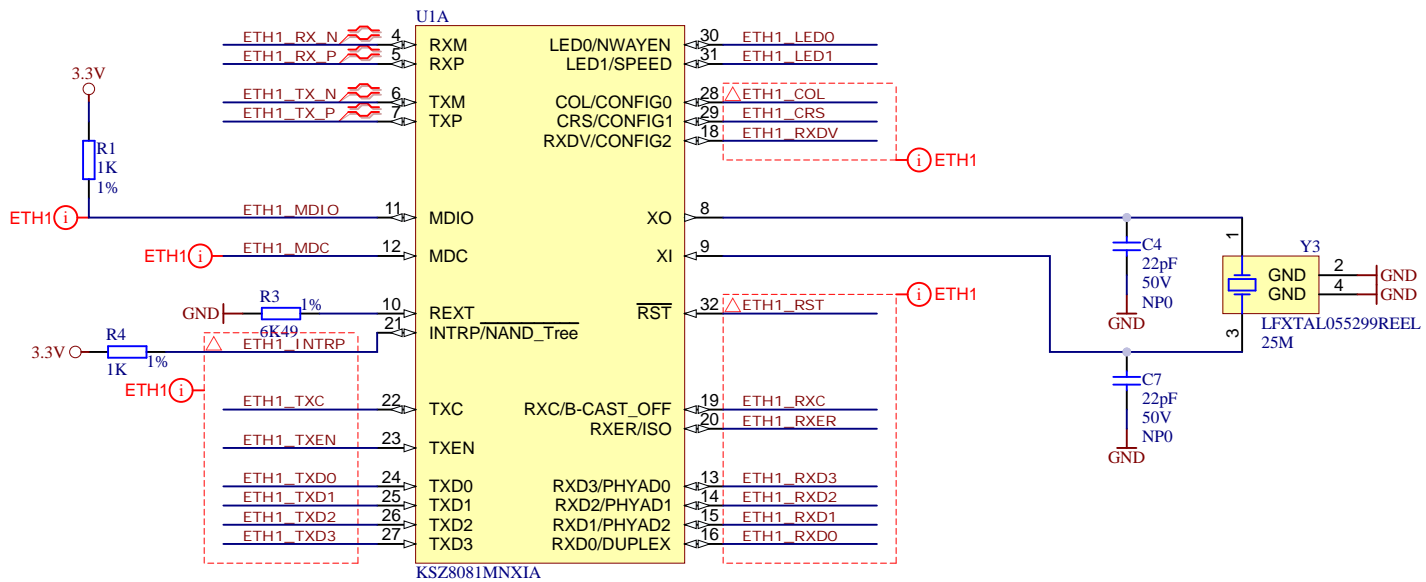
C

D

D



Title: TEM0005 - DDR Memory		
A4	Number: TEM0005 0101	Rev. 02
Date: 2020-01-22	Copyright: Trenz Electronic GmbH	Page6 of 9
Filename: DDR3-RAM.SchDoc		

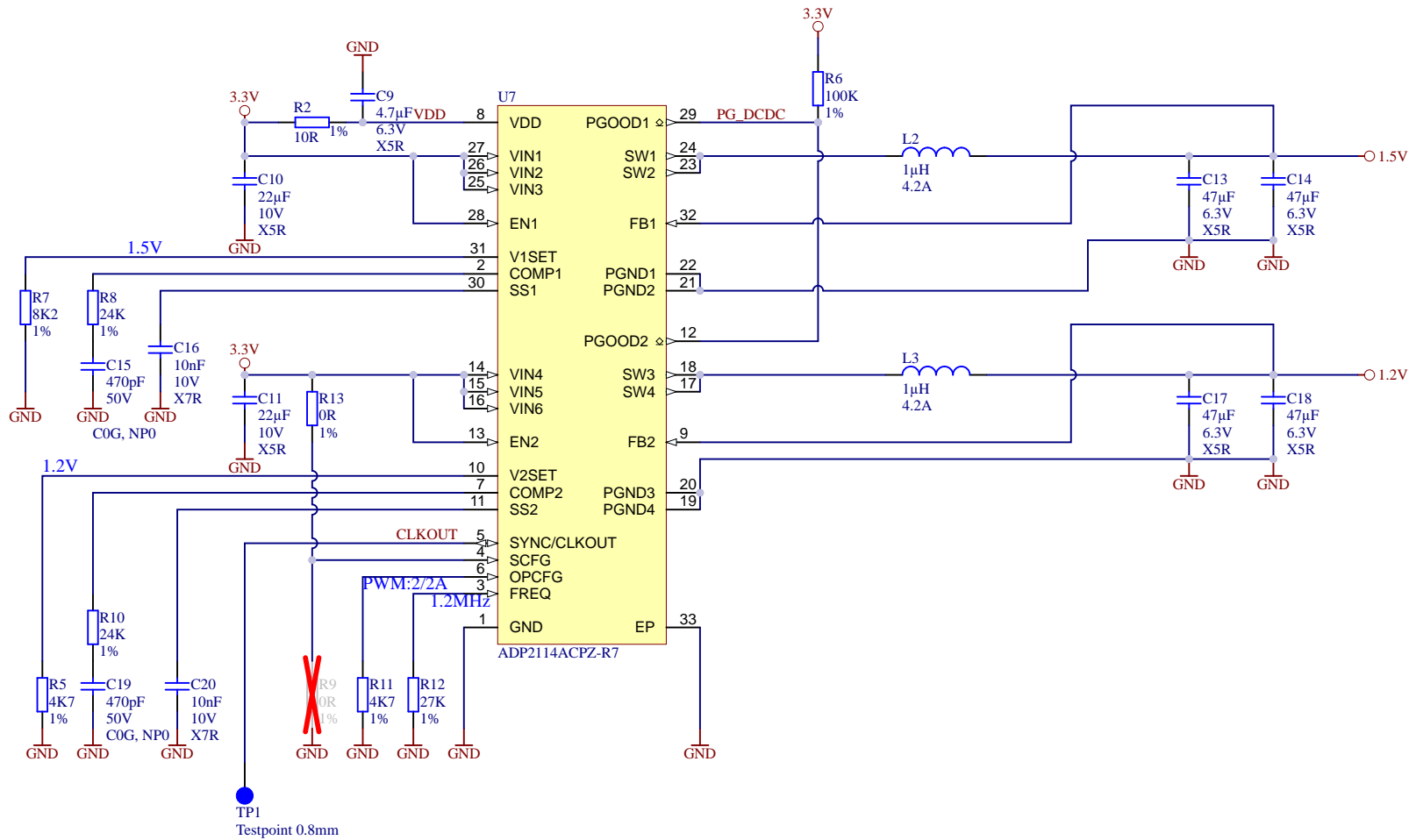



Slave address: 0b1010000



Title: TEM0005 - ETH_PHY		
A4	Number: TEM0005 010I	Rev. 02
Date: 2020-01-22	Copyright: Trenz Electronic GmbH	
Page 7		of 9
Filename: ETH.SchDoc		





			Title: TEM0005 - PowerSupply	
			A4	Number: TEM0005 010I
Date: 2020-01-22		Copyright: Trenz Electronic GmbH		Page8 of 9
Filename: PowerSupply.SchDoc				



1

2

3

4

VT: Initial Rev (07.2019)

REV02: (01.2020)

VT: 1) Support M2S060 and M2S025 -> added R29,R30, C24..C26,C31

VT: 2) Added resistor R32

VT: 3) Full upd LIB

05.12.2022:

VY: 1) Changed Crystal G83270021 to ECS-.327-12.5-34B-TR

VY: 2) Changed CryptoAuthentication™ Device ATECC608A-MAHDA-S to ATECC608B-MAHCZ-S

A

A

B


B

C

C

D

D

		Title: TEM0005 - Revision changes	
		A4	Number: TEM0005 010I
Date: 2020-01-22		Copyright: Trenz Electronic GmbH	
Filename: Revision_Changes.SchDoc		Page9 of 9	

1

2

3

4