



Regarding the usage of our schematics and alike documentation for Trenz module TE0725 .

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0725 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

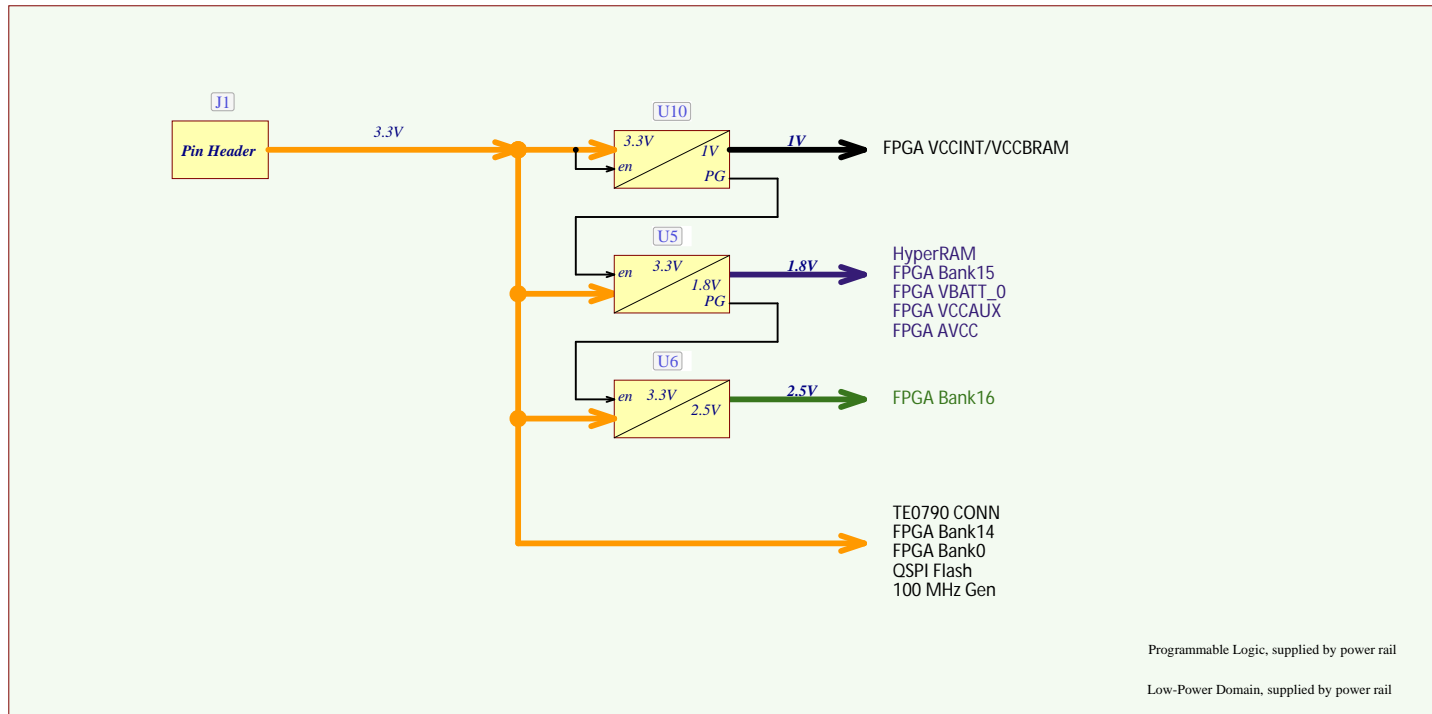
Schematics and other handouts serve for informational purposes only!

	Title: <b>Legal Notices Modules</b>		
	A4	Number: <b>TE0725 72C-1-F</b>	Rev. <b>04</b>
	Date: <b>18.04.2023</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>1</b> of <b>13</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		

REV	Description	
-01	Initial revision	
-02		
-03	<ul style="list-style-type: none"> <li>1. Fixed LVPECL termination for 125MBit modules</li> <li>2. Fixed wrong XADC decoupling capacitors</li> <li>3. Added serial number (traceability pad)</li> <li>4- Added thermal vias to mounting holes</li> </ul>	
-04	<ul style="list-style-type: none"> <li>1. DC-DC EN5311QI is replaced by MPM3834CGPA. Designator of the component is changed U11 --&gt; U5;</li> <li>2. U10 EN6347QI replaced by MPM3860GQW-Z;</li> <li>3. Removed "trace pad";</li> <li>4. U4 (S27KS0641DPBH000) is EOL and replaced with IS66WVH8M8FALL-166B1LI;</li> <li>5. Added pull-up resistor R37 to HyperRAM #CS signal;</li> <li>6. Added Diode D4;</li> <li>7. Added Diode D1 for INIT reset;</li> <li>8. Added J3 (JTAG only Enable);</li> <li>9. Added testpoints TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10;</li> <li>10. L1, L2, L3, L4, L6 Ferrit beads BKP0603HS121-T replaced with MPZ0603S121HT000;</li> <li>11. U3 replaced by SiT8008BI-73-XXS-100.000000E;</li> <li>12. Components updated from the library;;</li> <li>13. Added Legal notices and power diagram pages.</li> <li>14. Power sequence is updated according to DS181: 1V --&gt; 1,8V --&gt; 2,5V.</li> </ul>	<p>VG (18.04.2023)</p>

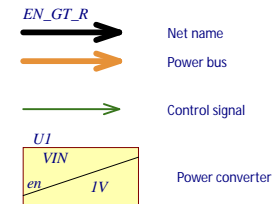
	Title: <b>Revision Changes</b>		
	A4	Number: <b>TE0725 72C-1-F</b>	Rev. <b>04</b>
	Date: <b>18.04.2023</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>2</b> of <b>13</b>
	Filename: <b>Revision_Changes.SchDoc</b>		

## Power-on sequencing:

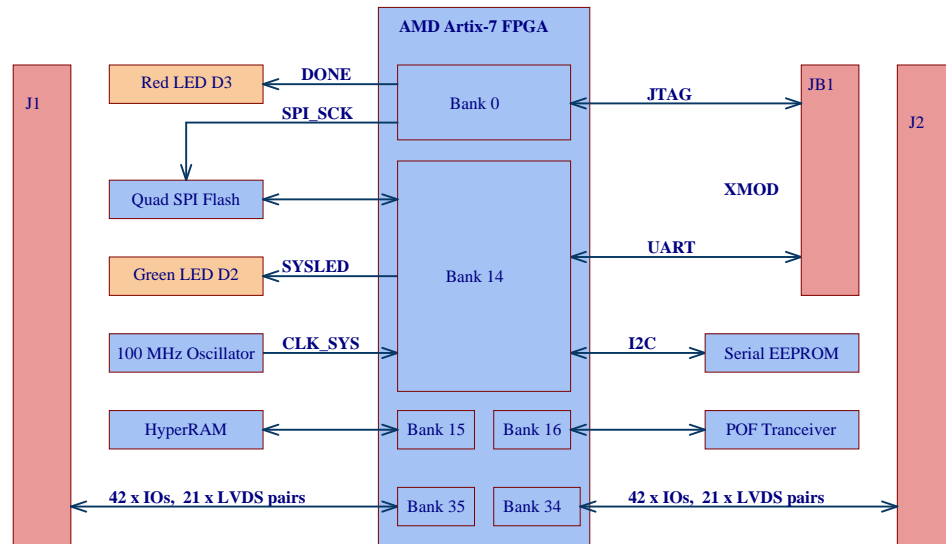


## Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3V from J1, J2	IN	3.3V	+/-3%	Micromodule Power	TE0790 CONN, FPGA Bank14, FPGA Bank0, QSPI Flash, 100 MHz Gen, Optical Transceiver



	Title: <b>Power Diagram</b>		
	A4	Number: <b>TE0725 72C-1-F</b>	Rev. <b>04</b>
	Date: <b>18.04.2023</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>3</b> of <b>13</b>
	Filename: <b>Power_Diagram.SchDoc</b>		



### I2C Address:

Device	I2C BUS	I2C ADDR	Note
EEPROM <span style="border: 1px solid black; padding: 0 2px;">U2</span>	I2C	0x50	-

U\_FPGA PWR  
FPGA\_PWR\_MISC.SchDoc

U\_PowerSupply  
POWER.SchDoc

**Legend:**  B2B Connector  LED Interface  On-board Components

LOGO1

TE Logo PRINT Layer

LOGO PRINT  
CE

CE Logo on Top Overlay

CE-TOPOVERLAY

MECH1

TE Address Overlay

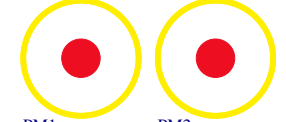
LOGO ADDRESS

Serial

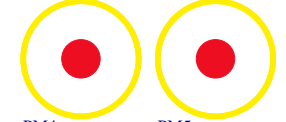
Serial

Serialnumber 6,3 x 6.3mm

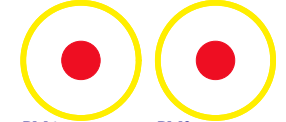
FIDU-DOT - mini FIDU-DOT - mini



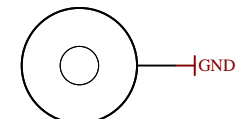
PM1 FIDU-DOT - mini PM2 FIDU-DOT - mini



PM4 FIDU-DOT - mini PM5 FIDU-DOT - mini



PM6 PM3

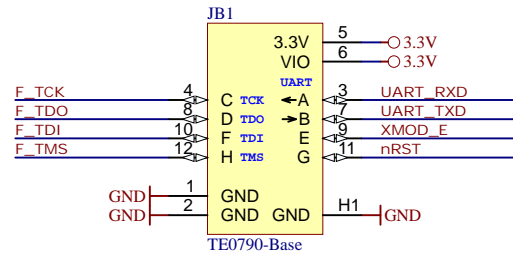


Mount.Hole 3.2mm

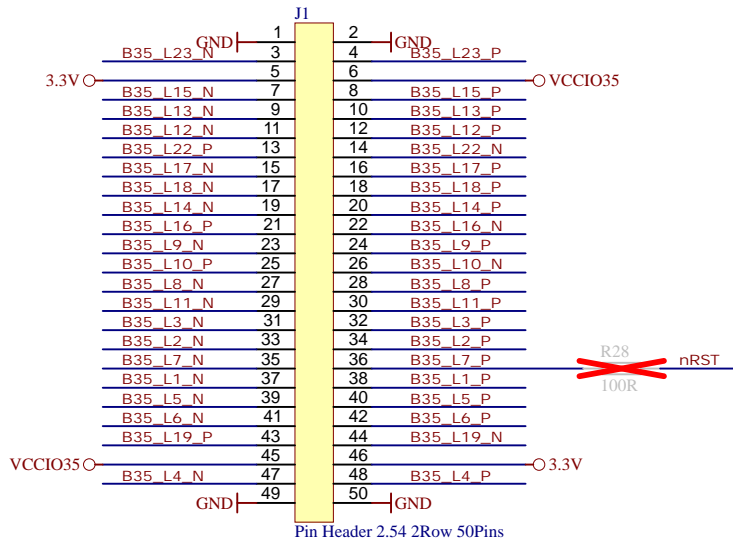
Drawn by	VG
Checked by	IG
Assembly variant	72C-1-F
Created by	AL
Modified by	VG
Modified at	18.04.2023



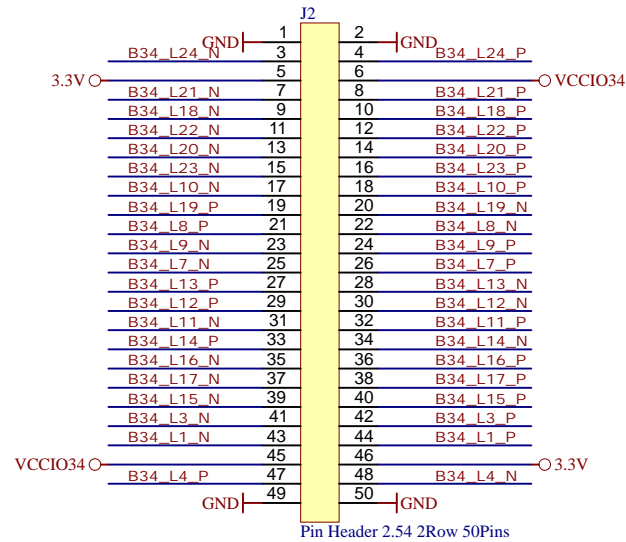
Title: Overview		
A4	Number: TE0725 72C-1-F	Rev. 04
Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT	Page4 of 13
Filename: TE0725.SchDoc		



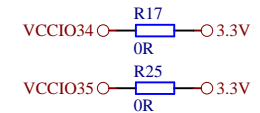
TE0790-Base



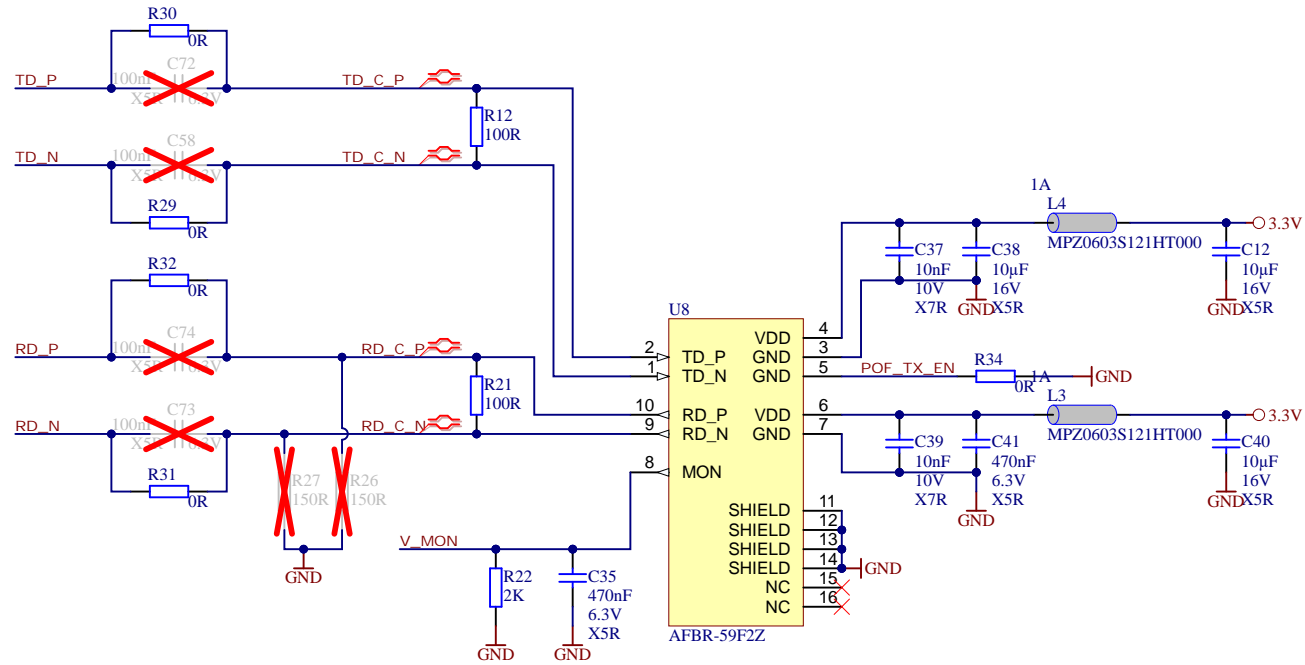
Pin Header 2.54 2Row 50Pins




Pin Header 2.54 2Row 50Pins



Title: <b>B2B Connectors</b>		
A4	Number: <b>TE0725 72C-1-F</b>	Rev. <b>04</b>
Date: <b>18.04.2023</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>5</b> of <b>13</b>
Filename: <b>B2B_Connector.SchDoc</b>		



	Title: Optical transceiver		
	A4	Number: TE0725 72C-1-F	Rev. 04
	Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT	Page 6 of 13
	Filename: Optical_transceiver.SchDoc		

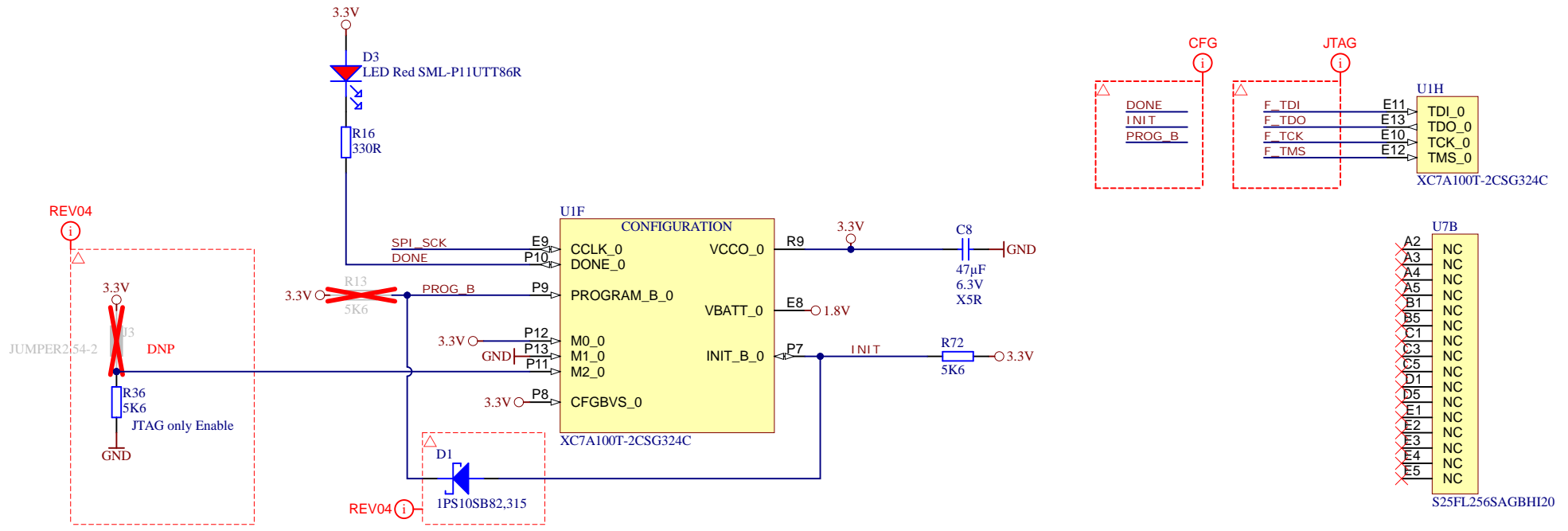
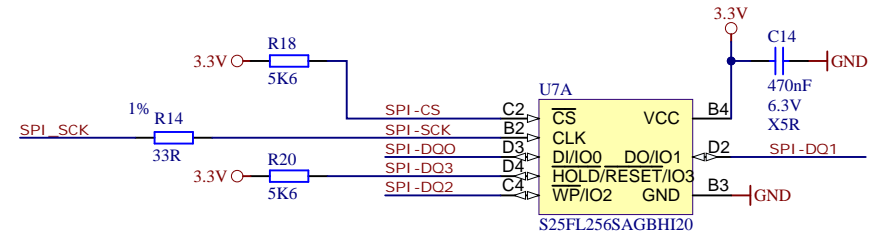
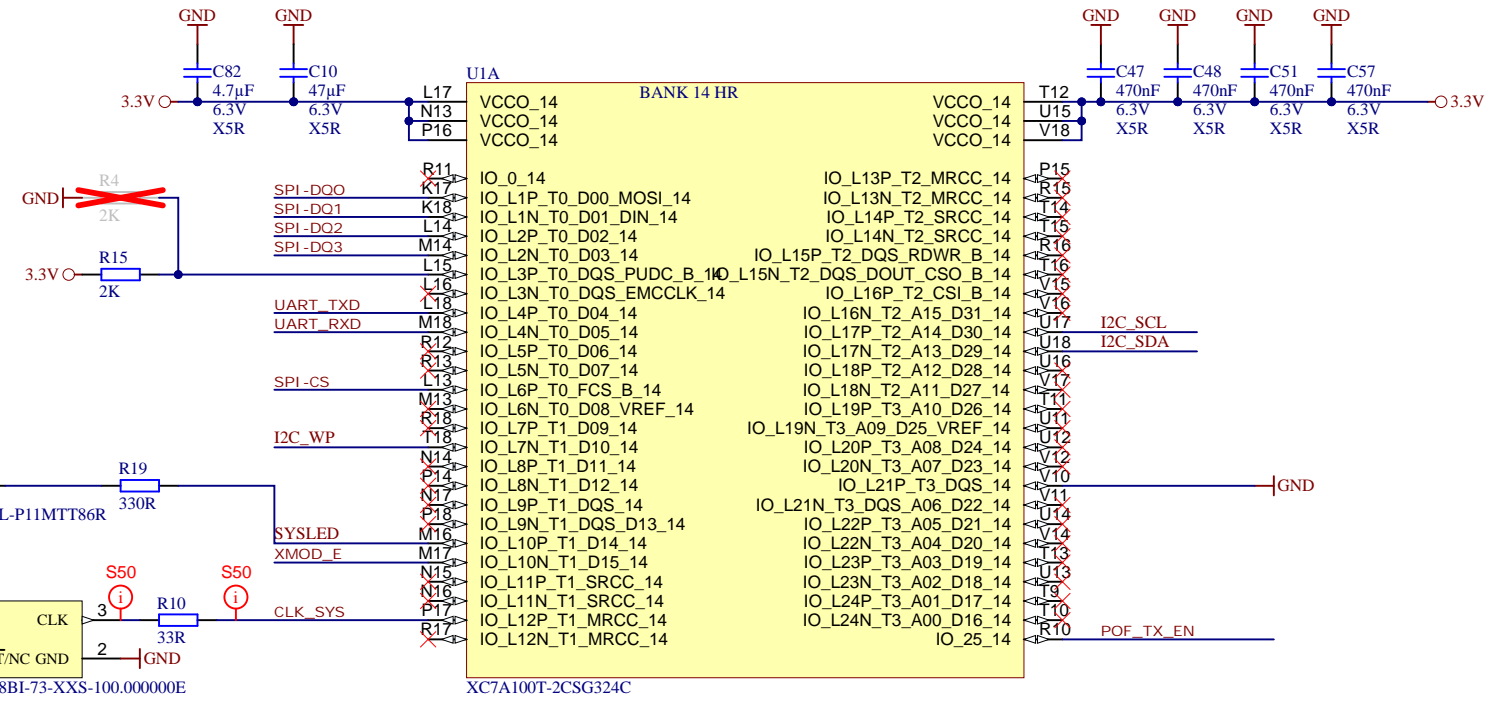
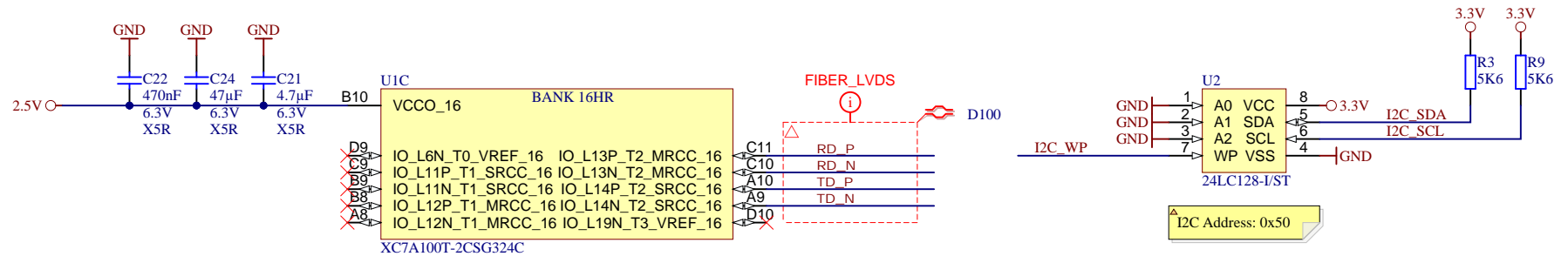



Table 2-1: 7 Series FPGA Configuration Modes (UG470)

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32 <sup>(1)</sup>	Input
Slave Serial <sup>(2)</sup>	111	x1	Input

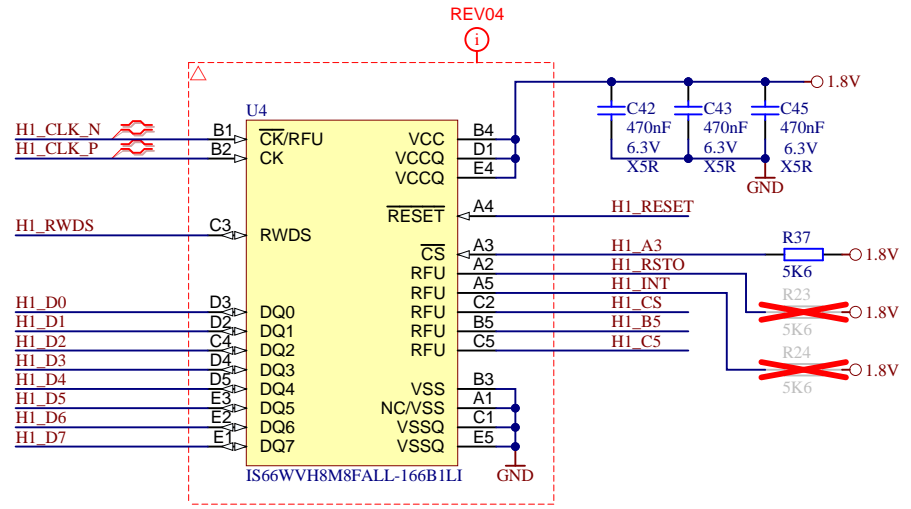
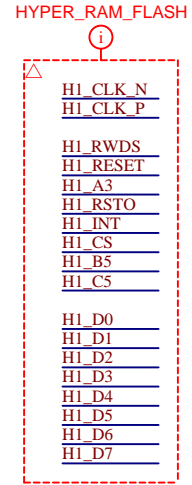
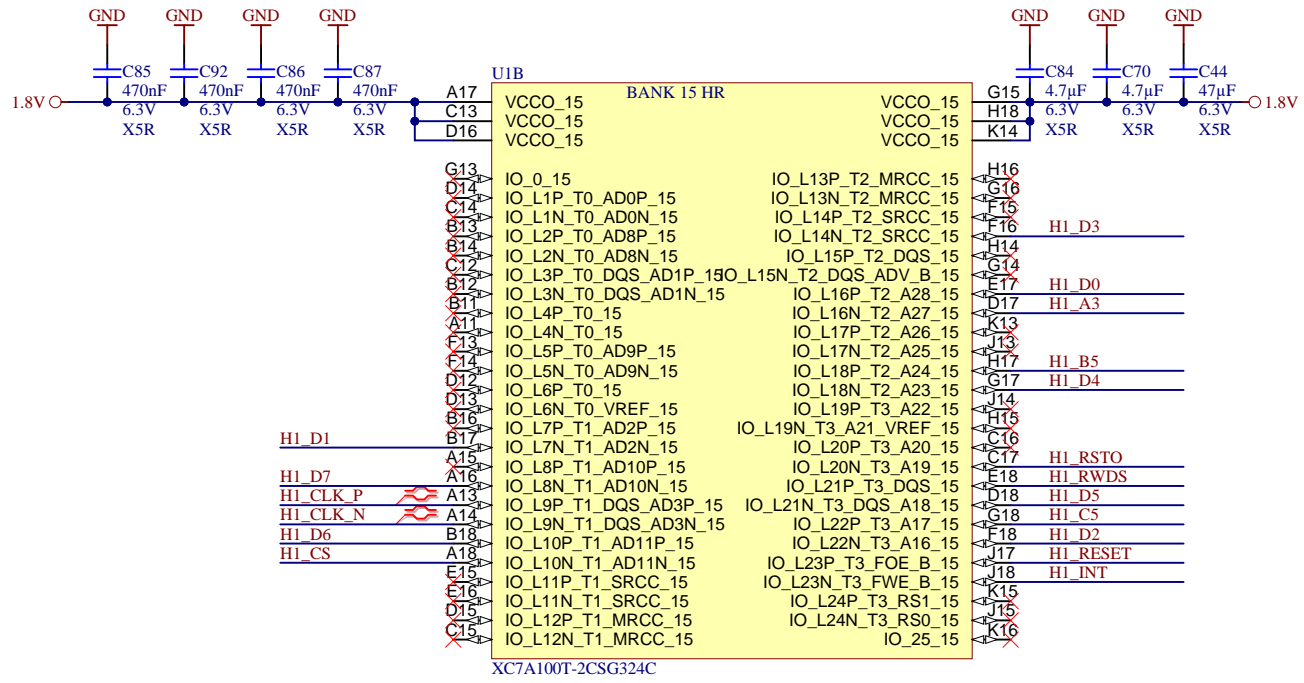


Title: <b>FPGA CFG</b>		
A4	Number: <b>TE0725 72C-1-F</b>	Rev. <b>04</b>
Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT	Page 7 of 13
Filename: <b>FPGA_CFG.SchDoc</b>		

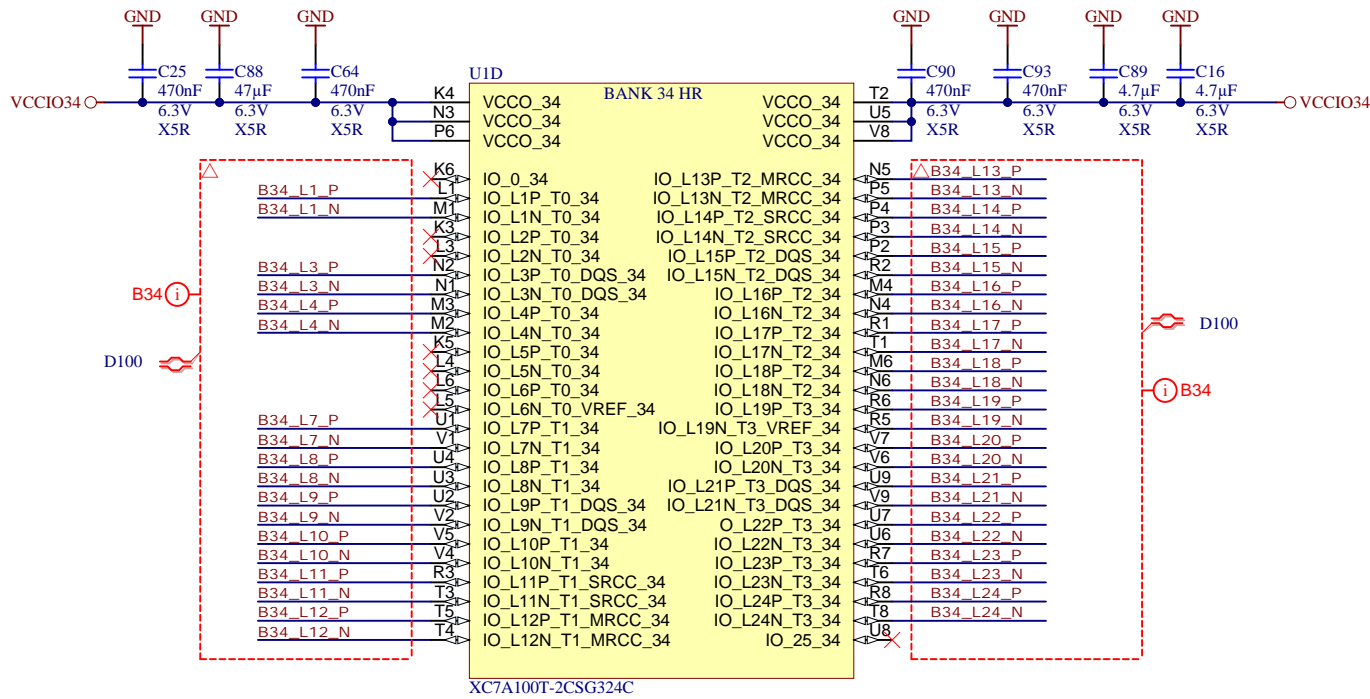




Title: <b>B14 &amp; B16</b>		
A4	Number: <b>TE0725 72C-1-F</b>	Rev. <b>04</b>
Date: <b>18.04.2023</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>8</b> of <b>13</b>
Filename: <b>B14_B16.SchDoc</b>		

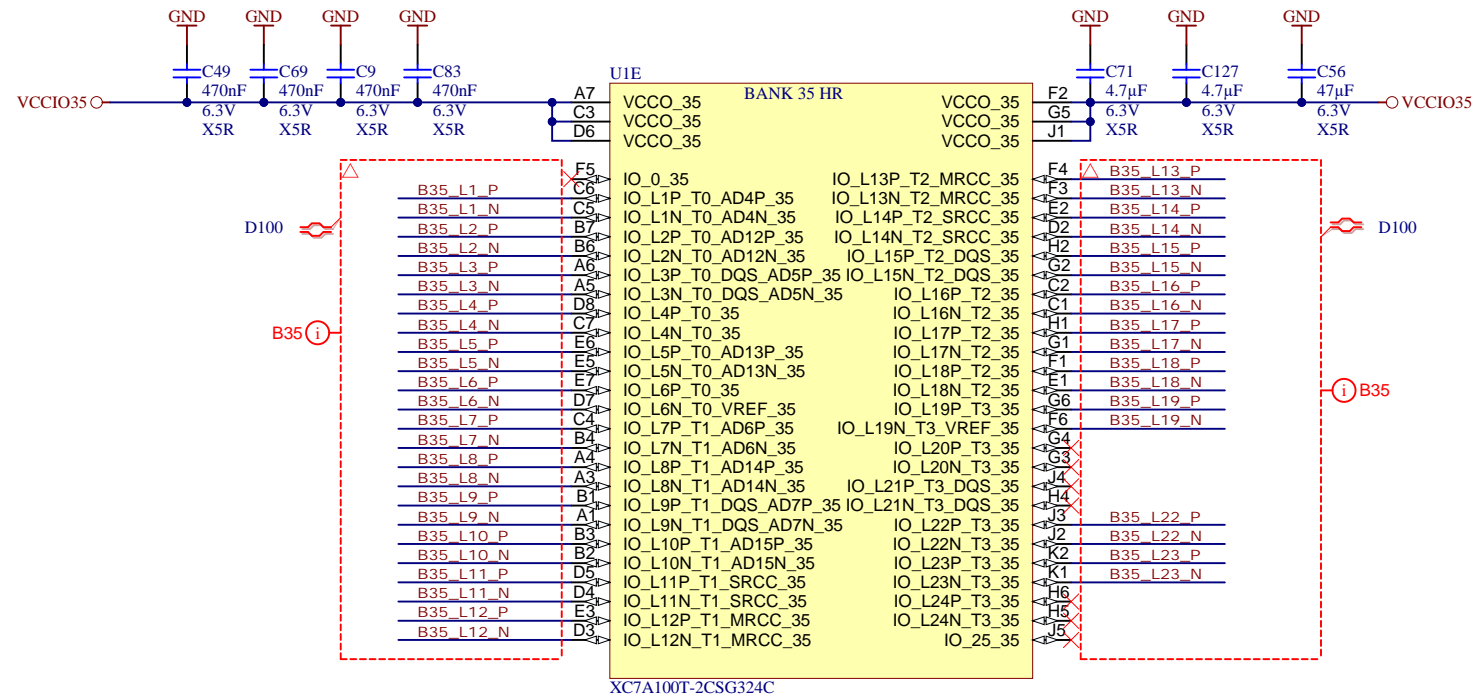




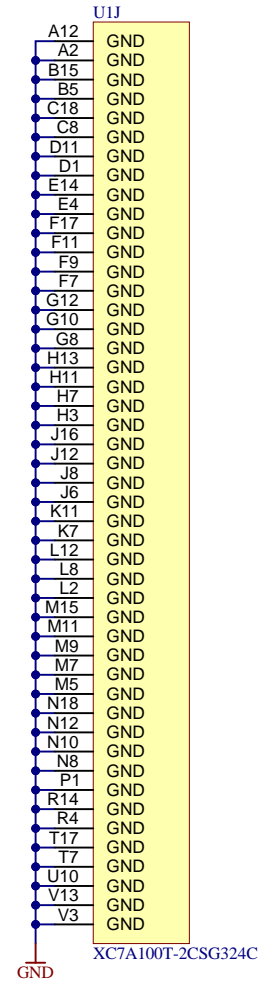
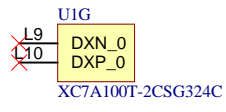
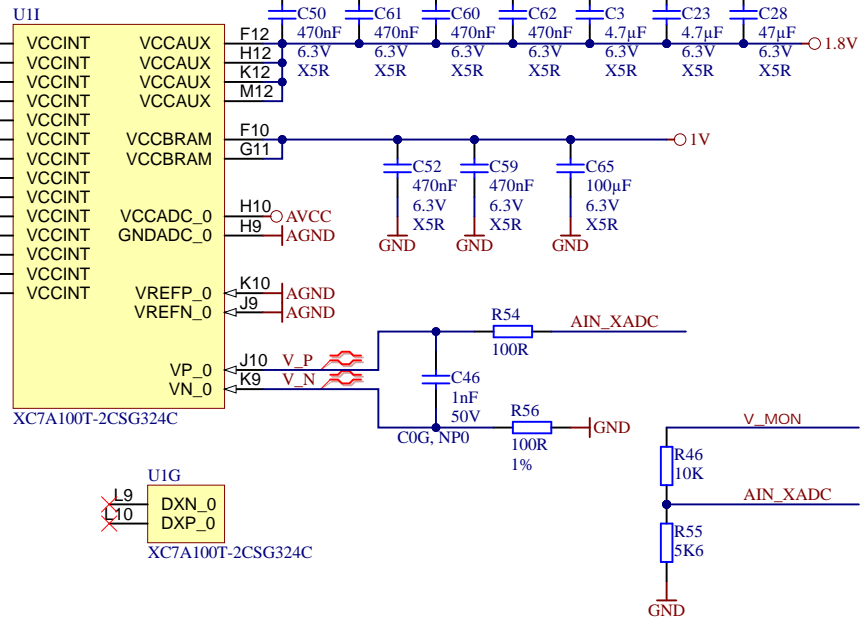
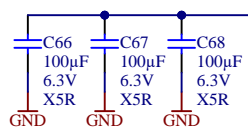
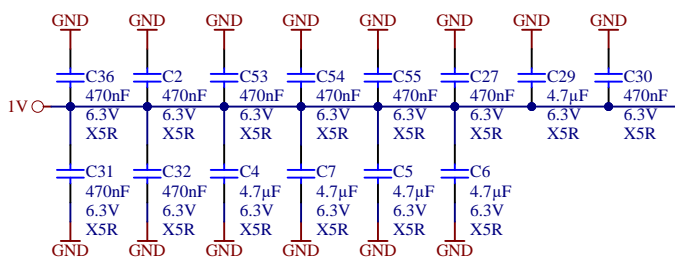
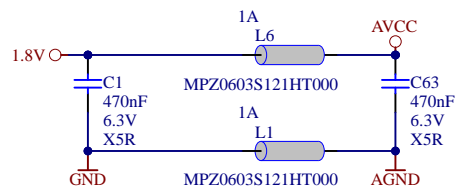
Title: <b>B15</b>		
A4	Number: <b>TE0725 72C-1-F</b>	Rev. <b>04</b>
Date: <b>18.04.2023</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>9</b> of <b>13</b>
Filename: <b>B15.SchDoc</b>		



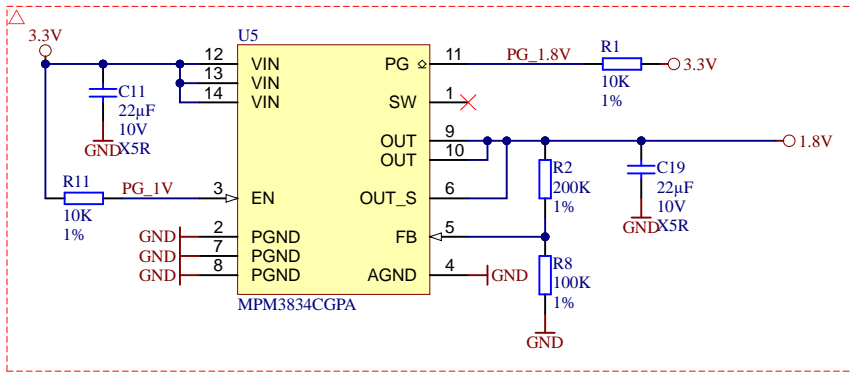
	Title: <b>B34</b>		
	A4	Number: <b>TE0725 72C-1-F</b>	Rev. <b>04</b>
	Date: <b>18.04.2023</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>10</b> of <b>13</b>
	Filename: <b>B34.SchDoc</b>		



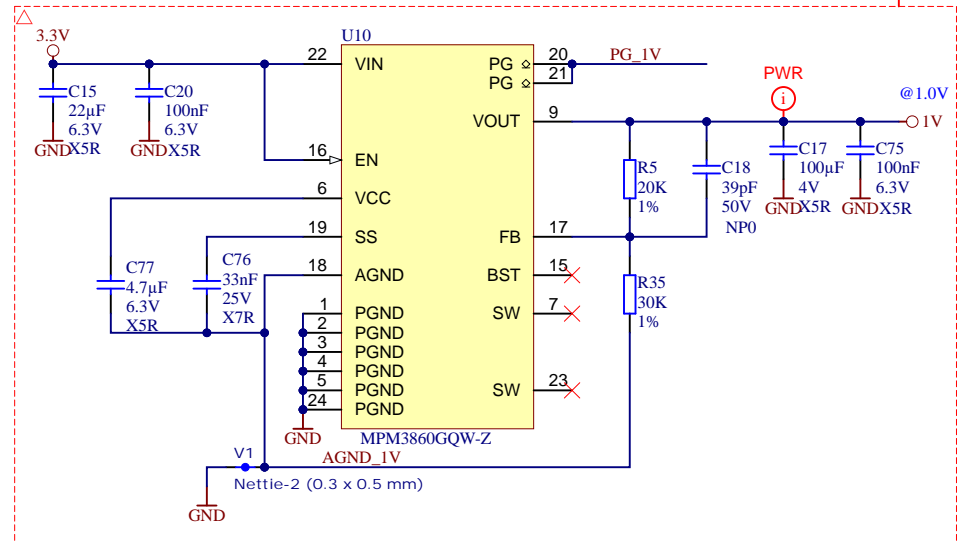
	Title: <b>B35</b>		
	A4	Number: <b>TE0725 72C-1-F</b>	Rev. <b>04</b>
	Date: <b>18.04.2023</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>11</b> of <b>13</b>
	Filename: <b>B35.SchDoc</b>		



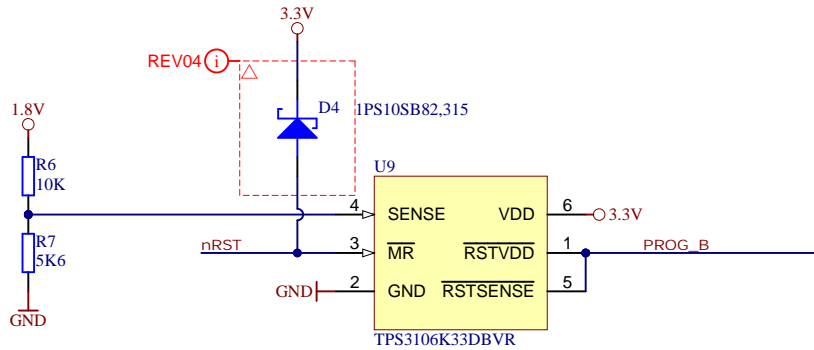
Title: FPGA PWR MISC		
A4	Number: TE0725 72C-1-F	Rev. 04
Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT	Page 12 of 13
Filename: FPGA_PWR_MISC.SchDoc		



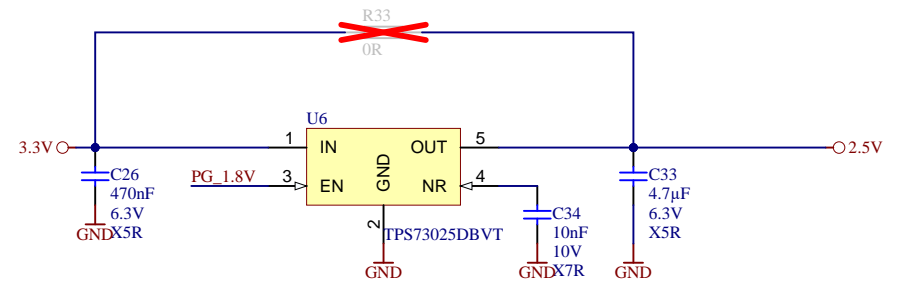
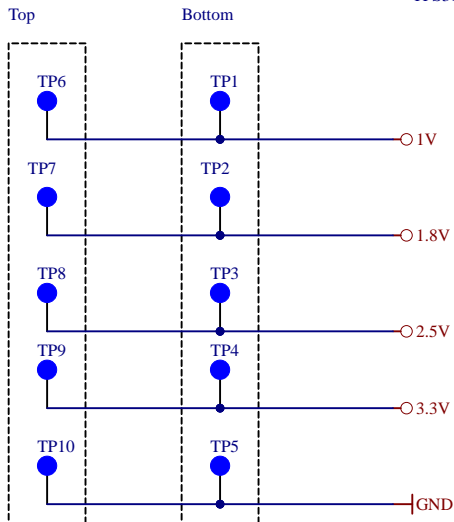
REV04



REV04



REV04



Title: POWER		
A4	Number: TE0725 72C-1-F	Rev. 04
Date: 18.04.2023	Copyright: Trenz Electronic GmbH	Page13 of 13
Filename: POWER.SchDoc		