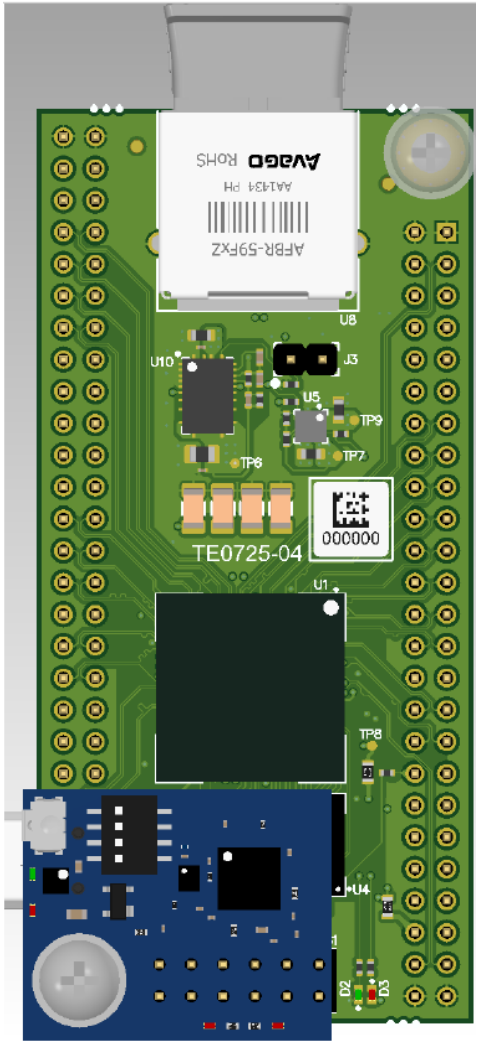
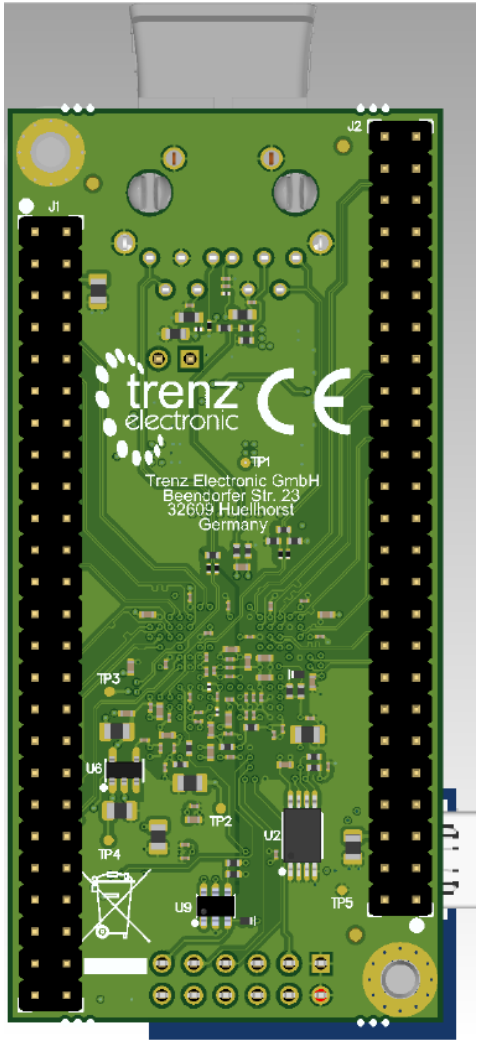




Regarding the usage of our schematics and alike documentation for Trenz module TE0725 .

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0725 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

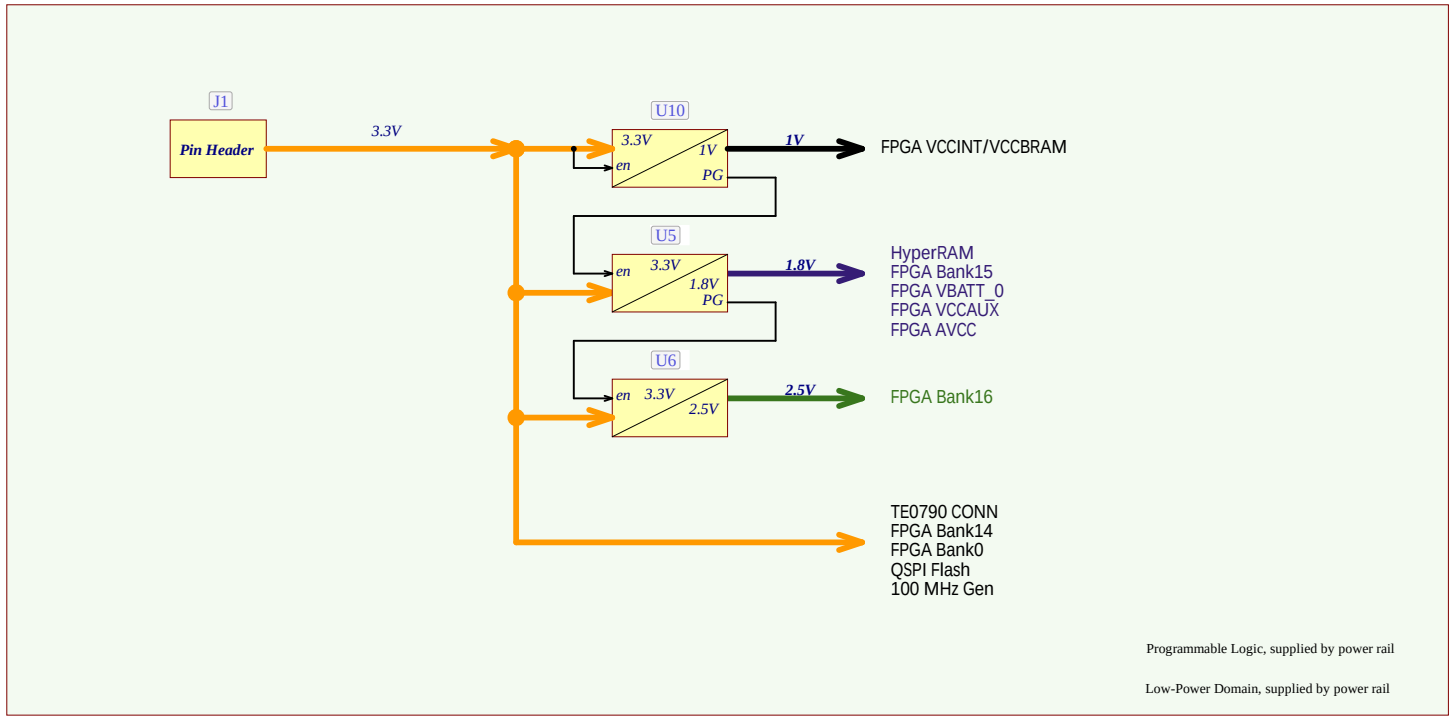
trenz electronic	Title: Legal Notices Modules		
	A4	Number: TE0725 72I-1-B	Rev. 04
	Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT	Page 1 of 13
	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02		
-03	1. Fixed LVPECL termination for 125MBit modules 2. Fixed wrong XADC decoupling capacitors 3. Added serial number (tracebility pad) 4- Added thermal vias to mounting holes	
-04	1. DC-DC EN5311QI is replaced by MPM3834CGPA. Designator of the component is changed U11 --> U5; 2. U10 EN6347QI replaced by MPM3860GQW-Z; 3. Removed "trace pad"; 4. U4 (S27KS0641DPBHI000) is EOL and replaced with IS66WVH8M8FALL-166B1LI; 5. Added pull-up resistor R37 to HyperRAM #CS signal; 6. Added Diode D4; 7. Added Diode D1 for INIT reset; 8. Added J3 (JTAG only Enable); 9. Added testpoints TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10; 10. L1 , L2 , L3 , L4 , L6 Ferrit beads BKP0603HS121-T replaced with MPZ0603S121HT000; 11. U3 replaced by SiT8008BI-73-XXS-100.000000E; 12. Components updated from the library;; 13. Added Legal notices and power diagram pages. 14. Power sequence is updated according to DS181: 1V --> 1,8V --> 2,5V.	VG (18.04.2023)

trenz electronic

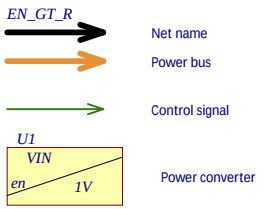
Title: Revision Changes		
A4	Number: TE0725 72I-1-B	Rev. 04
Date: 18.04.2023	Copyright: Trenz Electronic GmbH	Page2 of 13
Filename: Revision_Changes.SchDoc		

Power-on sequencing:

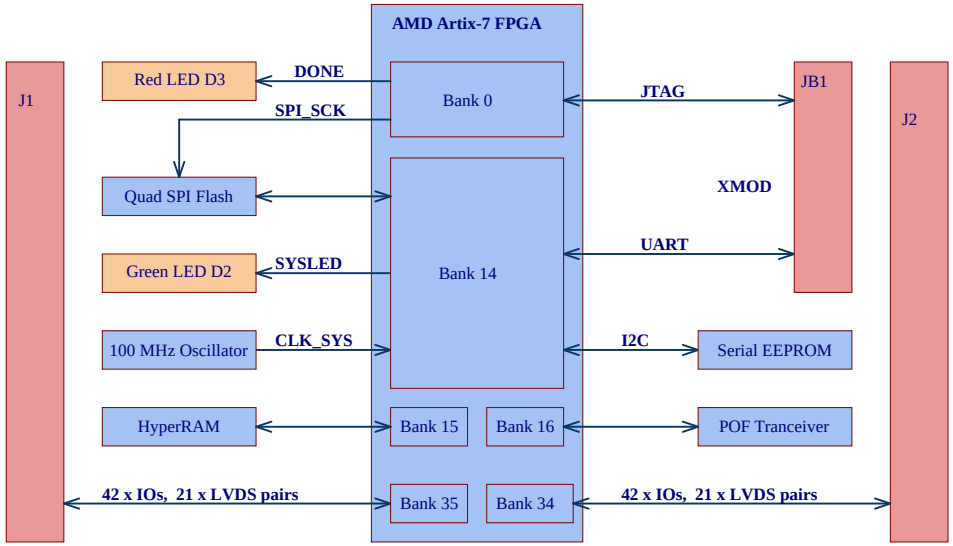


Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3V from J1, J2	IN	3.3V	+/-3%	Micromodule Power	TE0790 CONN, FPGA Bank14, FPGA Bank0, QSPI Flash, 100 MHz Gen, Optical Transceiver



trenz electronic	Title: Power Diagram		
A4	Number: TE0725 72I-1-B		Rev. 04
Date: 18.04.2023	Copyright: Trenz Electronic GmbH		Page3 of 13
Filename: Power_Diagram.SchDoc			



LOGO1

TE Logo PRINT Layer

LOGO PRINT

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

MECH1

TE Address Overlay

LOGO ADDRESS

Serial

Serial

Serialnumber 6,3 x 6.3mm

FIDU-DOT - mini FIDU-DOT - mini

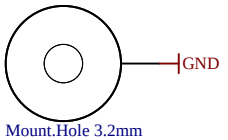
PM1 PM2

FIDU-DOT - mini FIDU-DOT - mini

PM4 PM5

FIDU-DOT - mini FIDU-DOT - mini

PM6 PM3



Mount.Hole 3.2mm

I2C Address:

Device	I2C BUS	I2C ADDR	Note
EEPROM U2	I2C	0x50	-

U_FPGA PWR

FPGA_PWR_MISC.SchDoc

U_PowerSupply

POWER.SchDoc

Legend: B2B Connector LED Interface On-board Components

Drawn by	VG
Checked by	IG
Assembly variant	72I-1-B
Created by	AL
Modified by	VG
Modified at	18.04.2023

trenz electronic

Title: Overview

A4	Number: TE0725 72I-1-B	Rev. 04
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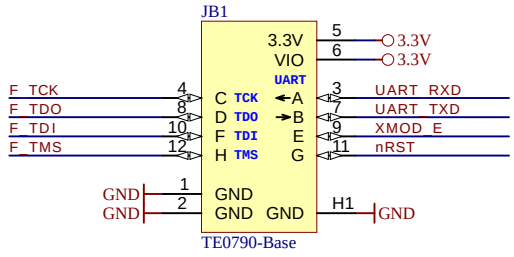
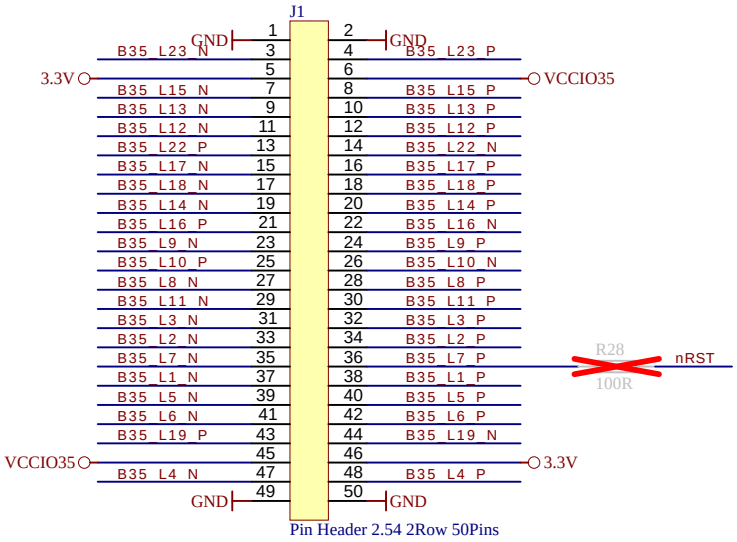
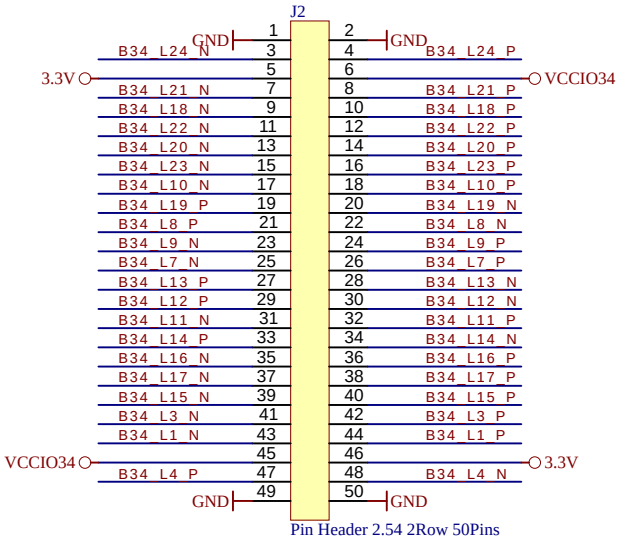
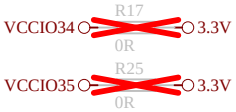
Filename: TE0725.SchDoc		









trenz electronic	Title: B2B Connectors		
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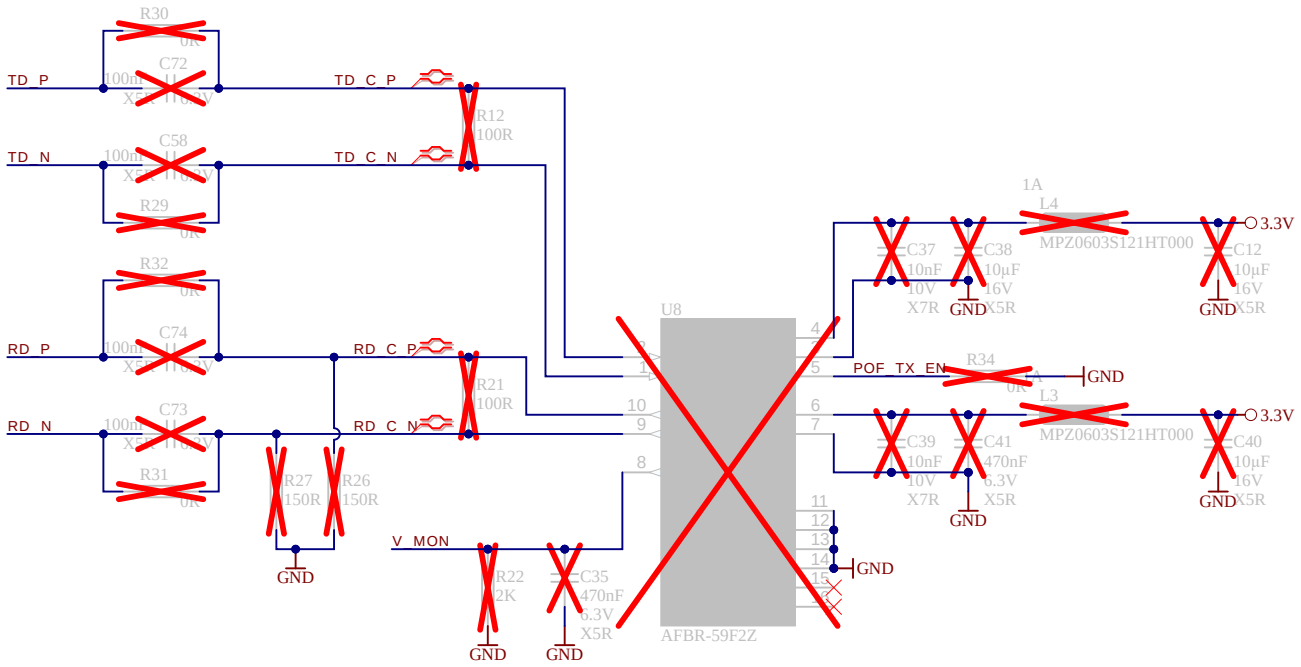
	Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT	Page5 of 13
	Filename: B2B_Connector.SchDoc		



trenz electronic	Title: Optical transceiver		
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	Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT	Page6 of 13
	Filename: Optical_transceiver.SchDoc		

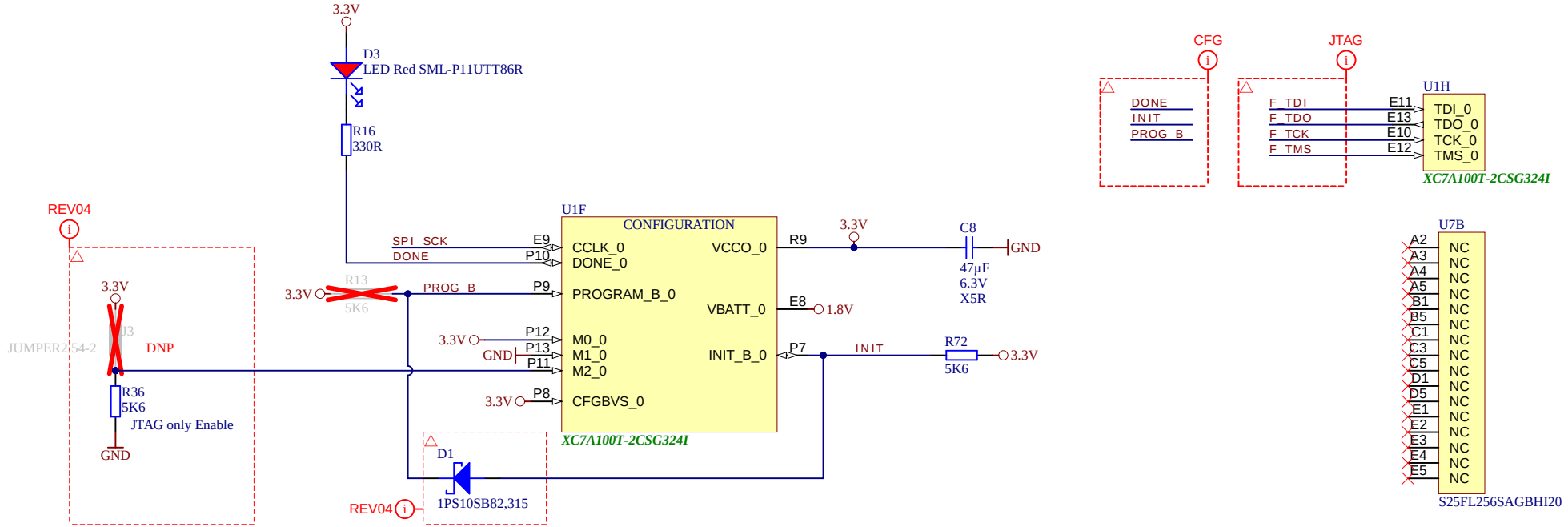
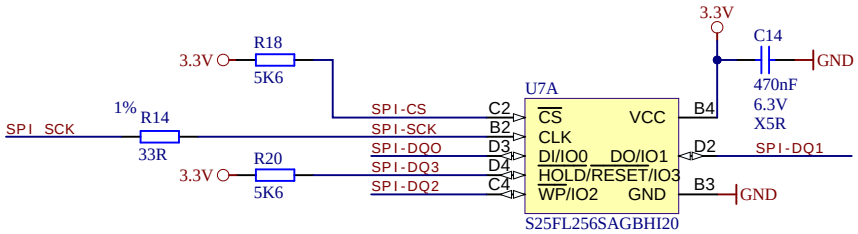


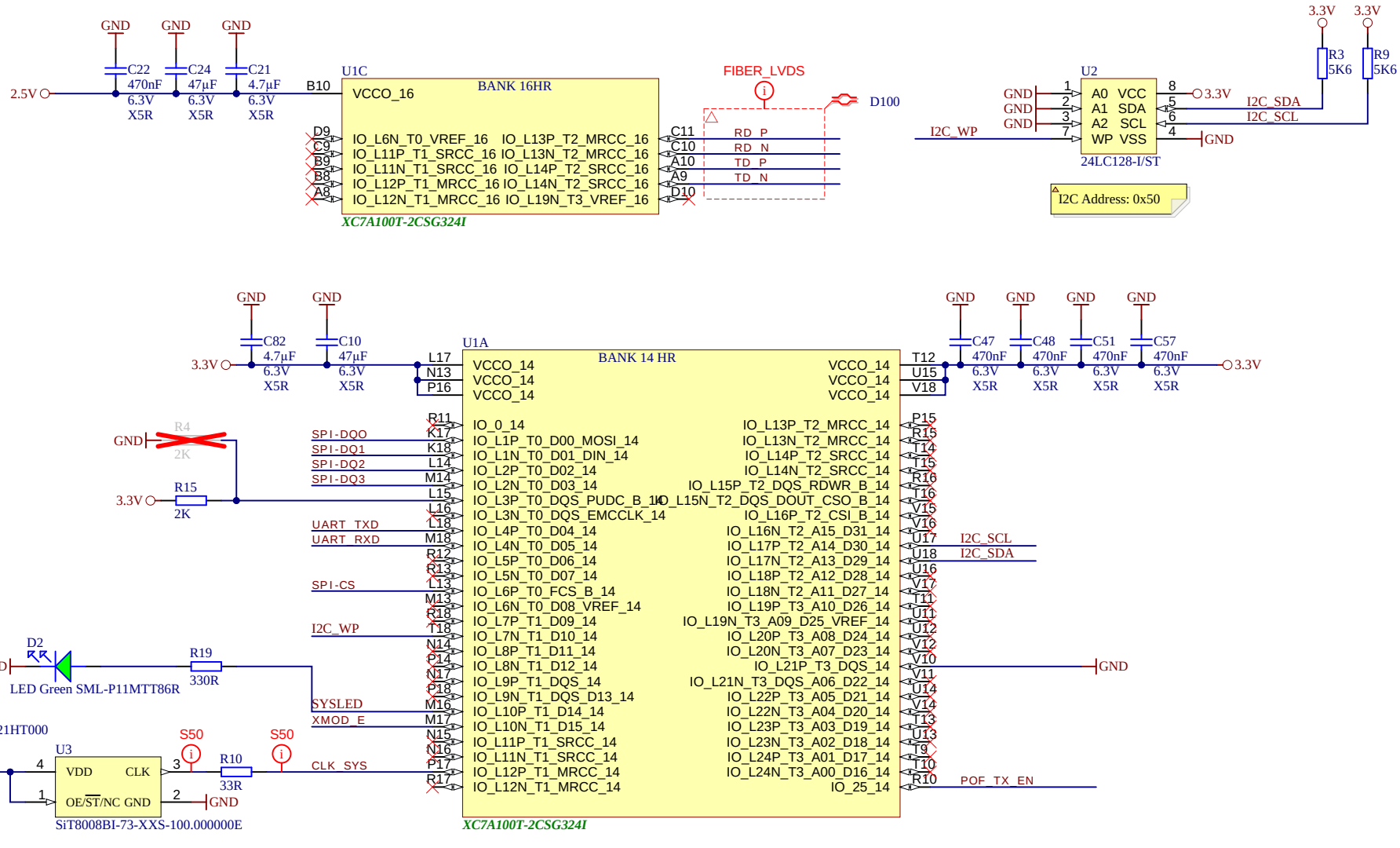
Table 2-1: **7 Series FPGA Configuration Modes (UG470)**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32(1)	Input
Slave Serial(2)	111	x1	Input

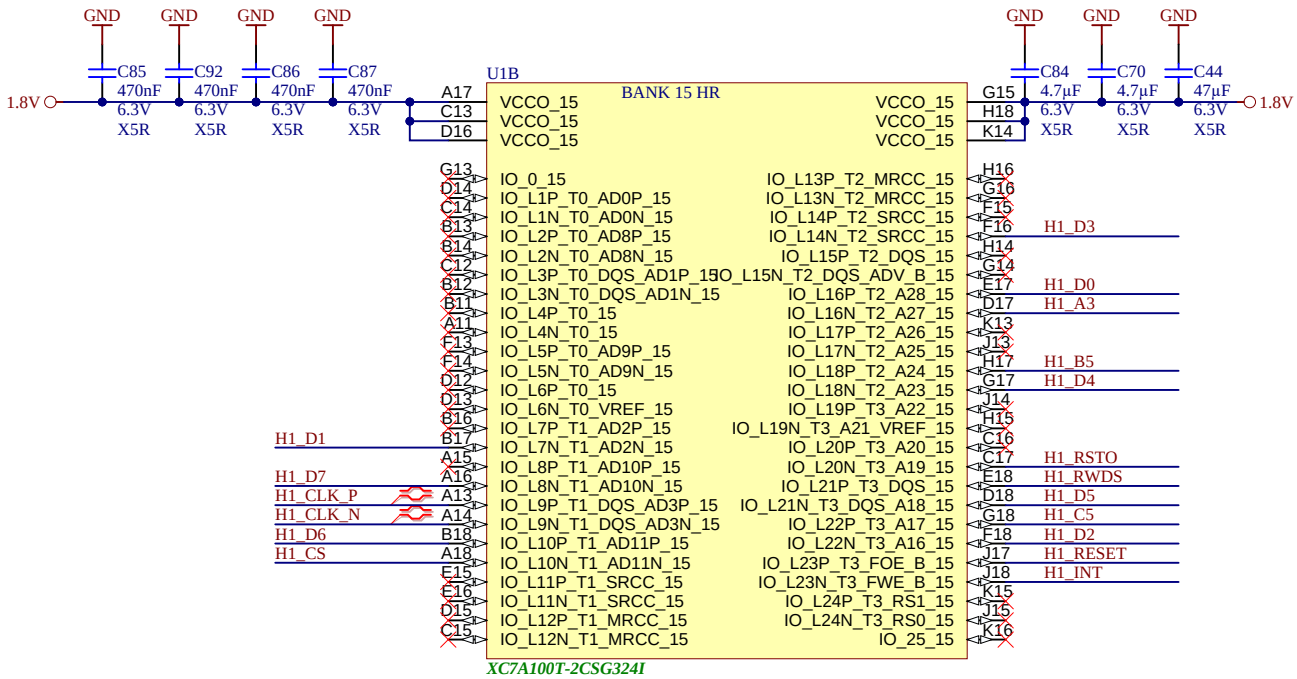


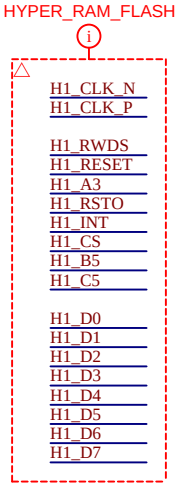
trenz electronic

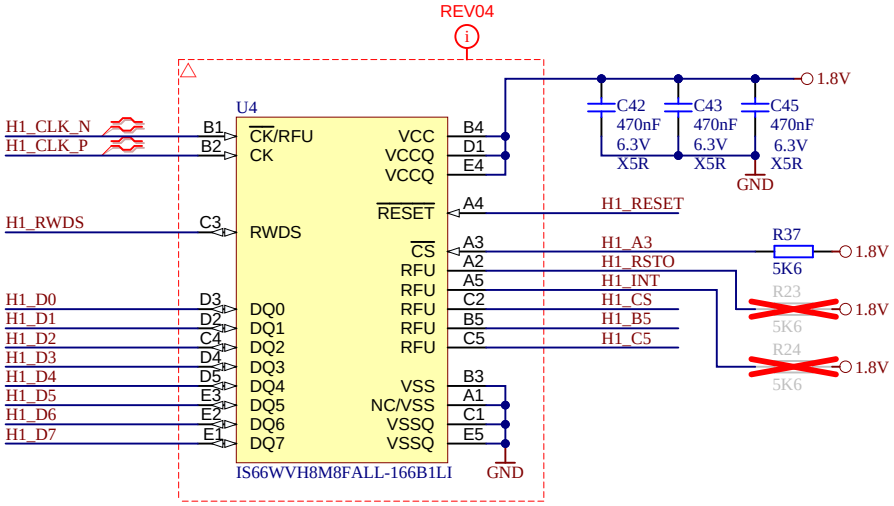
Title: FPGA CFG			
A4	Number: TE0725 72I-1-B		Rev. 04
Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT		Page7 of 13
Filename: FPGA_CFG.SchDoc			



trenz electronic	Title: B14 & B16		
	A4	Number: TE0725 72I-1-B	Rev. 04
	Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT	Page8 of 13
	Filename: B14_B16.SchDoc		







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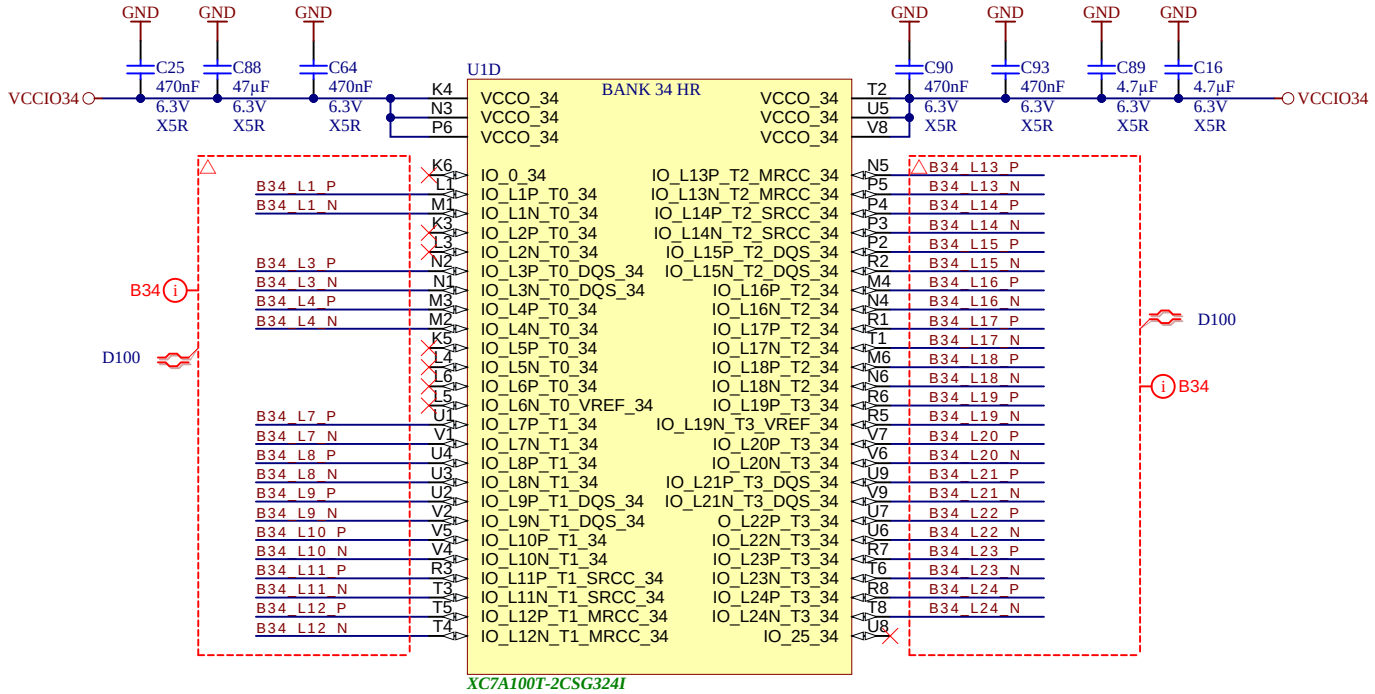
Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT		Page9 of 13
Filename: B15.SchDoc			



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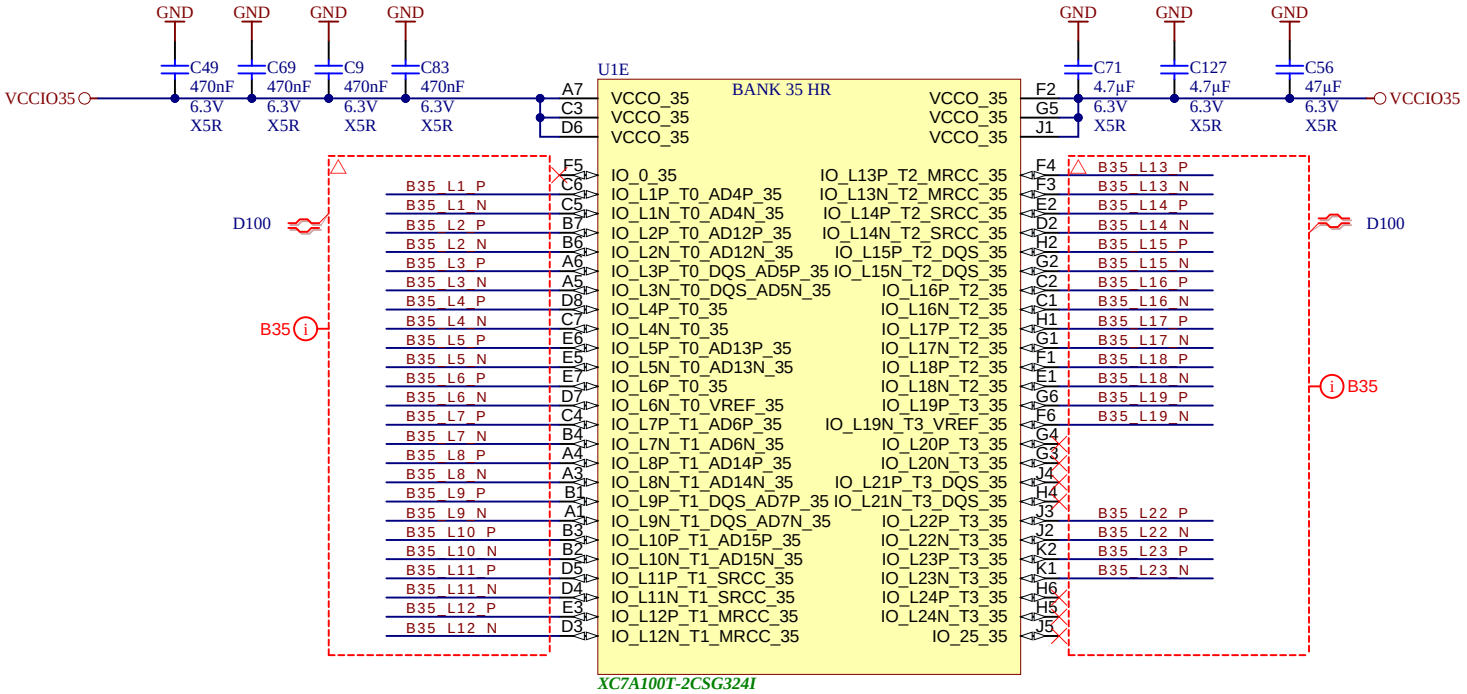
	Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT	Page10 of 13
	Filename: B34.SchDoc		



trenz electronic	Title: B35		
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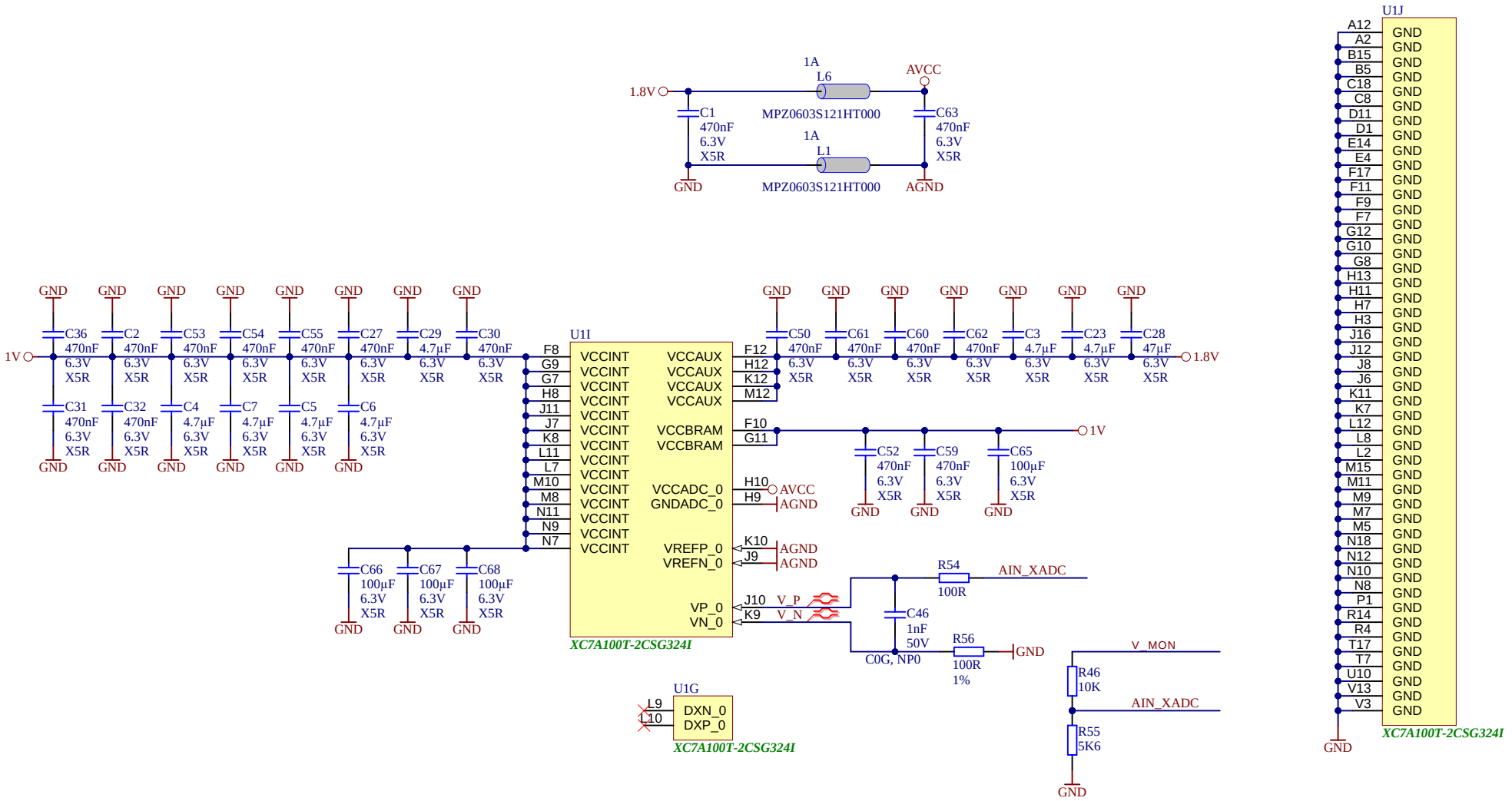
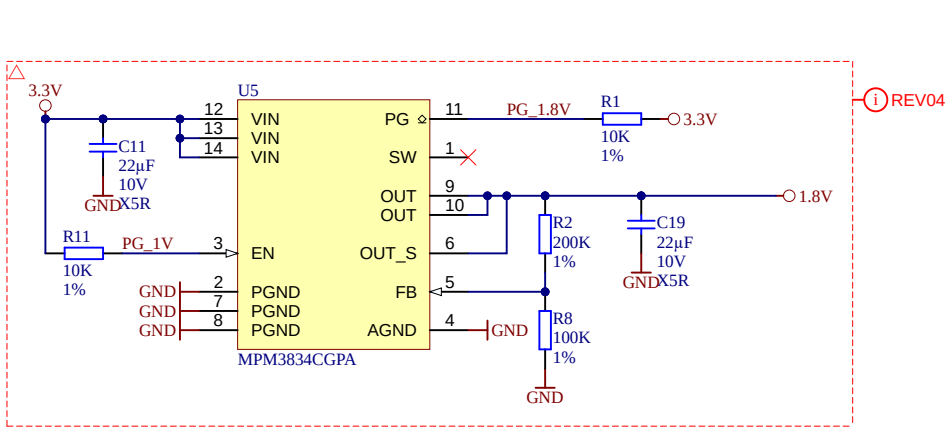
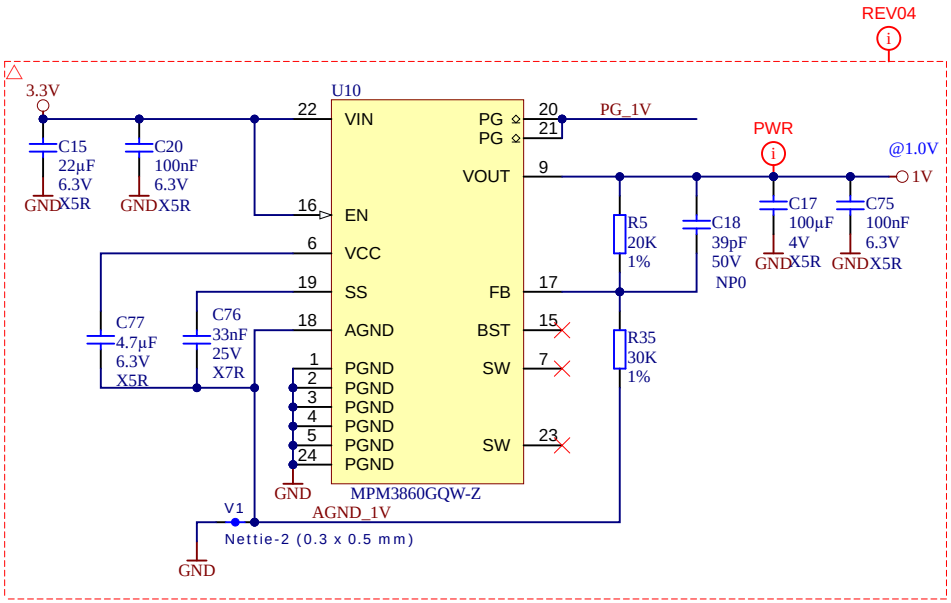
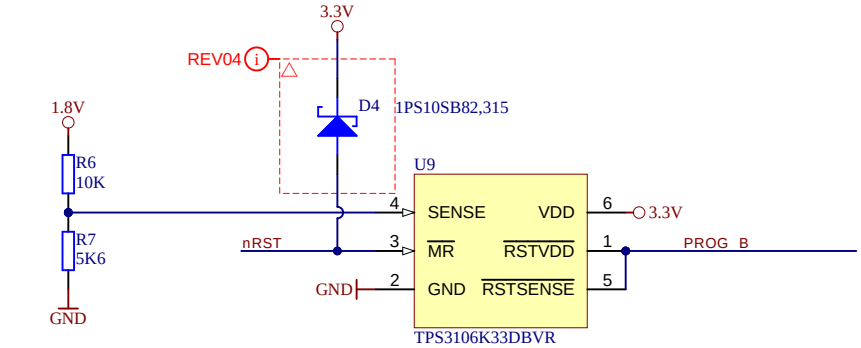
	Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT	Page11 of 13
	Filename: B35.SchDoc		

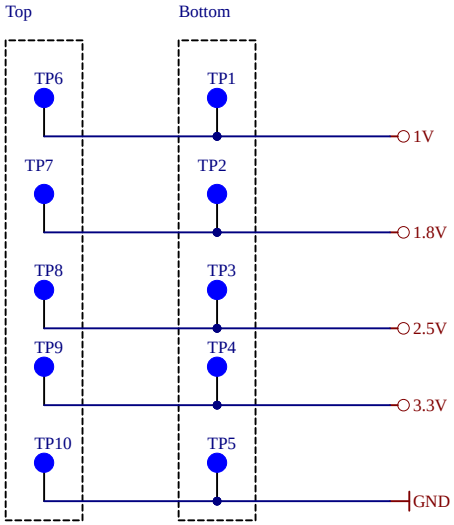


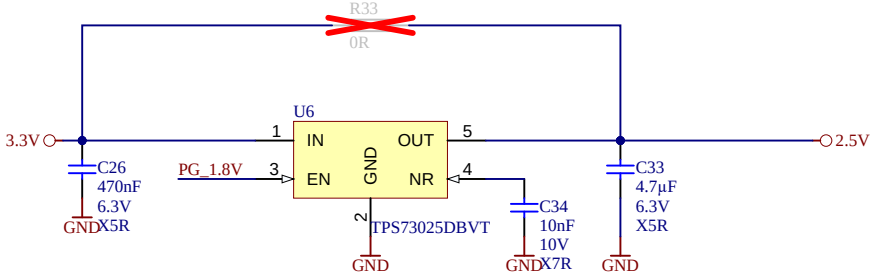
Title: FPGA PWR MISC			
A4	Number: TE0725 72I-1-B		Rev. 04
Date: 18.04.2023	Copyright: Trenz Electronic GmbH / TT		Page12 of 13
Filename: FPGA_PWR_MISC.SchDoc			











trenz electronic	Title: POWER		
	A4	Number: TE0725 72I-1-B	Rev. 04
	Date: 18.04.2023	Copyright: Trenz Electronic GmbH	Page13 of 13
	Filename: POWER.SchDoc		