TE0725 Test Board

Revision v.13

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Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0725+Test+Board

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4 Overview

MicroBlaze Design with Hello TE0725 example in endless loop.

Refer to http://trenz.org/te0725-info for the current online version of this manual and other available documentation.

4.1 Key Features

- Vivado/Vitis 2019.2
- MicroBlaze
- QSPI
- I2C
- UART

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-04-20	2019.2	TE0725-test_board_noprebuilt-vivado_2019.2-build_10_20200420092827.zip TE0725-test_board-vivado_2019.2-build_10_20200420092815.zip	John Hartfiel	• 2019.2 release
2018-08-09	2018.2	TE0725-test_board_noprebuilt-vivado_2018.2-build_02_20180809122533.zip TE0725-test_board-vivado_2018.2-build_02_20180809122018.zip	John Hartfiel	• 2018.2 update
2018-03-18	2017.4	TE0725-test_board_noprebuilt-vivado_2017.4-build_07_20180319171220.zip TE0725-test_board-vivado_2017.4-build_07_20180319171209.zip	John Hartfiel	• Board Part update reference link only
2018-03-16	2017.4	TE0725-test_board_noprebuilt-vivado_2017.4-build_07_20180316163402.zip	John Hartfiel	• initial release

Date	Vivado	Project Built	Authors	Description
		TE0725-test_board-vivado_2017.4-build_07_20180316163351.zip		

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[1]

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0725-03-15-1C	15_1c	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	NA

1 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0725-03-35-2C	35_2c	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	NA
TE0725-03-100-2C	100_2c	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	NA
TE0725-03-100-2CF	100_2c	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	POF assembled
TE0725-03-100-2I9	100_2i	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	NA
TE0725-03-35-2I	35_2i	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	NA

Table 4: Hardware Modules

Design supports following carriers:

Carrier Model	Notes

Table 5: Hardware Carrier

Additional Hardware	Notes
TE0790 JTAG Programmer	It's not recommended to use TE0790 for power supply(TE0790 TRM[2])
External power supply	

Table 6: Additional Hardware

2 https://wiki.trenz-electronic.de/display/PD/TE0790+TRM#TE0790TRM-PowerandPower-OnSequence

4.5 Content

For general structure and of the reference design, see Project Delivery - Xilinx devices[3]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
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Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Debian SD-Image	*.img	Debian Image for SD-Card

3 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

File	File-Extension	Description
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebult content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0725 "Test Board" Reference Design[4]

4 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/3.5x7.3/TE0725/Reference_Design/2019.2/test_board

5 Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

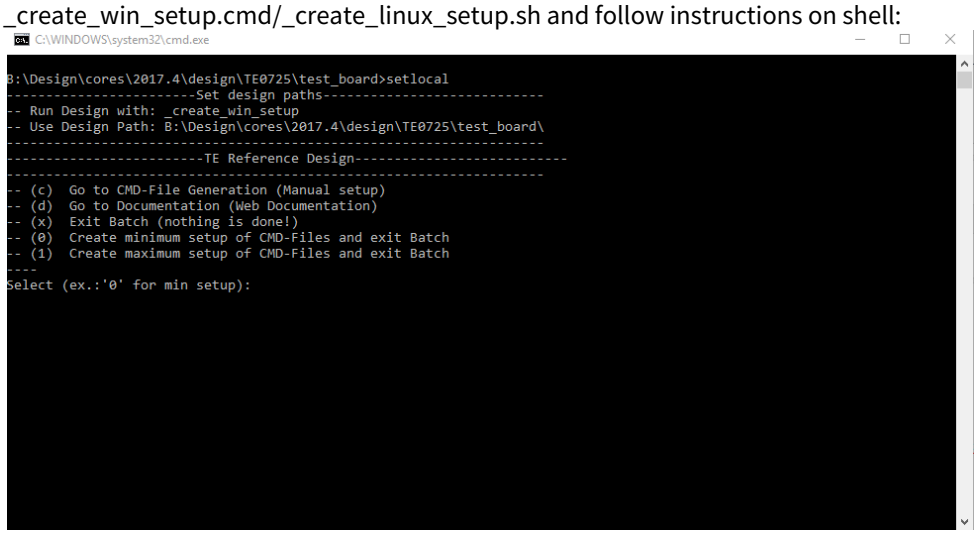
See also:

- Xilinx Development Tools[5]
- Vivado Projects - TE Reference Design[6]
- Project Delivery.[7]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[8]

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process)
   a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
   Note: Select correct one, see alsoTE Board Part Files[9]
5. Create XSA and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
   Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate Programming Files with Vitis

5 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
6 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
8 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality
9 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

   a. Run on Vivado TCL: TE::sw_run_vitis -all
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
      App from Firmware folder will be add into BlockRAM. If you add other app, you must select *.elf manually on Vivado
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
      Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used. See Vitis[10]
7. Copy Application (hello_te0725.elf) into \firmware\microblaze_0\
8. Regenerate Design:
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: App from Firmware folder will be add into BlockRAM. If you add other app, you must select *.elf manually on Vivado
   b. (alternative) Use SDK or Vivado to update generate Bitfile with new Application and regenerate mcs manually.

10 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging[11]

6.1.1 Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder
   Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

6.1.2 QSPI

1. Connect JTAG and power on PCB
2. (if not done) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" or open with "vivado_open_project_guimode.cmd", if generated.
3. Type on Vivado Console: TE::pr_program_flash
   Note: Alternative use SDK or setup Flash on Vivado manually
4. Reboot (if not done automatically)

6.1.3 SD

Not used on this Example.

6.1.4 JTAG

1. Connect JTAG and power on PCB
2. (if not done) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" or open with "vivado_open_project_guimode.cmd", if generated.
3. Open Vivado HW Manager
4. Program Bitfile

11 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging

6.2 Usage

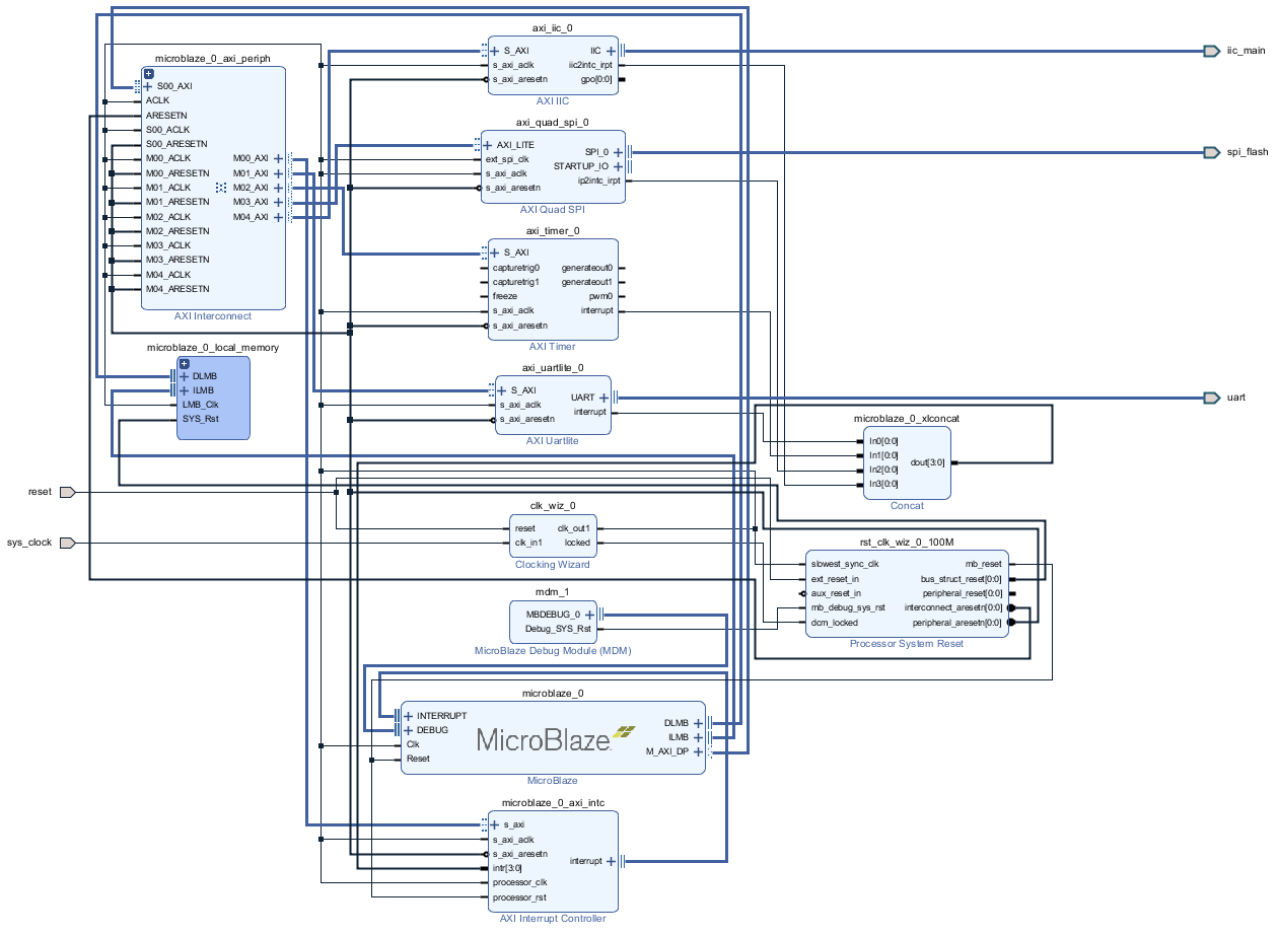
1. Prepare HW like described on section Programming(see page 13)
2. Connect UART USB (most cases same as JTAG)
3. Power On PCB (Do not restart, if you use Bitfile programming)
   Note: FPGA Loads Bitfile from Flash

6.2.1 UART

1. Open Serial Console (e.g. putty)
   a. Speed: 9600
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Uart Console:
   Hello TE0725 will run on endless loop.

7 System Design - Vivado

7.1 Block Design



7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
```

```
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

7.2.2 Design specific constrain

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8 Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis[12]

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 hello_te0725

Hello TE0725 is a Xilinx Hello World example as endless loop instead of one console output.

12 https://wiki.trenz-electronic.de/display/PD/Vitis

9 Additional Software

No additional software is needed.

10 Appx. A: Change History and Legal Notices

10.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2020-04-27	v.13 (see page 6)	@ John Hartfiel[13]	• typo
2020-04-20	v.12	John Hartfiel	• 2019.2 update • Documentation style update
2018-08-09	v.9	John Hartfiel	• 2018.2 update
2018.06.05	v.8	John Hartfiel	• Board Part Documentation update • Typo correction UART Speed
2018-03-16	v.5	John Hartfiel	• 2017.4 release
2018-03-12	v.1	@ John Hartfiel[14]	• Initial release
	All	@ John Hartfiel[15]	

Table 10: Document change history.

10.2 Legal Notices

10.3 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

13 https://wiki.trenz-electronic.de/display/~j.hartfiel
14 https://wiki.trenz-electronic.de/display/~j.hartfiel
15 https://wiki.trenz-electronic.de/display/~j.hartfiel

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16 http://guidance.echa.europa.eu/

Candidate List[17] are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA)[18].

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2019-06-07

17 https://echa.europa.eu/candidate-list-table
18 http://www.echa.europa.eu/