

U\_FPGA\_IO  
FPGA\_IO.SchDoc



U\_FPGA\_MGT  
FPGA\_MGT.SchDoc



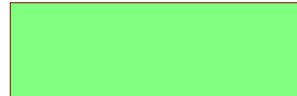
U\_FPGA\_MISC  
FPGA\_MISC.SchDoc



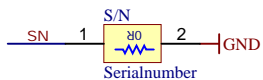
U\_B2B\_Connector  
B2B\_Connector.SchDoc



U\_POWER  
POWER.SchDoc



U\_Revision  
Revision Changes.SchDoc

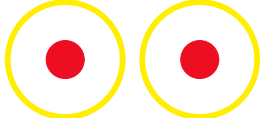


LOGO1

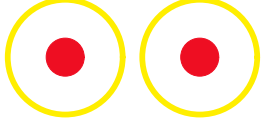


LOGO PRINT

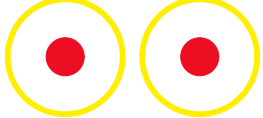
FIDU-DOT - small FIDU-DOT - small



PM1 PM2  
FIDU-DOT - small FIDU-DOT - small



PM4 PM5  
FIDU-DOT - small FIDU-DOT - small

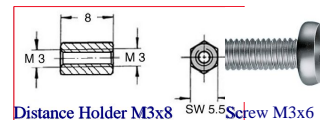


PM6 PM3

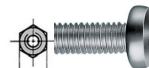
Top of Board



Screw M3x4

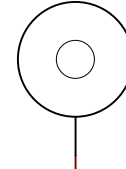


Distance Holder M3x8



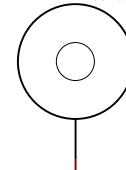
Screw M3x6

Mount.Hole 3.2mm



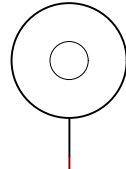
GND

Mount.Hole 3.2mm



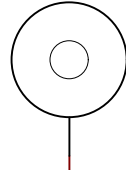
GND

Mount.Hole 3.2mm



GND

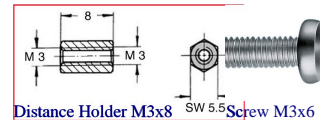
Mount.Hole 3.2mm



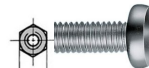
GND



Screw M3x4



Distance Holder M3x8



Screw M3x6



Title: TE0714		
A4	Number: 1 35-213	Rev. 02
Date: 2016-08-04	Copyright: Trenz Electronic GmbH / TT	Page 1 of 7
Filename: TE0714.SchDoc		

A

B

C

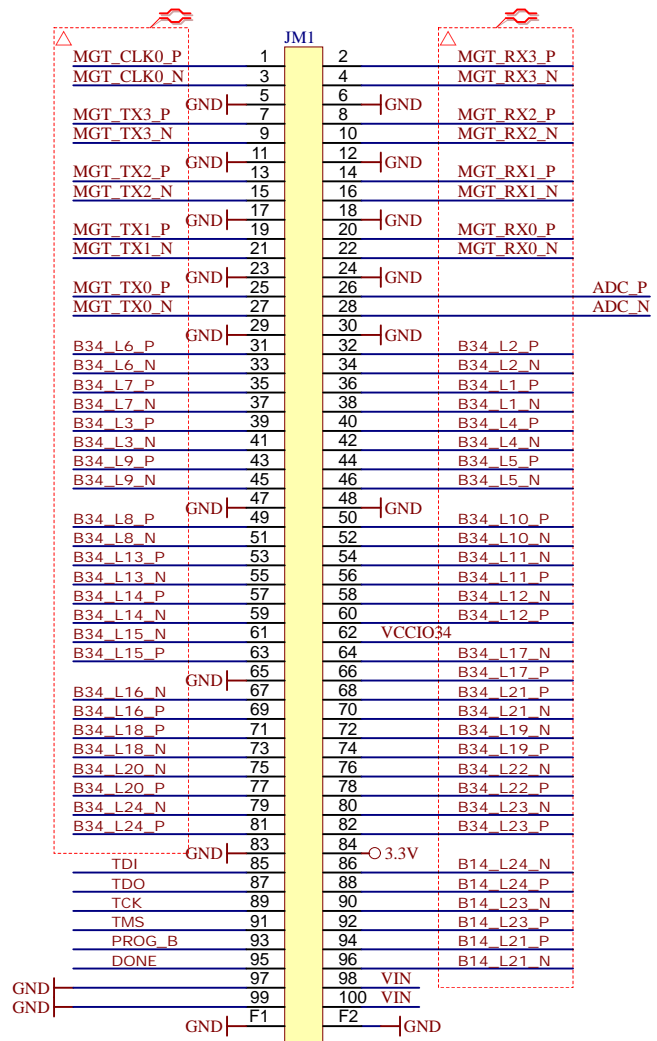
D

A

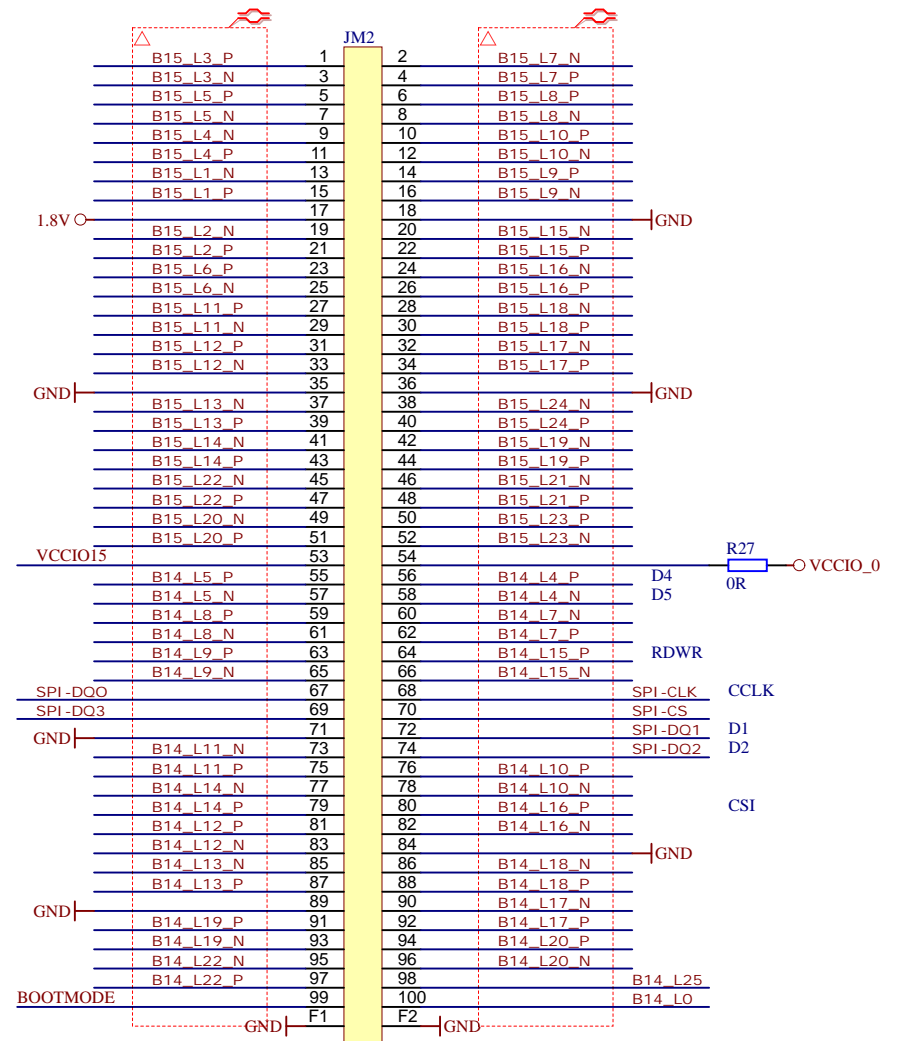
B

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D



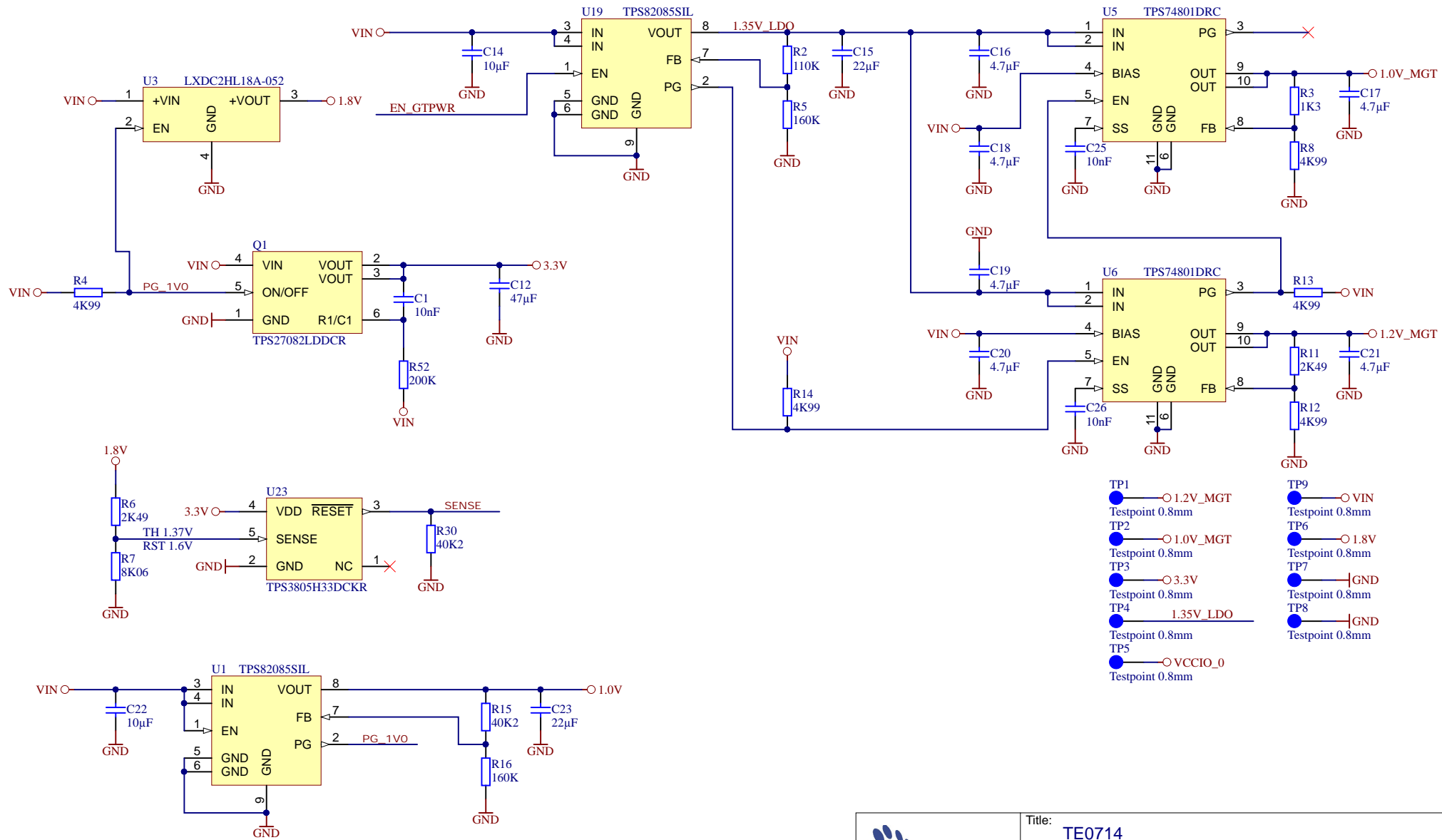
LSHM-150-02.5-L-DV-A-S-K-TR



LSHM-150-02.5-L-DV-A-S-K-TR



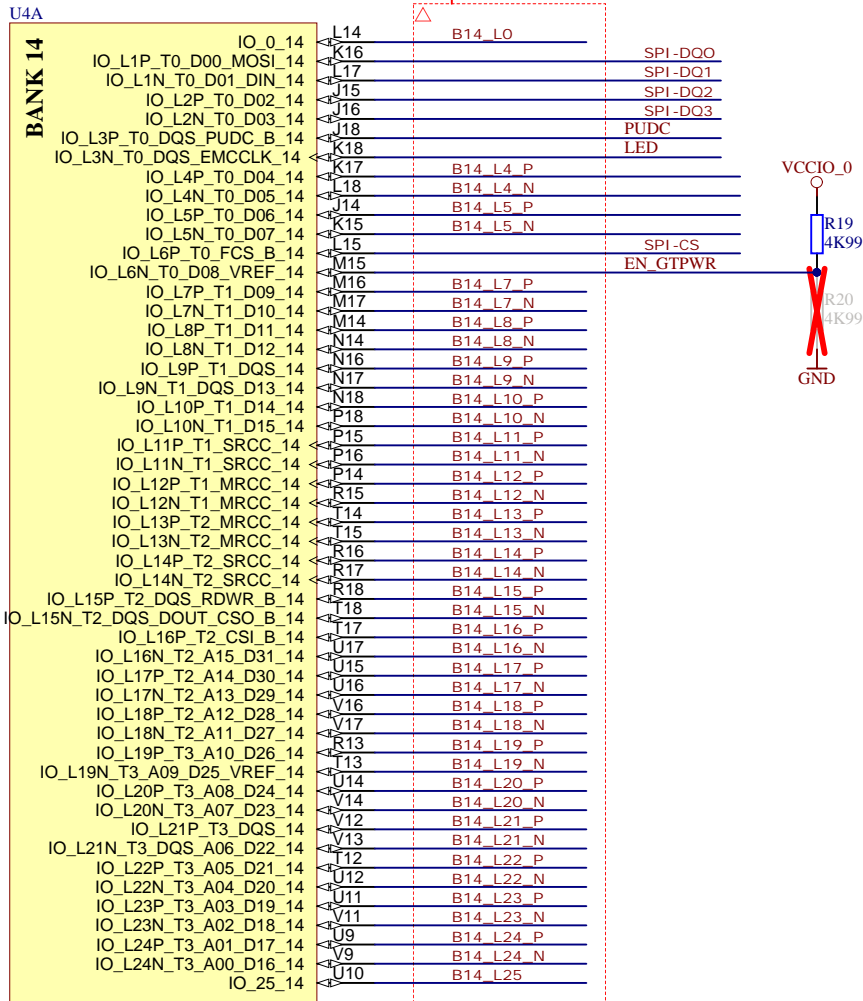
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A4	Number: 2	Rev. 02	
Date: 2016-08-04		Copyright: Trenz Electronic GmbH / TT	Page2 of 7
Filename: B2B_Connector.SchDoc			



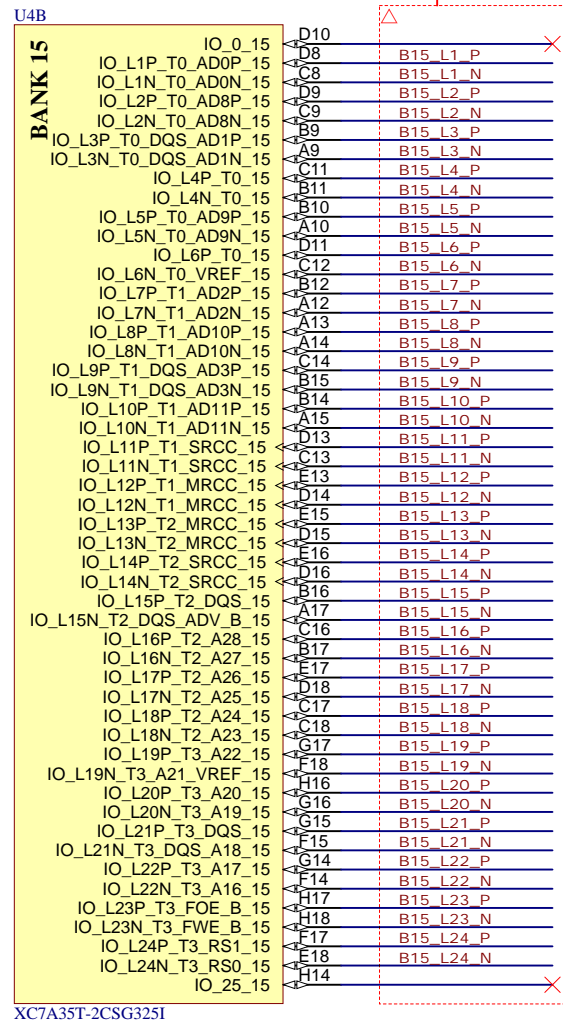
- TP1 ○ 1.2V\_MGT Testpoint 0.8mm
- TP2 ○ 1.0V\_MGT Testpoint 0.8mm
- TP3 ○ 3.3V Testpoint 0.8mm
- TP4 ○ 1.35V\_LDO Testpoint 0.8mm
- TP5 ○ VCCIO\_0 Testpoint 0.8mm
- TP6 ○ 1.8V Testpoint 0.8mm
- TP7 | GND Testpoint 0.8mm
- TP8 | GND Testpoint 0.8mm
- TP9 ○ VIN Testpoint 0.8mm



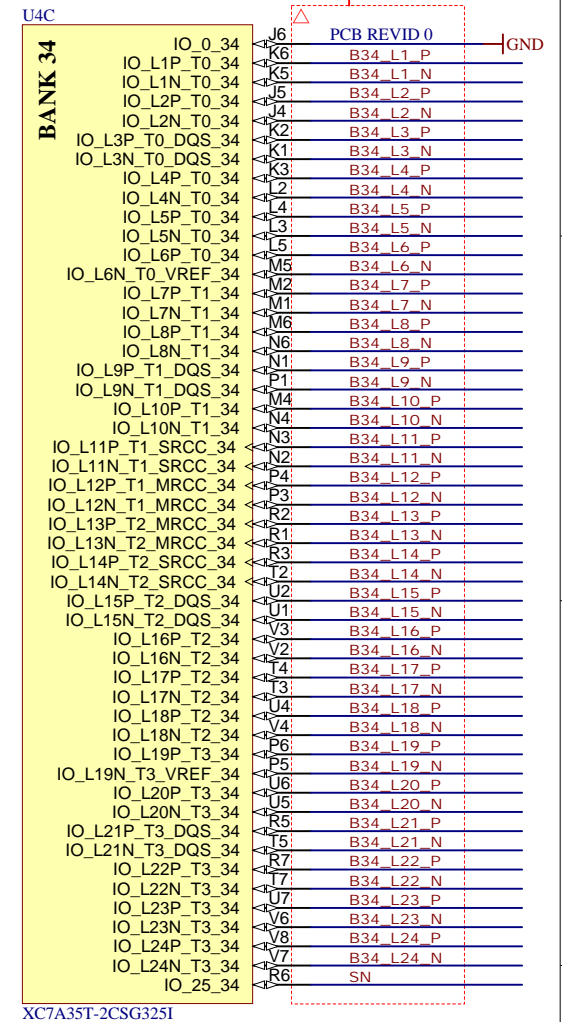
Title: TE0714		
A4	Number: 3 35-213	Rev. 02
Date: 2016-08-04	Copyright: Trenz Electronic GmbH	Page3 of 7
Filename: POWER.SchDoc		



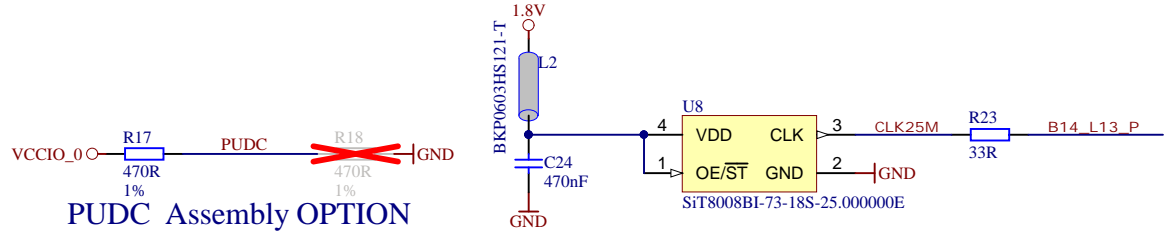
XC7A35T-2CSG325I



XC7A35T-2CSG325I



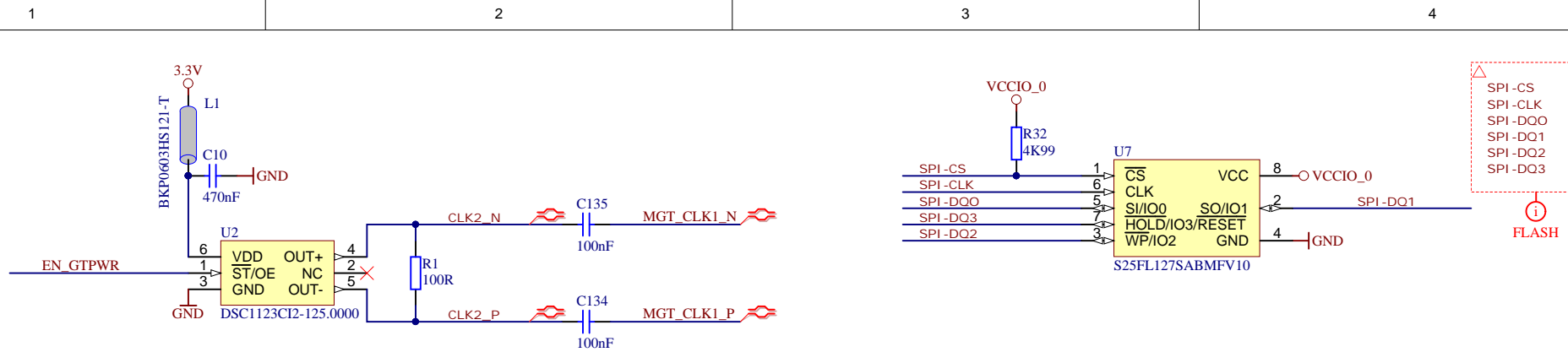
XC7A35T-2CSG325I



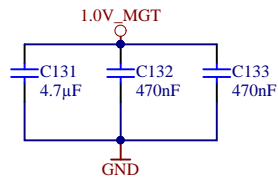
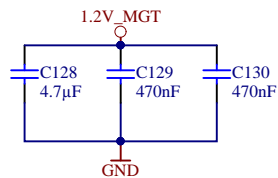
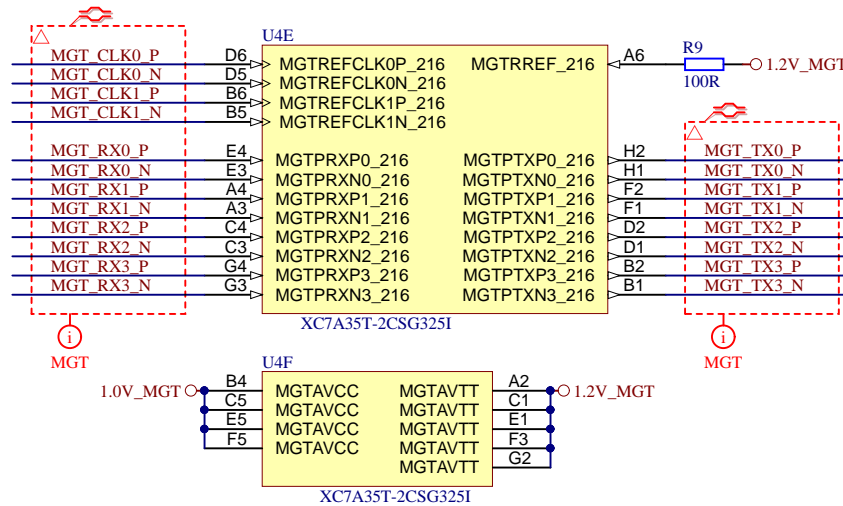
PUDC Assembly OPTION



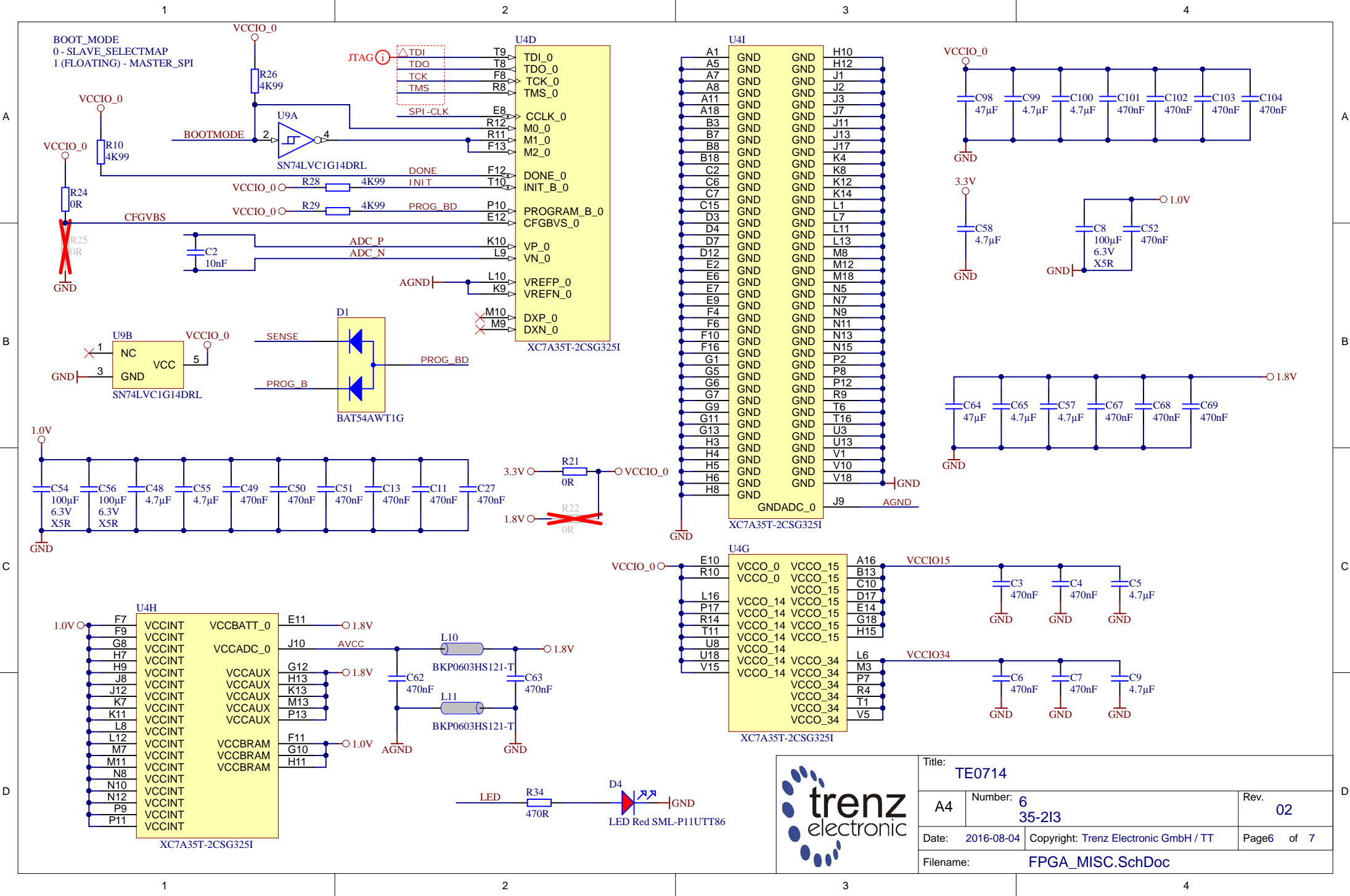
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A4	Number: 4	35-213	
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OSC FREQ is Assembly OPTION = 125MHZ



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Changes REV 02:

- 1. Added 0 ohm strap option to supply VCCIO0 on B2B connector
- 2. Added PCB Revision sense support. PCB Revision readout possible from HDL Design
- 3. Updated FPGA pin PROG\_B connection. TPS3805H33 push-pull output RESET\_N not affected on baseboard circuit, connected to PROG\_B.
- 4. C8, C54, C56 updated to 100uF for variant 50-2I
- 5. Added testpoints

Changes REV 02A (12.2018):

- 1. New FLASH memory U7 S25FL127SABMFV10

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A

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	Title: <b>TE0714</b>		
	A4	Number: <b>7</b> <b>35-213</b>	Rev. <b>02</b>
	Date: <b>2016-08-04</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>7</b> of <b>7</b>
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