

U_FPGA_IO
FPGA_IO.SchDoc

U_FPGA_MGT
FPGA_MGT.SchDoc

U_FPGA_MISC
FPGA_MISC.SchDoc

U_B2B_Connector
B2B_Connector.SchDoc

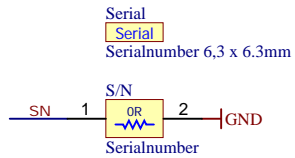
U_POWER
POWER.SchDoc

U_Revision
Revision Changes.SchDoc

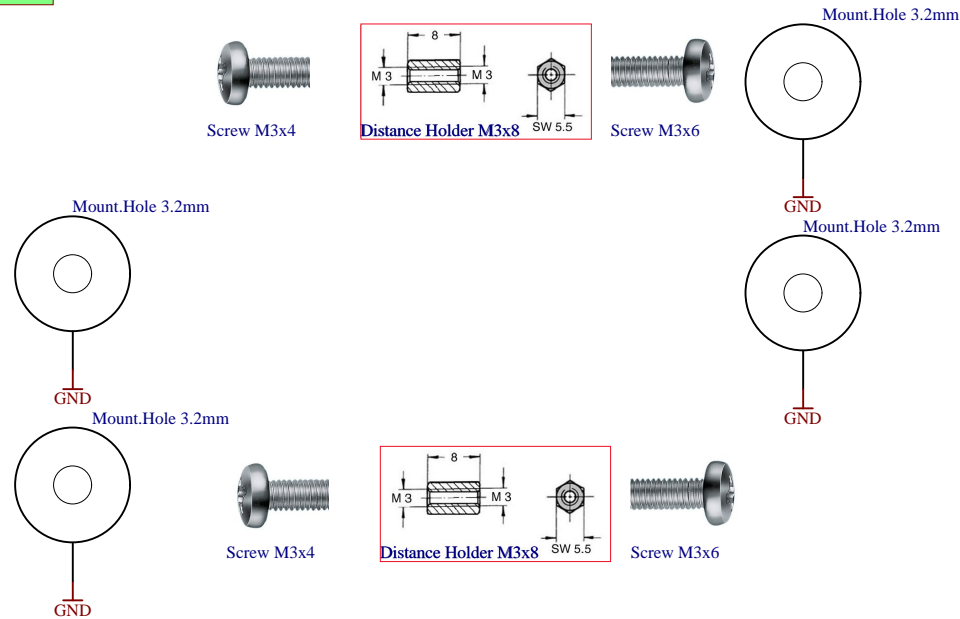
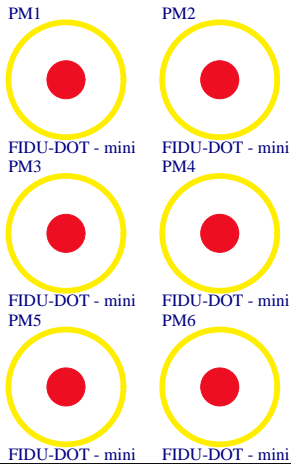
Special notes:

-
-

Top of Board



LOGO1
TE Logo PRINT Layer
LOGO PRINT



Assembly variant	50-2IC6
Created by	
Modified by	
Modified at	
SVN Revision	8634



Title: TE0714		
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A

B

C

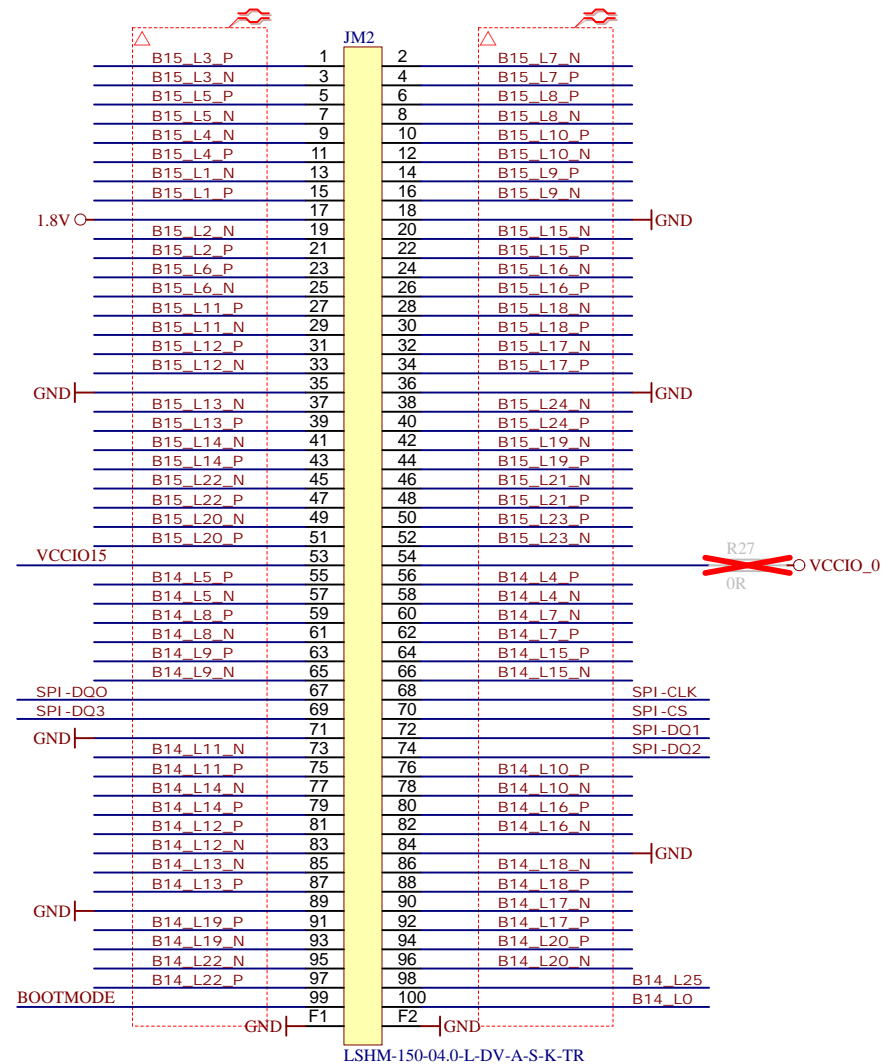
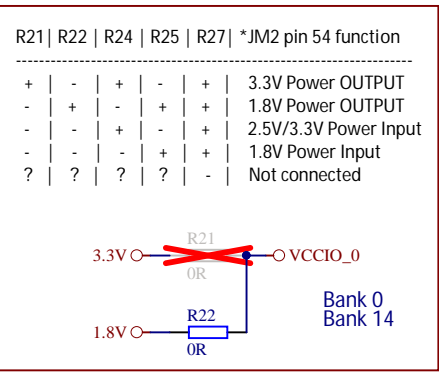
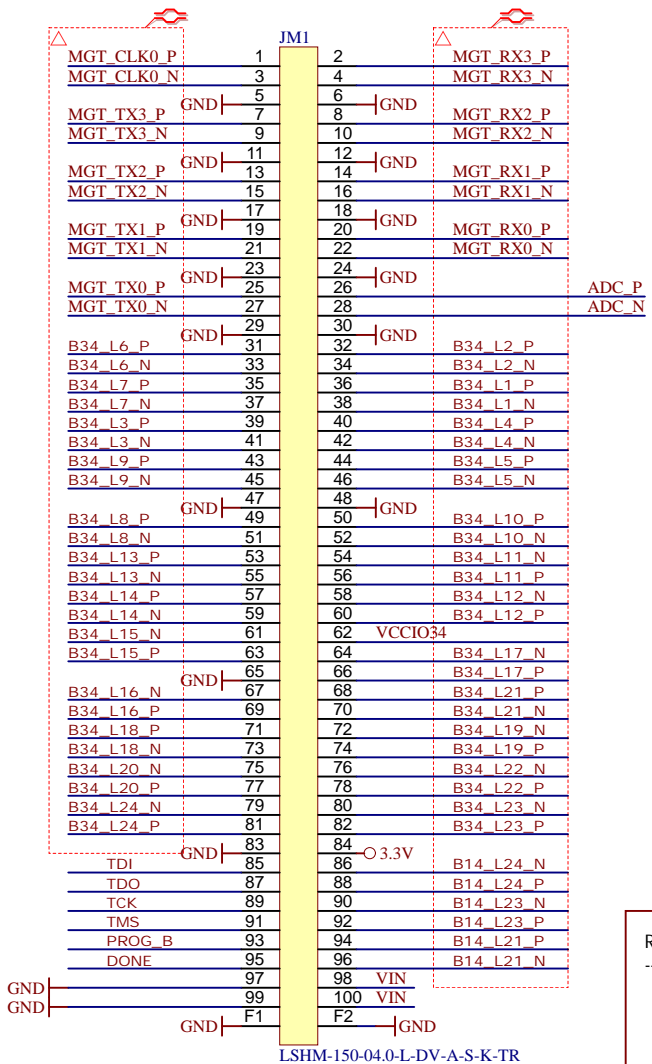
D

A

B

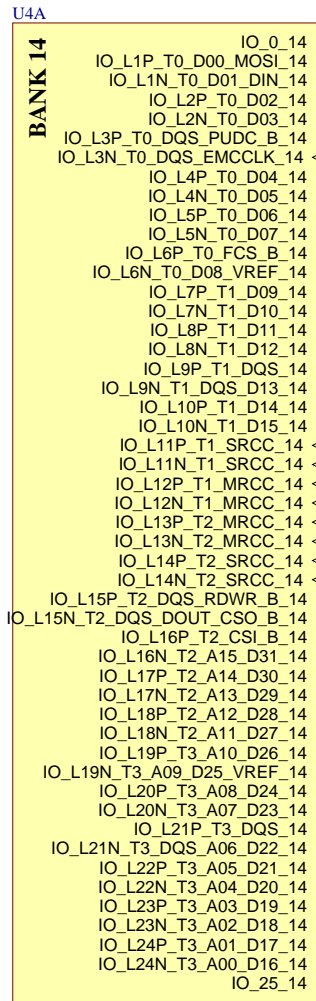
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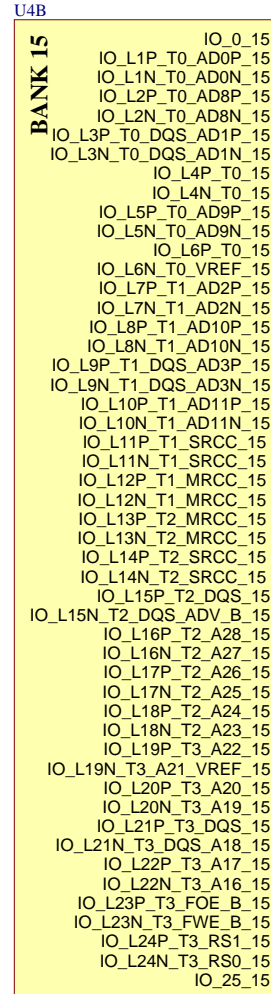


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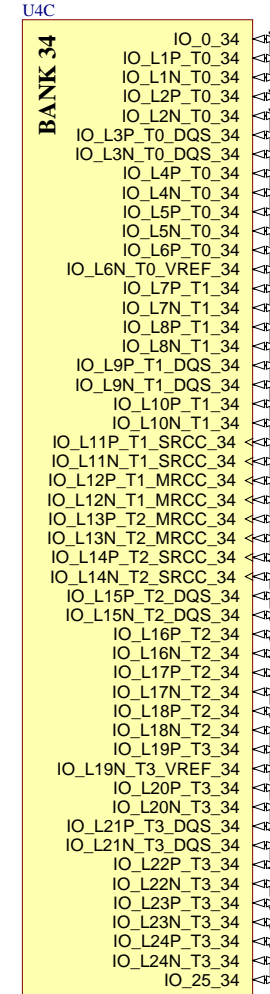
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Filename: B2B_Connector.SchDoc		



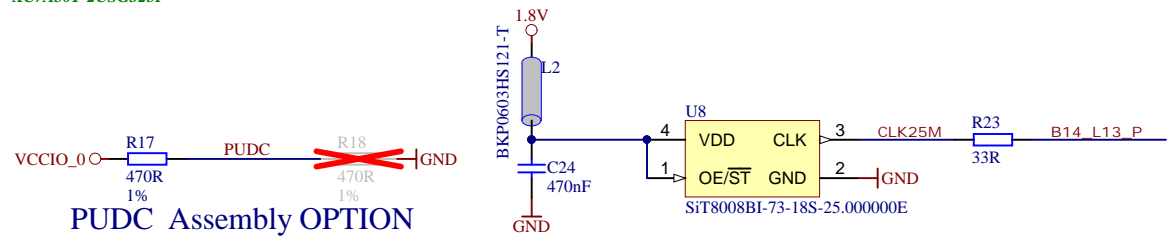
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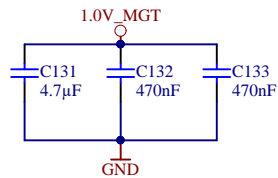
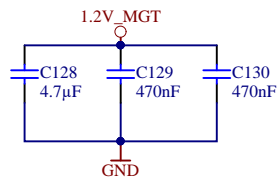
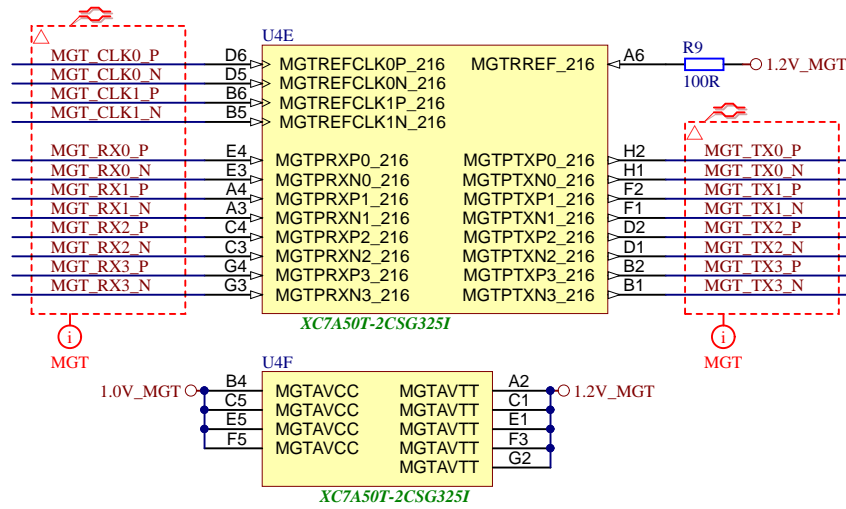
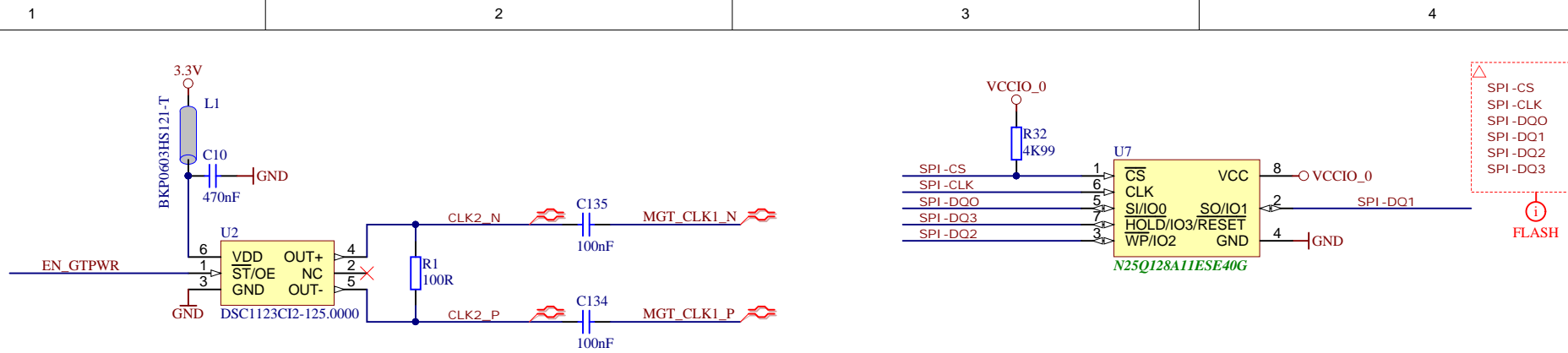
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XC7A50T-2CSG3251



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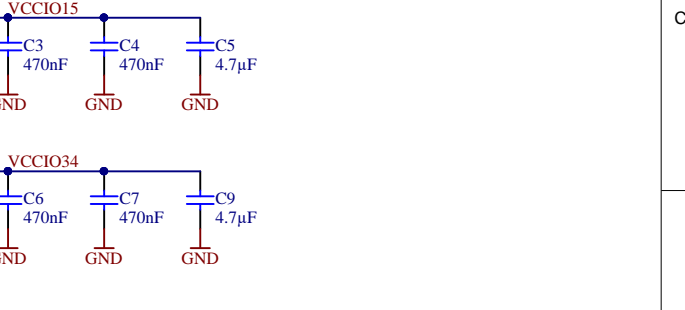
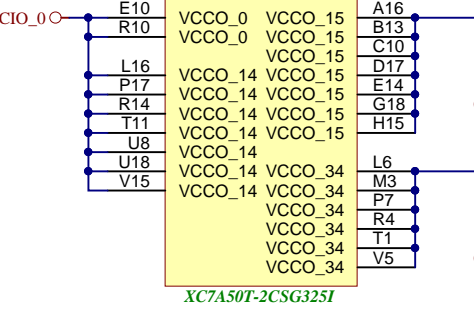
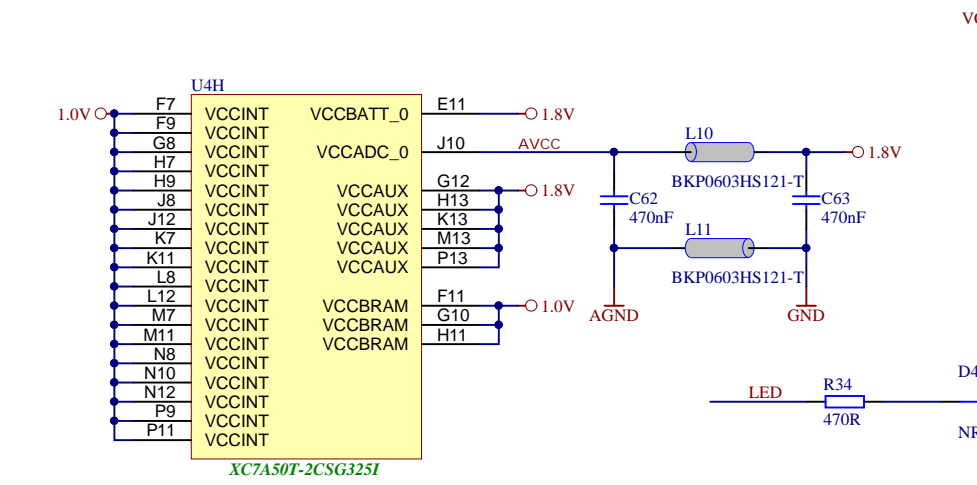
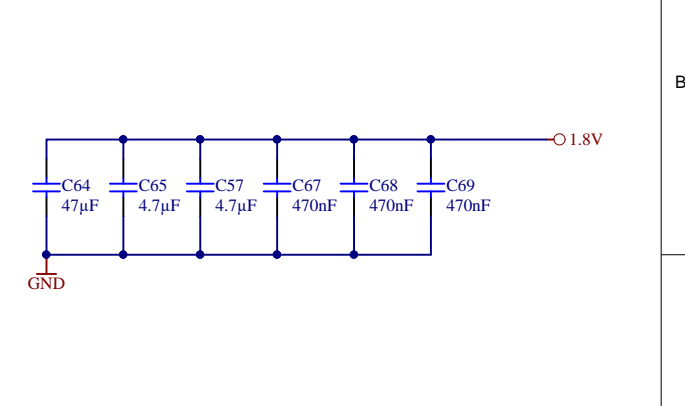
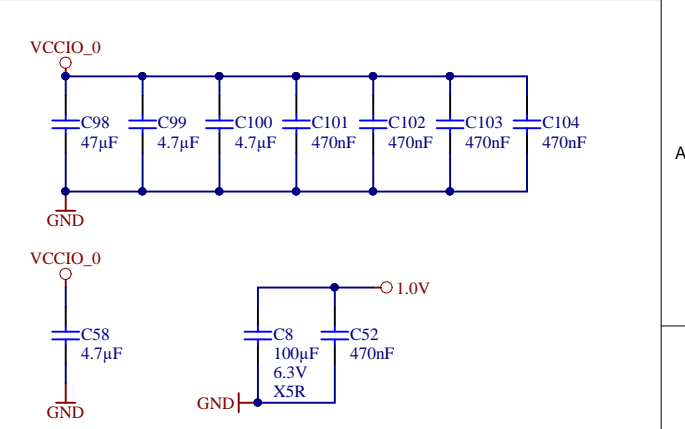
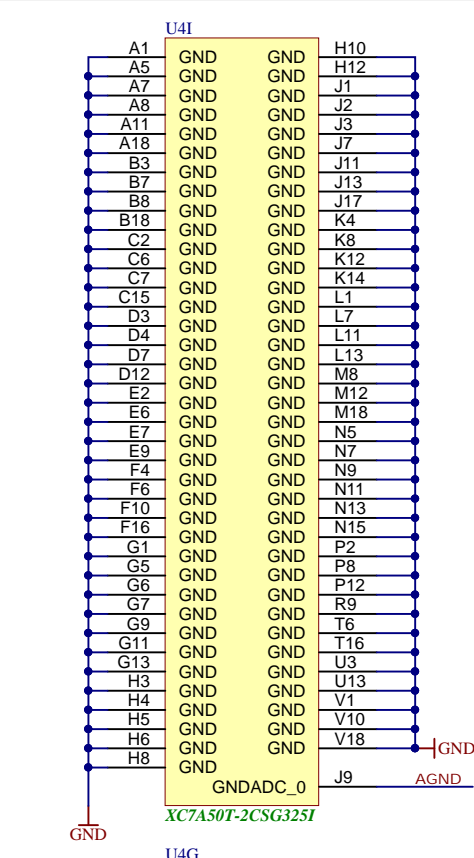
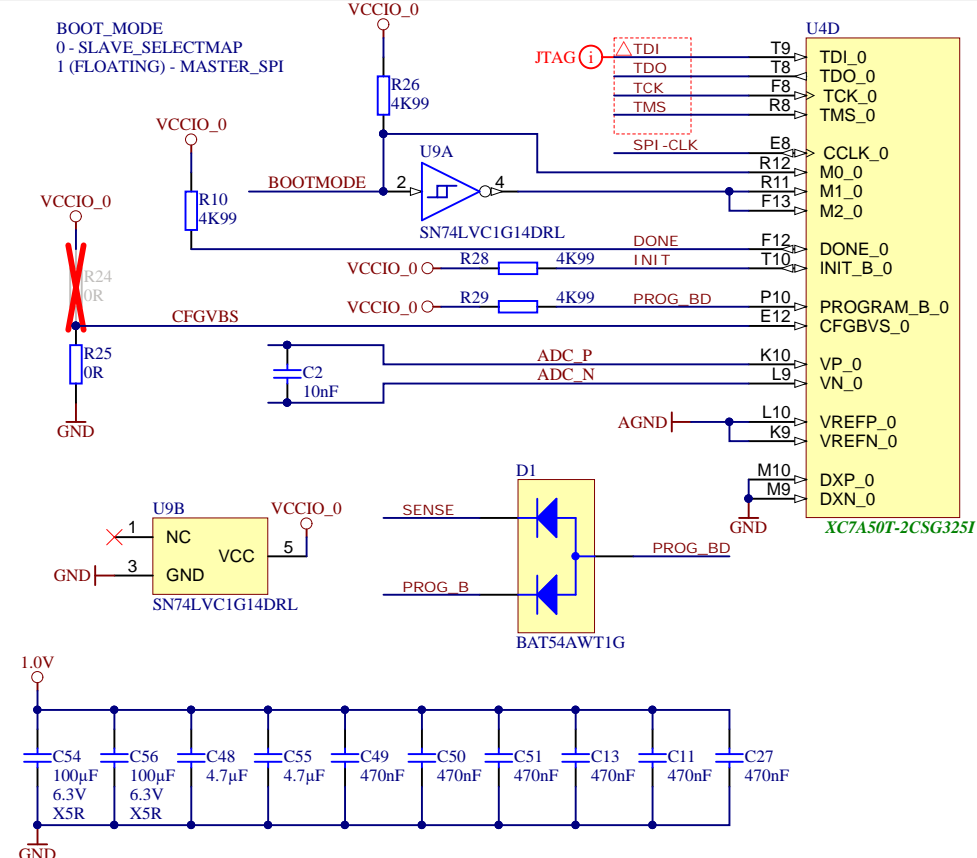
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Filename: FPGA_MGT.SchDoc				

A

B

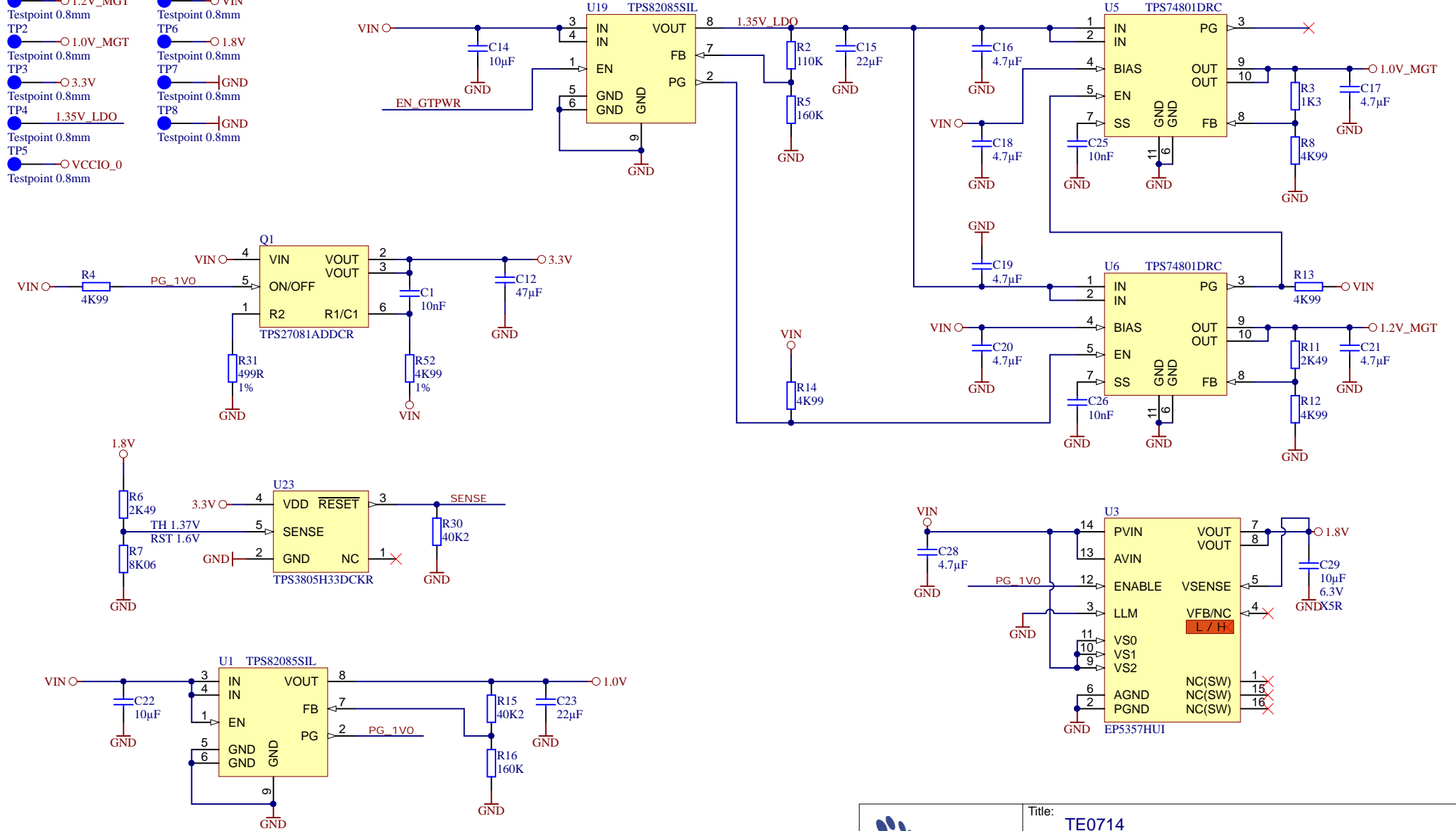
C

D



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- TP1 ● ○ 1.2V_MGT
Testpoint 0.8mm
- TP2 ● ○ 1.0V_MGT
Testpoint 0.8mm
- TP3 ● ○ 3.3V
Testpoint 0.8mm
- TP4 ● ○ 1.35V_LDO
Testpoint 0.8mm
- TP5 ● ○ VCCIO_0
Testpoint 0.8mm
- TP9 ● ○ VIN
Testpoint 0.8mm
- TP6 ● ○ 1.8V
Testpoint 0.8mm
- TP7 ● ○ GND
Testpoint 0.8mm
- TP8 ● ○ GND
Testpoint 0.8mm



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Changes REV 02:


- 1. Added 0 ohm strap option to supply VCCIO0 on B2B connector
- 2. Added PCB Revision sense support. PCB Revision readout possible from HDL Design
- 3. Updated FPGA pin PROG_B connection. TPS3805H33 push-pull output RESET_N not affected on baseboard circuit, connected to PROG_B.
- 4. C8, C54, C56 updated to 100uF for variant 50-2I
- 5. Added testpoints

Changes REV 02A (12.2018):

- 1. New FLASH memory U7 S25FL127SABMFV10

Changes REV 03:

- 1) Changed obsolete component U3 (LXDC2HL18A-052 -> EP5357HUI)
- 2) DXP/DXN connected to GND (recommendation UG475, p31)
- 3) Added serial number to silk
- 4) Changed obsolete component Q1 (TPS27082LDDCR ->TPS27081ADDCR)
- 5) Full update LIB
- 6) Optimized testpoints placement

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