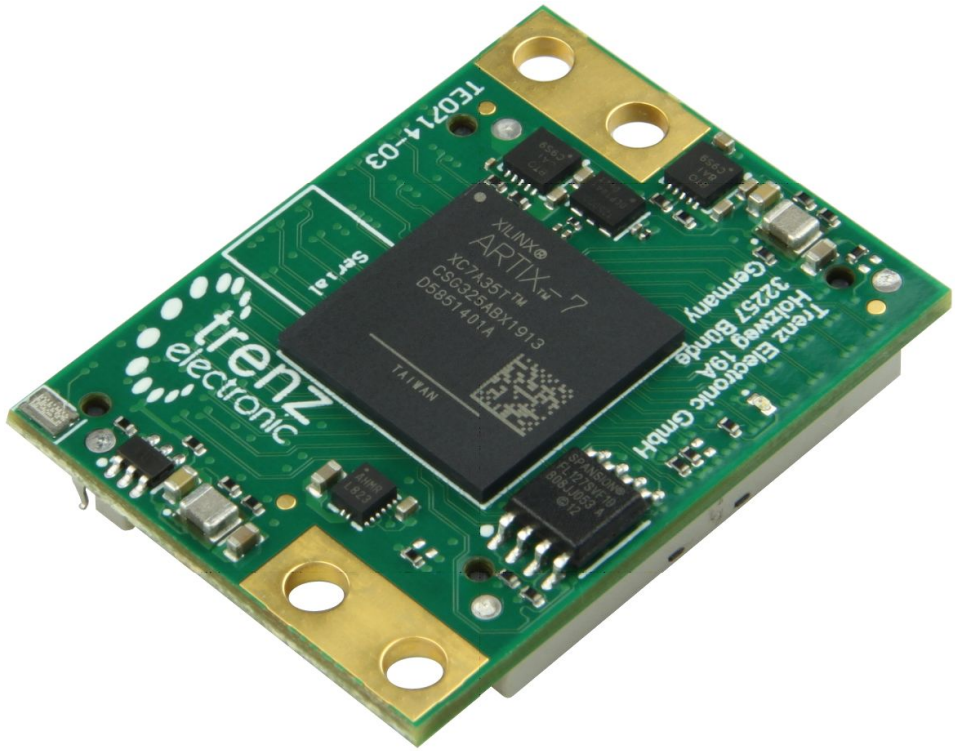

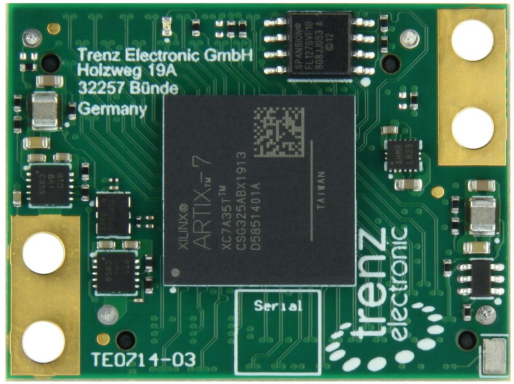

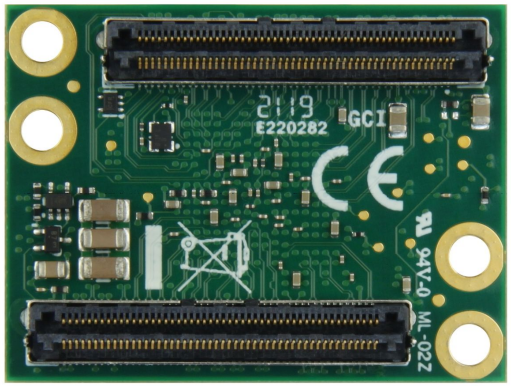

Regarding the usage of our schematics and alike documentation for Trenz module TE0714.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0714 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

Drawn by	ED
Checked by	VT
Assembly variant	42I-7-C
Created by	ED
Modified by	ED
Modified at	2022-12-07

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Title: Legal Notices Modules

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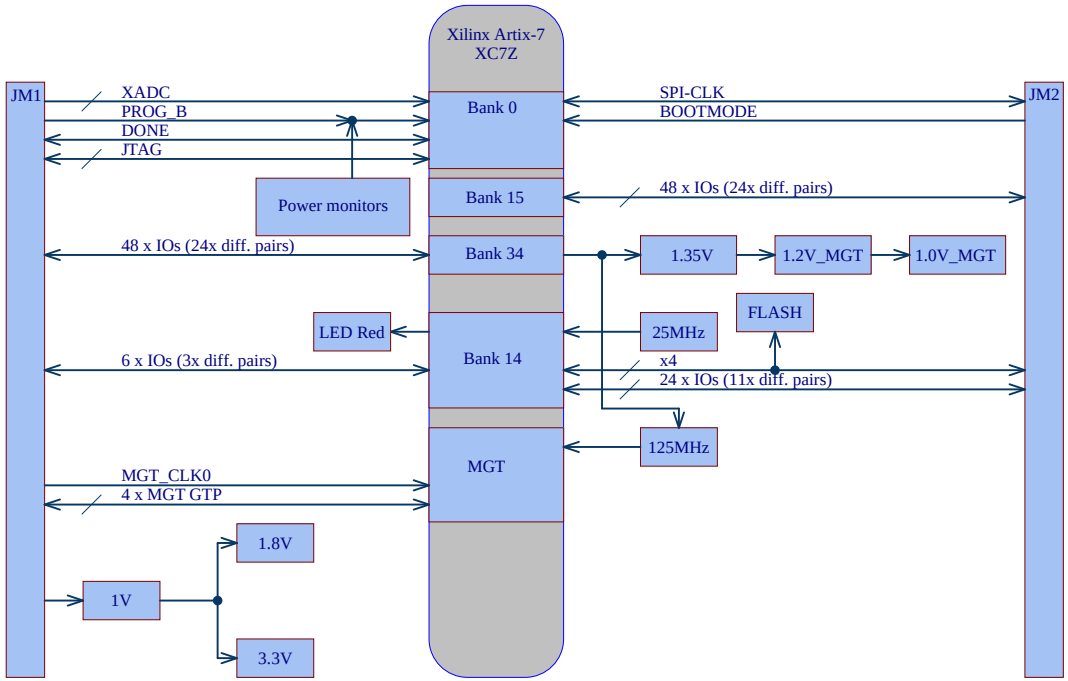
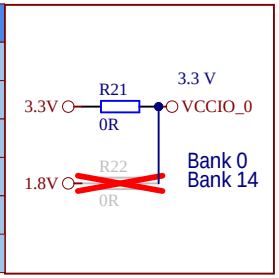


PCB Revision

Revision	PCB REVID 3	PCB REVID 2	PCB REVID 1	PCB REVID 0
REV03	N/A	N/A	N/A	GND
REV04	GND	VCCIO15	GND	GND

VCCIO_0 Power Function

*JM2 pin 54 function	R21	R22	R24	R25	R27
3.3V Power OUTPUT	+	-	+	-	+
1.8V Power OUTPUT	-	+	-	+	+
2.5V/3.3V Power Input	-	-	+	-	+
1.8V Power Input	-	-	-	+	+
Not connected	X	X	X	X	-
Legend: + = Assembled; - = Not assembled; X = Do not care;					



Bootmode

BOOTMODE	Bootmode
0	SLAVE_SELECTMAP
1 / Floating	MASTER_SPI

U_Legal Notices Modules | U_TE0714 | U_Power_Diagram | U_Revision Changes

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Title: Overview		
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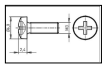
Special notes:

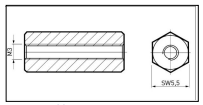
•

•

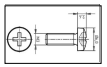
Top of Board



Screw M3x4

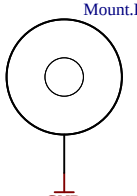


Standoff M3x8 II



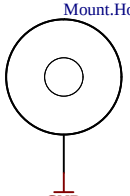
Screw M3x6

Mount.Hole 3.2mm



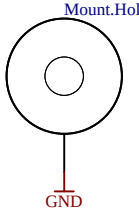
GND

Mount.Hole 3.2mm



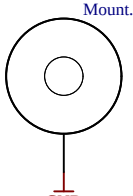
GND

Mount.Hole 3.2mm

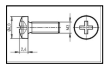


GND

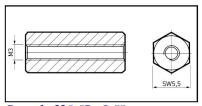
Mount.Hole 3.2mm



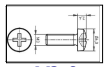
GND



Screw M3x4



Standoff M3x8 II



Screw M3x6

Serial

Serial

Serialnumber 6,3 x 6.3mm

LOGO2

CE Logo on Top Overlay

CE-TOPOVERLAY

LOGO3

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

LOGO4

TE Address Overlay

ADDRESS

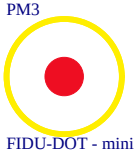
PM1

FIDU-DOT - mini

PM2

FIDU-DOT - mini

PM3

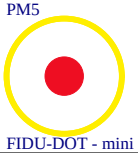


FIDU-DOT - mini

PM4

FIDU-DOT - mini

PM5



FIDU-DOT - mini

PM6

FIDU-DOT - mini

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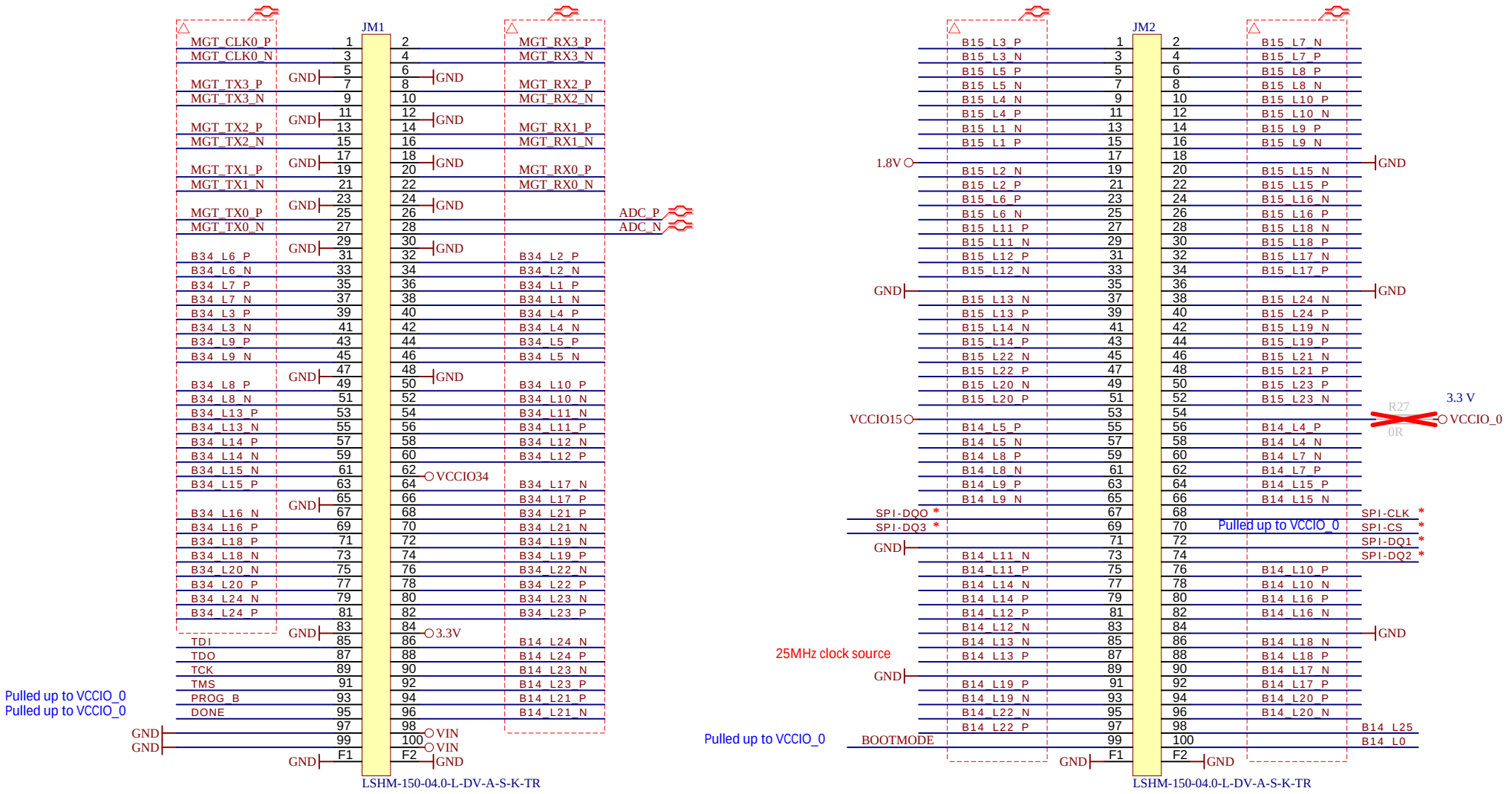
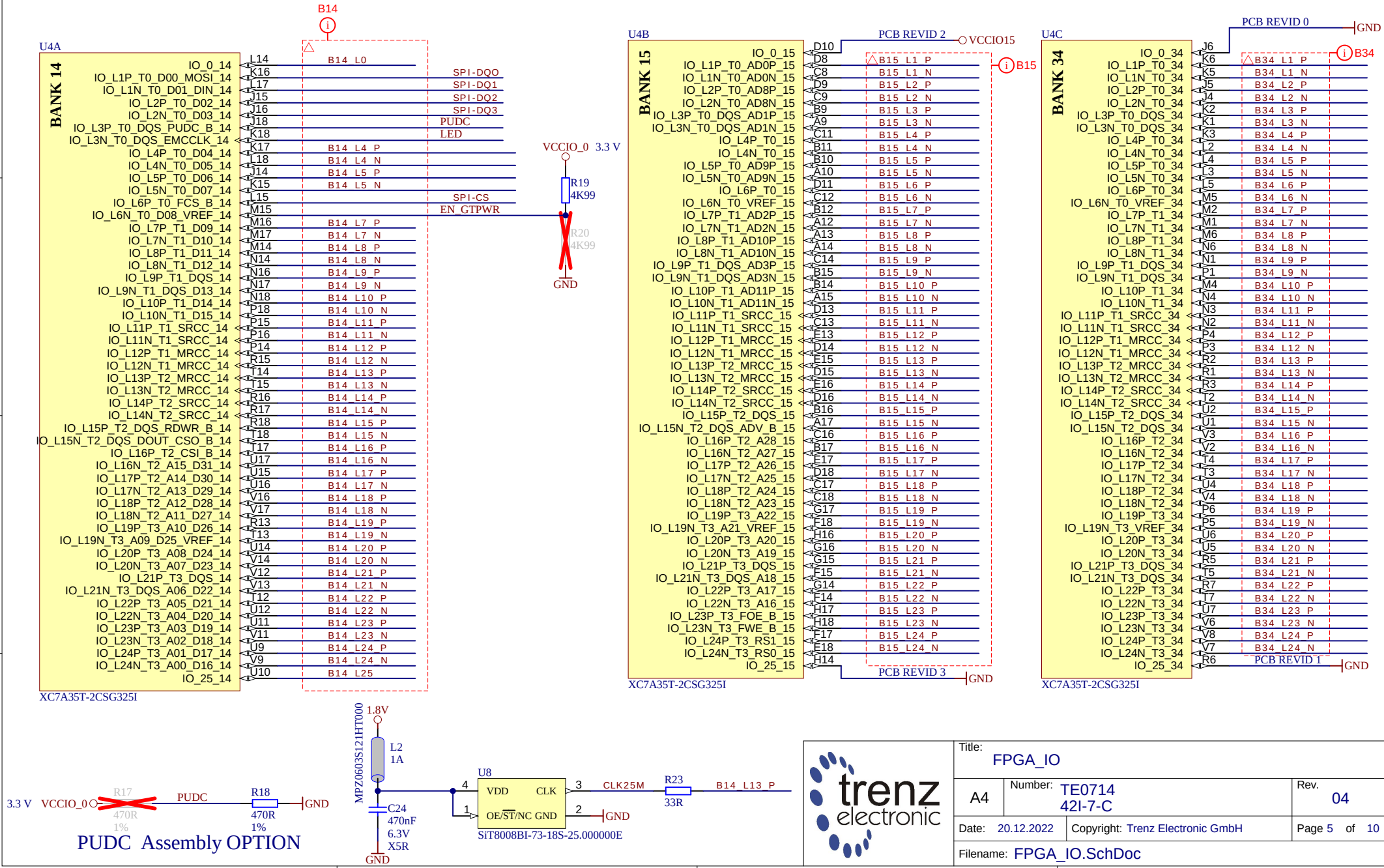
Title: TE0714			
A4	Number: TE0714 42I-7-C		Rev. 04
Date: 20.12.2022	Copyright: Trenz Electronic GmbH		Page 3 of 10
Filename: TE0714.SchDoc			



* B2B IOs SPI-xx are shared with FLASH and can not be used as normal IOs.

trenz electronic	Title: B2B_Connector		
A4	Number: TE0714 42I-7-C		Rev. 04
Date: 20.12.2022	Copyright: Trenz Electronic GmbH		Page 4 of 10
Filename: B2B_Connector.SchDoc			



Title: FPGA_IO			
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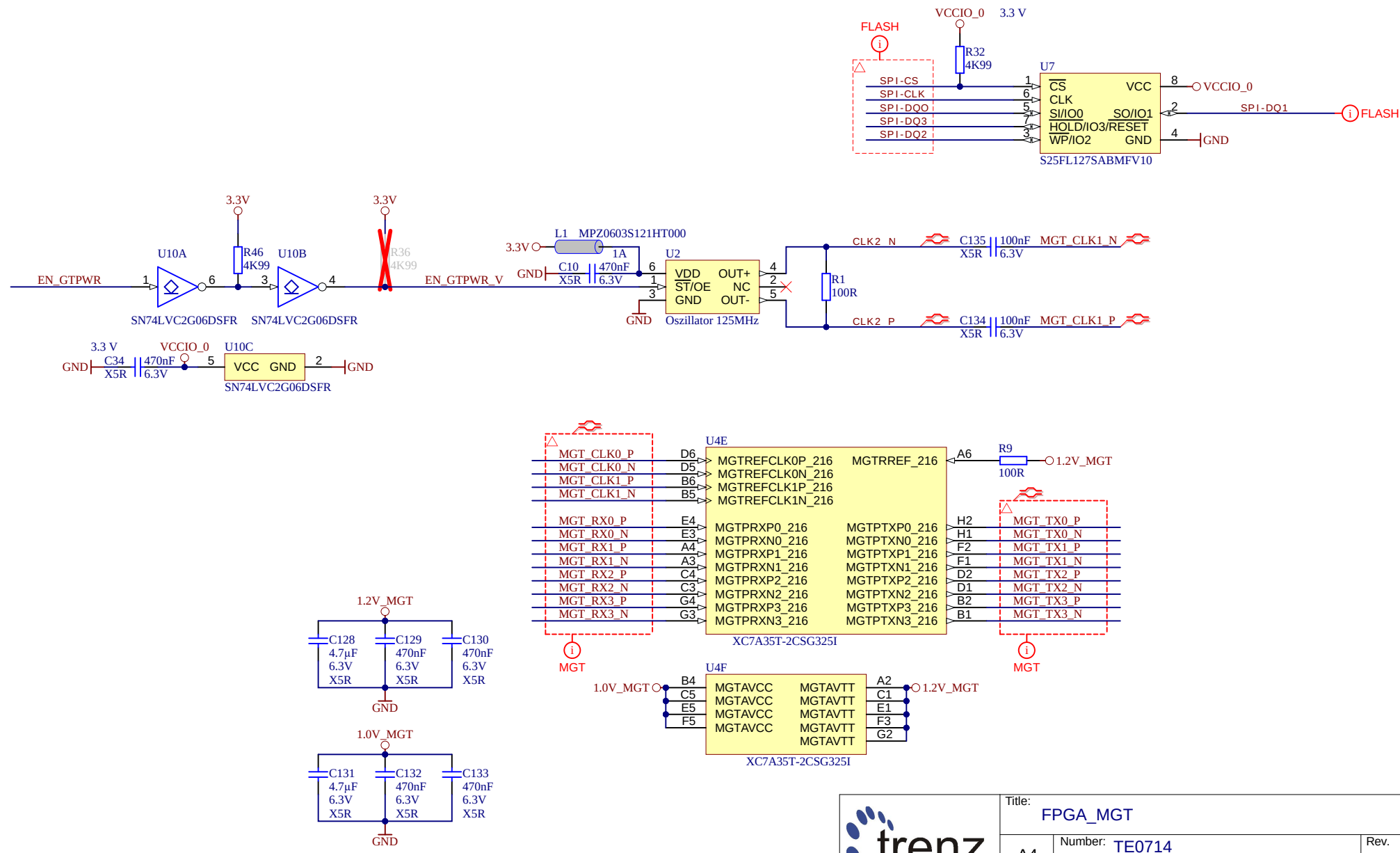
Date: 20.12.2022	Copyright: Trenz Electronic GmbH		Page 5 of 10
Filename: FPGA_IO.SchDoc			



trenz electronic	Title: FPGA_MGT		
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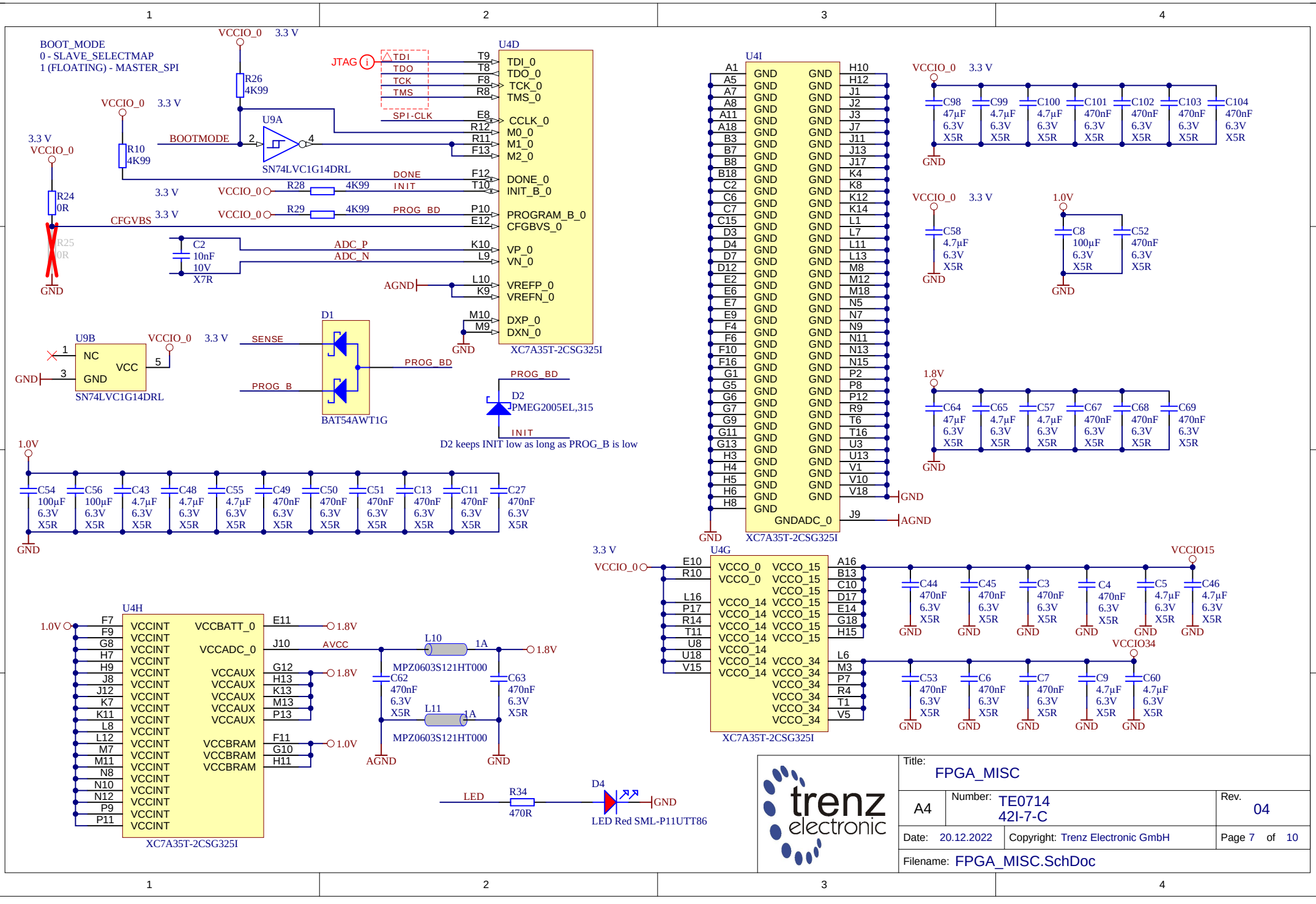
	Date: 20.12.2022	Copyright: Trenz Electronic GmbH	Page 6 of 10
	Filename: FPGA_MGT.SchDoc		


BOOT_MODE
0 - SLAVE_SELECTMAP
1 (FLOATING) - MASTER_SPI
VCCIO_0 3.3 V
R26 4K99
R10 4K99
R24 0R
R25 0R
BOOTMODE
CFGVBS
U9A
SN74LVC1G14DRL
JTAG
TDI
TDO
TCK
TMS
SPI-CLK
DONE
INIT
PROG_BD
R28 4K99
R29 4K99
C2 10nF 10V X7R
ADC_P
ADC_N
AGND
U4D
TDI_0
TDO_0
TCK_0
TMS_0
CCLK_0
M0_0
M1_0
M2_0
DONE_0
INIT_B_0
PROGRAM_B_0
CFGBVS_0
VP_0
VN_0
VREFP_0
VREFN_0
DXP_0
DXN_0
XC7A35T-2CSG325I
U9B
NC
GND
VCC
SN74LVC1G14DRL
SENSE
PROG_B
D1
BAT54AWT1G
D2
JPMEG2005EL,315
D2 keeps INIT low as long as PROG_B is low
1.0V
C54 100µF 6.3V X5R
C56 100µF 6.3V X5R
C43 4.7µF 6.3V X5R
C48 4.7µF 6.3V X5R
C55 4.7µF 6.3V X5R
C49 470nF 6.3V X5R
C50 470nF 6.3V X5R
C51 470nF 6.3V X5R
C13 470nF 6.3V X5R
C11 470nF 6.3V X5R
C27 470nF 6.3V X5R
U4H
VCCINT
VCCBATT_0
VCCADC_0
VCCAUX
VCCBRAM
XC7A35T-2CSG325I
AVCC
L10 1A
MPZ0603S121HT000
C62 470nF 6.3V X5R
C63 470nF 6.3V X5R
L11 1A
LED
R34 470R
D4
LED Red SML-P11UTT86
U4I
GND
GNDADC_0
XC7A35T-2CSG325I
C98 47µF 6.3V X5R
C99 4.7µF 6.3V X5R
C100 4.7µF 6.3V X5R
C101 470nF 6.3V X5R
C102 470nF 6.3V X5R
C103 470nF 6.3V X5R
C104 470nF 6.3V X5R
C58 4.7µF 6.3V X5R
C8 100µF 6.3V X5R
C52 470nF 6.3V X5R
C64 47µF 6.3V X5R
C65 4.7µF 6.3V X5R
C57 4.7µF 6.3V X5R
C67 470nF 6.3V X5R
C68 470nF 6.3V X5R
C69 470nF 6.3V X5R
U4G
VCCO_0
VCCO_14
VCCO_15
VCCO_34
XC7A35T-2CSG325I
VCCIO15
C44 470nF 6.3V X5R
C45 470nF 6.3V X5R
C3 470nF 6.3V X5R
C4 470nF 6.3V X5R
C5 4.7µF 6.3V X5R
C46 4.7µF 6.3V X5R
VCCIO34
C53 470nF 6.3V X5R
C6 470nF 6.3V X5R
C7 470nF 6.3V X5R
C9 4.7µF 6.3V X5R
C60 4.7µF 6.3V X5R
GND
AGND
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Title: FPGA_MISC
A4
Number: TE0714 42I-7-C
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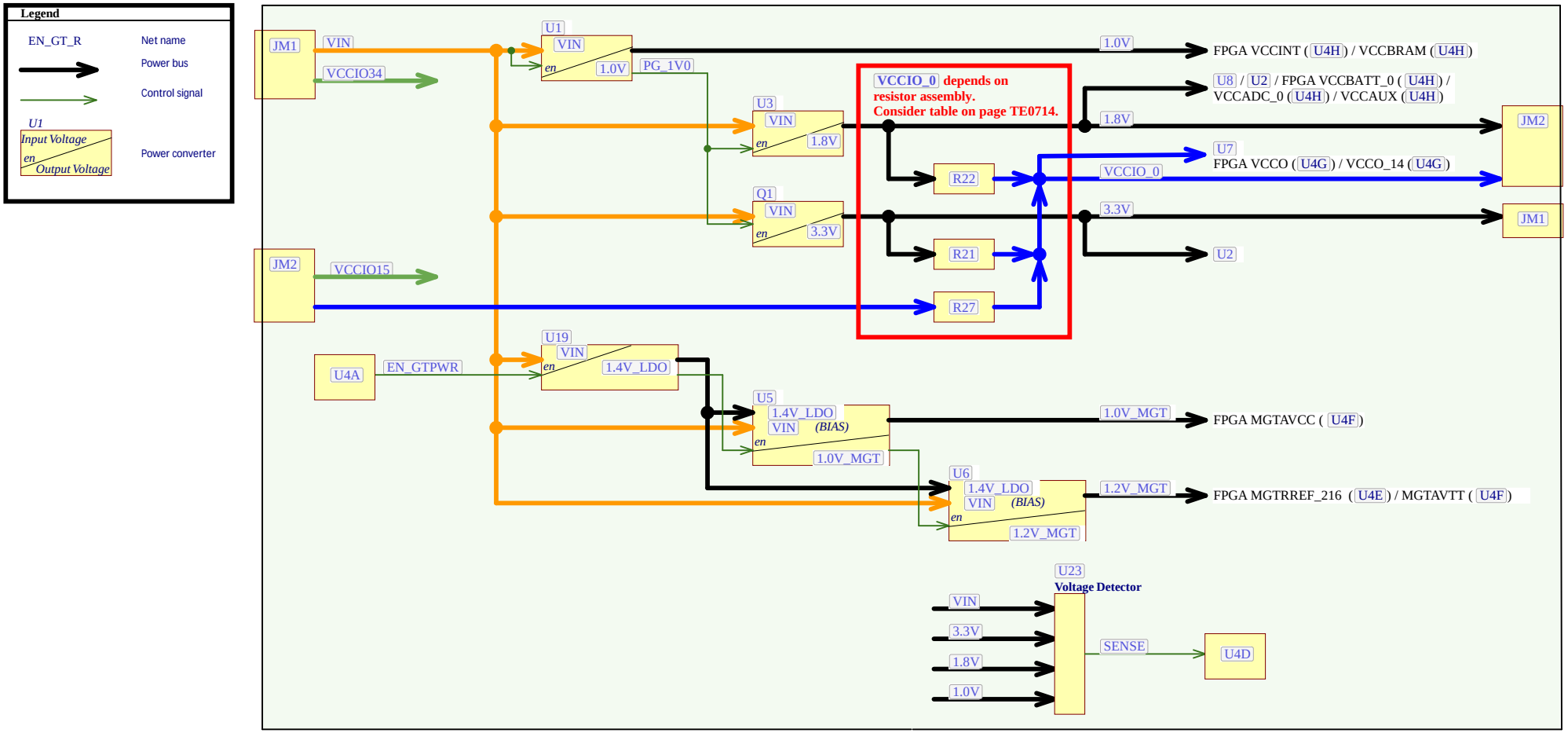
Filename: FPGA_MISC.SchDoc



Recommended Operating Conditions

Power Rail	Direction	Range in V	Tolerance	Description	Note
VIN	IN	3.3	+/- 3 %	Micromodule Power	Mandatory
VCCIO_0	IN/OUT	1.8 - 3.3	+/- 3 %	HR IO Bank 0 and Bank 14	Mandatory. Depends on assembly option.
VCCIO15	IN	1.2 - 3.3	+/- 3 %	HR IO Bank 15	-
VCCIO34	IN	1.2 - 3.3	+/- 3 %	HR IO Bank 34	-
1.8V	OUT	1.8	+/- 3 %	For Carrier card Periphery	-
3.3V	OUT	3.3	+/- 3 %	For Carrier card Periphery	-

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Title: Power_Diagram		
A4	Number: TE0714 42I-7-C	Rev. 04
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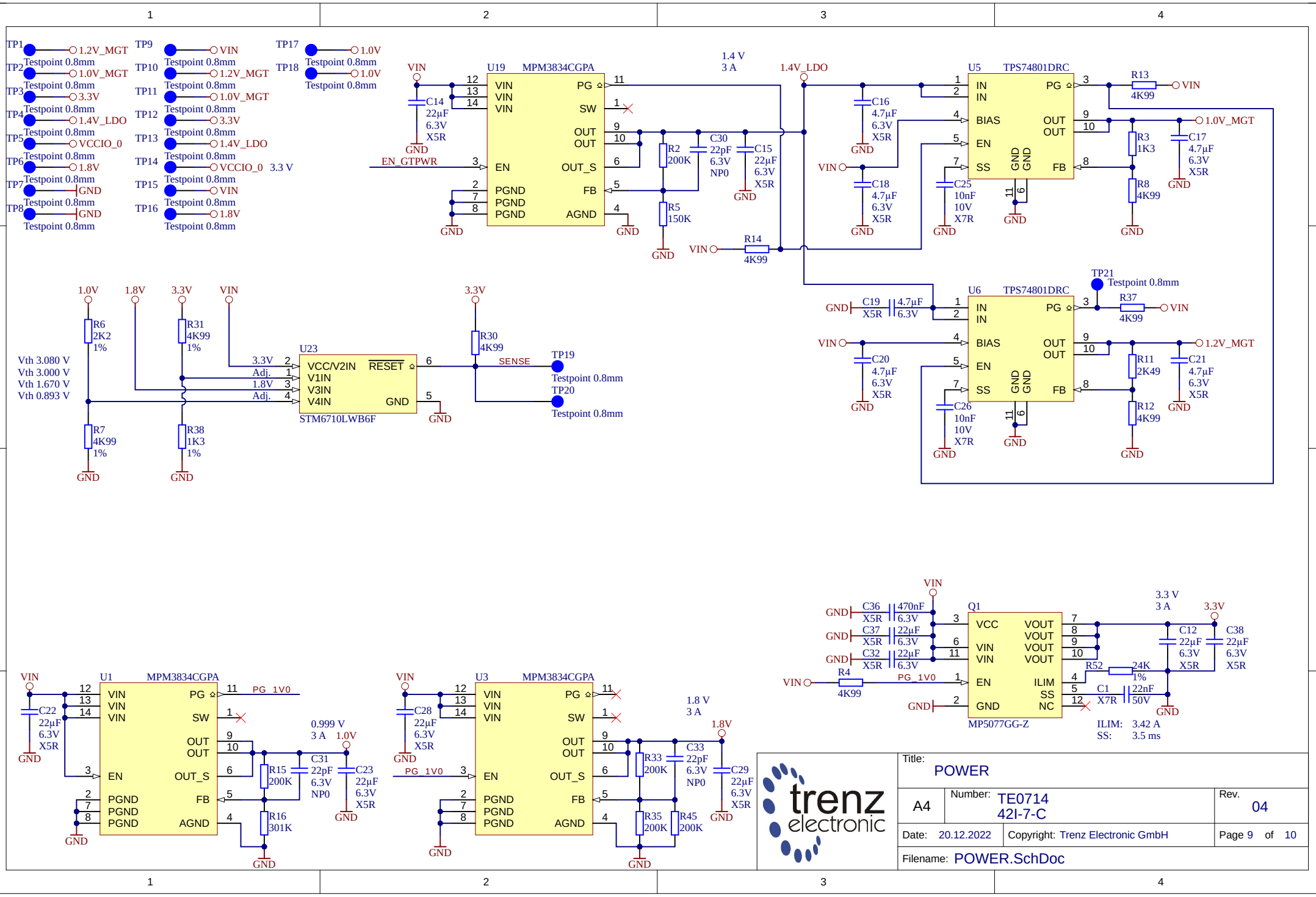
Filename: Power_Diagram.SchDoc		



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Title: POWER			
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Filename: POWER.SchDoc			

REVISION HISTORY

REV	Description	
-02	1) Added 0 ohm strap option to supply VCCIO0 on B2B connector 2) Added PCB Revision sense support. PCB Revision readout possible from HDL Design 3) Updated FPGA pin PROG_B connection. TPS3805H33 push-pull output RESET_N not affected on baseboard circuit, connected to PROG_B. 4) C8, C54, C56 updated to 100uF for variant 50-2I 5) Added testpoints	
-02A 12.2018	1) New FLASH memory U7 S25FL127SABMFV10	
-03	1) Changed obsolete component U3 (LXDC2HL18A-052 -> EP5357HUI) 2) DXP/DXN connected to GND (recommendation UG475, p31) 3) Added serial number to silk 4) Changed obsolet component Q1 (TPS27082LDDCR ->TPS27081ADDCR) 5) Full update LIB 6) Optimized testpoints placement 2022-04-08: 7) VY: traceability pad S/N replaced by Resistor 0R	
-04	1) Removed serial number S/N and use FPGA U4 pin R6 for PCB REV identification. 2) Changed inductors from BKP0603HS121-T to MPZ0603S121HT000 for L1, L2, L10, and L11. 3) Changed DCDCs from TPS82085SIL to MPM3834CGPA-Z for U1 and U19. 4) Changed DCDC from EP5357HUI to MPM3834CGPA for U3. 5) Changed TPS27081ADDCR to MP5077GG-Z for Q1. 6) Added voltage translator for signal "EN_GTPWR" (U10, C34, R36, R46). 7) Added diode D2. 8) Changed voltage monitor TPS3805H33DCKR to STM6710LWB6F for U23 and added resistor R38. 9) Added UKCA and RoHS logo. 10) Added system overview, power diagram, and legal notices. 11) Added testpoints TP10...16 on top layer. 12) Added testpoints for 1.0V (TP17 and TP18) and for SENSE net (TP19 and TP20). 13) Changed power sequence for U5 and U6. 14) Changed voltage rail 1.35V_LDO to 1.4V_LDO and increased voltage accodingly. 15) Inserted PCB revision connections: - PCB REVID0 at FPGA U4 pin J6. - PCB REVID1 at FPGA U4 pin R6. - PCB REVID2 at FPGA U4 pin D10. - PCB REVID3 at FPGA U4 pin H14. 16) Updated decoupling capacitors (added C43...46, C53, C60). 17) Added pull-up resistor R37 and testpoint TP21 for DCDC U6 PG pin. 18) Updated components from library.	ED

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Title: Revision Changes		
A4	Number: TE0714 42I-7-C	Rev. 04
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Filename: Revision Changes.SchDoc		