

Regarding the usage of our schematics and alike documentation for Trenz module TE0714.

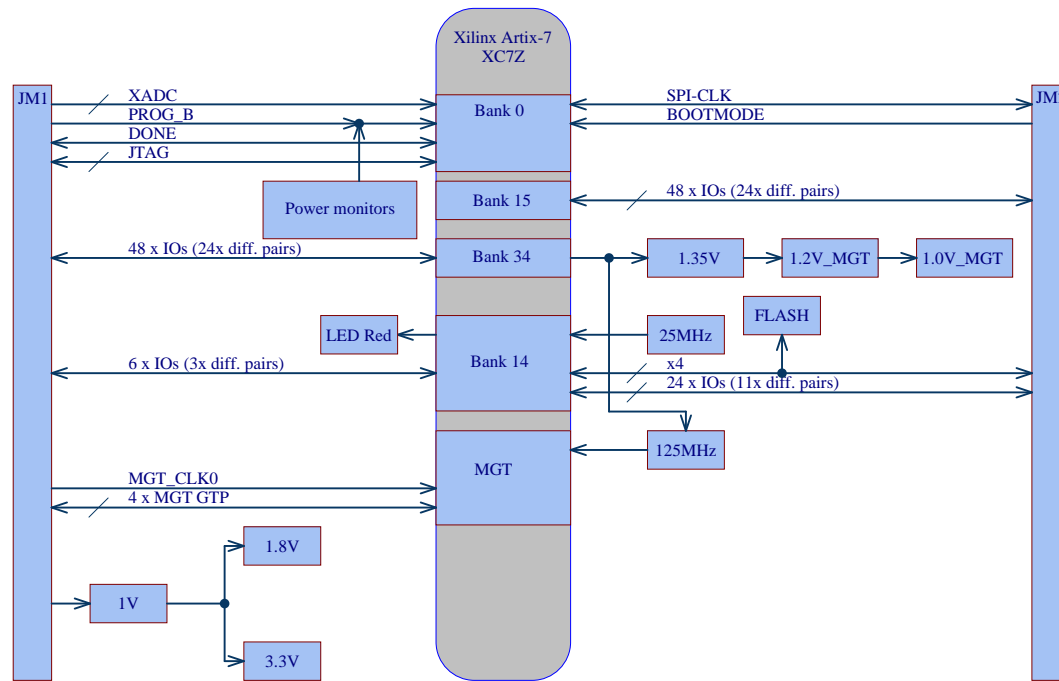
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Schematics and other handouts serve for informational purposes only!

| | |
|------------------|------------|
| Drawn by | ED |
| Checked by | VT |
| Assembly variant | 52I-8-A |
| Created by | ED |
| Modified by | ED |
| Modified at | 2022-12-07 |



| | | |
|---|---|----------------------------|
| Title: Legal Notices Modules | | |
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PCB Revision

| Revision | PCB REVID 3 | PCB REVID 2 | PCB REVID 1 | PCB REVID 0 |
|----------|-------------|-------------|-------------|-------------|
| REV03 | N/A | N/A | N/A | GND |
| REV04 | GND | VCCIO15 | GND | GND |

VCCIO_0 Power Function

| *JM2 pin 54 function | R21 | R22 | R24 | R25 | R27 |
|-----------------------|-----|-----|-----|-----|-----|
| 3.3V Power OUTPUT | + | - | + | - | + |
| 1.8V Power OUTPUT | - | + | - | + | + |
| 2.5V/3.3V Power Input | - | - | + | - | + |
| 1.8V Power Input | - | - | - | + | + |
| Not connected | X | X | X | X | - |

Legend: + = Assembled; - = Not assembled; X = Do not care;

Bootmode

| BOOTMODE | Bootmode |
|--------------|-----------------|
| 0 | SLAVE_SELECTMAP |
| 1 / Floating | MASTER_SPI |

U_Legal Notices Modules

U_TE0714

U_Power_Diagram

U_Revision Changes

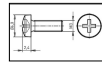


| | | |
|----------------------------------|-----------------------------------|----------------|
| Title: Overview | | |
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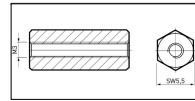
Special notes:

-
-

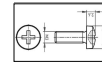
Top of Board



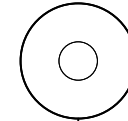
Screw M3x4



Standoff M3x8 II



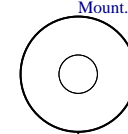
Screw M3x6



Mount.Hole 3.2mm



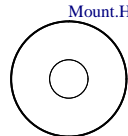
GND



Mount.Hole 3.2mm



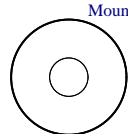
GND



Mount.Hole 3.2mm



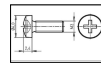
GND



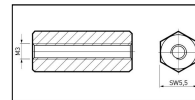
Mount.Hole 3.2mm



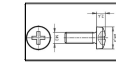
GND



Screw M3x4



Standoff M3x8 II



Screw M3x6

Serial
Serial
SerialNumber 6,3 x 6.3mm
LOGO2

CE Logo on Top Overlay

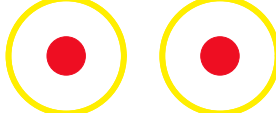
CE-TOPOVERLAY
LOGO3

UKCA Logo on Top Overlay

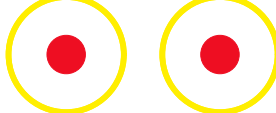
UKCA-TOPOVERLAY
LOGO4

TE Address Overlay

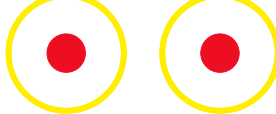
ADDRESS
PM1 PM2



FIDU-DOT - mini
PM3 PM4



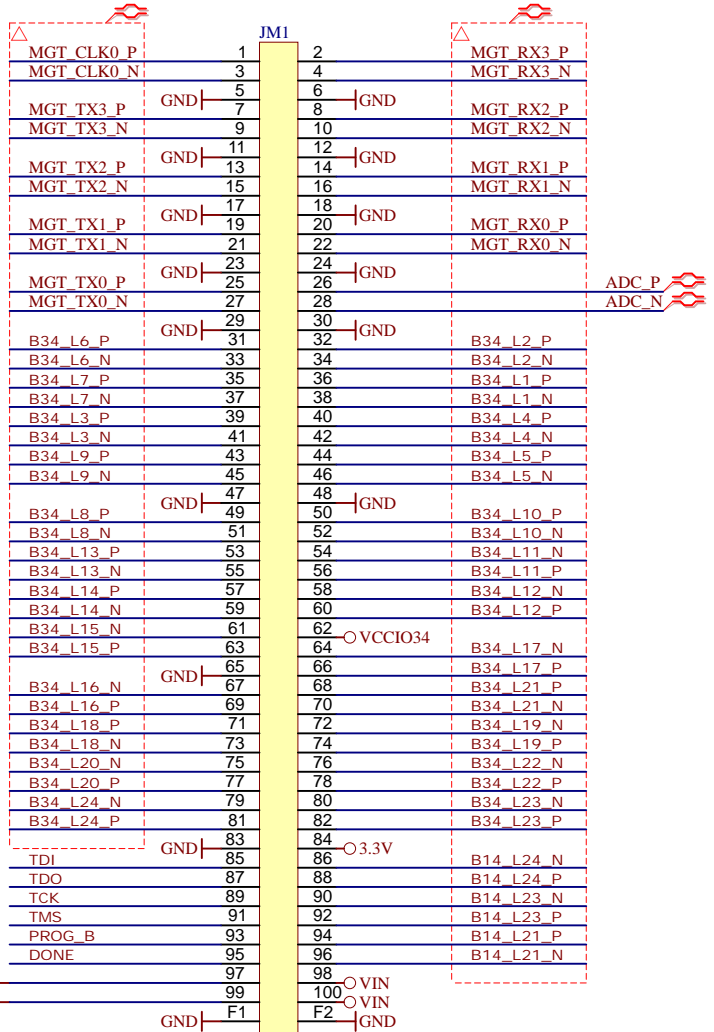
FIDU-DOT - mini
PM5 PM6



FIDU-DOT - mini
FIDU-DOT - mini



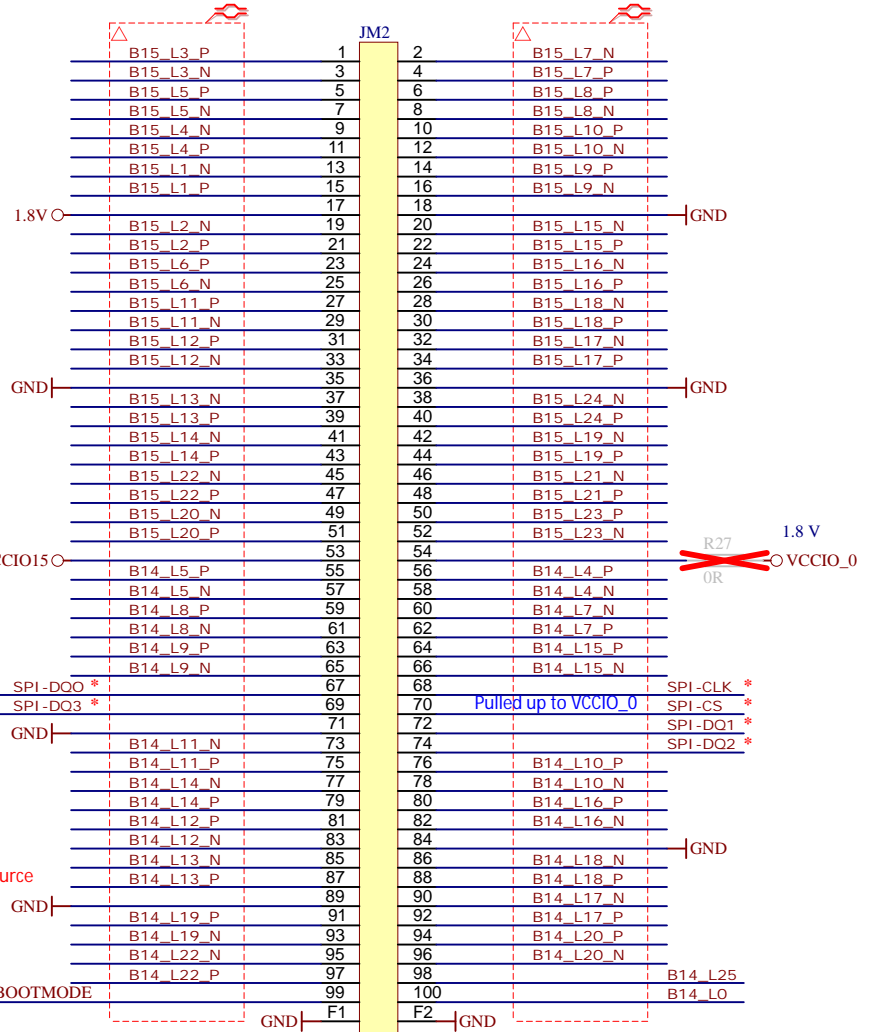
| | | |
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| Title: TE0714 | | |
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LSHM-150-04.0-L-DV-A-S-K-TR

Pulled up to VCCIO_0
Pulled up to VCCIO_0

* B2B IOs SPI-xx are shared with FLASH and can not be used as normal IOs.



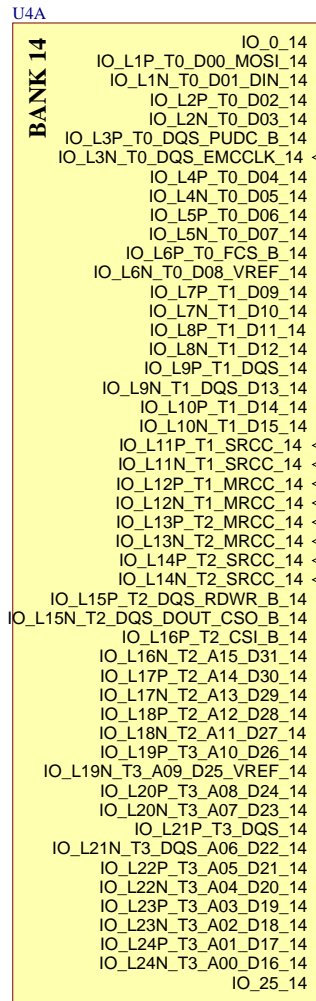
LSHM-150-04.0-L-DV-A-S-K-TR

Pulled up to VCCIO_0

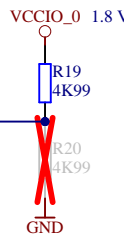
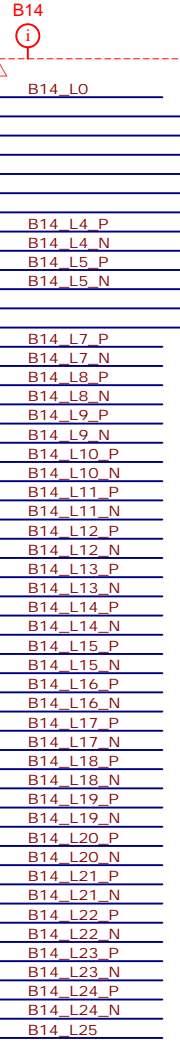
25MHz clock source



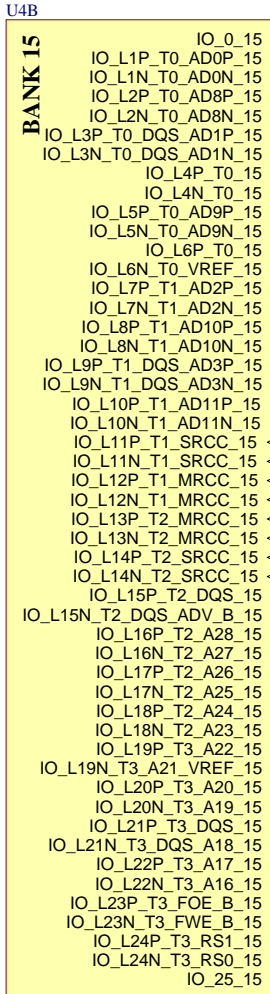
| | | |
|--------------------------------|----------------------------------|--------------|
| Title: B2B_Connector | | |
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XC7A50T-2CSG325I



U4B



XC7A50T-2CSG325I

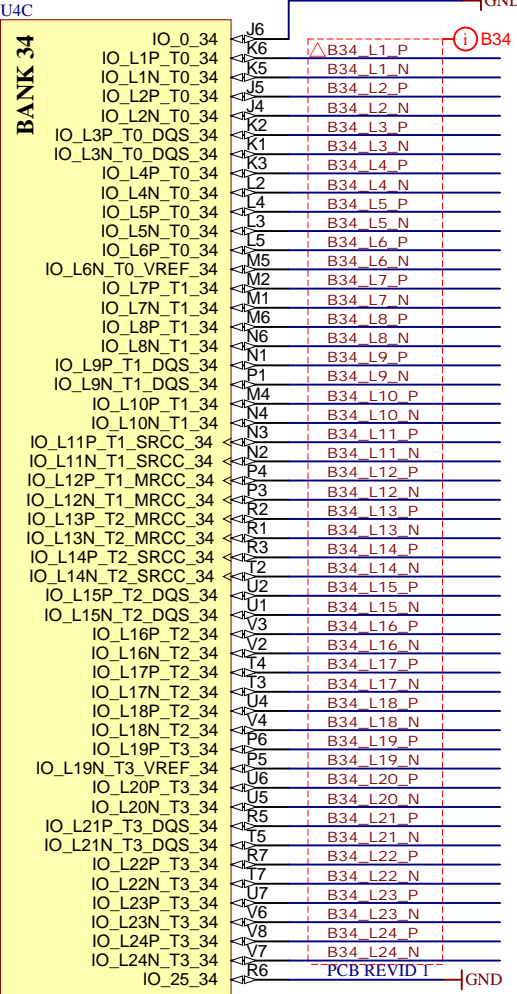
PCB REVID 2

VCCIO15



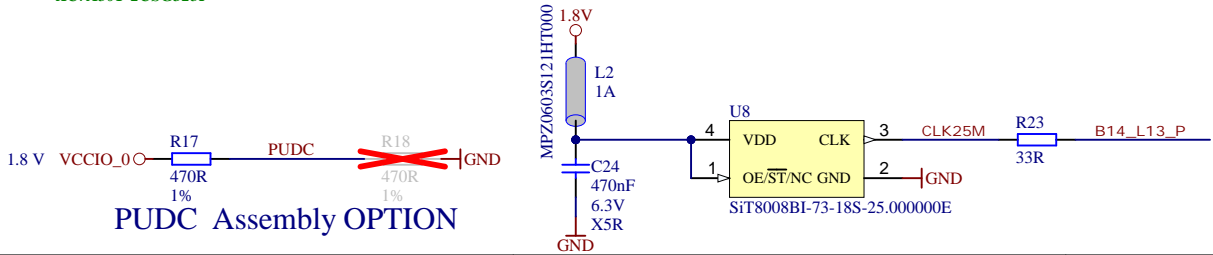
PCB REVID 3

U4C

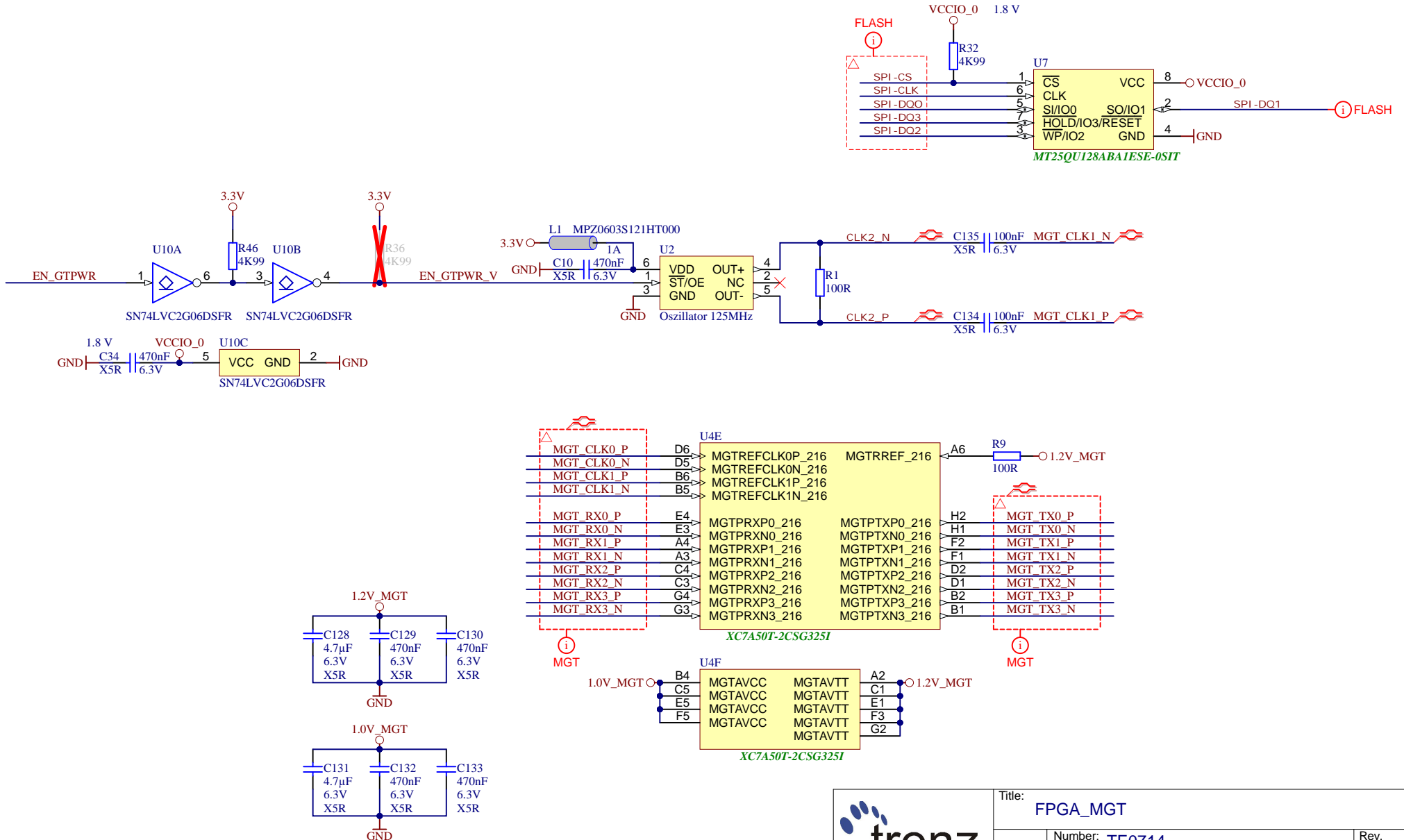


XC7A50T-2CSG325I

PCB REVID 0



| | | |
|---------------------------------|---|----------------------------|
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| | | |
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1

2

3

4

A

A

B

B

C

C

D

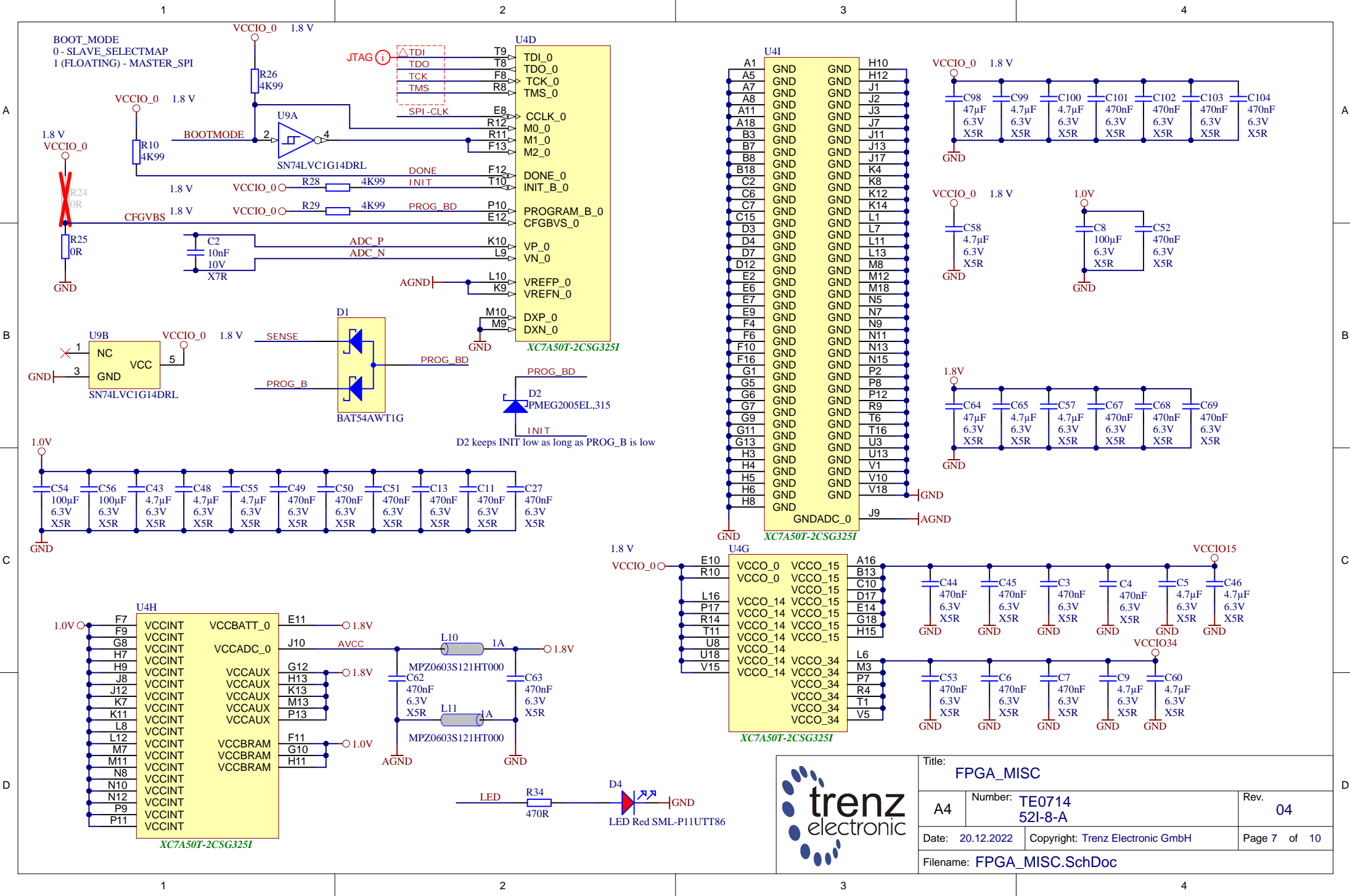
D

1

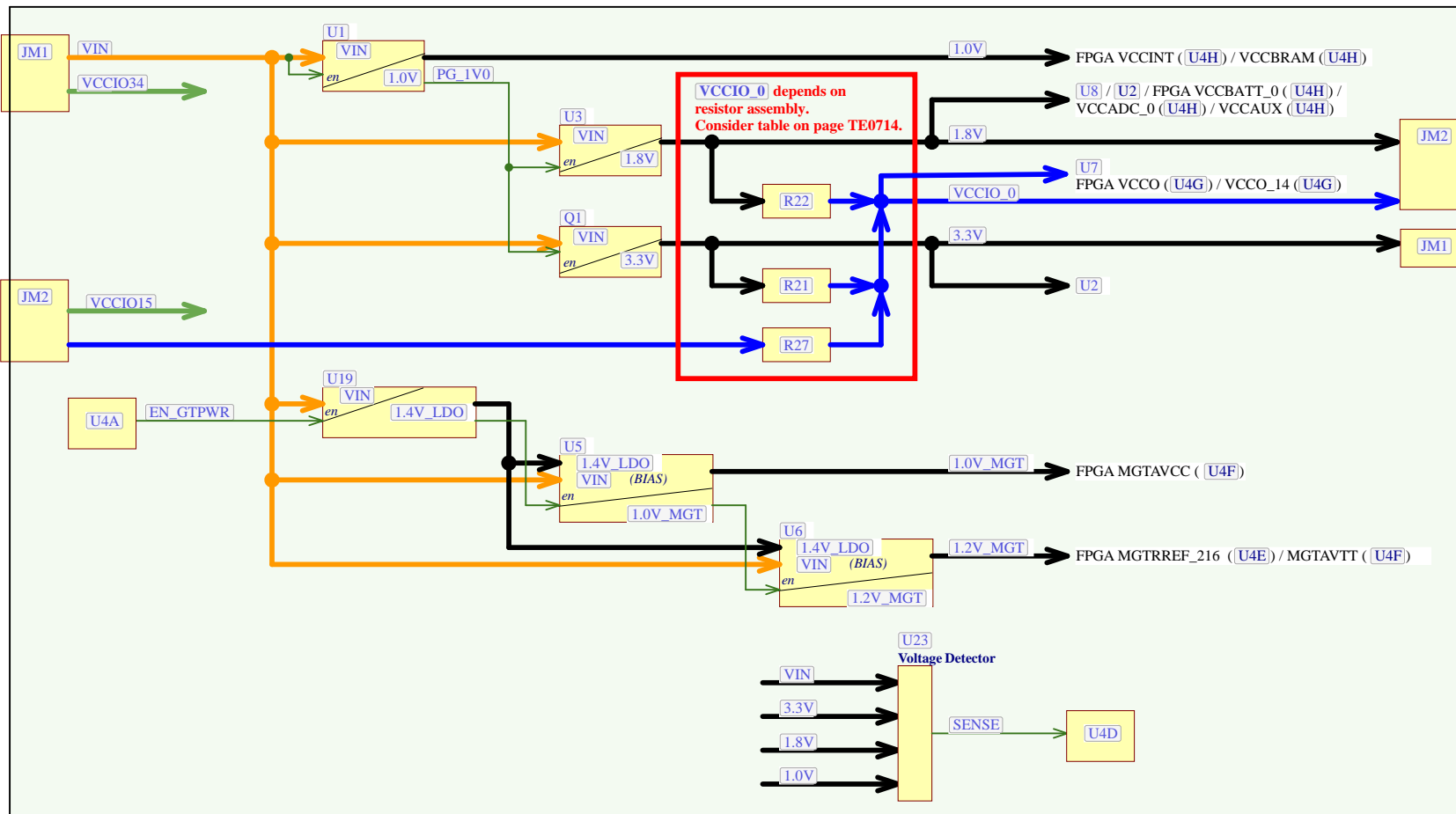
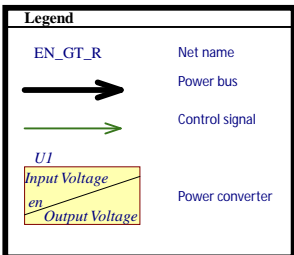
2

3

4



| | | |
|-----------------------------------|---|----------------------------|
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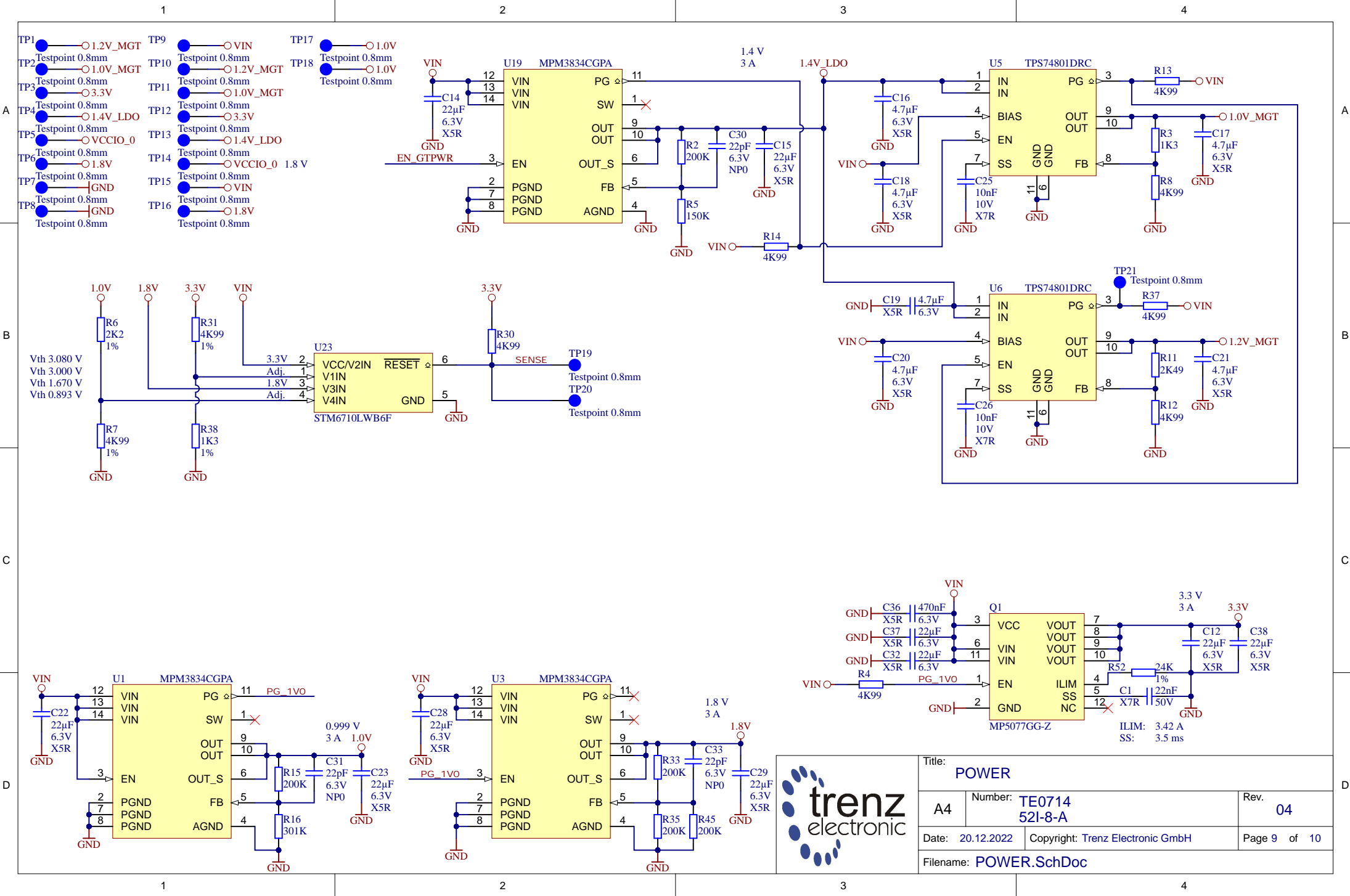


Recommended Operating Conditions

| Power Rail | Direction | Range in V | Tolerance | Description | Note |
|------------|-----------|------------|-----------|----------------------------|--|
| VIN | IN | 3.3 | +/- 3 % | Micromodule Power | Mandatory |
| VCCIO_0 | IN/OUT | 1.8 - 3.3 | +/- 3 % | HR IO Bank 0 and Bank 14 | Mandatory. Depends on assembly option. |
| VCCIO15 | IN | 1.2 - 3.3 | +/- 3 % | HR IO Bank 15 | - |
| VCCIO34 | IN | 1.2 - 3.3 | +/- 3 % | HR IO Bank 34 | - |
| 1.8V | OUT | 1.8 | +/- 3 % | For Carrier card Periphery | - |
| 3.3V | OUT | 3.3 | +/- 3 % | For Carrier card Periphery | - |



| | | |
|--------------------------------|----------------------------------|--------------|
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- TP1 Testpoint 0.8mm 1.2V_MGT
- TP2 Testpoint 0.8mm 1.0V_MGT
- TP3 Testpoint 0.8mm 3.3V
- TP4 Testpoint 0.8mm 1.4V_LDO
- TP5 Testpoint 0.8mm VCCIO_0
- TP6 Testpoint 0.8mm 1.8V
- TP7 Testpoint 0.8mm GND
- TP8 Testpoint 0.8mm GND
- TP9 Testpoint 0.8mm VIN
- TP10 Testpoint 0.8mm 1.2V_MGT
- TP11 Testpoint 0.8mm 1.0V_MGT
- TP12 Testpoint 0.8mm 3.3V
- TP13 Testpoint 0.8mm 1.4V_LDO
- TP14 Testpoint 0.8mm VCCIO_0 1.8 V
- TP15 Testpoint 0.8mm VIN
- TP16 Testpoint 0.8mm 1.8V
- TP17 Testpoint 0.8mm 1.0V
- TP18 Testpoint 0.8mm 1.0V

| | | |
|-------------------------------|-----------------------------------|----------------|
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REVISION HISTORY

| REV | Description | |
|-----------------|--|----|
| -02 | <ul style="list-style-type: none"> 1) Added 0 ohm strap option to supply VCCIO0 on B2B connector 2) Added PCB Revision sense support, PCB Revision readout possible from HDL Design 3) Updated FPGA pin PROG_B connection. TPS3805H33 push-pull output RESET_N not affected on baseboard circuit, connected to PROG_B. 4) C8, C54, C56 updated to 100uF for variant 50-2I 5) Added testpoints | |
| -02A 12.2018 | 1) New FLASH memory U7 S25FL127SABMFV10 | |
| -03 | <ul style="list-style-type: none"> 1) Changed obsolete component U3 (LXDC2HL18A-052 -> EP5357HUI) 2) DXP/DXN connected to GND (recommendation UG475, p31) 3) Added serial number to silk 4) Changed obsolete component Q1 (TPS27082LDDCR ->TPS27081ADDCR) 5) Full update LIB 6) Optimized testpoints placement <p>2022-04-08: 7) VY: traceability pad S/N replaced by Resistor 0R</p> | |
| -04 | <ul style="list-style-type: none"> 1) Removed serial number S/N and use FPGA U4 pin R6 for PCB REV identification. 2) Changed inductors from BKP0603HS121-T to MPZ0603S121HT000 for L1, L2, L10, and L11. 3) Changed DCDCs from TPS82085SIL to MPM3834CGPA-Z for U1 and U19. 4) Changed DCDC from EP5357HUI to MPM3834CGPA for U3. 5) Changed TPS27081ADDCR to MP5077GG-Z for Q1. 6) Added voltage translator for signal "EN_GTPWR" (U10, C34, R36, R46). 7) Added diode D2. 8) Changed voltage monitor TPS3805H33DCCR to STM6710LWB6F for U23 and added resistor R38. 9) Added UKCA and RoHS logo. 10) Added system overview, power diagram, and legal notices. 11) Added testpoints TP10...16 on top layer. 12) Added testpoints for 1.0V (TP17 and TP18) and for SENSE net (TP19 and TP20). 13) Changed power sequence for U5 and U6. 14) Changed voltage rail 1.35V_LDO to 1.4V_LDO and increased voltage accordingly. 15) Inserted PCB revision connections: <ul style="list-style-type: none"> - PCB REVID0 at FPGA U4 pin J6. - PCB REVID1 at FPGA U4 pin R6. - PCB REVID2 at FPGA U4 pin D10. - PCB REVID3 at FPGA U4 pin H14. 16) Updated decoupling capacitors (added C43...46, C53, C60). 17) Added pull-up resistor R37 and testpoint TP21 for DCDC U6 PG pin. 18) Updated components from library. | ED |

| | | | | |
|---|--|-----------------------------------|----------------------------------|---------------|
|  | | Title: Revision Changes | | |
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