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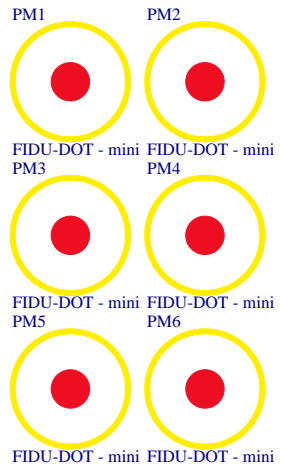
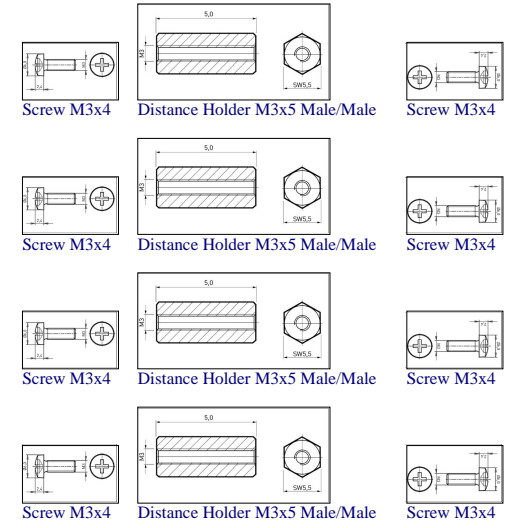
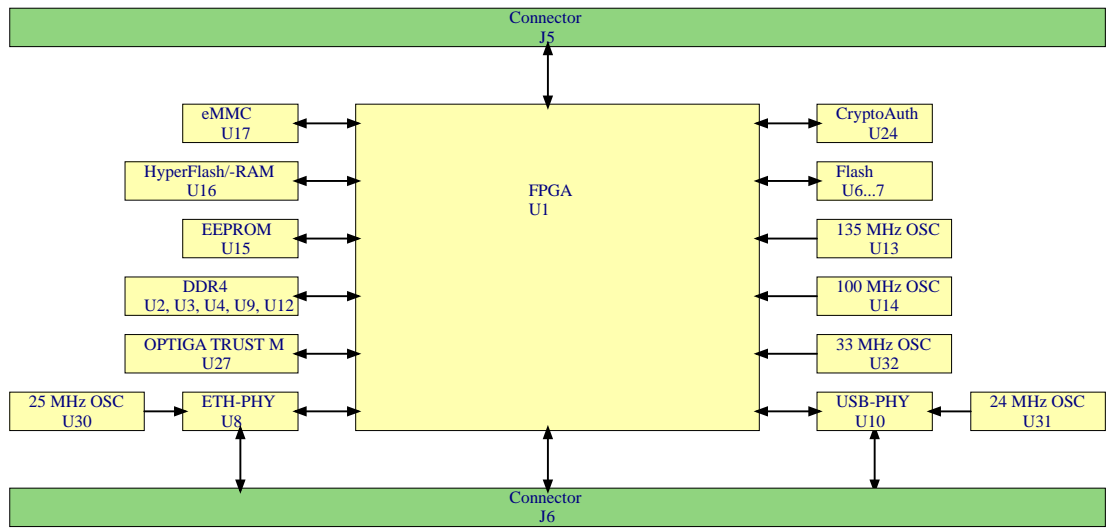
Schematics and other handouts serve for informational purposes only!

	Title: AM0010 – Legal Notices Modules		
	A4	Number: Legal Notices Modules 2AE21MA	Rev. 02
	Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 1 of 30
	Filename: Legal Notices Modules.SchDoc		

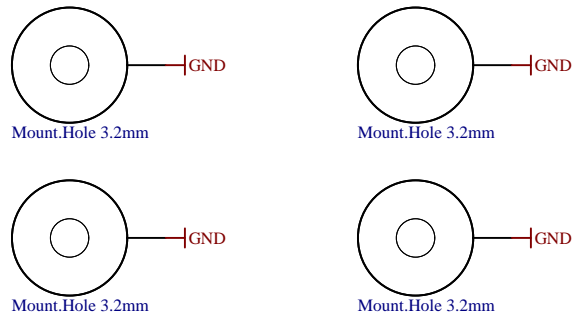
- U_B2B_Connector_1
B2B_Connector_1.SchDoc
- U_B2B_Connector_2
B2B_Connector_2.SchDoc
- U_MPSoC
MPSoC.SchDoc
- U_DDR4-RAM
DDR4-RAM.SchDoc
- U_DDR4-RAM_2
DDR4-RAM_2.SchDoc
- U_DDR4-RAM_3
DDR4-RAM_3.SchDoc
- U_DDR4-RAM_4
DDR4-RAM_4.SchDoc
- U_DDR4-RAM_5
DDR4-RAM_5.SchDoc
- U_DDR4-CAPS
DDR4-CAPS.SchDoc
- U_DDR4-TERM
DDR4-TERM.SchDoc
- U_ETHPHY
ETHPHY.SchDoc
- U_USBPHY
USBPHY.SchDoc
- U_eMMC
eMMC.SchDoc
- U_MISC
MISC.SchDoc

- U_POWER_1
POWER_1.SchDoc
- U_POWER_2
POWER_2.SchDoc
- U_REV_CH
Revision_Changes.SchDoc
- U_Legal_Notices_Modules
Legal_Notices_Modules.SchDoc

Special notes:



Serial
Serialnumber 6,3 x 6.3mm



UKCA
UKCA Logo on Top Overlay
UKCA-TOPOVERLAY



Assembly variant	2AE21MA
Created by	ED
Modified by	ED
Modified at	02.07.21
SVN Revision	

Title: AM0010		
A4	Number: AM0010 2AE21MA	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 2 of 30
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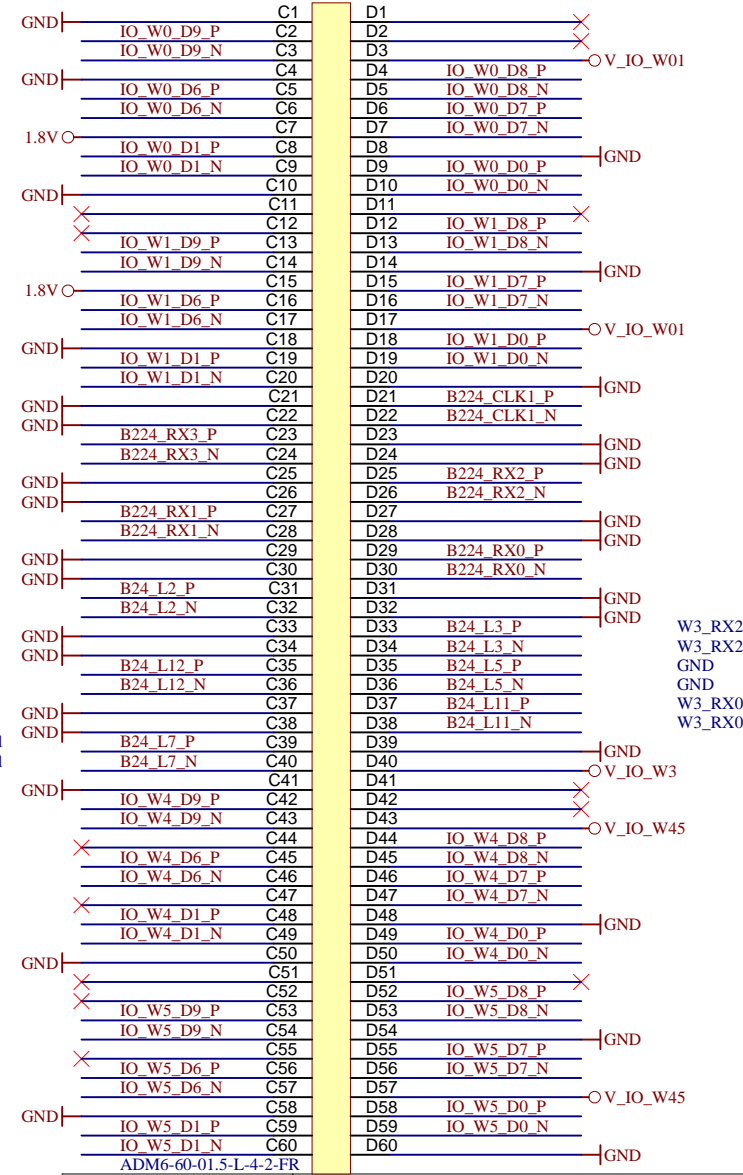
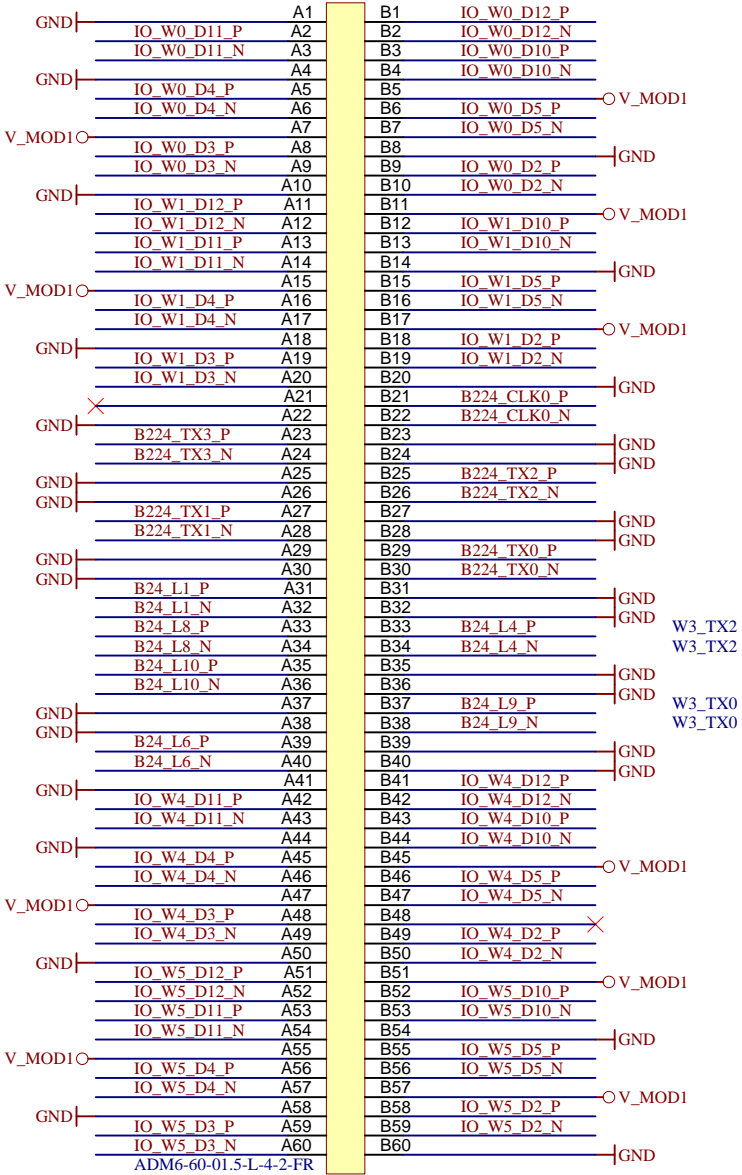
D

D

Connector W

J5A

J5B



W3_TX3
W3_TX3
GND
W3_TX1
W3_TX1

W3_CLK0
W3_CLK0

W3_TX2
W3_TX2

W3_TX0
W3_TX0

W3_RX3
W3_RX3

W3_RX1
W3_RX1

W3_CLK1
W3_CLK1

W3_RX2
W3_RX2
GND
W3_RX0
W3_RX0



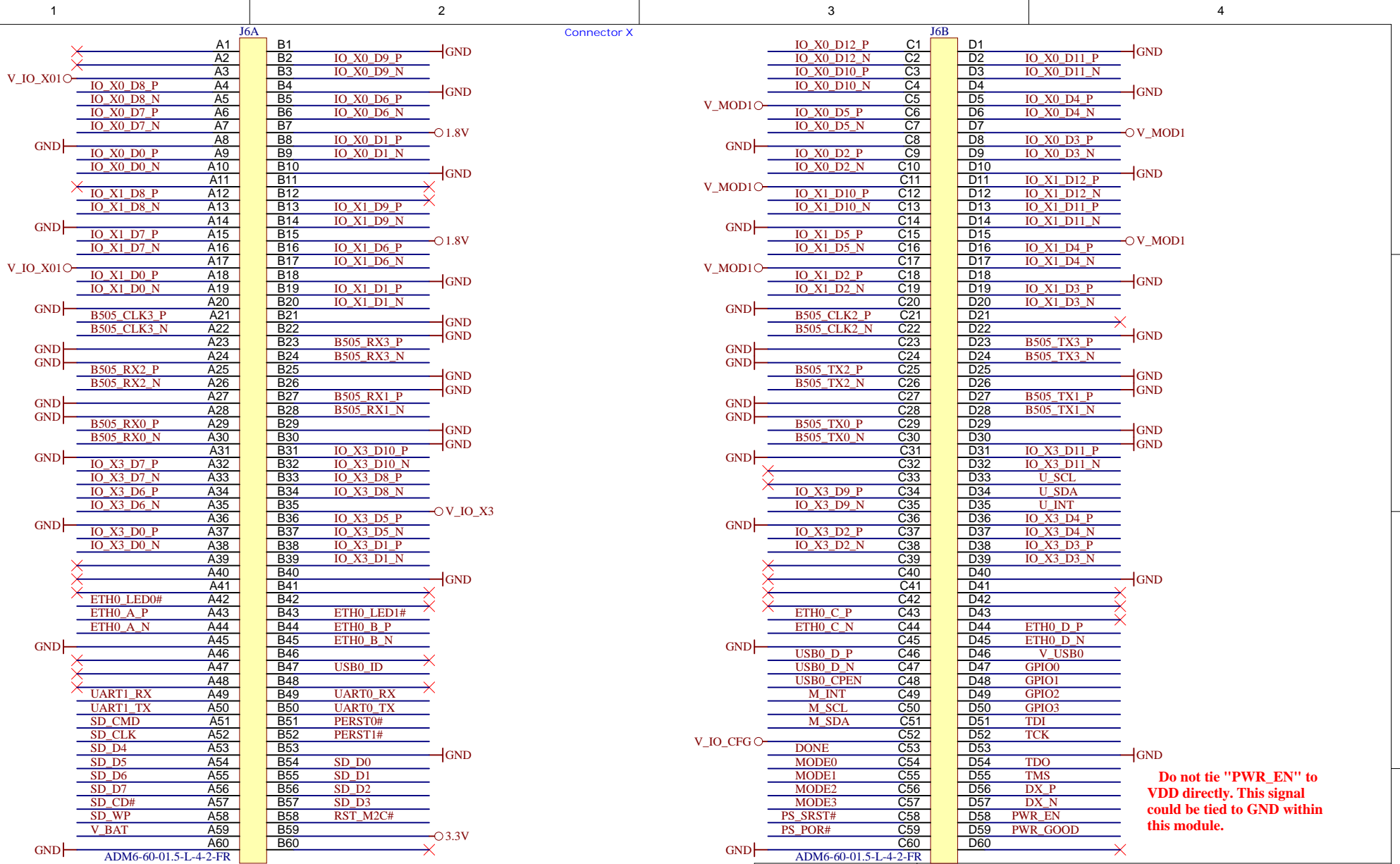
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Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 3 of 30
Filename: B2B_Connector_1.SchDoc		

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Do not tie "PWR_EN" to VDD directly. This signal could be tied to GND within this module.



Title: AM0010 – B2B_Connector_2		
A4	Number: B2B_Connector_2 2AE21MA	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 4 of 30
Filename: B2B_Connector_2.SchDoc		

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A

A

- U_B64
B64.SchDoc
- U_B65
B65.SchDoc
- U_B66
B66.SchDoc
- U_B_HD
B_HD.SchDoc
- U_B_MIO
B_MIO.SchDoc
- U_PS_DDR
PS_DDR.SchDoc
- U_B_PS_GT
B_PS_GT.SchDoc
- U_B_GT
B_GT.SchDoc
- U_CONFIG
CONFIG.SchDoc
- U_ZU_POWER
ZU_POWER.SchDoc
- U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

B

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D


D

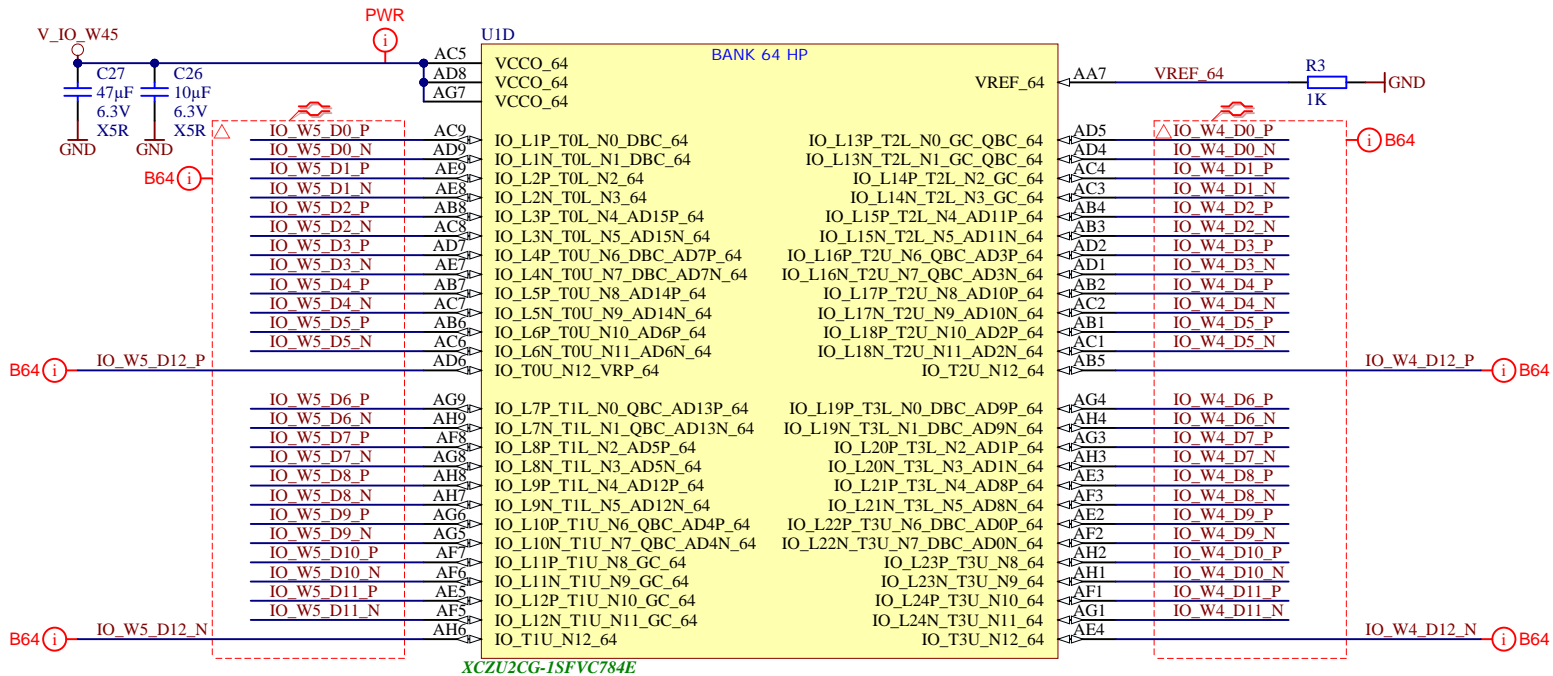
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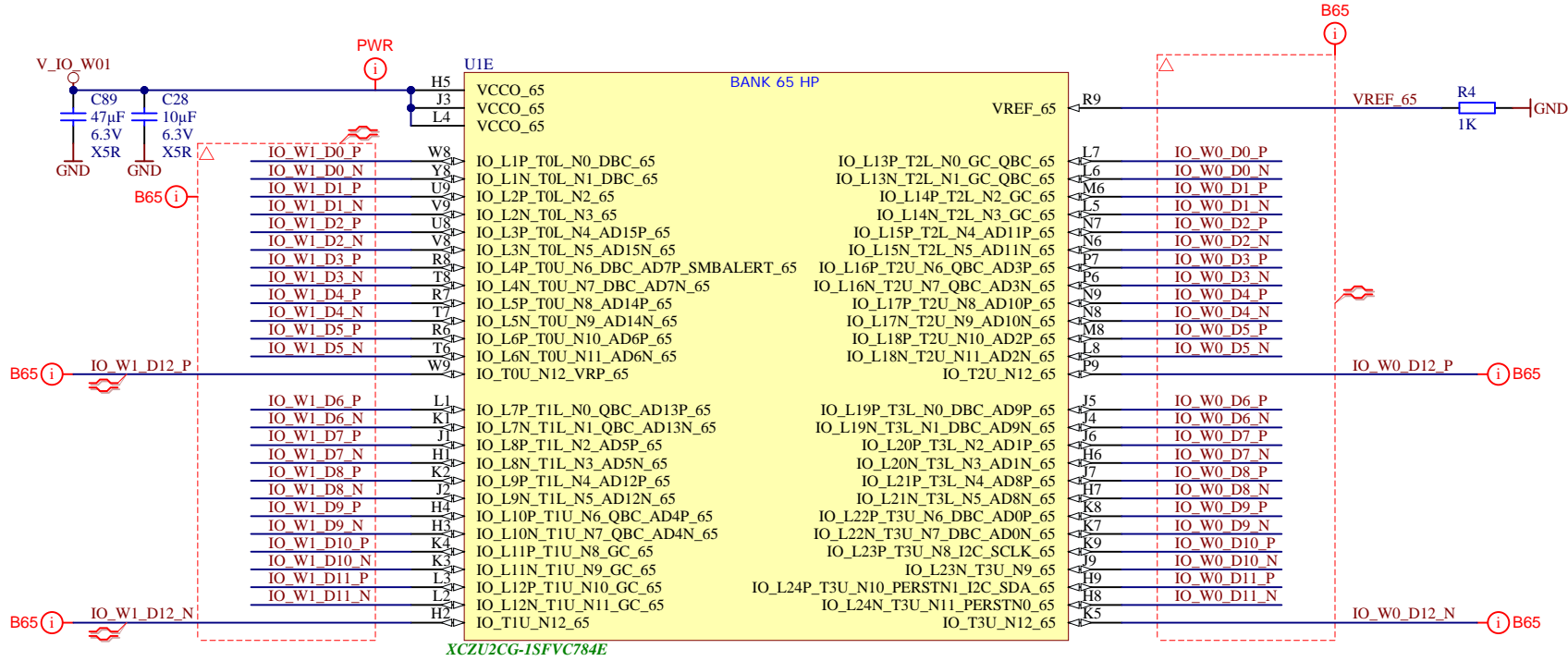
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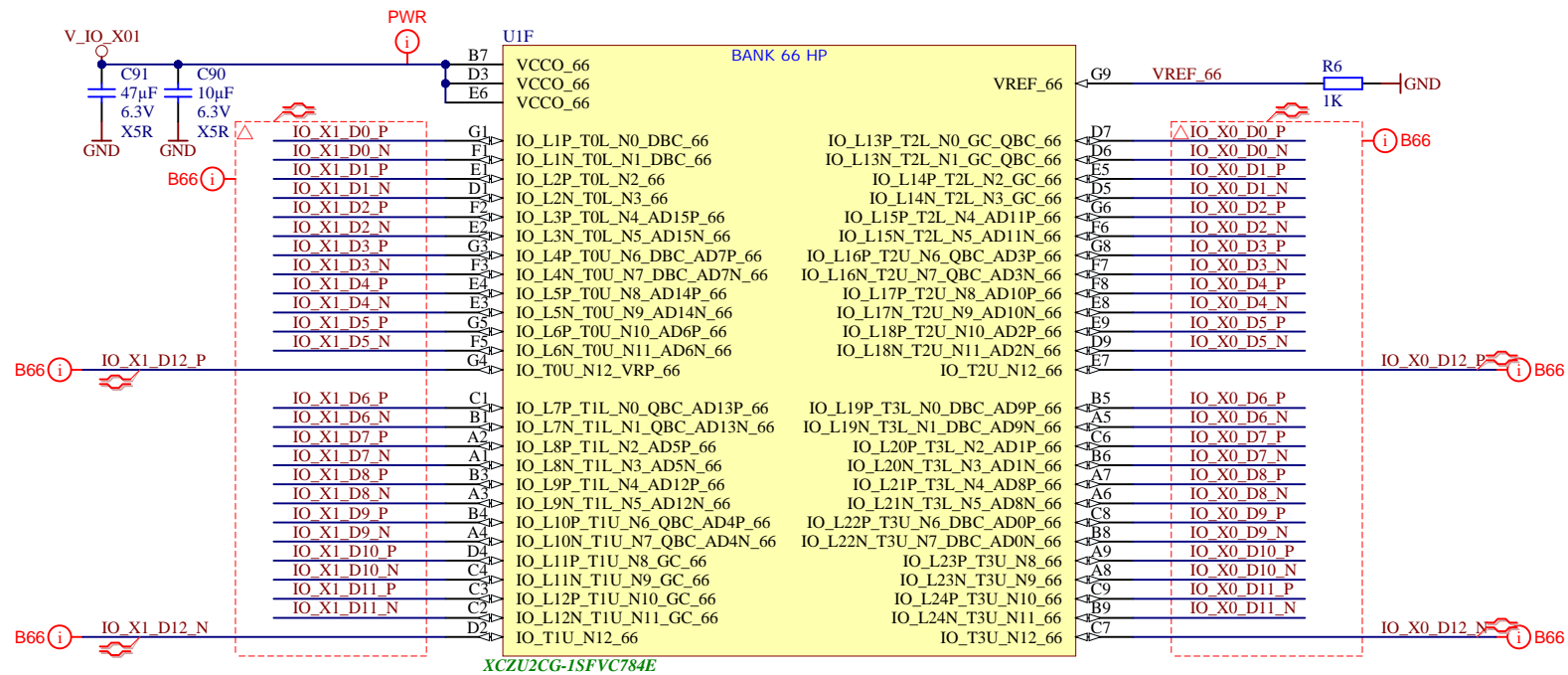
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	Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 5 of 30
	Filename: MPSoC.SchDoc		




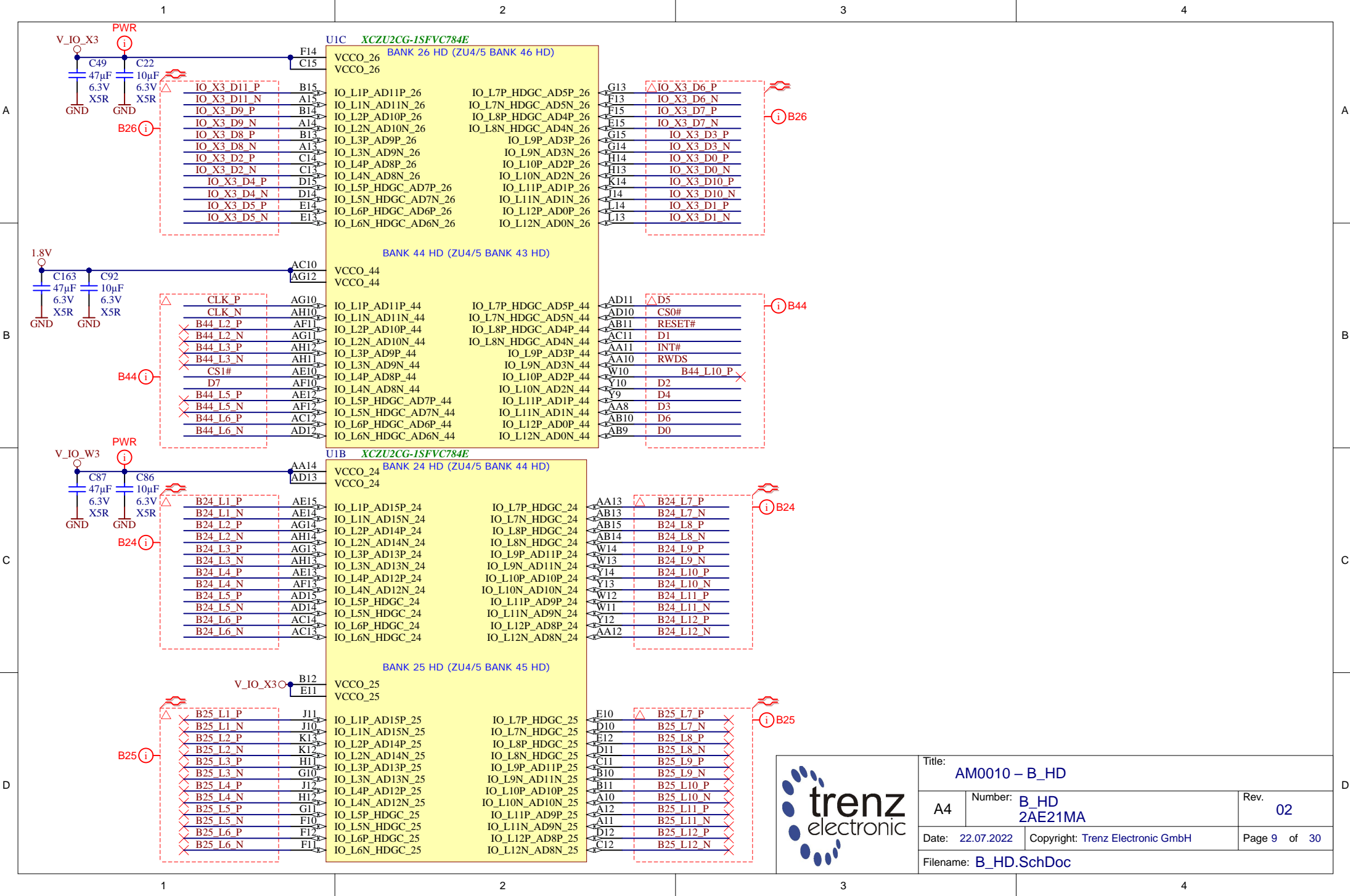
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Filename: B64.SchDoc		



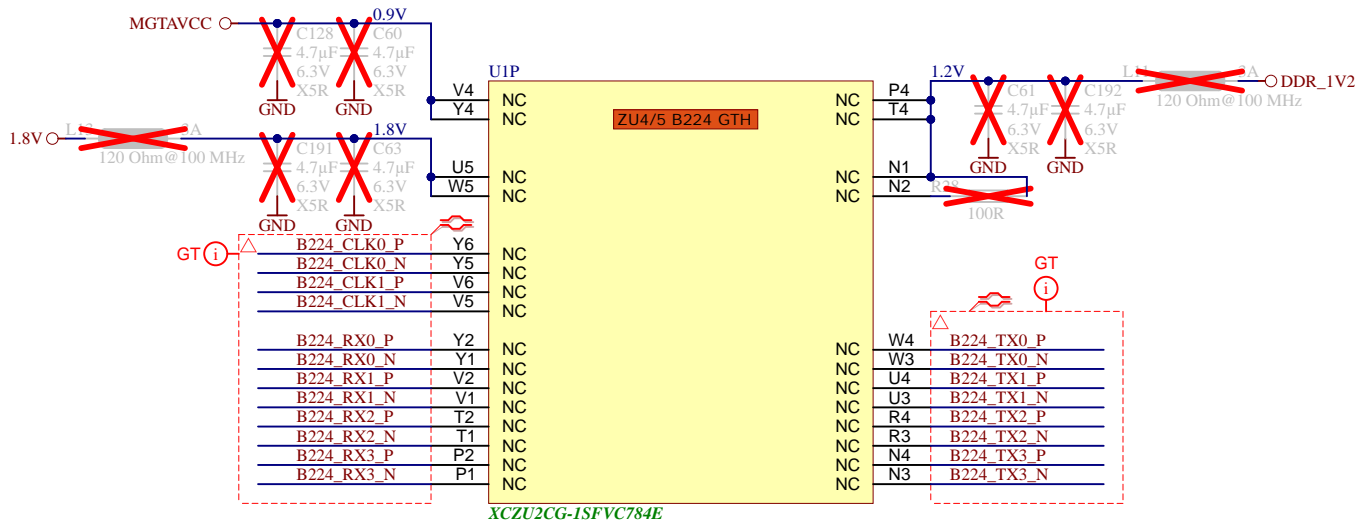
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Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 7 of 30
Filename: B65.SchDoc		



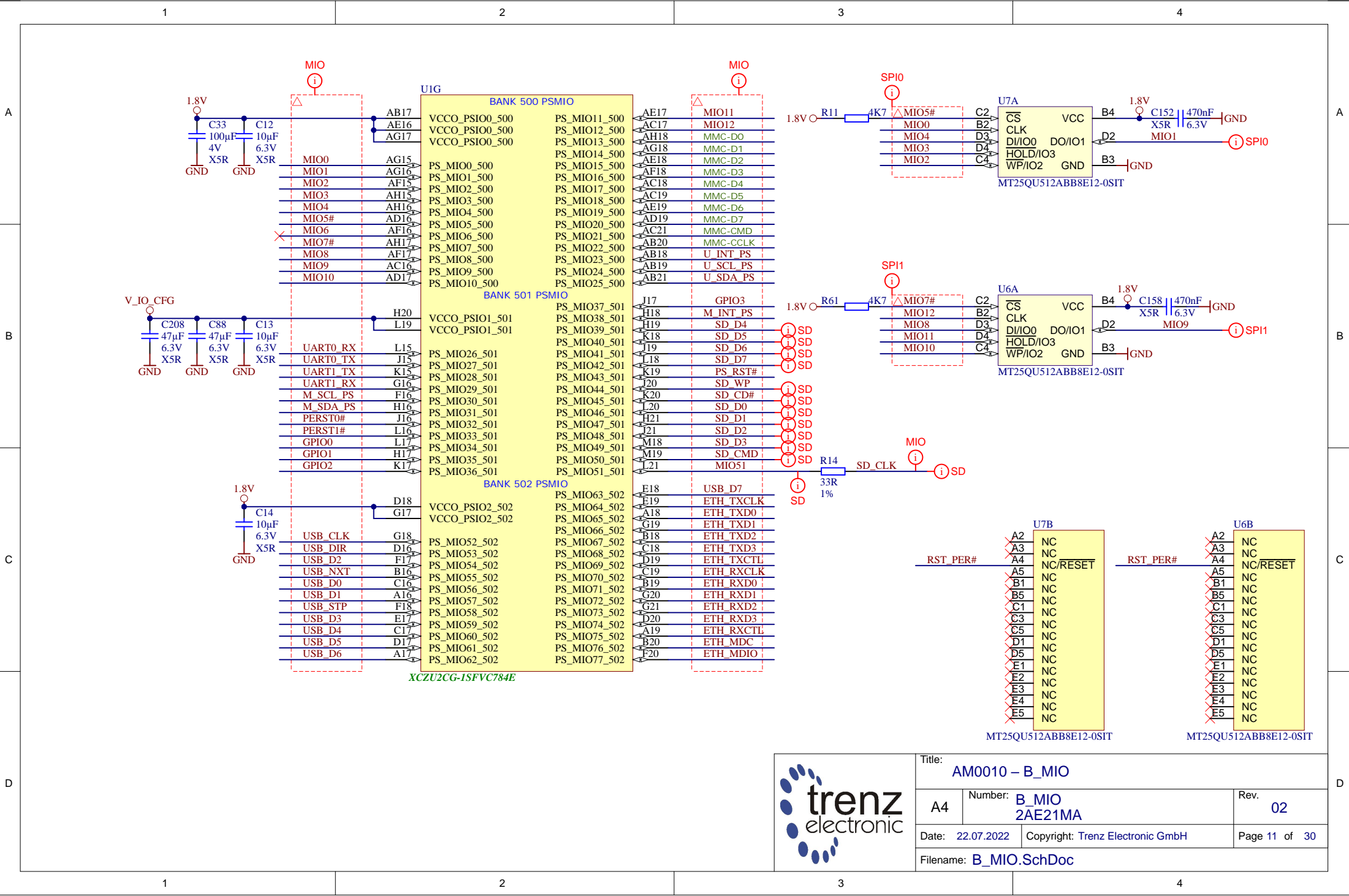
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			A4	Number: B66 2AE21MA
Date: 22.07.2022		Copyright: Trenz Electronic GmbH		Page 8 of 30
Filename: B66.SchDoc				



Title: AM0010 - B_HD		
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Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 9 of 30
Filename: B_HD.SchDoc		

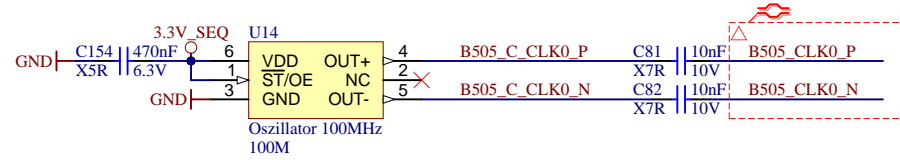
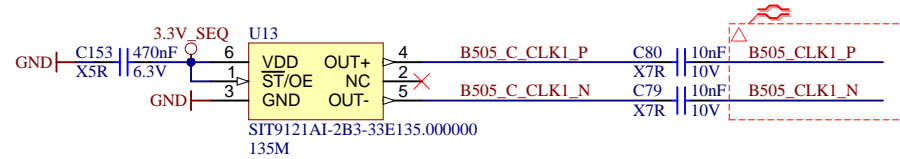
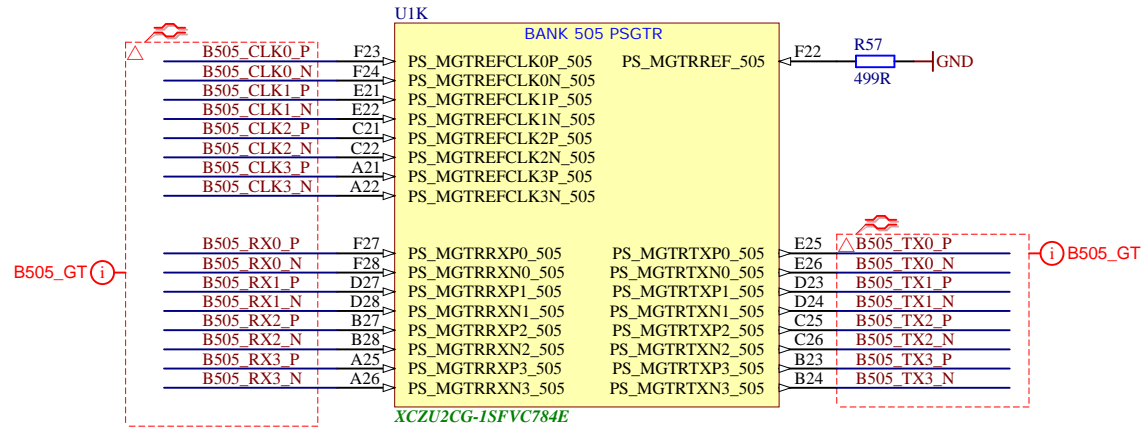


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Filename: B_GT.SchDoc		

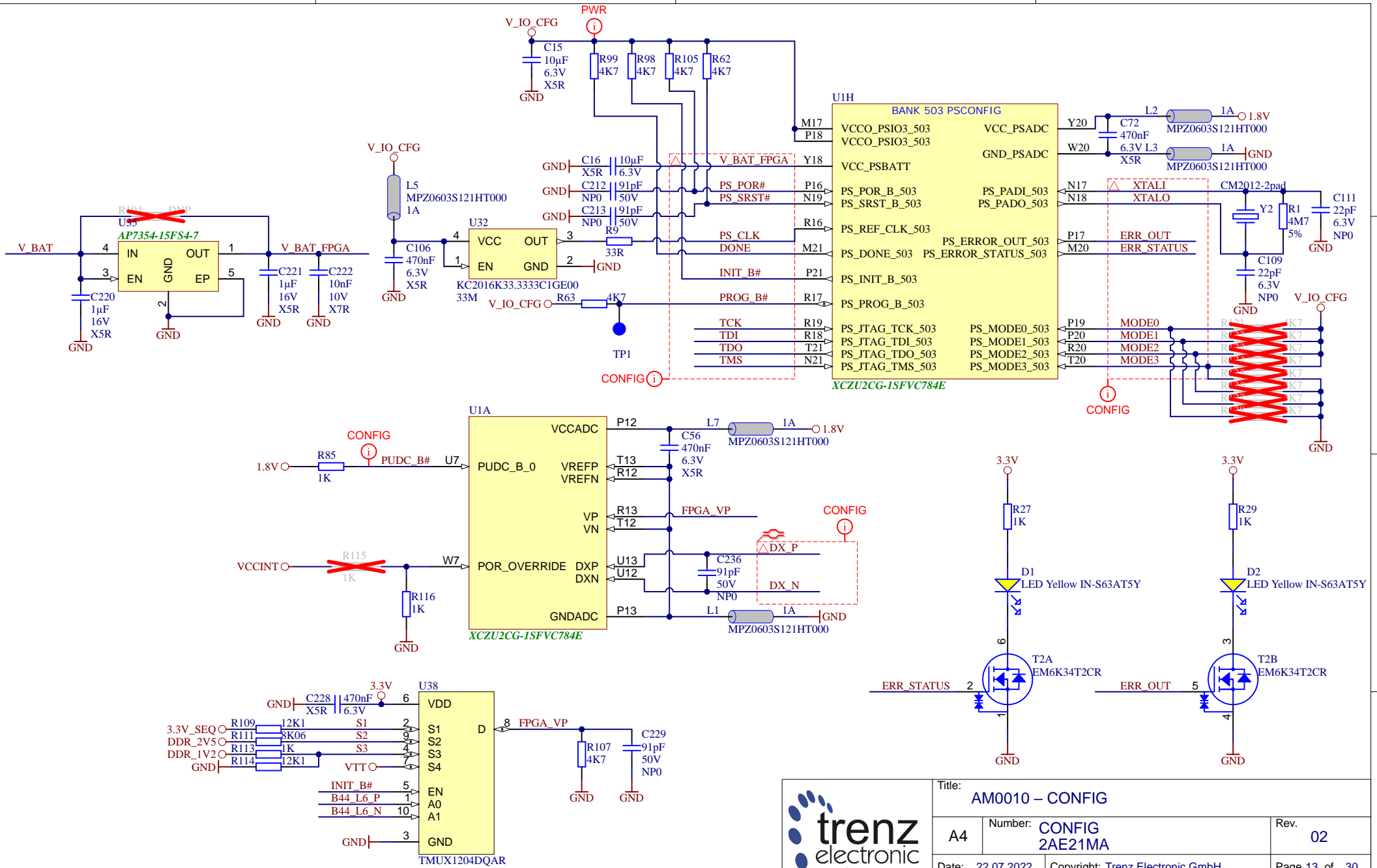


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	A4	Number: B_MIO 2AE21MA
	Date: 22.07.2022	Copyright: Trenz Electronic GmbH
	Filename: B_MIO.SchDoc	

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	Title: AM0010 - B_PS_GT		
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Title: AM0010 – CONFIG		
A4	Number: CONFIG 2AE21MA	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 13 of 30
Filename: CONFIG.SchDoc		

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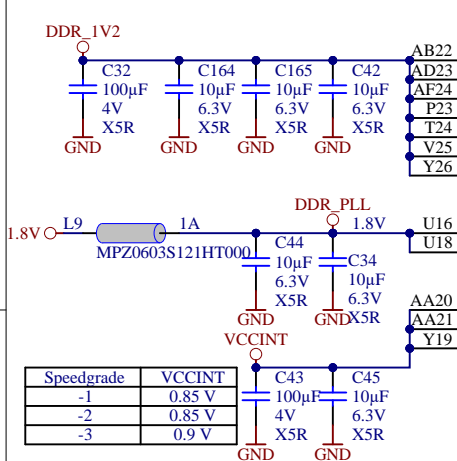
B

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D

D



U11 BANK 504 PSDDR		U1J BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	Y27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AA22	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AB23	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AA25	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AA26	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AB25	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AB26	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AB24	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AC24	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AC23	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504	AC22	DDR4-A17
PS_DDR_CS_N0_504	PS_DDR_CS_N1_504	W27	DDR4-CS#
PS_DDR_CS_N0_504	PS_DDR_CS_N1_504	V26	
PS_DDR_BA0_504	PS_DDR_BA1_504	V23	DDR4-BA0
PS_DDR_BA0_504	PS_DDR_BA1_504	W22	DDR4-BA1
PS_DDR_BG0_504	PS_DDR_BG1_504	W24	DDR4-BG0
PS_DDR_BG0_504	PS_DDR_BG1_504	V22	DDR4-BG1
PS_DDR_PARITY_504	PS_DDR_RAM_RST_N_504	V24	DDR4-PAR
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	U23	DDR4-RESET#
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	Y23	DDR4-ACT#
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	U25	DDR4-ALERT#
PS_DDR_ZQ_504	PS_DDR_ODT0_504	U24	DDR4-ZQ
PS_DDR_ODT0_504	PS_DDR_ODT1_504	U28	DDR4-ODT0
PS_DDR_ODT0_504	PS_DDR_ODT1_504	U26	

XCZU2CG-1SFVC784E

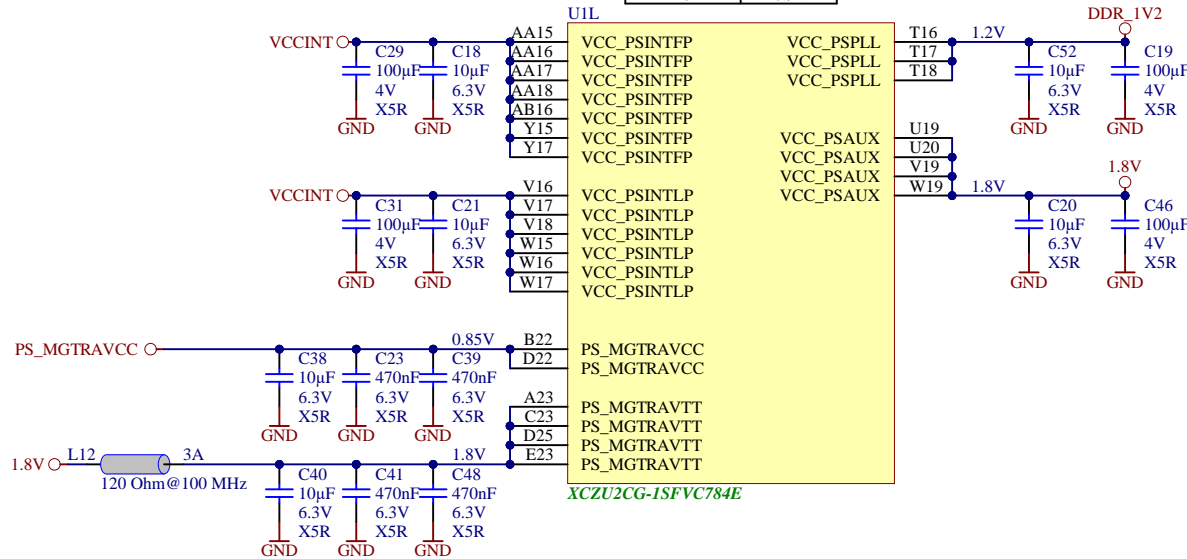
U1J BANK 504 PSDDR		U1J BANK 504 PSDDR	
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DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AD23	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504
DDR4-DQS0_P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504
DDR4-DQS0_N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504
DDR4-DQS1_P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504
DDR4-DQS1_N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504
DDR4-DQS2_P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504
DDR4-DQS2_N	AG25	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504
DDR4-DQS3_P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504
DDR4-DQS3_N	AF27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504
DDR4-DQS4_P	N23	PS_DDR_DQS_P4_504	PS_DDR_DM0_504
DDR4-DQS4_N	M23	PS_DDR_DQS_N4_504	PS_DDR_DM1_504
DDR4-DQS5_P	L23	PS_DDR_DQS_P5_504	PS_DDR_DM2_504
DDR4-DQS5_N	K23	PS_DDR_DQS_N5_504	PS_DDR_DM3_504
DDR4-DQS6_P	N26	PS_DDR_DQS_P6_504	PS_DDR_DM4_504
DDR4-DQS6_N	N27	PS_DDR_DQS_N6_504	PS_DDR_DM5_504
DDR4-DQS7_P	J26	PS_DDR_DQS_P7_504	PS_DDR_DM6_504
DDR4-DQS7_N	J27	PS_DDR_DQS_N7_504	PS_DDR_DM7_504
DDR4-DQS8_P	R27	PS_DDR_DQS_P8_504	PS_DDR_DM8_504
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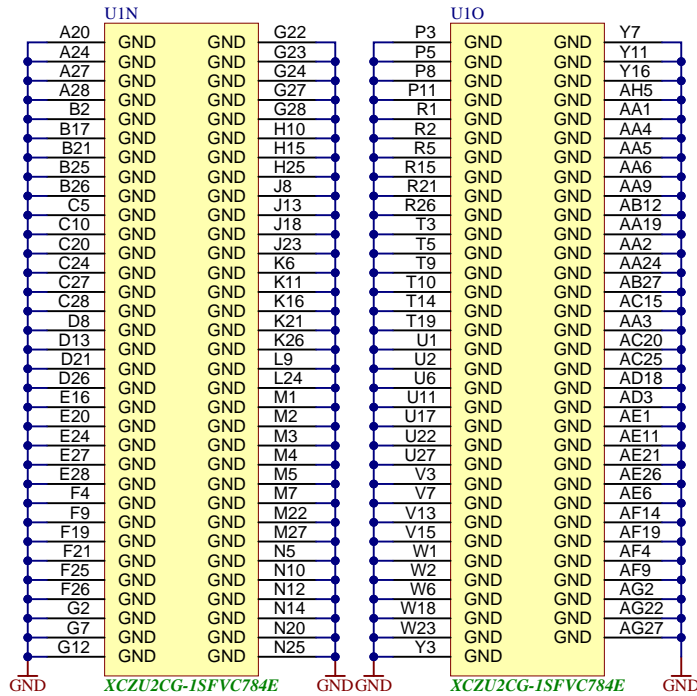


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Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 14 of 30
Filename: PS_DDR.SchDoc		

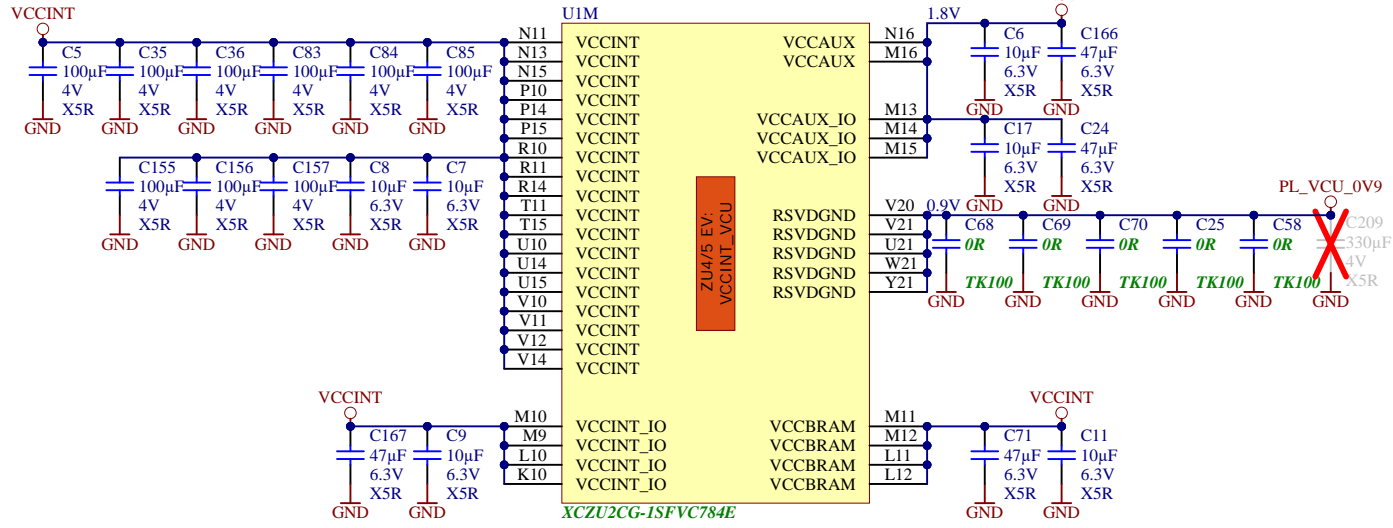
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-1	0.85 V
-2	0.85 V
-3	0.9 V



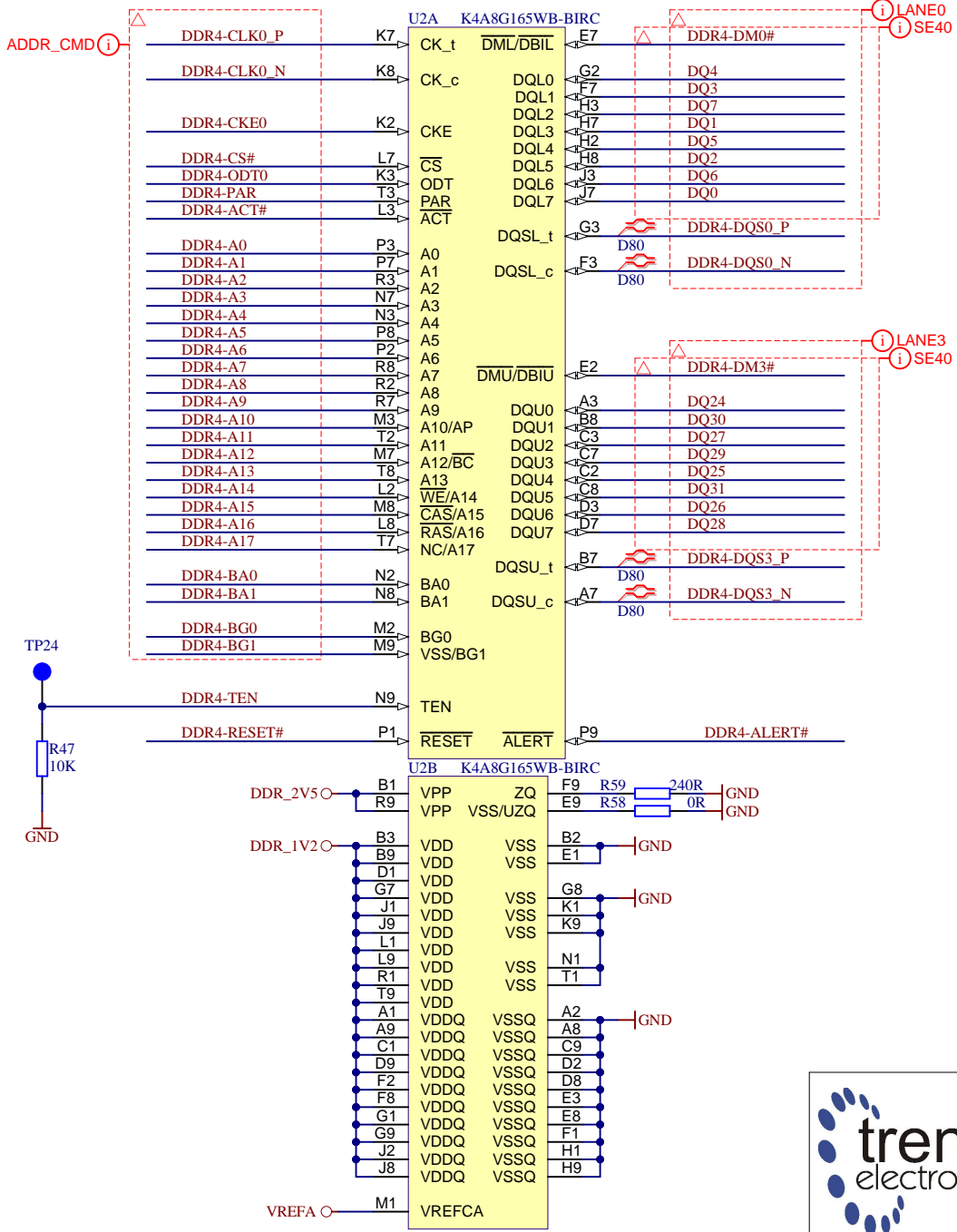
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	Date: 22.07.2022	Rev. 02
	Page 15 of 30	
Copyright: Trenz Electronic GmbH		
Filename: ZU_PS_POWER.SchDoc		



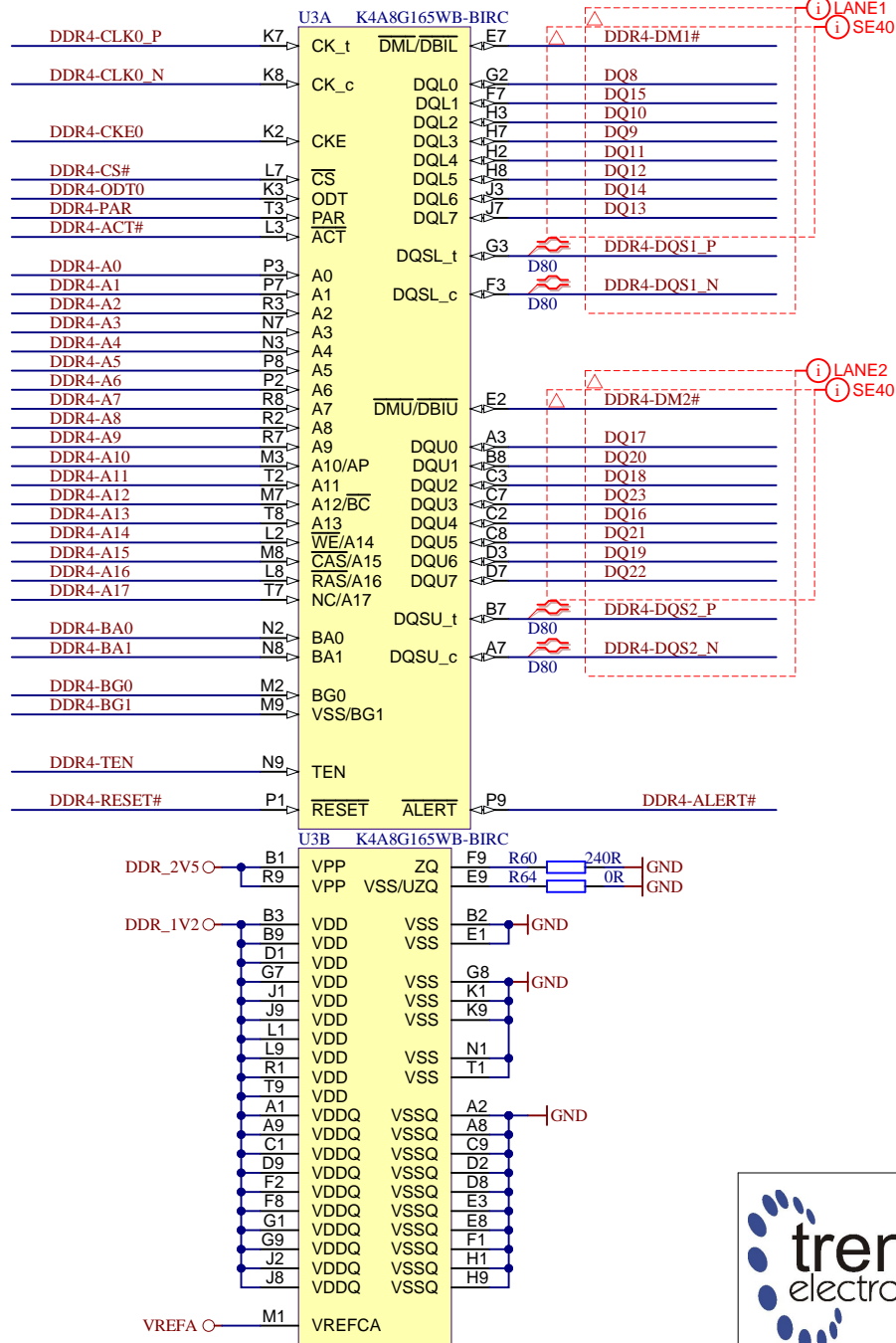

Speedgrade	VCCINT
-1	0.85 V
-2	0.85 V
-3	0.9 V



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	A4	Number: ZU_POWER 2AE21MA
	Date: 22.07.2022	Copyright: Trenz Electronic GmbH
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Filename: ZU_POWER.SchDoc		



Title: AM0010 – DDR4-RAM		
A4	Number: DDR4-RAM 2AE21MA	Rev. 02
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Filename: DDR4-RAM.SchDoc		

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A4	Number: DDR4-RAM_2 2AE21MA	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 18 of 30
Filename: DDR4-RAM_2.SchDoc		

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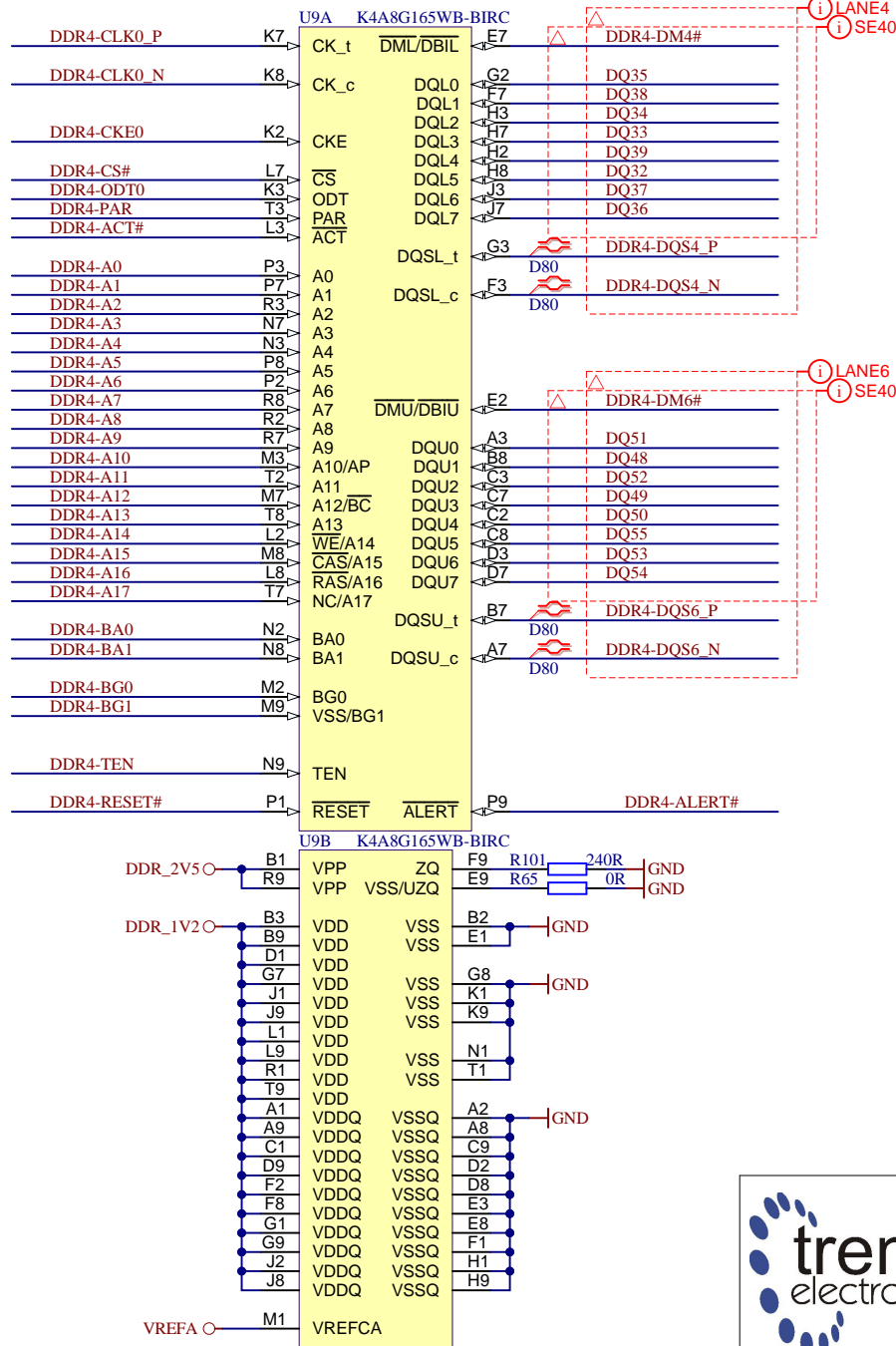

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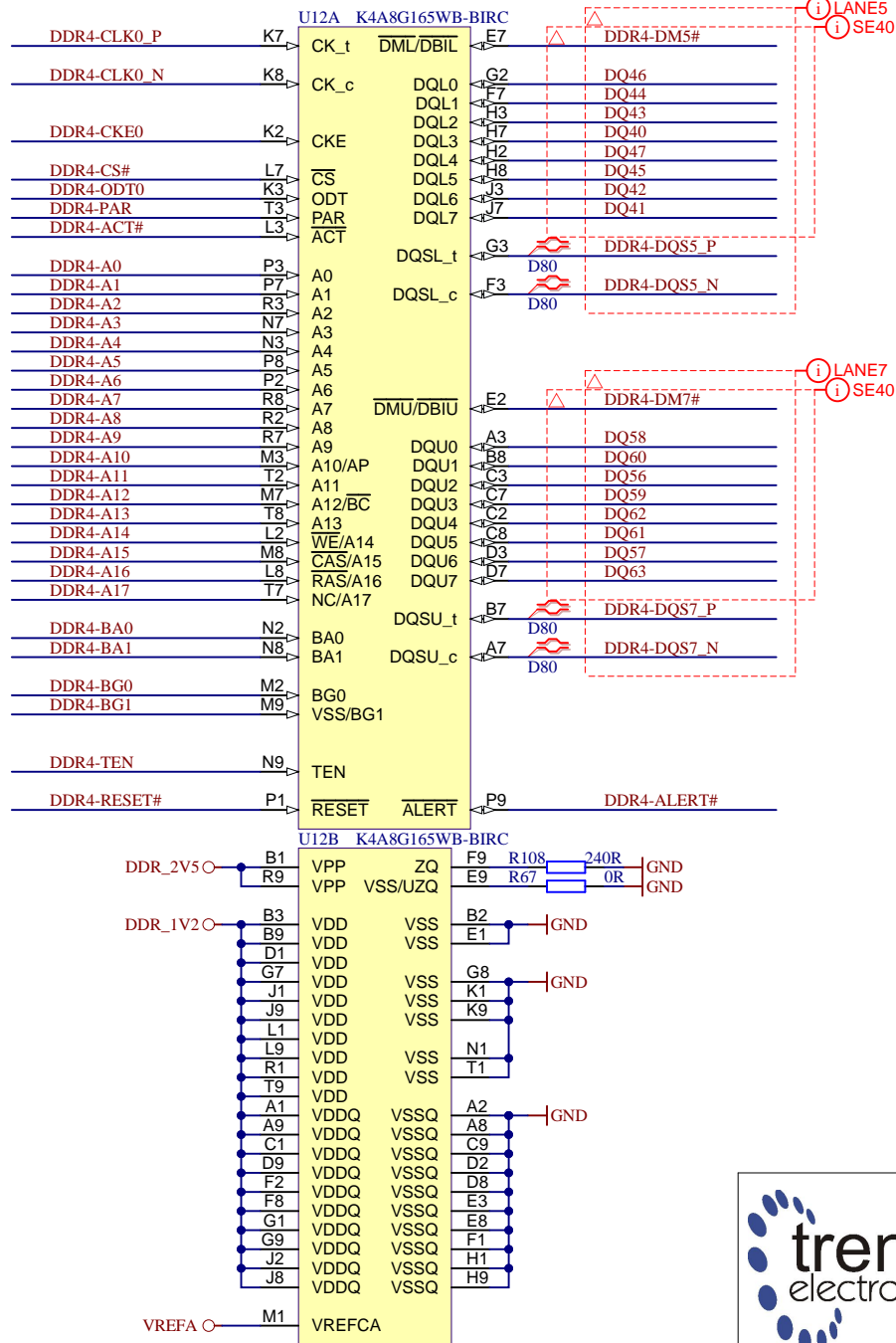
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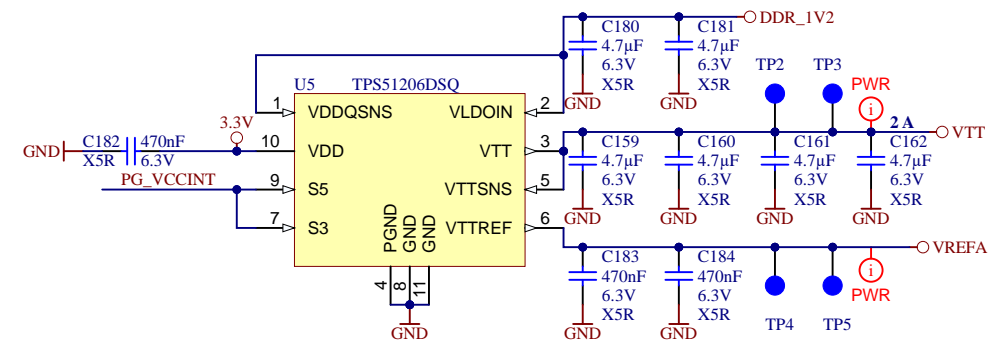
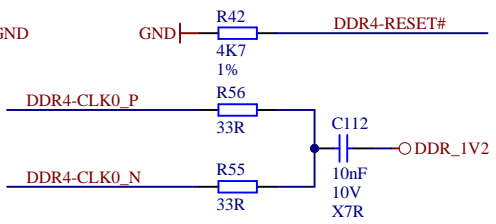
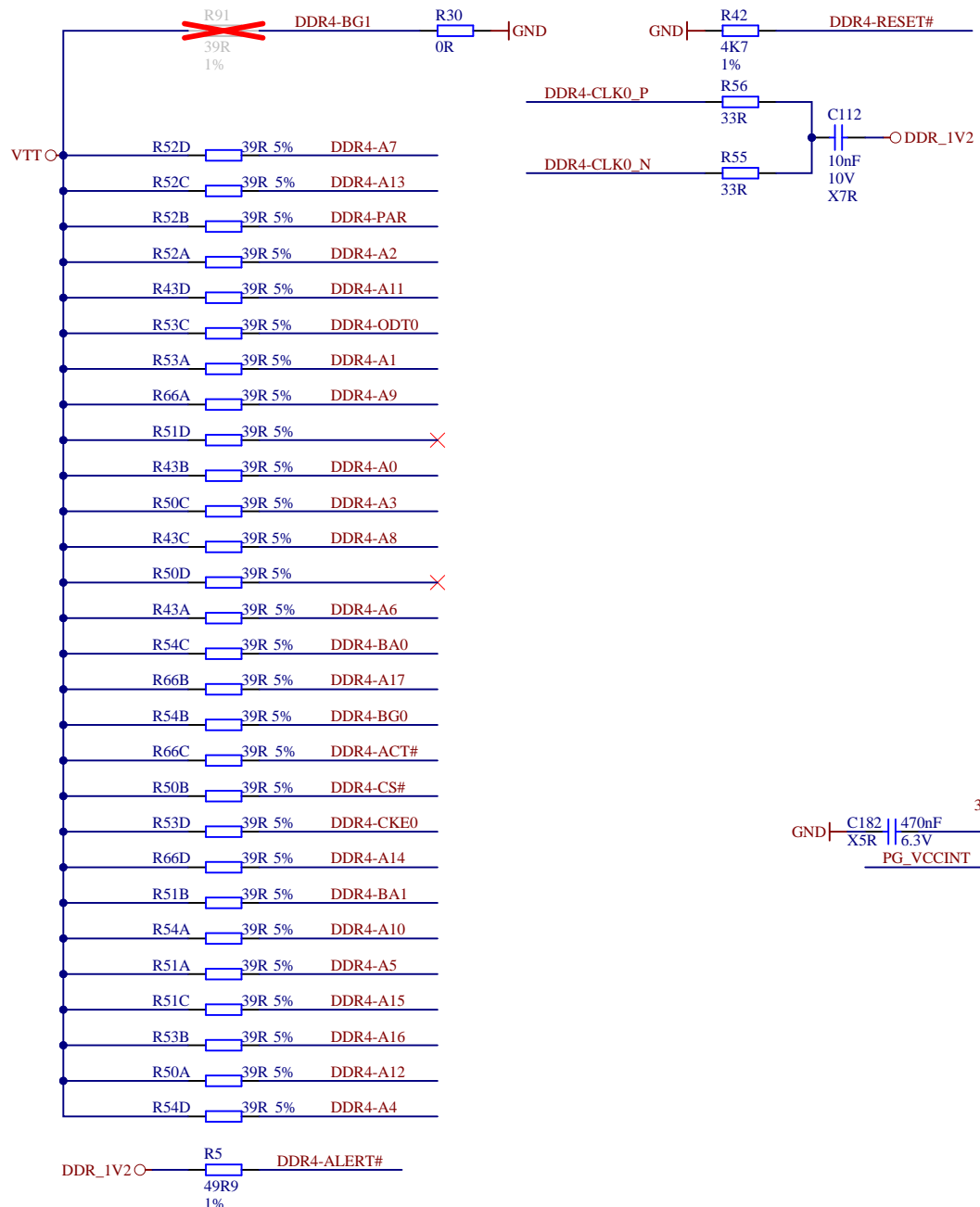
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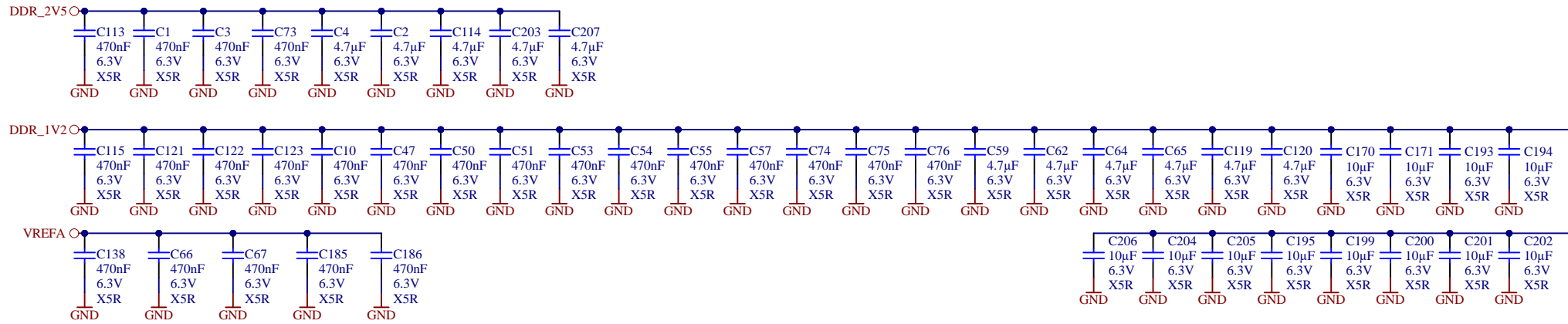
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Filename: DDR4-RAM_3.SchDoc		




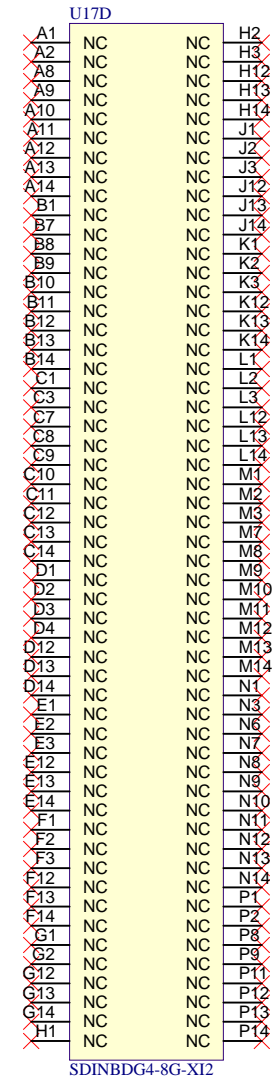
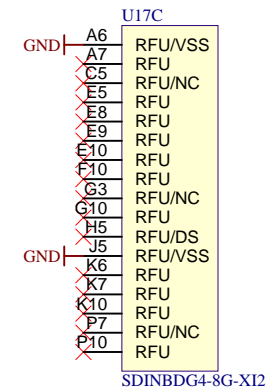
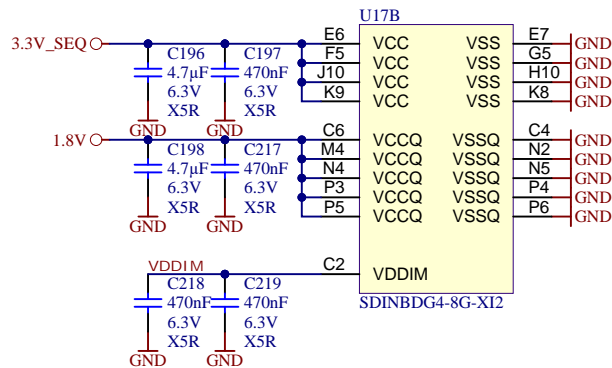
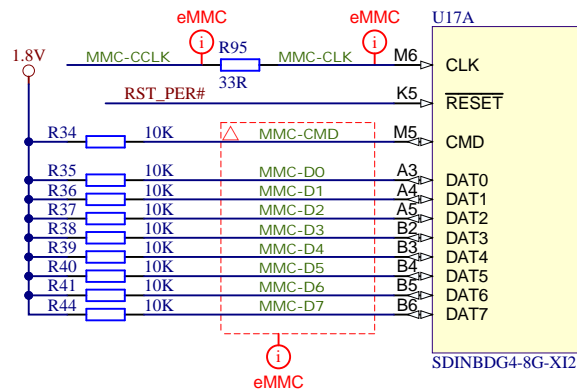
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Date: 22.07.2022		Copyright: Trenz Electronic GmbH	
Filename: DDR4-RAM_4.SchDoc		Page 20 of 30	



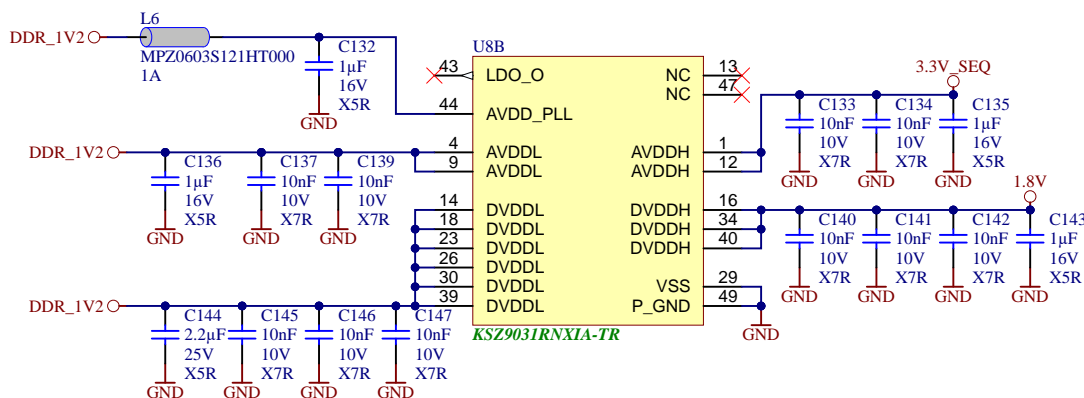
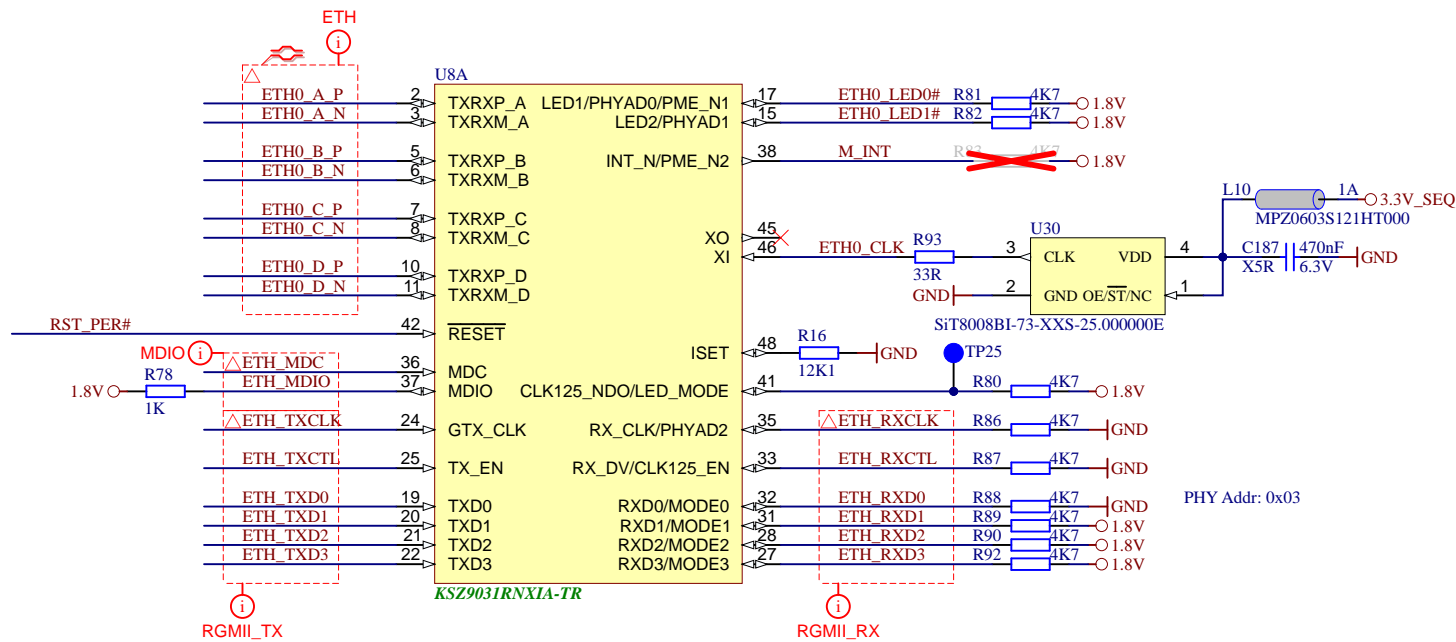
Title: AM0010 – DDR4-TERM		
A4	Number: DDR4-TERM 2AE21MA	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 22 of 30
Filename: DDR4-TERM.SchDoc		




	Title: AM0010 – DDR4-CAPS		
	A4	Number: DDR4-CAPS 2AE21MA	Rev. 02
	Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 23 of 30
	Filename: DDR4-CAPS.SchDoc		



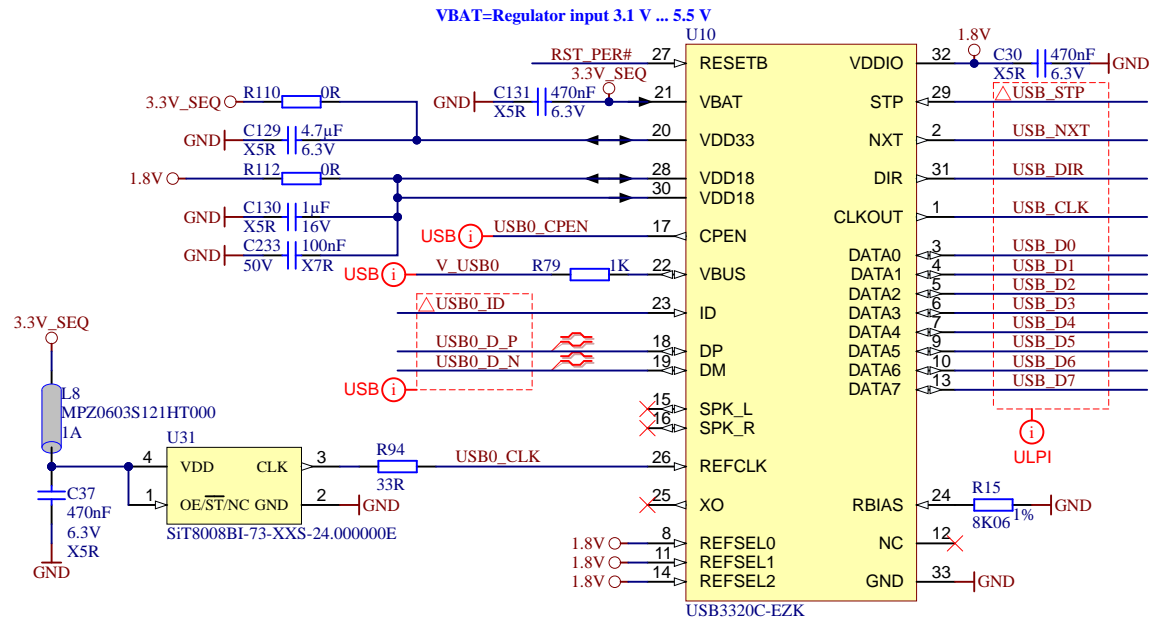
Title: AM0010 – eMMC		
A4	Number: eMMC 2AE21MA	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 24 of 30
Filename: eMMC.SchDoc		




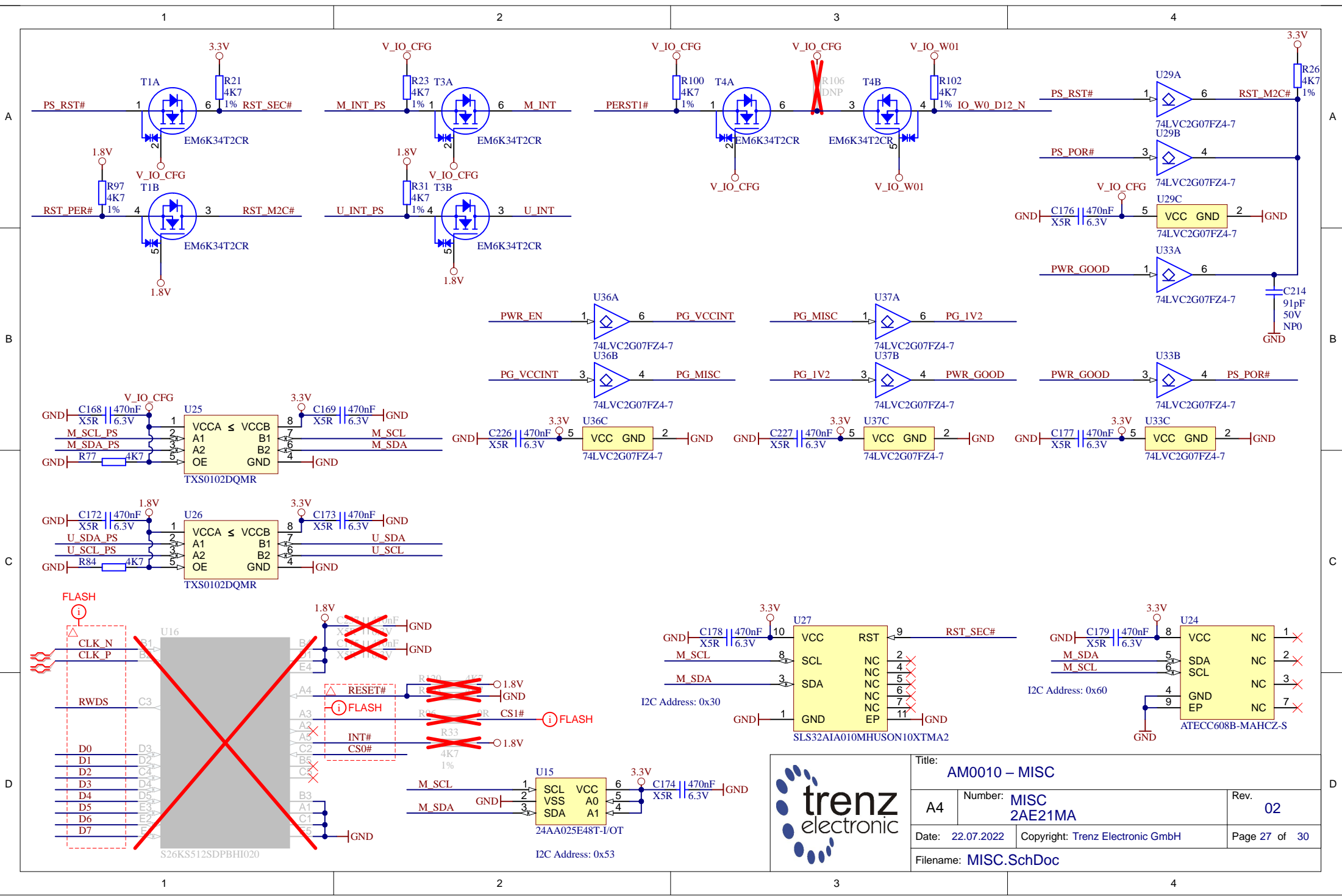
		Title: AM0010 – ETHPHY	
		A4	Number: ETHPHY 2AE21MA
Date: 22.07.2022		Copyright: Trenz Electronic GmbH	
Filename: ETHPHY.SchDoc		Page 25 of 30	
Rev. 02			

Modify variants!

	USB3320	USB3340
R110	0R	DNP
R112	0R	DNP
C129	4.7 μ F	1 μ F
C233	0.1 μ F	1 μ F



	Title: AM0010 – USBPHY	
	A4	Number: USBPHY 2AE21MA
	Date: 22.07.2022	Rev. 02
	Copyright: Trenz Electronic GmbH	
Page 26 of 30		
Filename: USBPHY.SchDoc		



Title: AM0010 – MISC		
A4	Number: MISC 2AE21MA	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 27 of 30
Filename: MISC.SchDoc		

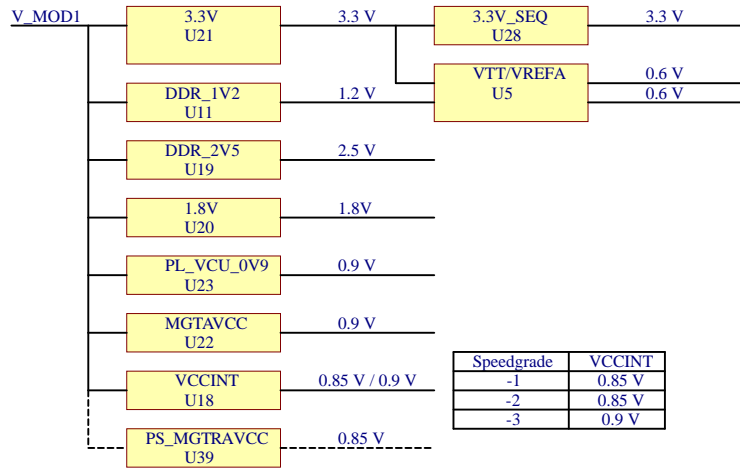
1

2

3

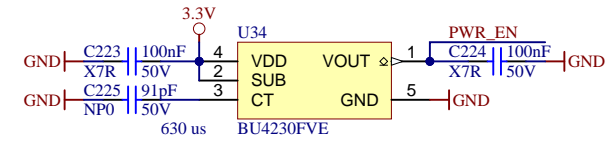
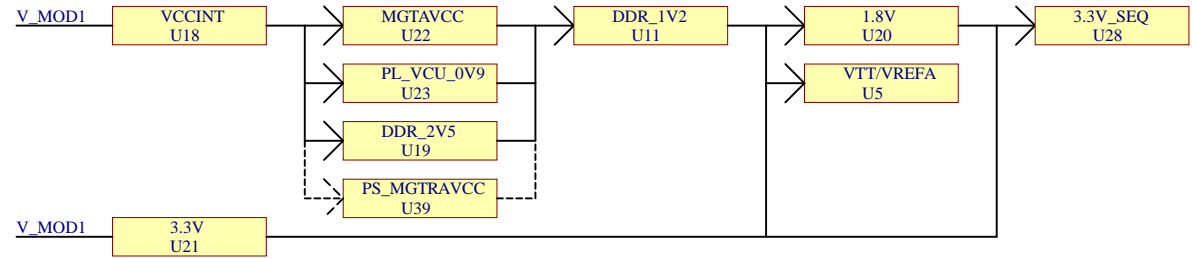
4

Power Supply Structure



Speedgrade	VCCINT
-1	0.85 V
-2	0.85 V
-3	0.9 V

Power Supply Sequencing



A

A

B

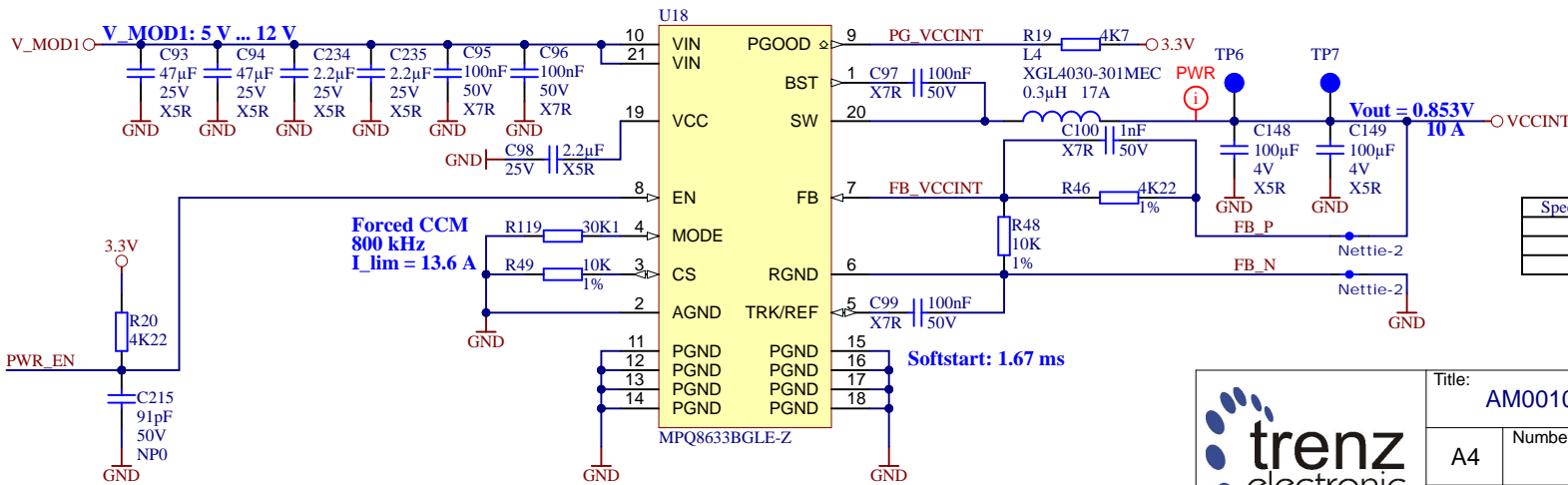
B

C

C

D

D



Forced CCM
800 kHz
I_{lim} = 13.6 A

Softstart: 1.67 ms

Speedgrade	R46	R48	C100	VCCINT
-1	4K22	10K	1 nF	0.853 V
-2	4K22	10K	1 nF	0.853 V
-3	10K	20K	680 pF	0.900 V



Title: AM0010 – POWER_1		
A4	Number: POWER_1 2AE21MA	Rev. 02
Date: 02.09.2022	Copyright: Trenz Electronic GmbH	Page 28 of 30
Filename: POWER_1.SchDoc		

1

2

3

4

A

A

B

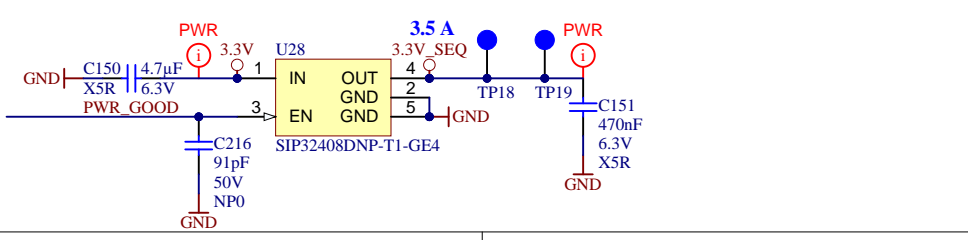
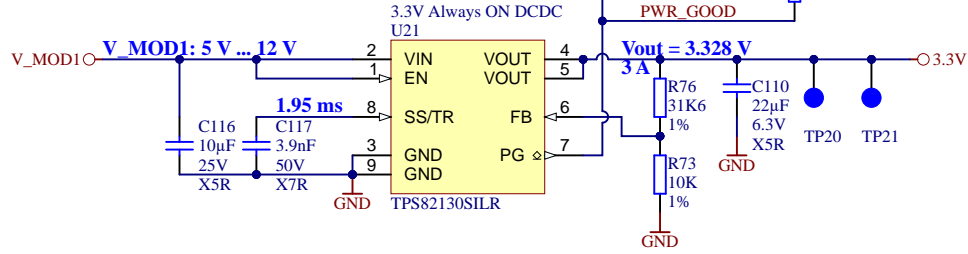
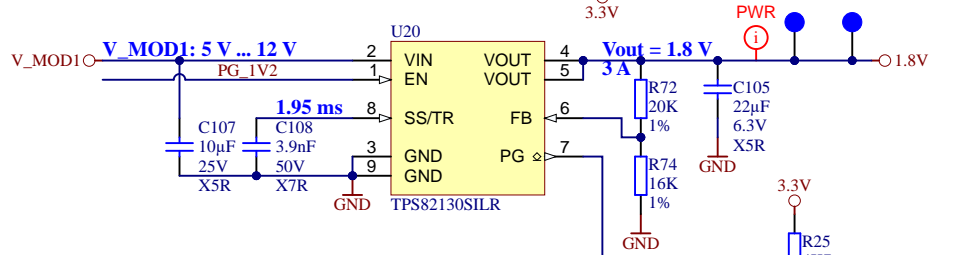
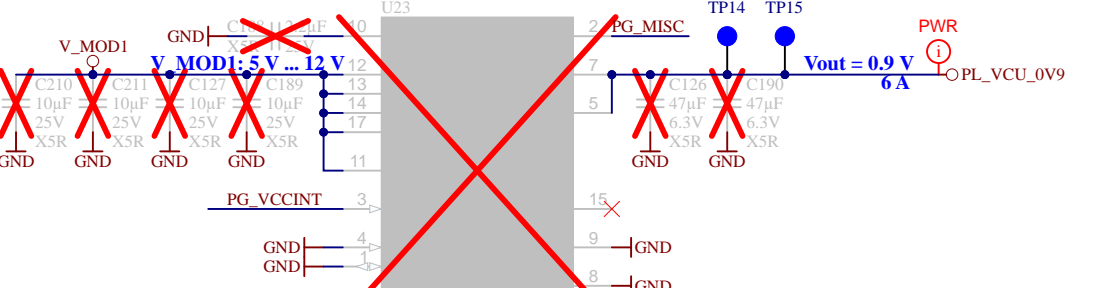
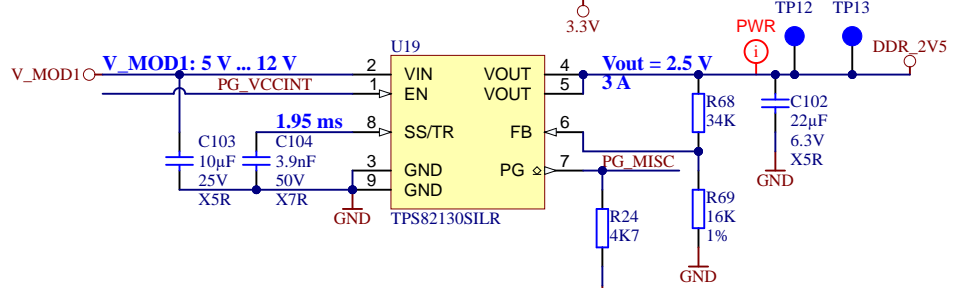
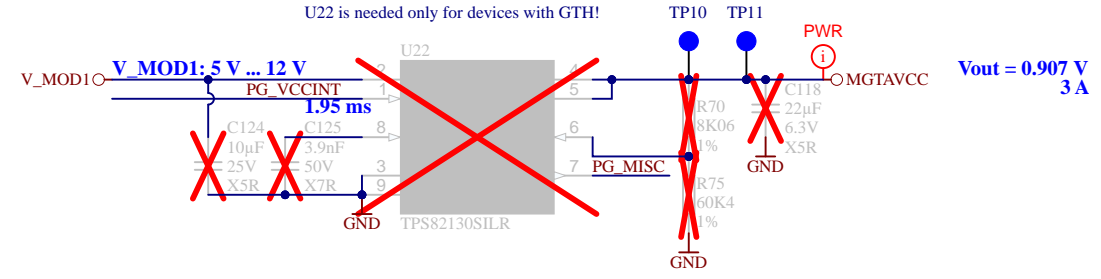
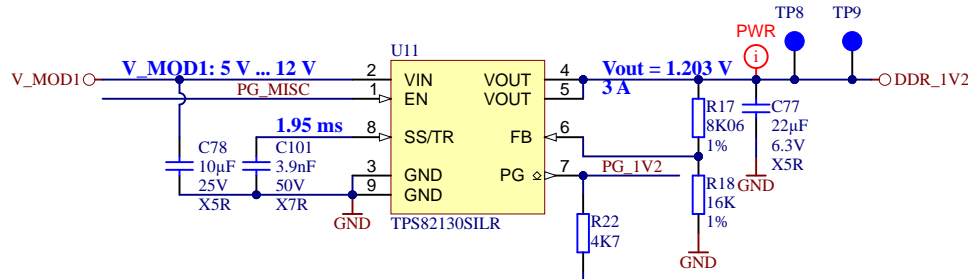
B

C

C

D

D



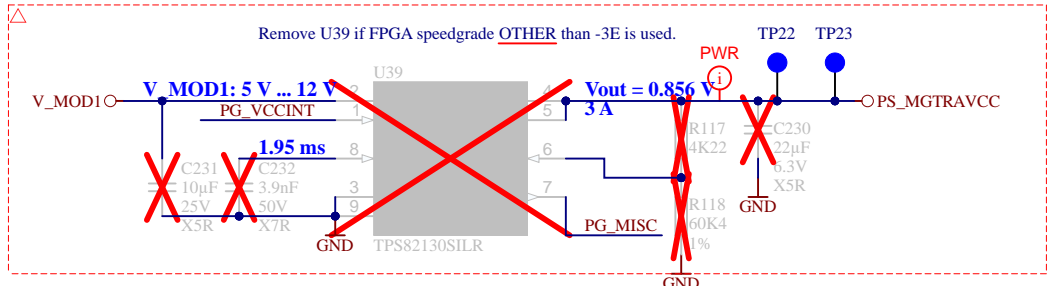
Modify variants!

Speedgrade	L14	VCCINT
-1	L14	0.85 V
-2	L14	0.85 V
-3	DNP	0.9 V

Remove L14 when FPGA speedgrade -3E is used

VCCINT — L14 (3A, 120 Ohm@100 MHz) — PS_MGTRAVCC

Vout_max = 0.876V (+3%)
 Vout_nom = 0.85V
 Vout_min = 0.833V (-2%)



Title: AM0010 – POWER_2		
A4	Number: POWER_2 2AE21MA	Rev. 02
Date: 22.07.2022	Copyright: Trenz Electronic GmbH	Page 29 of 30
Filename: POWER_2.SchDoc		

