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Schematics and other handouts serve for informational purposes only!

	Title: <b>AM0010 – Legal Notices Modules</b>		
	A4	Number: <b>Legal Notices Modules 5DE21MA</b>	Rev. <b>02</b>
	Date: <b>04.08.2022</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>1</b> of <b>30</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		

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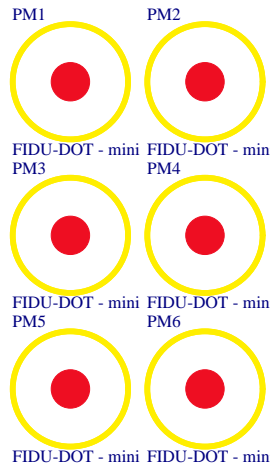
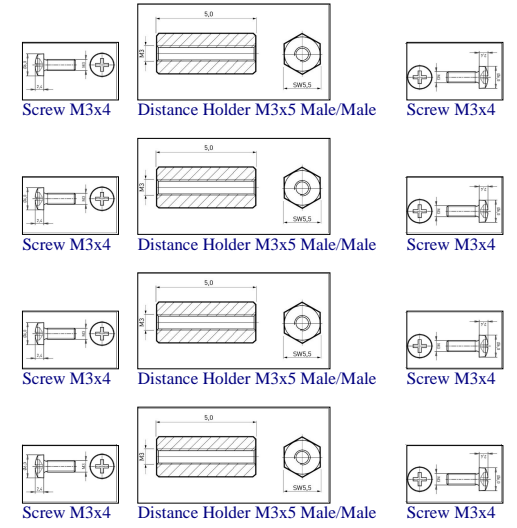
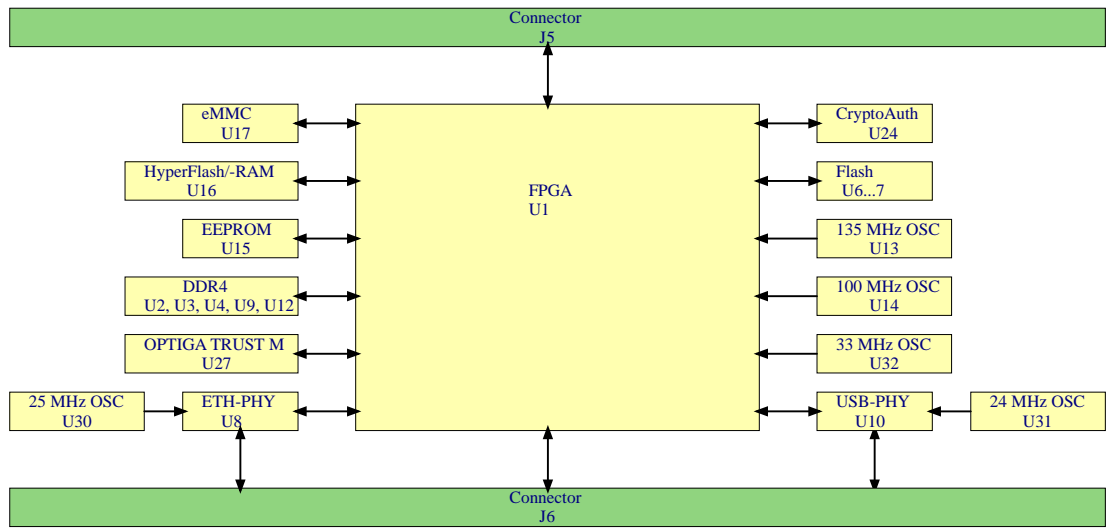
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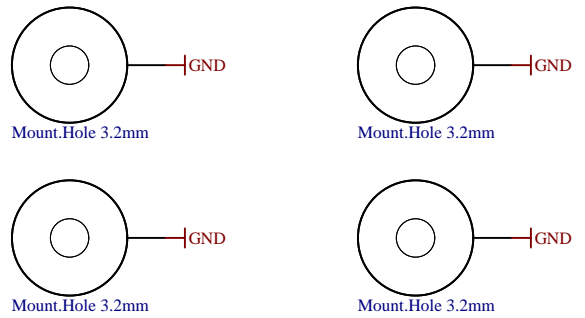
- U\_B2B\_Connector\_1  
B2B\_Connector\_1.SchDoc
- U\_B2B\_Connector\_2  
B2B\_Connector\_2.SchDoc
- U\_MPSoC  
MPSoC.SchDoc
- U\_DDR4-RAM  
DDR4-RAM.SchDoc
- U\_DDR4-RAM\_2  
DDR4-RAM\_2.SchDoc
- U\_DDR4-RAM\_3  
DDR4-RAM\_3.SchDoc
- U\_DDR4-RAM\_4  
DDR4-RAM\_4.SchDoc
- U\_DDR4-RAM\_5  
DDR4-RAM\_5.SchDoc
- U\_DDR4-CAPS  
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- U\_ETHPHY  
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- U\_POWER\_1  
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POWER\_2.SchDoc
- U\_REV\_CH  
Revision\_Changes.SchDoc
- U\_Legal\_Notices\_Modules  
Legal\_Notices\_Modules.SchDoc

Special notes:



Serial  
Serialnumber 6,3 x 6.3mm



UKCA  
UKCA Logo on Top Overlay  
UKCA-TOOVERLAY



Assembly variant	5DE21MA
Created by	VY
Modified by	VY
Modified at	25.11.2022
SVN Revision	588

Title: AM0010		
A4	Number: AM0010 5DE21MA	Rev. 02
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Filename: AM0010.SchDoc		

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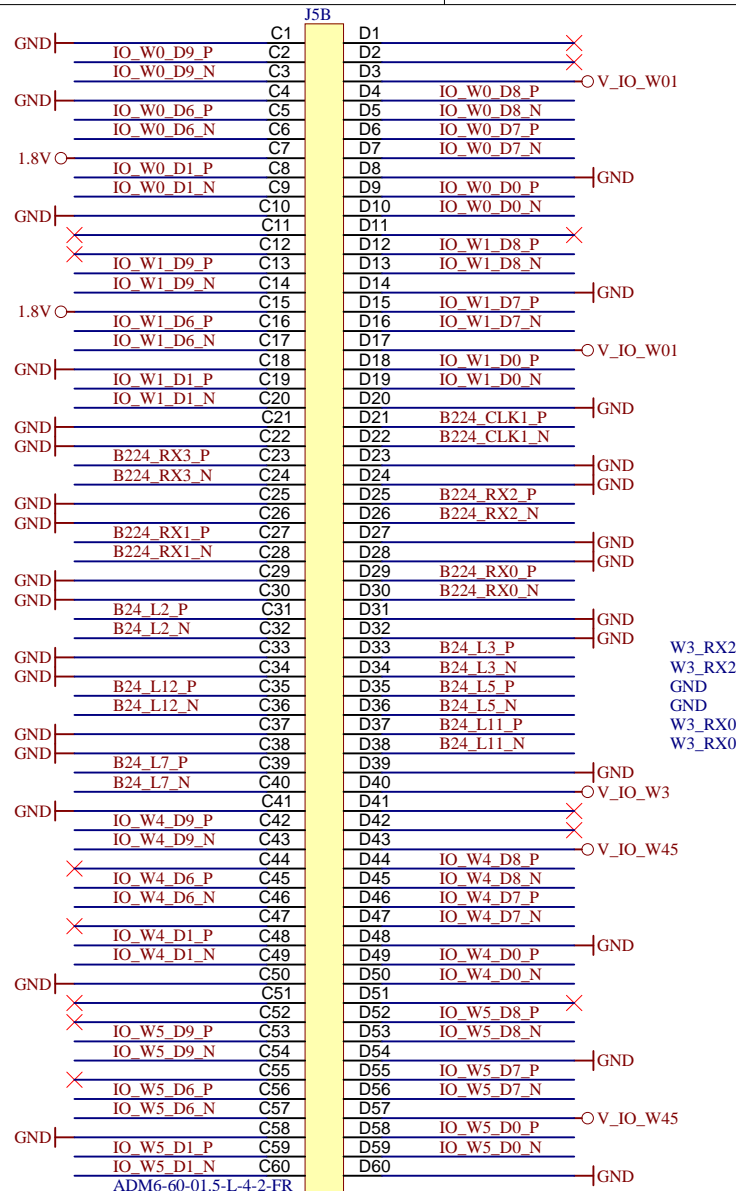
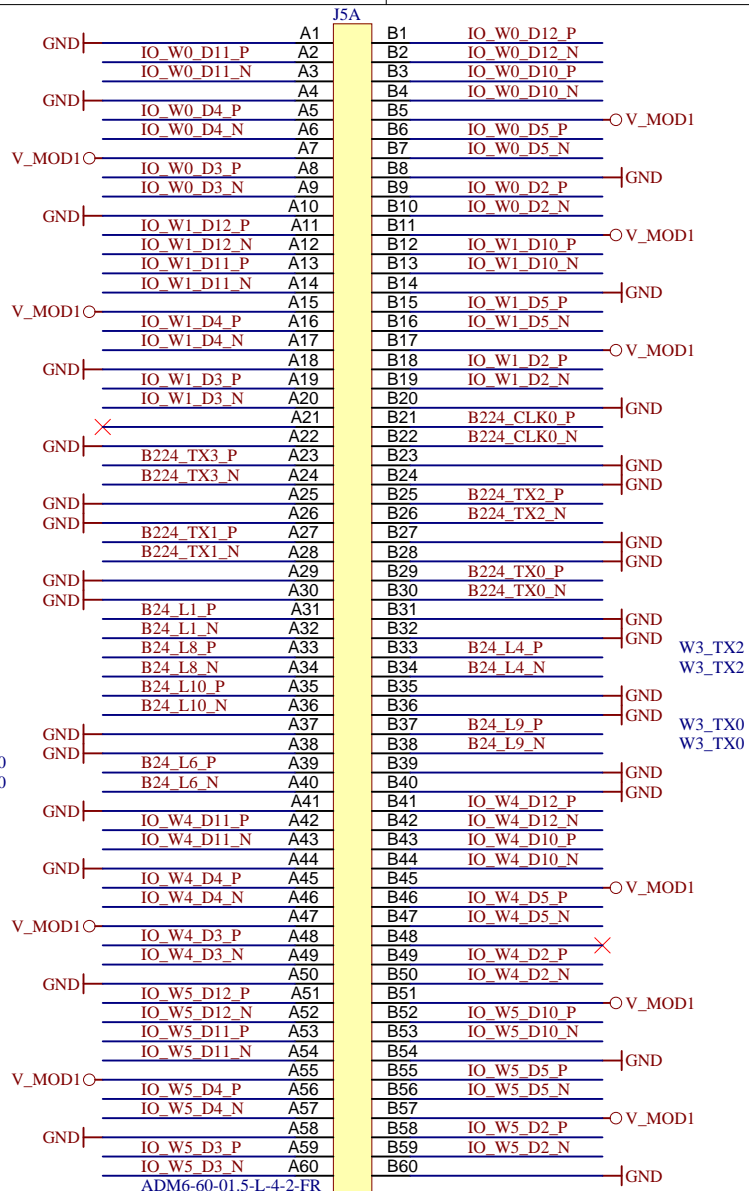
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Connector W



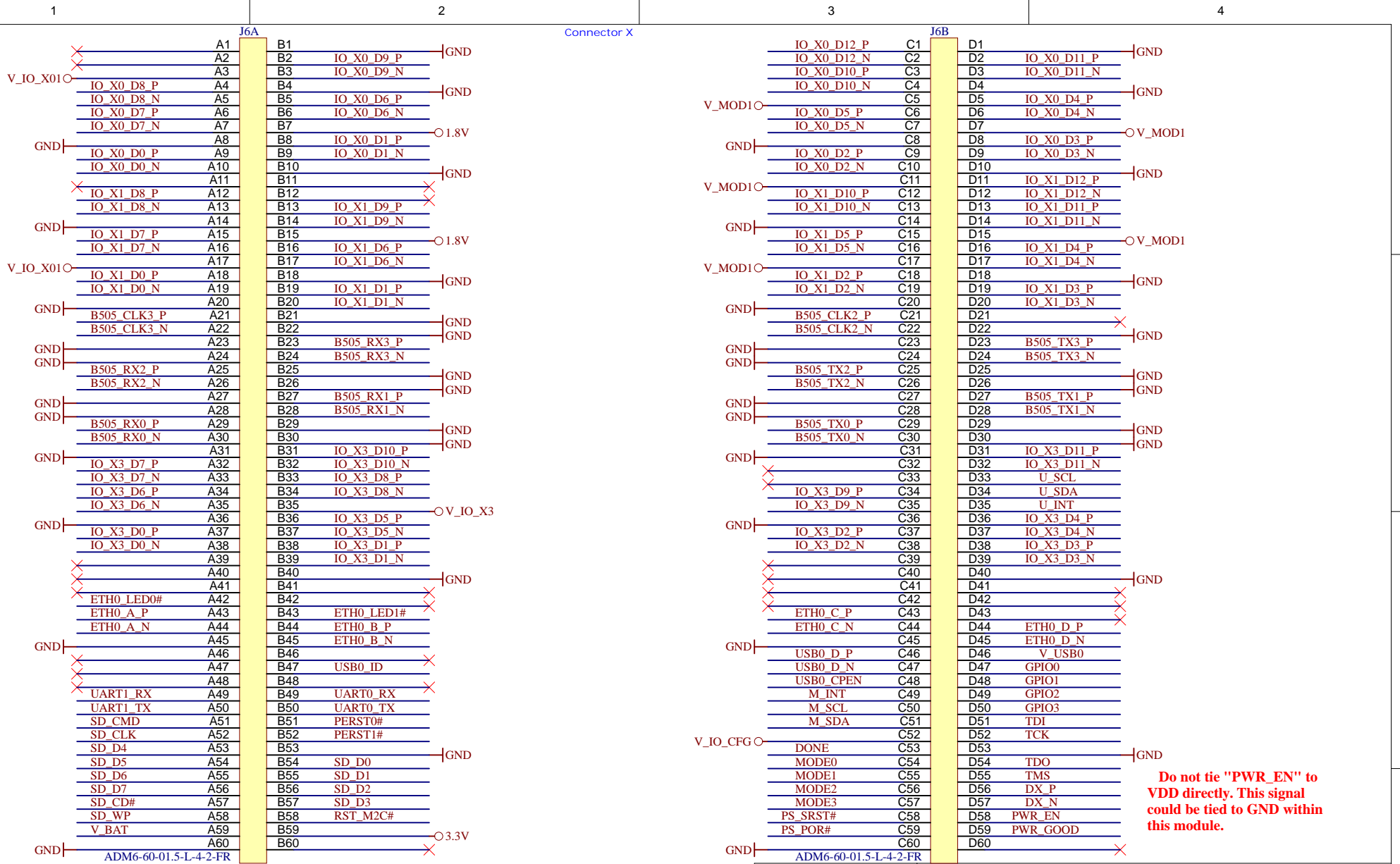
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Date: 04.08.2022	Copyright: Trenz Electronic GmbH	Page 3 of 30
Filename: B2B_Connector_1.SchDoc		

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**Do not tie "PWR\_EN" to VDD directly. This signal could be tied to GND within this module.**



Title: AM0010 – B2B_Connector_2		
A4	Number: B2B_Connector_2 5DE21MA	Rev. 02
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Filename: B2B_Connector_2.SchDoc		



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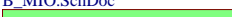






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- U\_B64  
B64.SchDoc  

- U\_B65  
B65.SchDoc  

- U\_B66  
B66.SchDoc  

- U\_B\_HD  
B\_HD.SchDoc  

- U\_B\_MIO  
B\_MIO.SchDoc  

- U\_PS\_DDR  
PS\_DDR.SchDoc  

- U\_B\_PS\_GT  
B\_PS\_GT.SchDoc  

- U\_B\_GT  
B\_GT.SchDoc  

- U\_CONFIG  
CONFIG.SchDoc  

- U\_ZU\_POWER  
ZU\_POWER.SchDoc  

- U\_ZU\_PS\_POWER  
ZU\_PS\_POWER.SchDoc  


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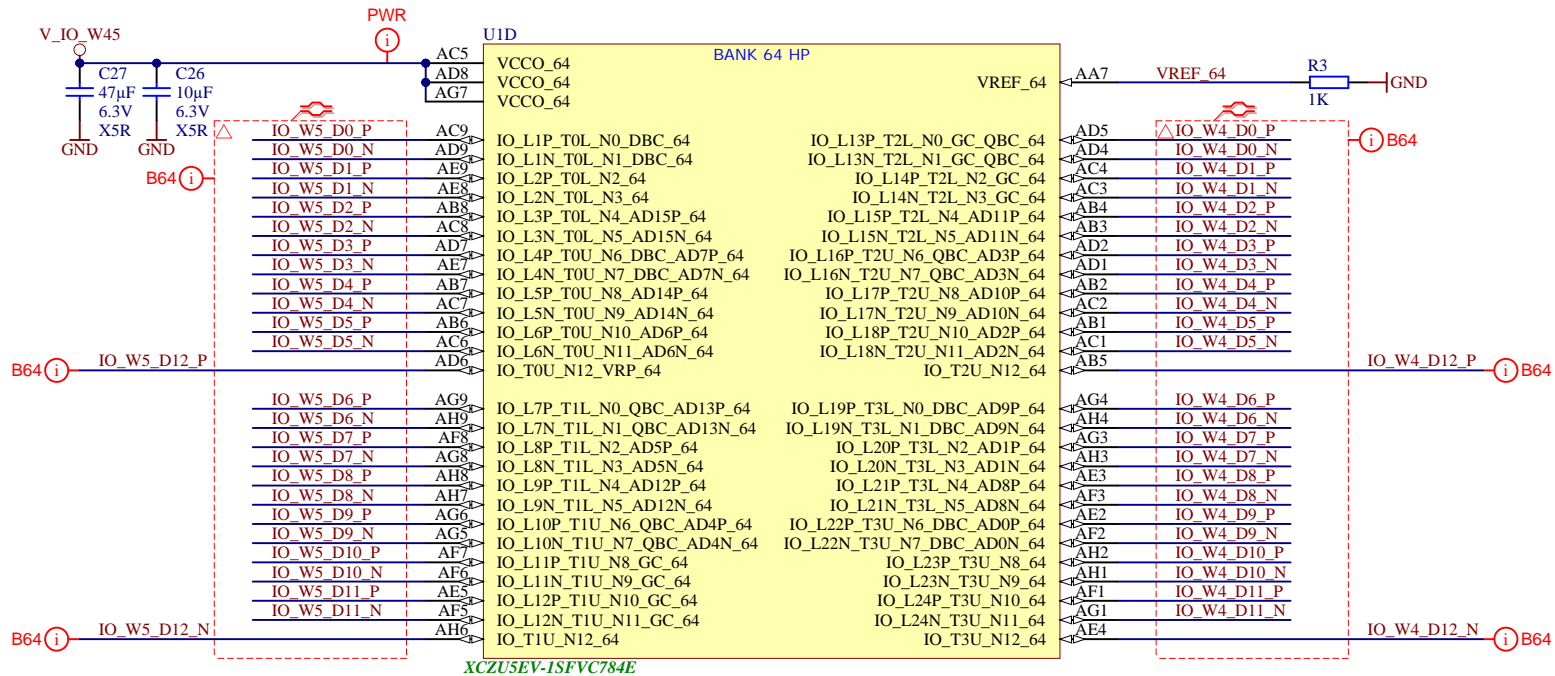
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	Date: 04.08.2022	Copyright: Trenz Electronic GmbH	Page 5 of 30
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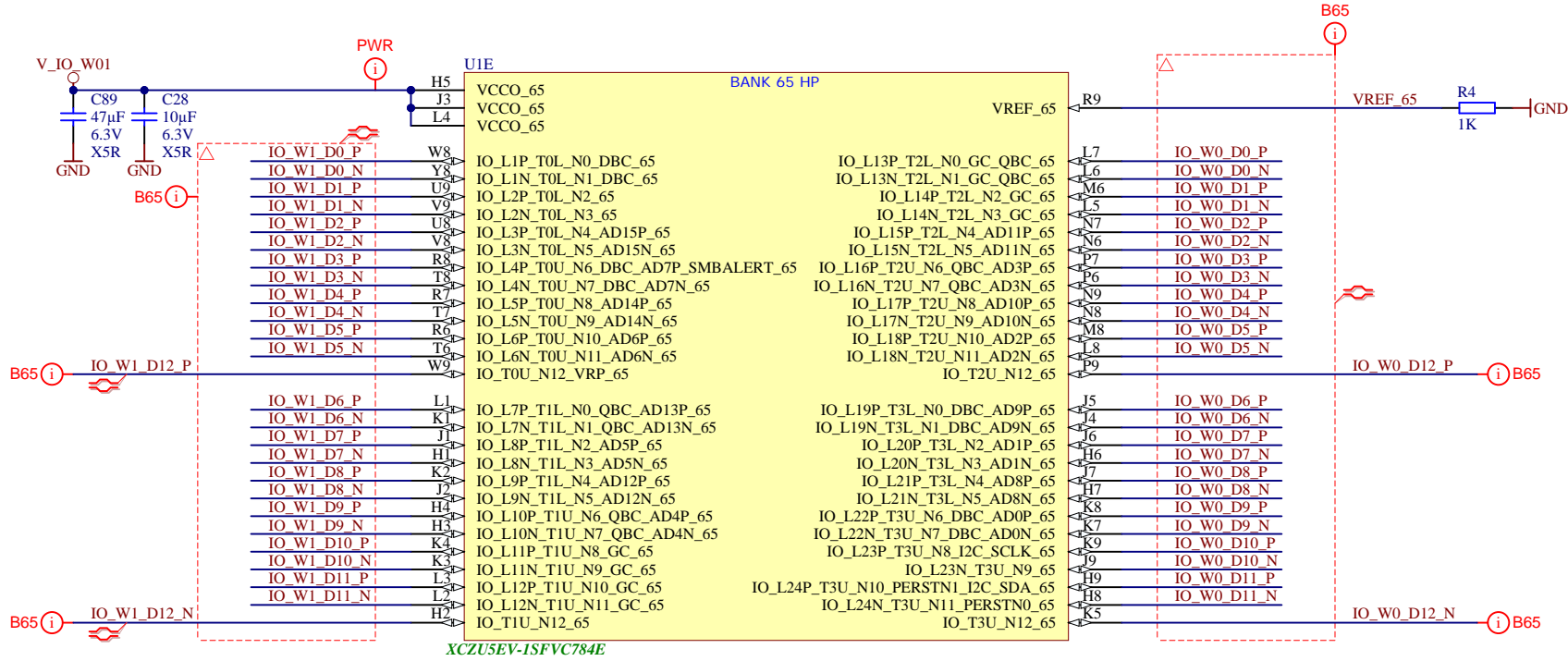
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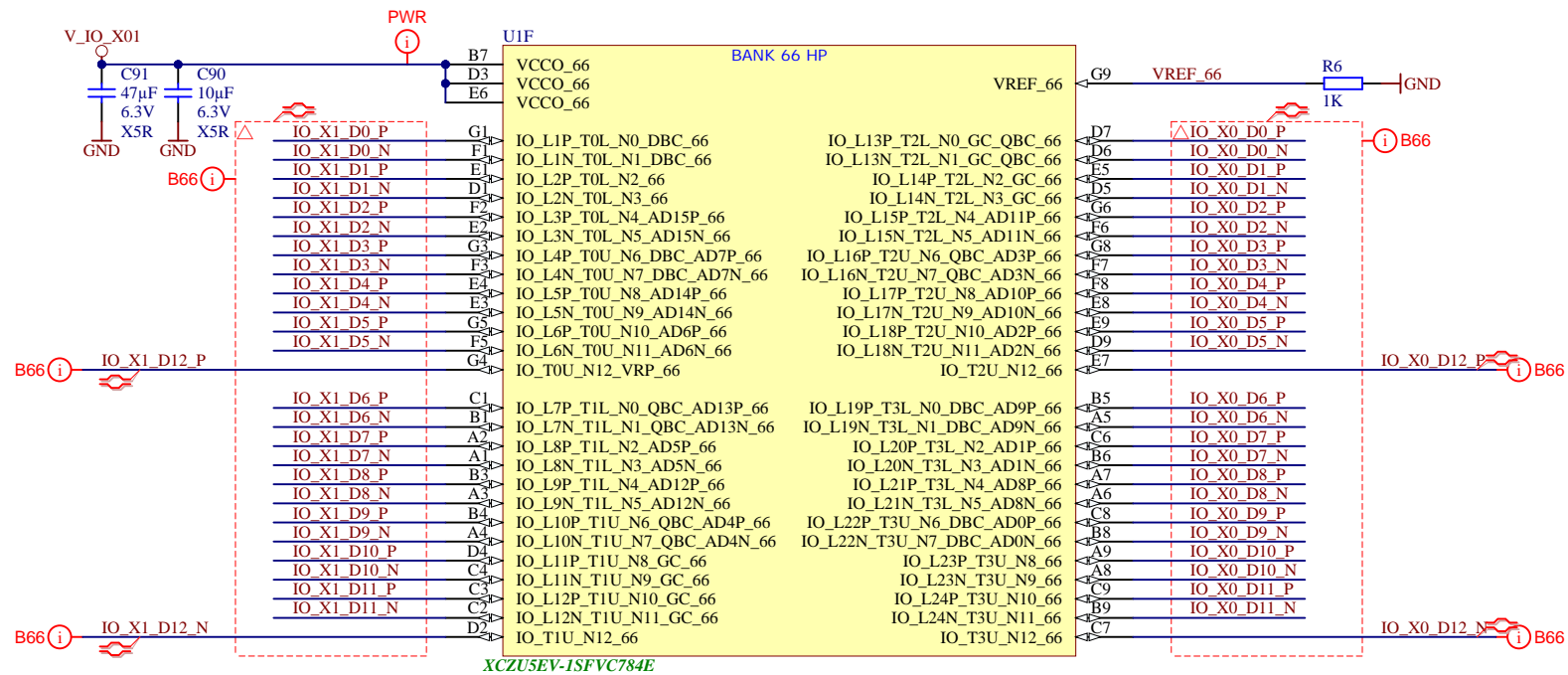
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Title: AM0010 – B65		
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Title: AM0010 – B66		
A4	Number: B66 5DE21MA	Rev. 02
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Filename: B66.SchDoc		

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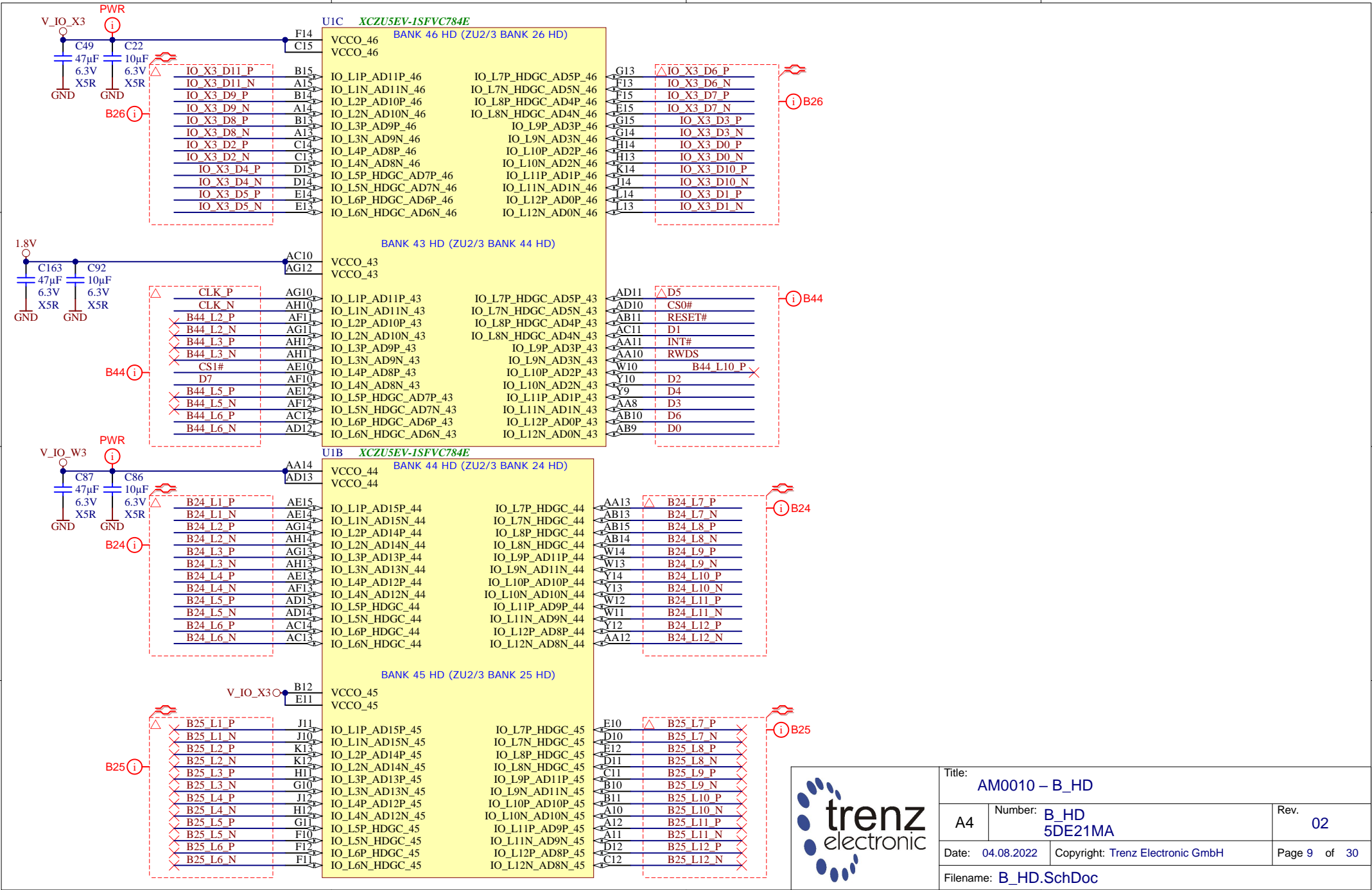
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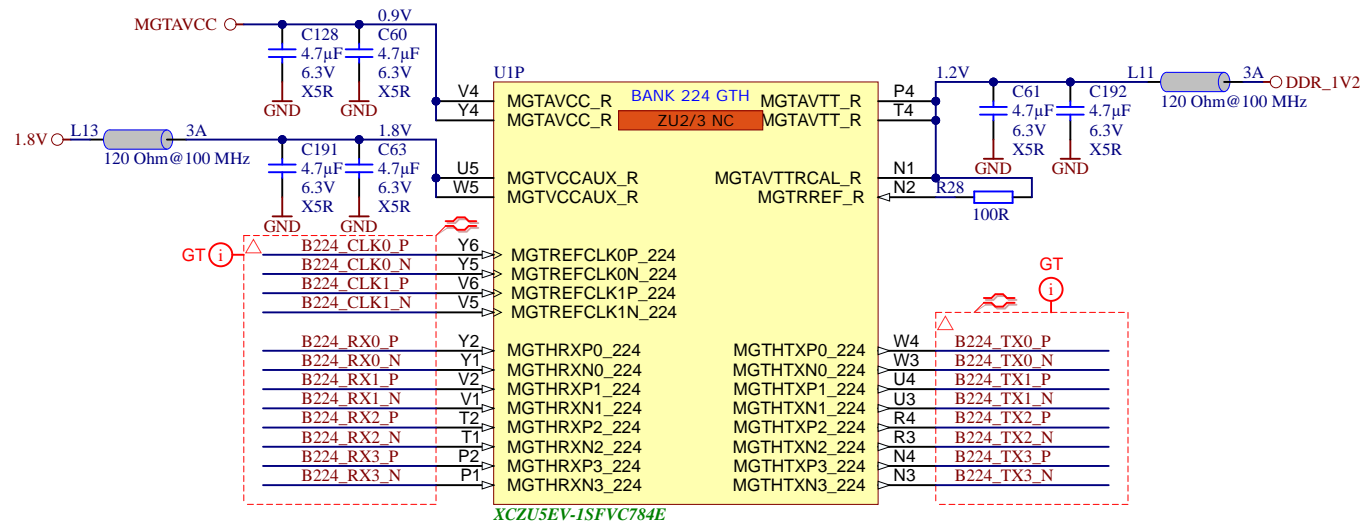
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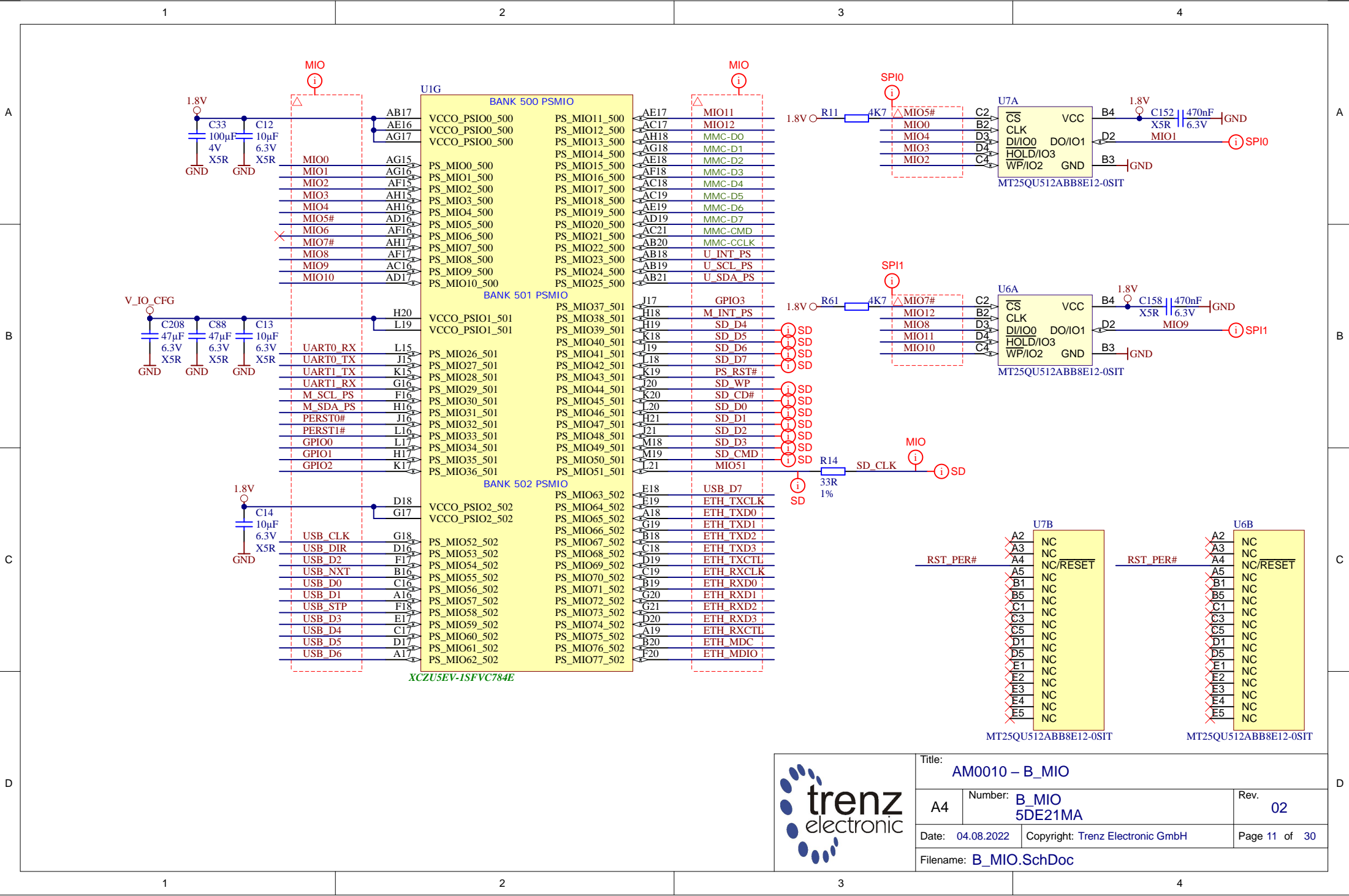
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Filename: B_HD.SchDoc		



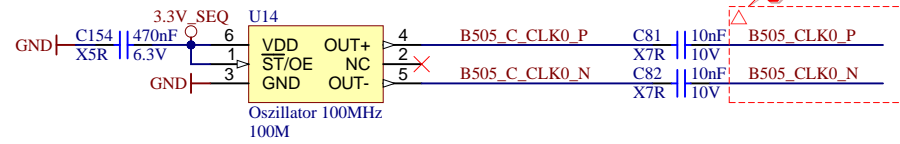
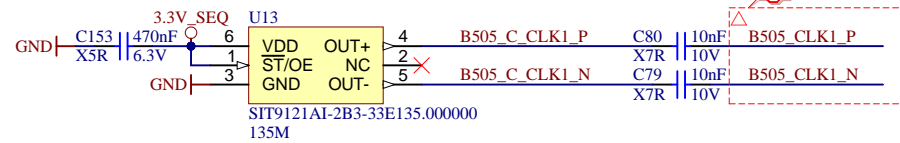
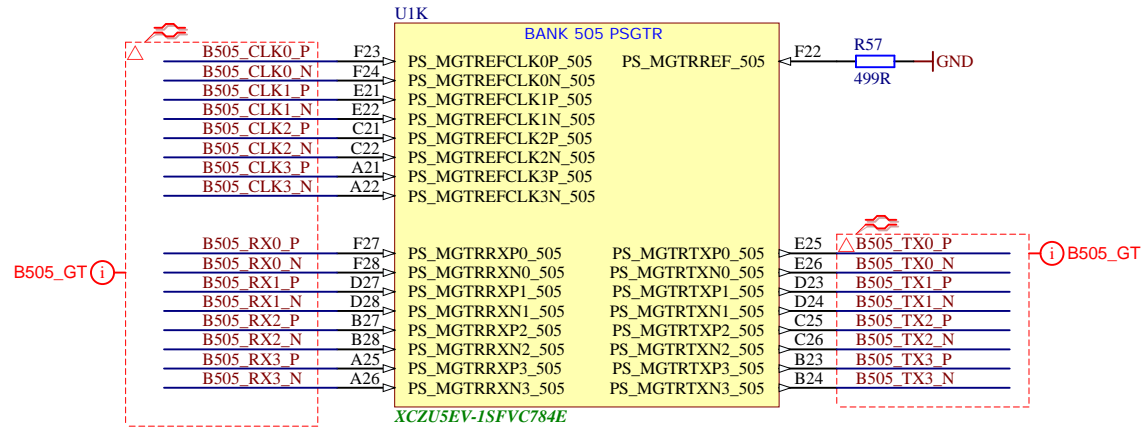


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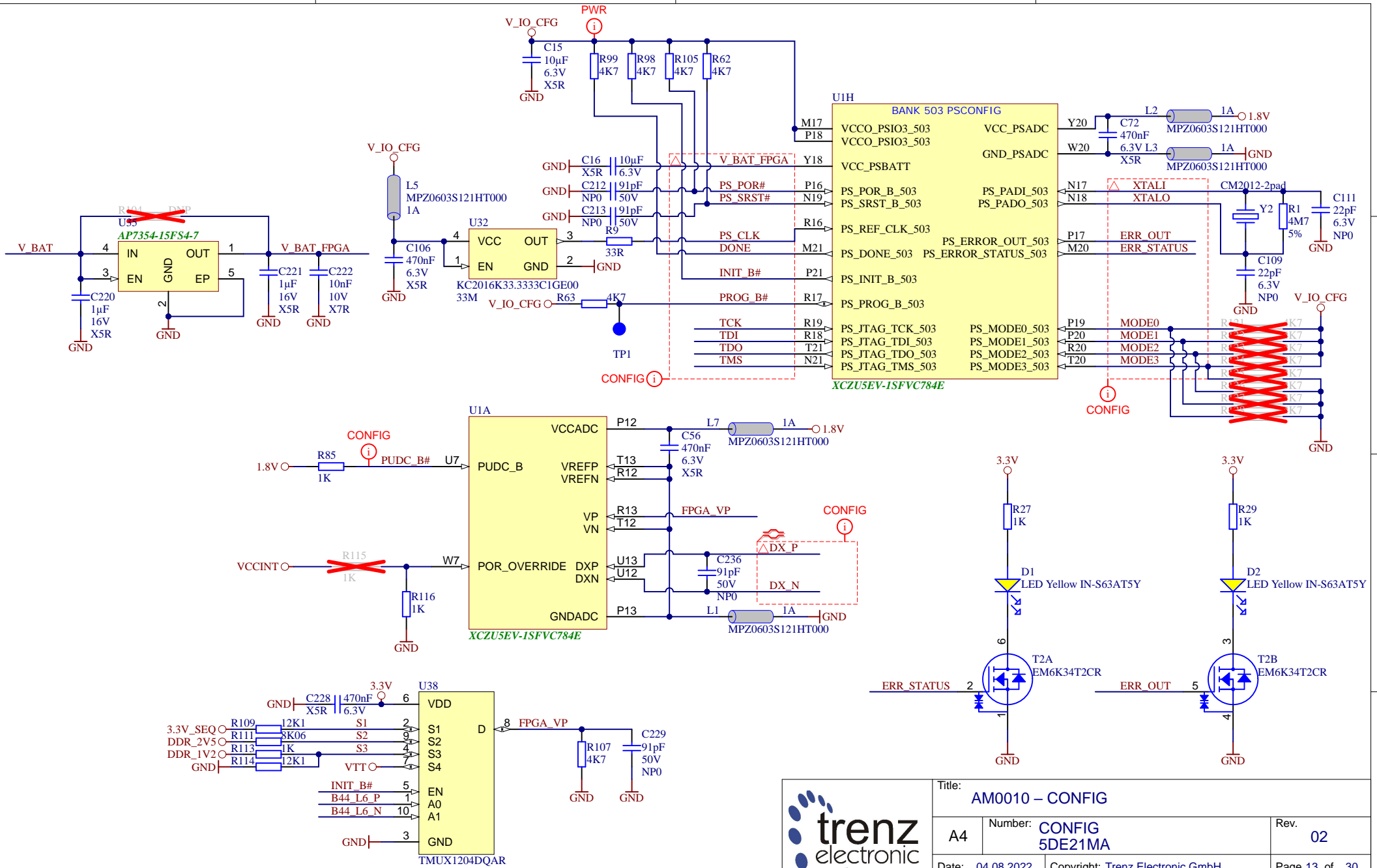
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Date: 04.08.2022		Copyright: Trenz Electronic GmbH	
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Title: AM0010 - B_MIO		
A4	Number: B_MIO 5DE21MA	Rev. 02
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	Title: AM0010 - B_PS_GT	
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Filename: B_PS_GT.SchDoc		



Title: AM0010 – CONFIG		
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Filename: CONFIG.SchDoc		

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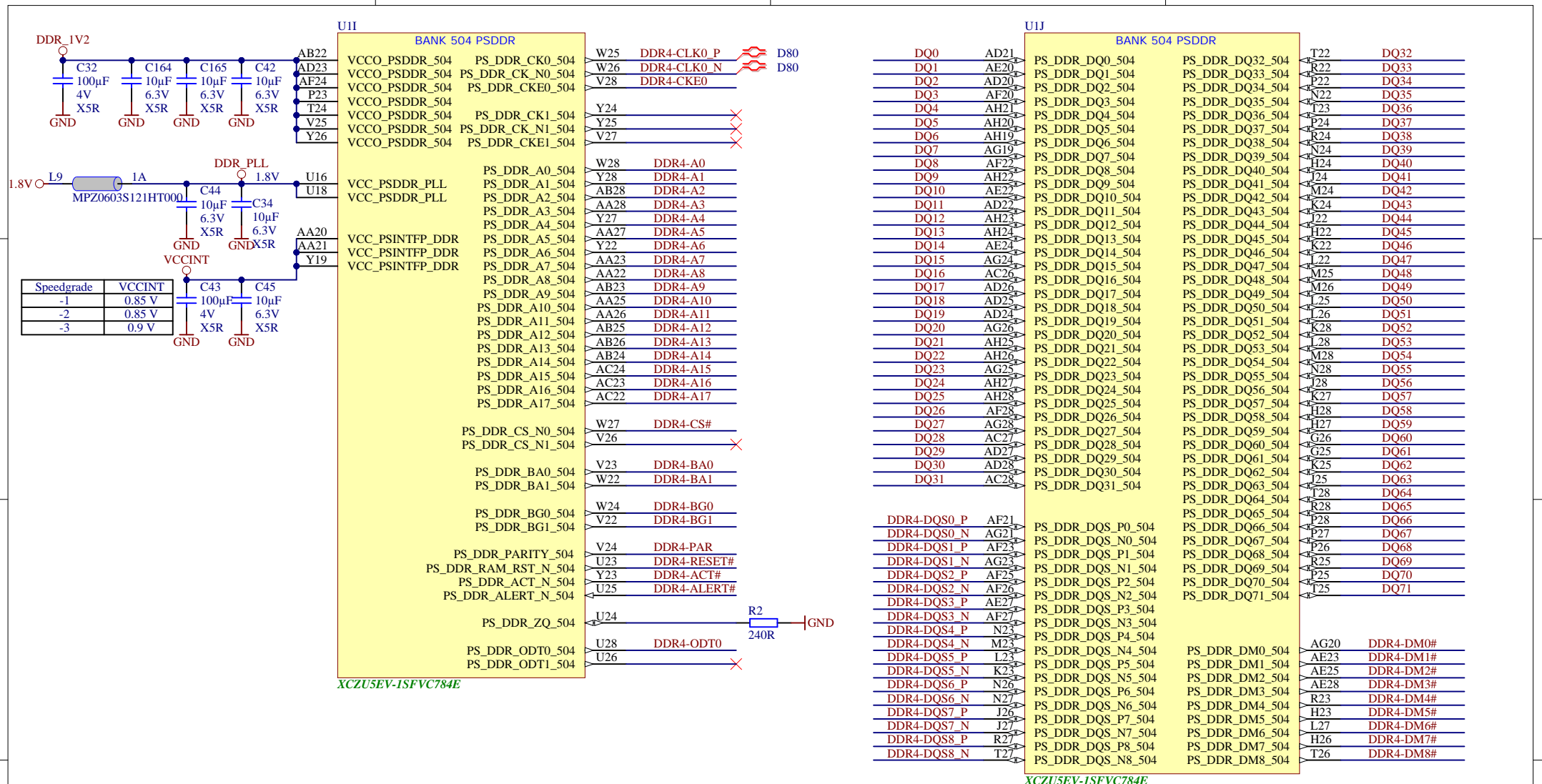
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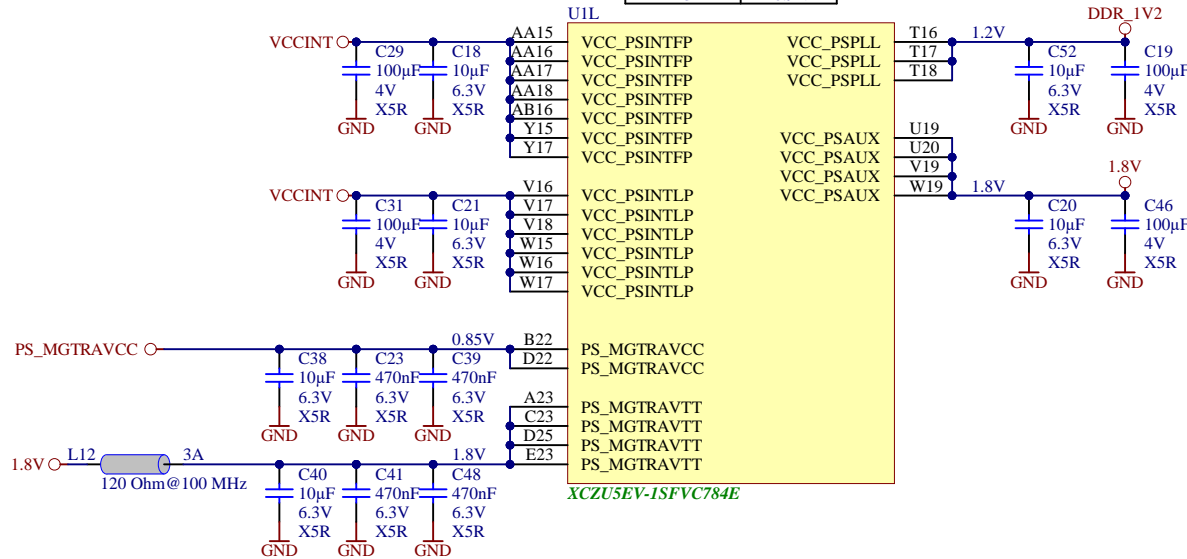
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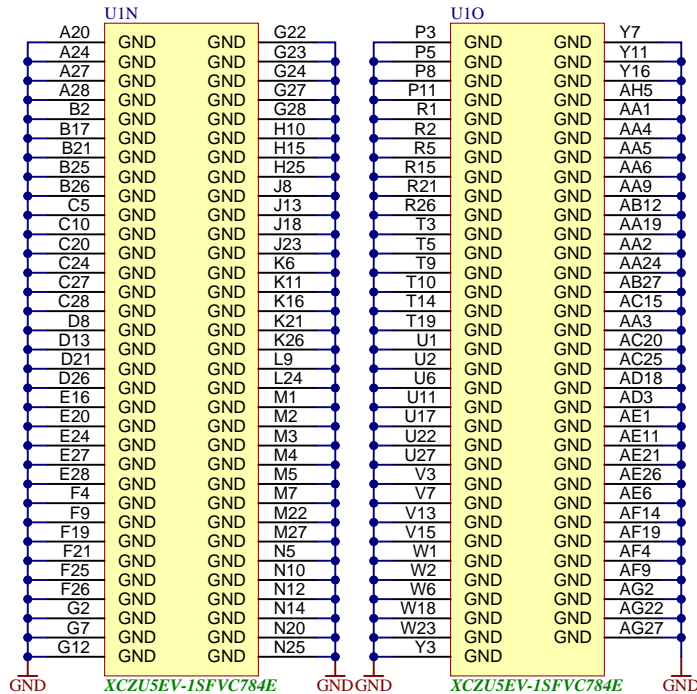
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Date: 04.08.2022	Copyright: Trenz Electronic GmbH	Page 14 of 30
Filename: PS_DDR.SchDoc		



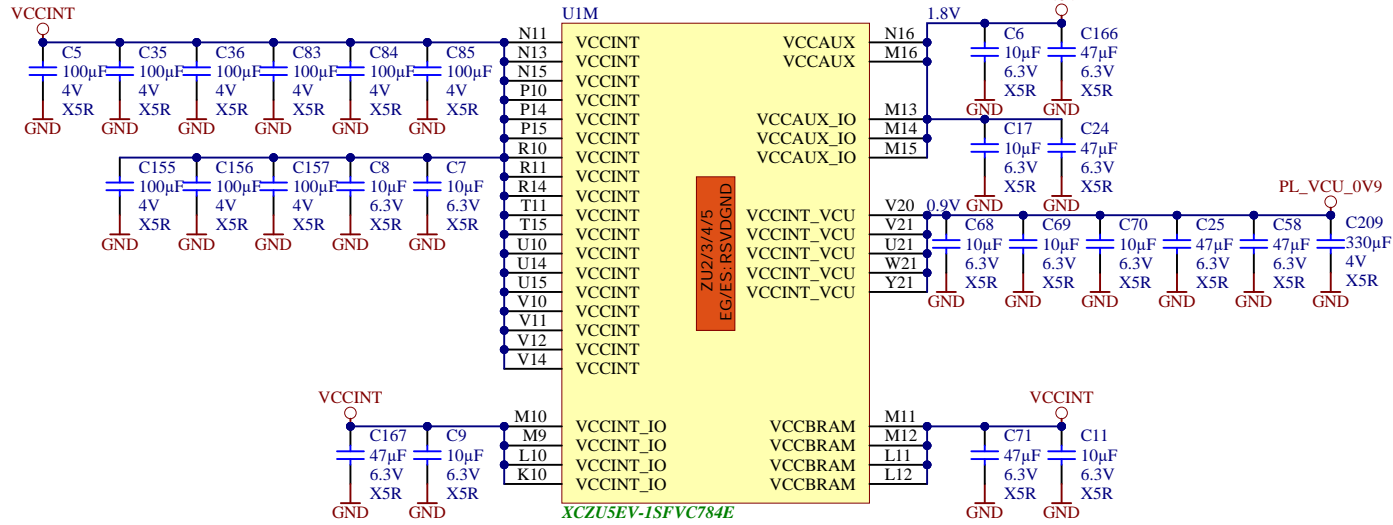

Speedgrade	VCCINT
-1	0.85 V
-2	0.85 V
-3	0.9 V



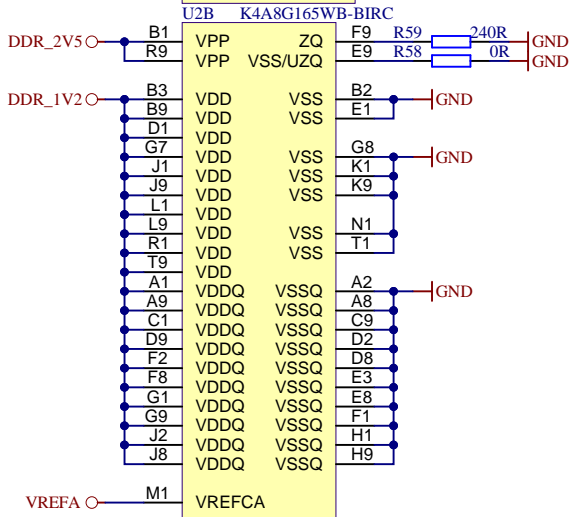
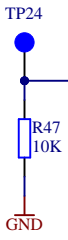
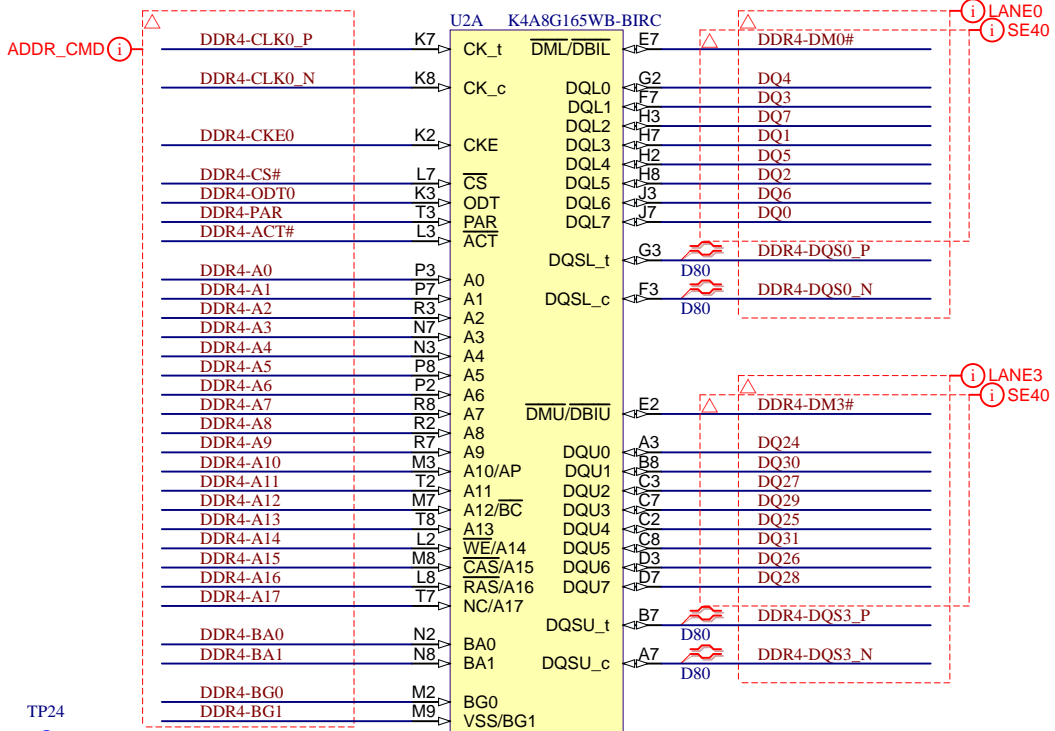
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	Date: 04.08.2022	Copyright: Trenz Electronic GmbH	Page 15 of 30
	Filename: ZU_PS_POWER.SchDoc		



Speedgrade	VCCINT
-1	0.85 V
-2	0.85 V
-3	0.9 V

Title: AM0010 – ZU_POWER		
A4	Number: ZU_POWER 5DE21MA	Rev. 02
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Title: AM0010 – DDR4-RAM		
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Date: 04.08.2022	Copyright: Trenz Electronic GmbH	Page 17 of 30
Filename: DDR4-RAM.SchDoc		

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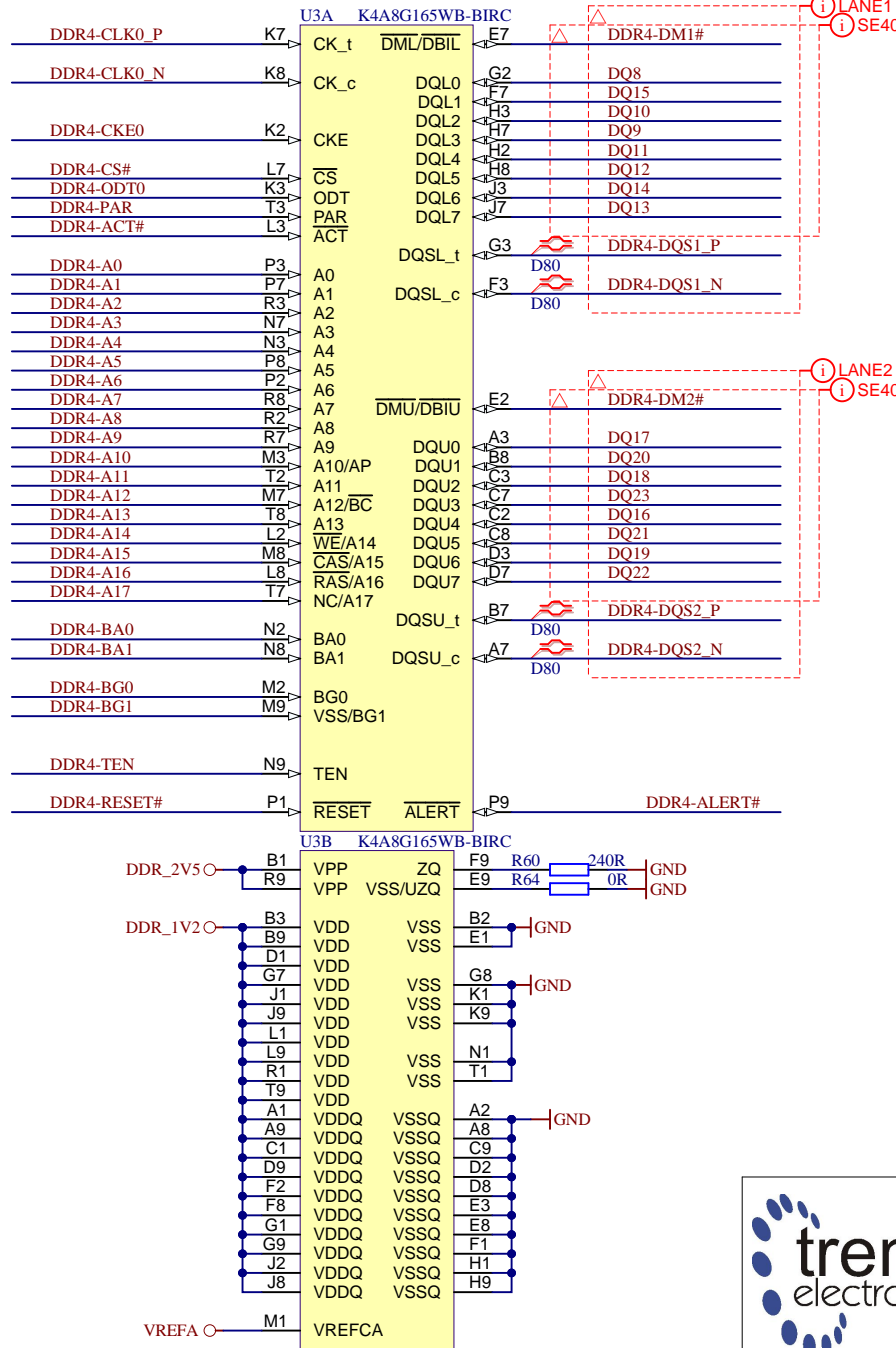

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A

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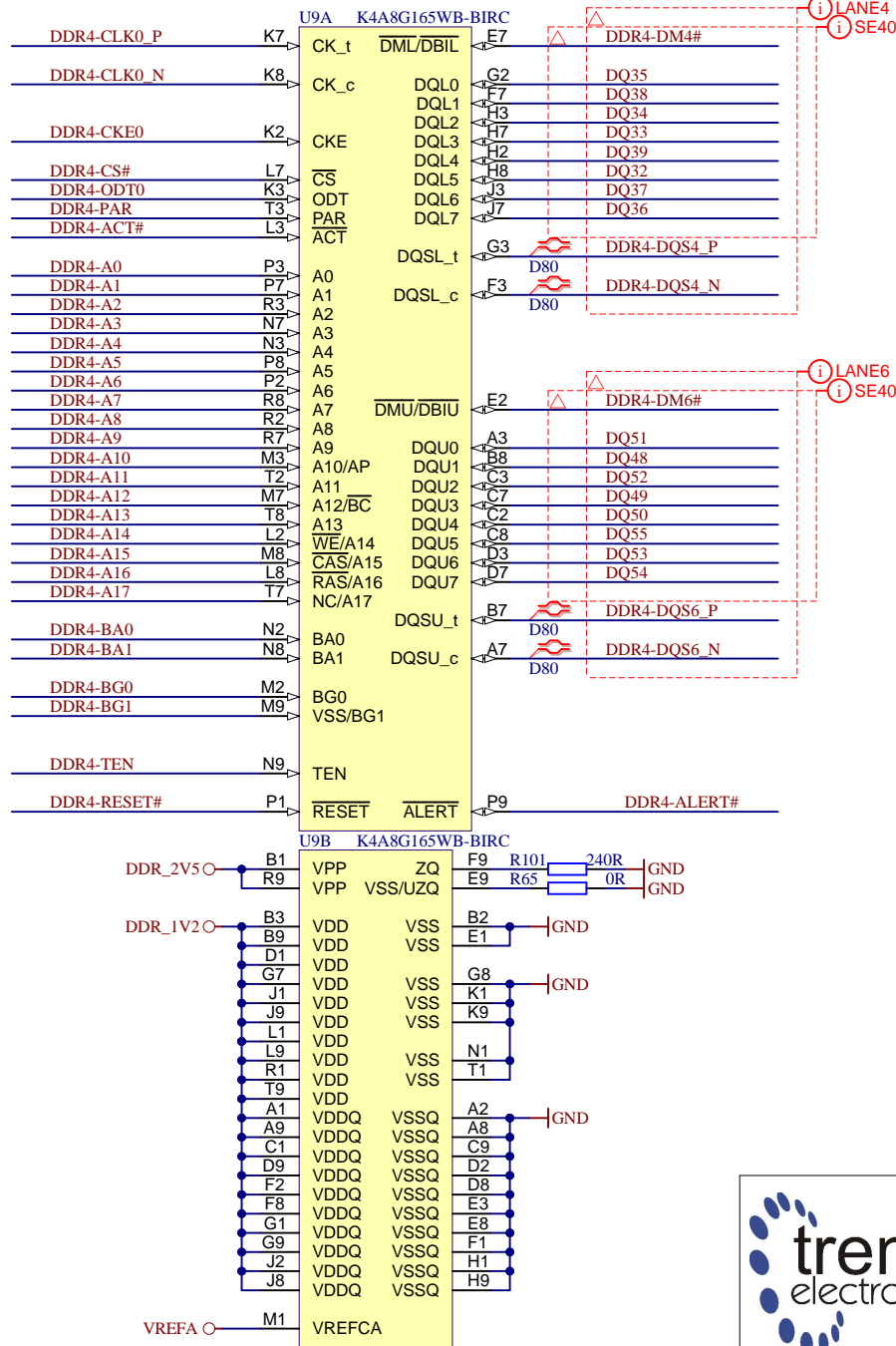

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Filename: DDR4-RAM_3.SchDoc		



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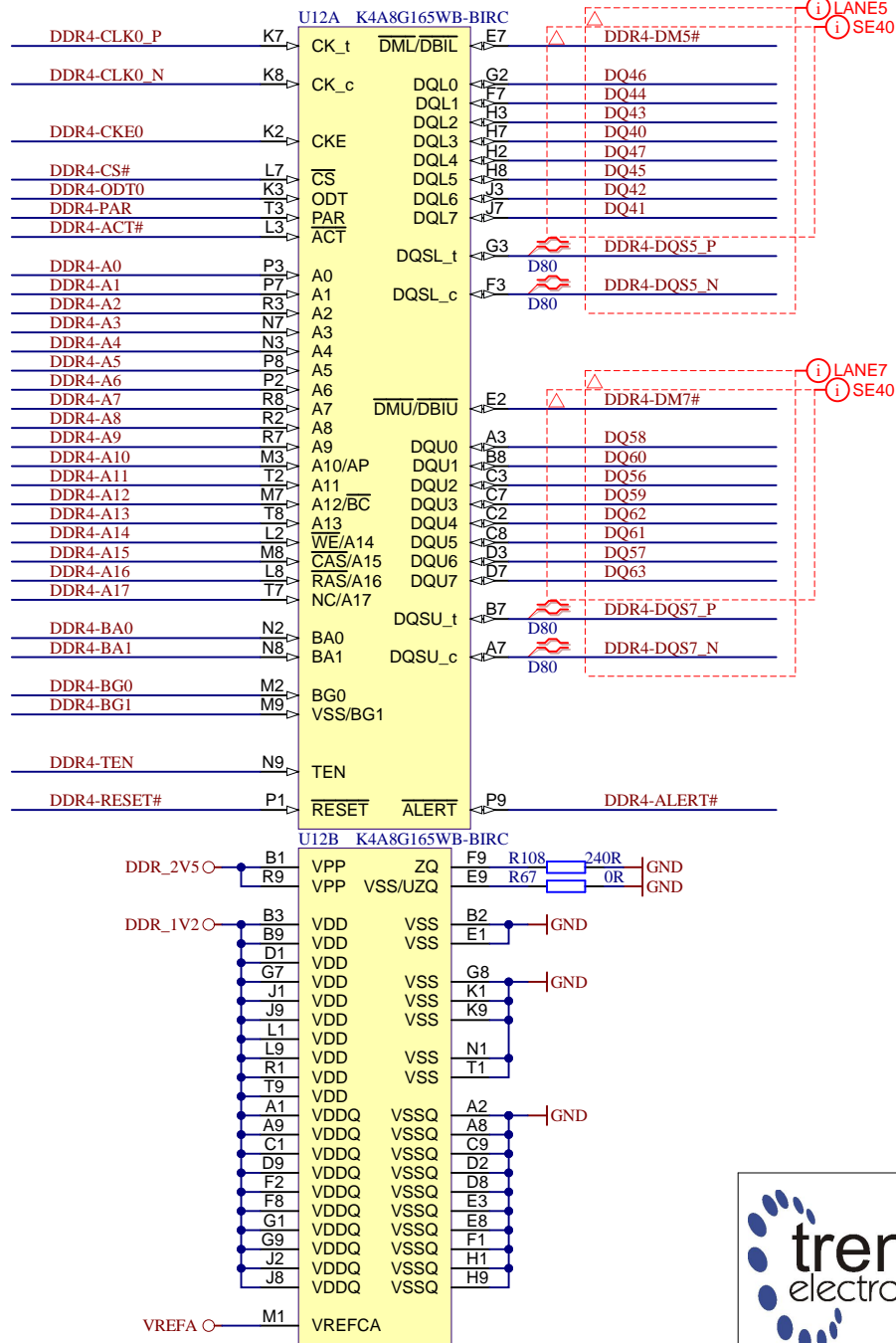

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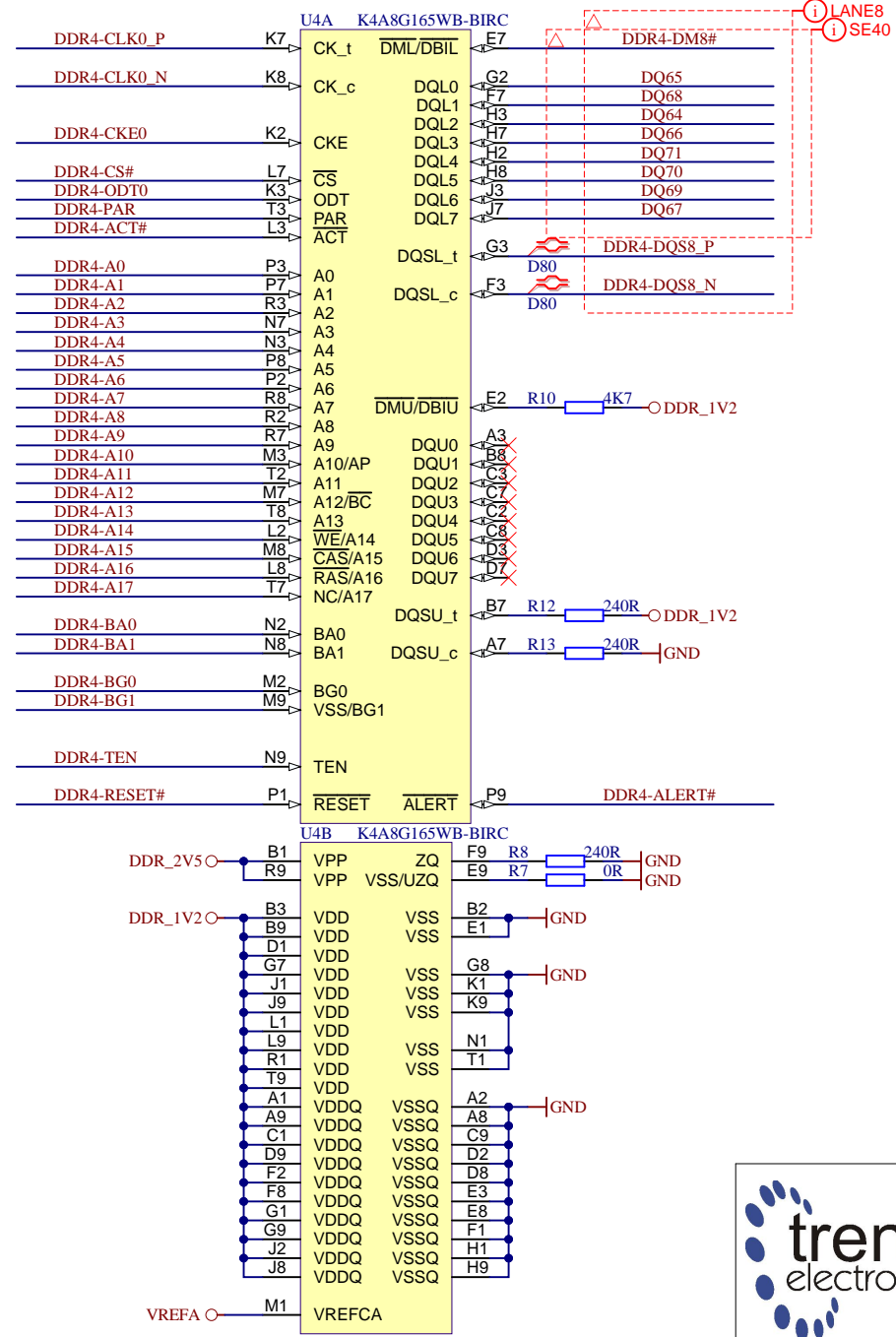
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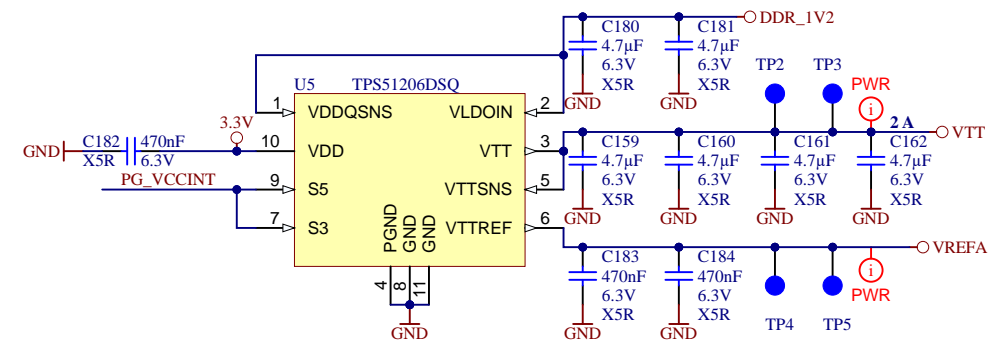
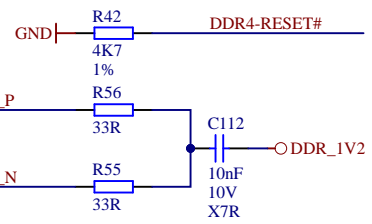
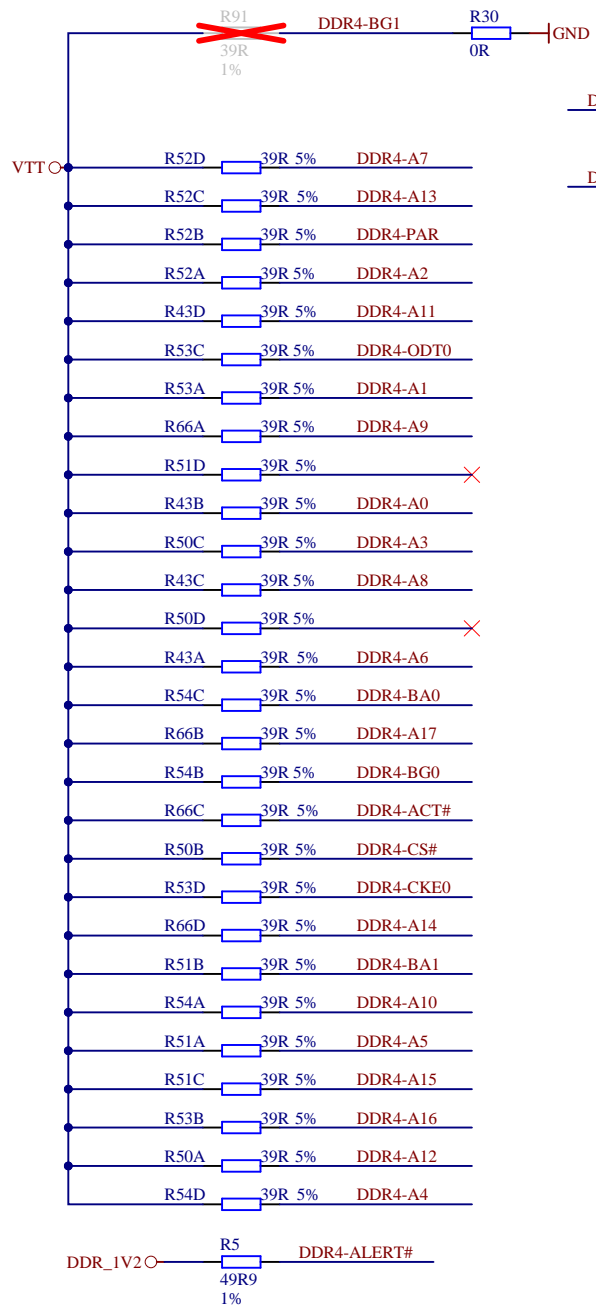
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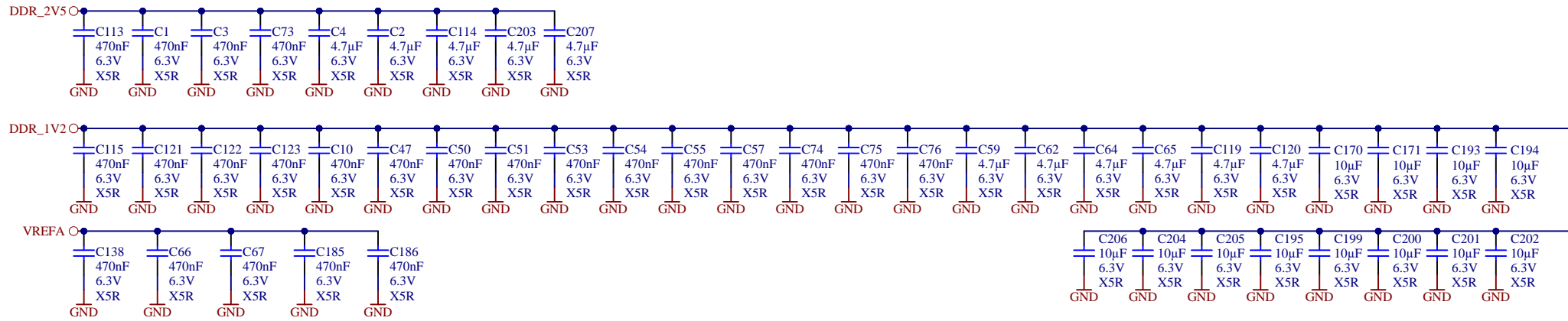
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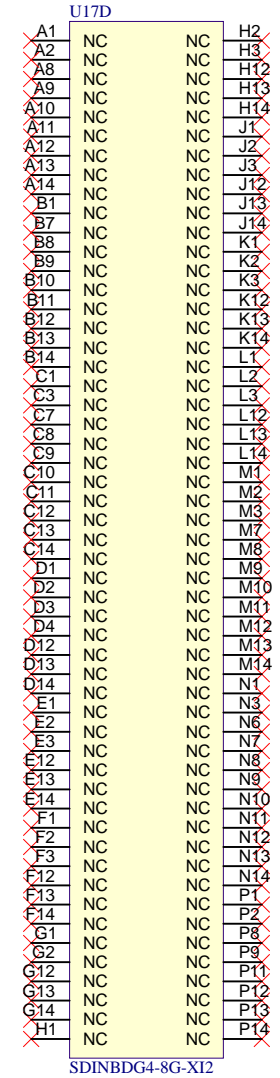
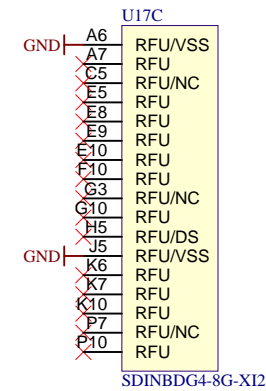
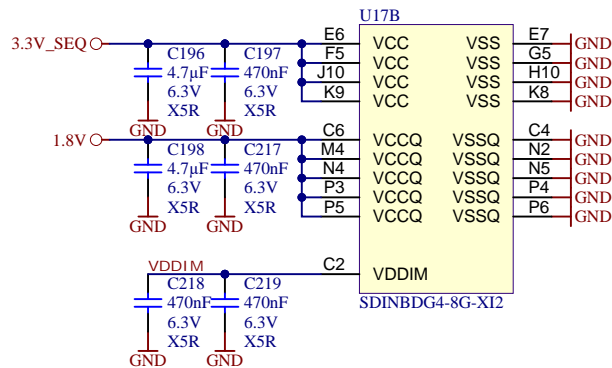
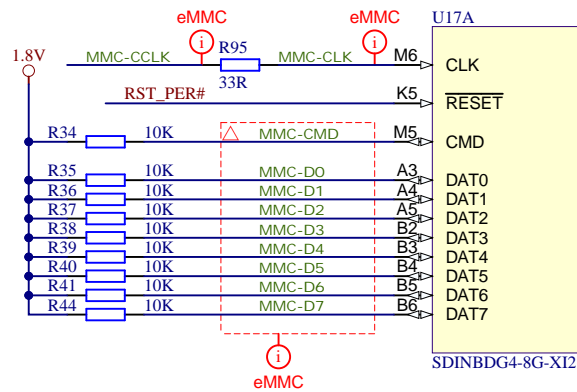
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Date: 04.08.2022	Copyright: Trenz Electronic GmbH	Page 21 of 30
Filename: DDR4-RAM_5.SchDoc		



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Filename: DDR4-CAPS.SchDoc		Page 23 of 30	

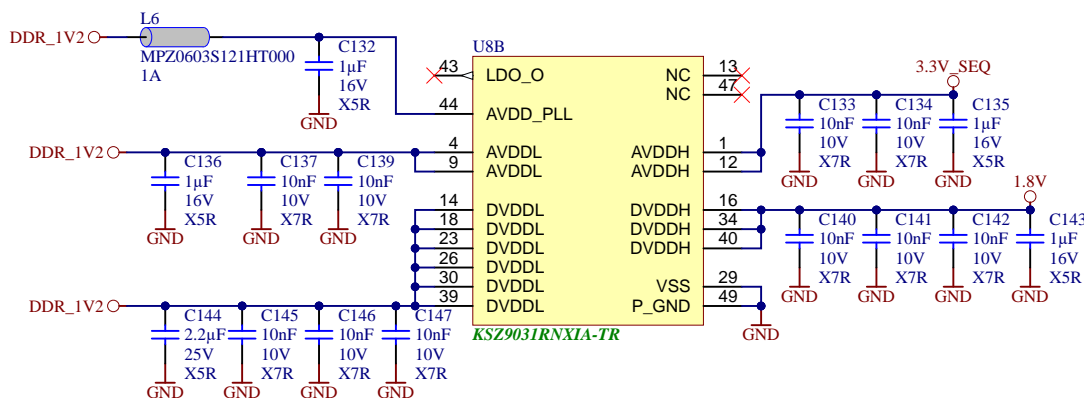
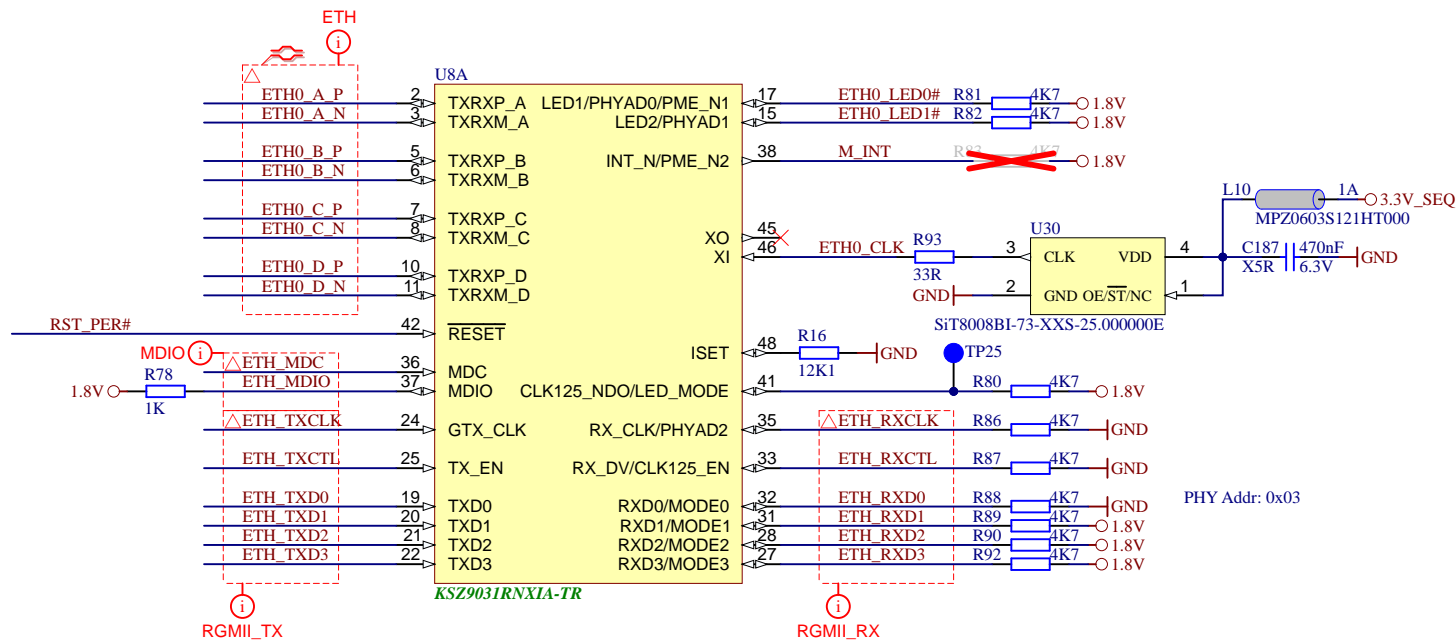



**trenz electronic**

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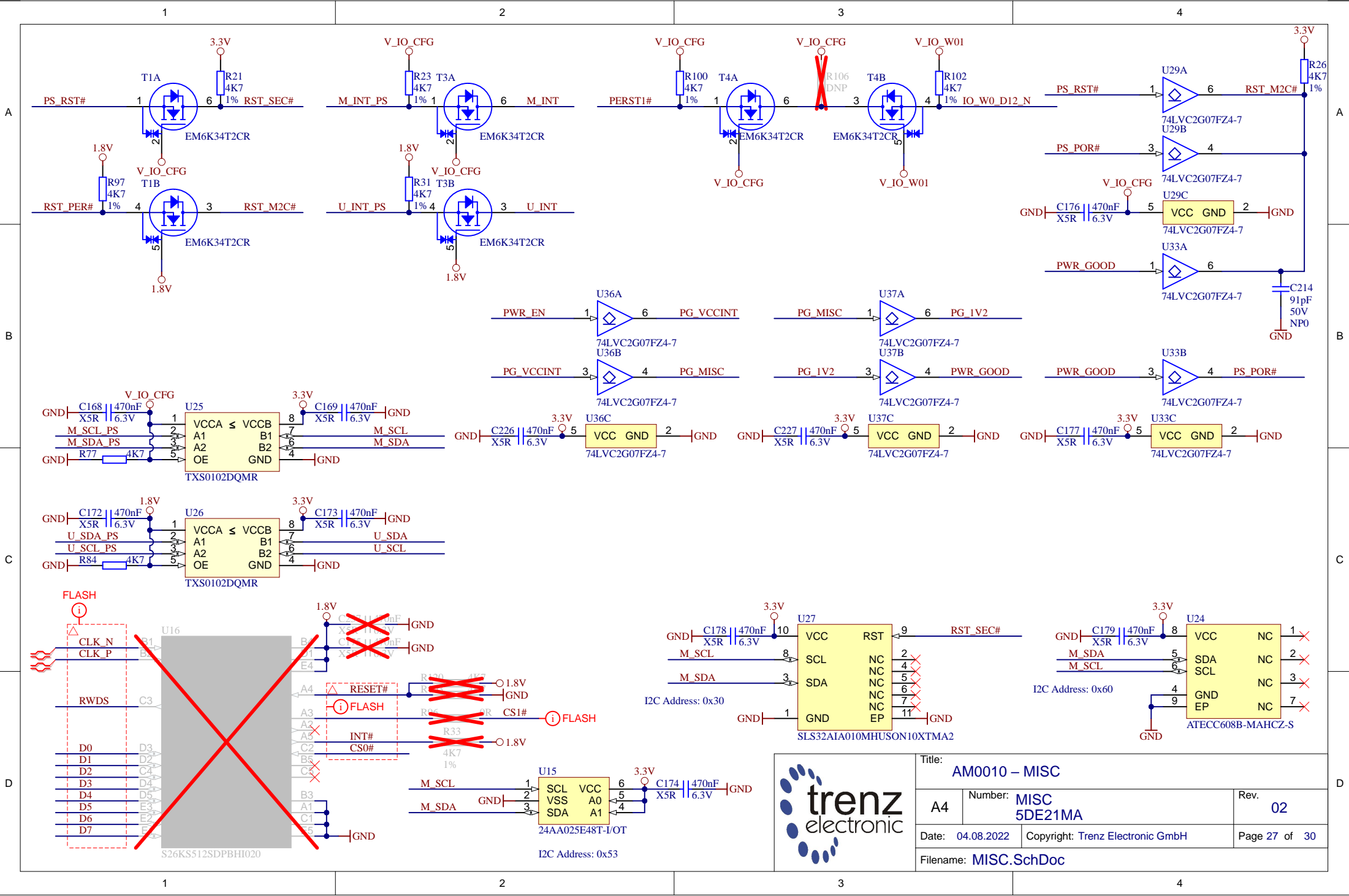
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		A4	Number: ETHPHY 5DE21MA
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Filename: ETHPHY.SchDoc		Page 25 of 30	
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Title: AM0010 – MISC		
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Filename: MISC.SchDoc		

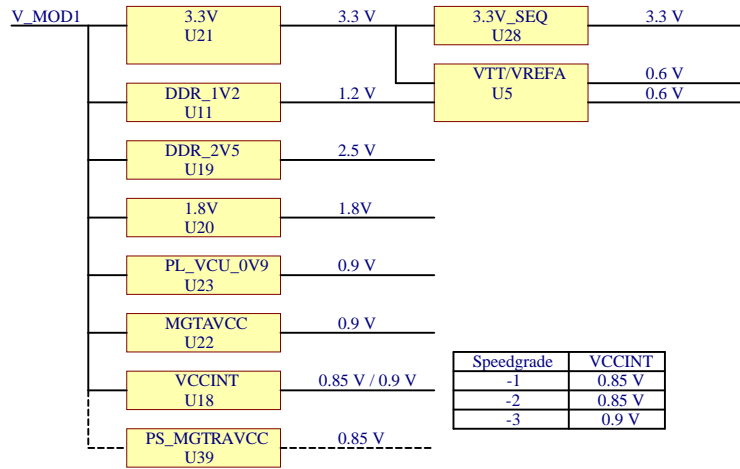
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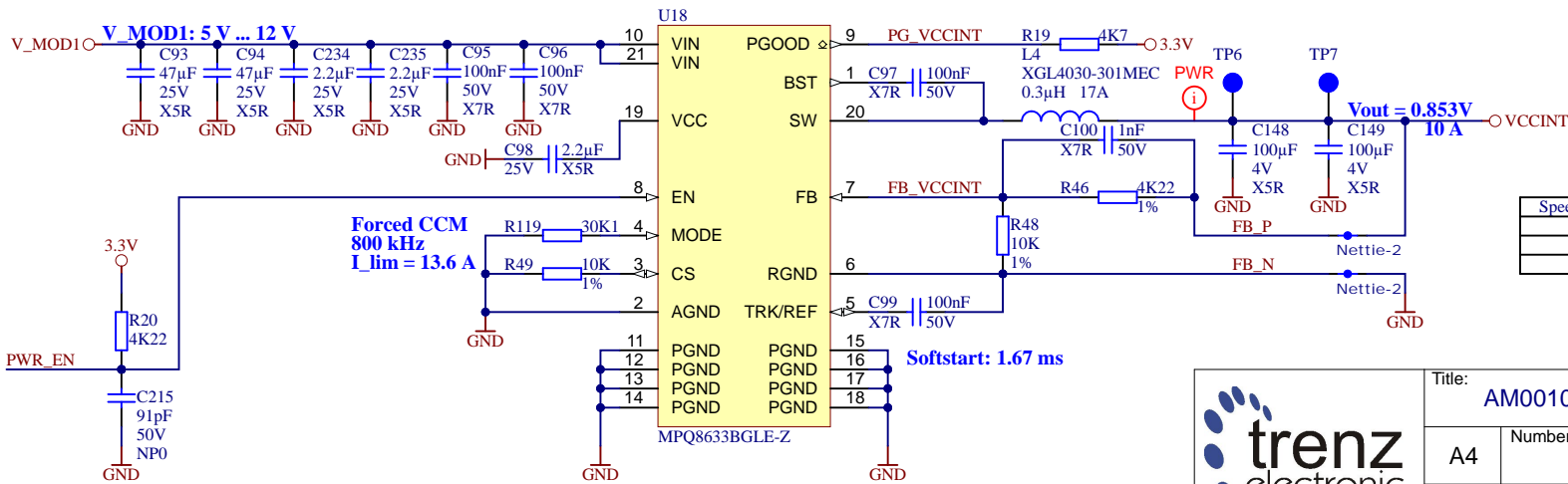
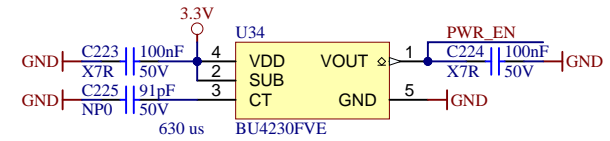
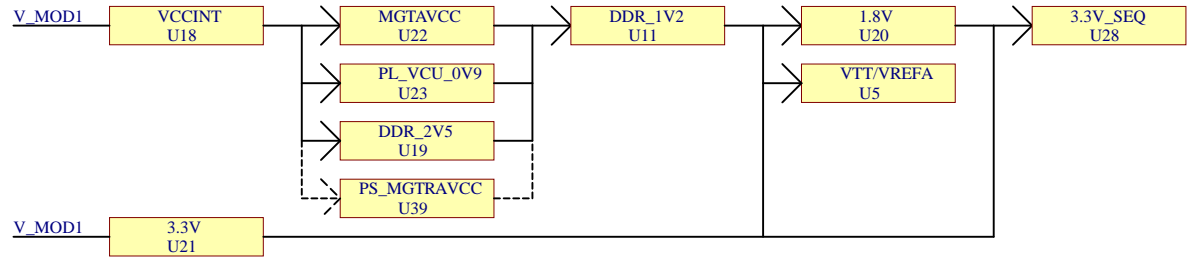
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### Power Supply Structure



Speedgrade	VCCINT
-1	0.85 V
-2	0.85 V
-3	0.9 V

### Power Supply Sequencing



Speedgrade	R46	R48	C100	VCCINT
-1	4K22	10K	1 nF	0.853 V
-2	4K22	10K	1 nF	0.853 V
-3	10K	20K	680 pF	0.900 V



Title: AM0010 - POWER_1		
A4	Number: POWER_1 5DE21MA	Rev. 02
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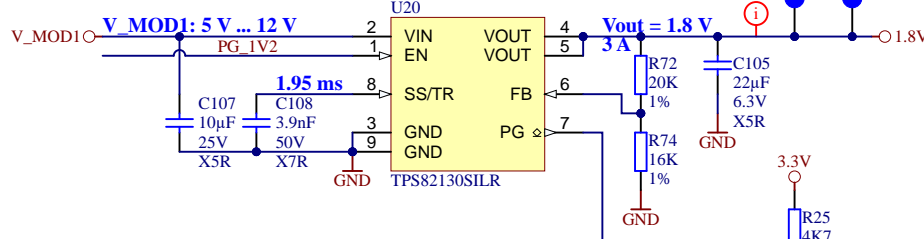
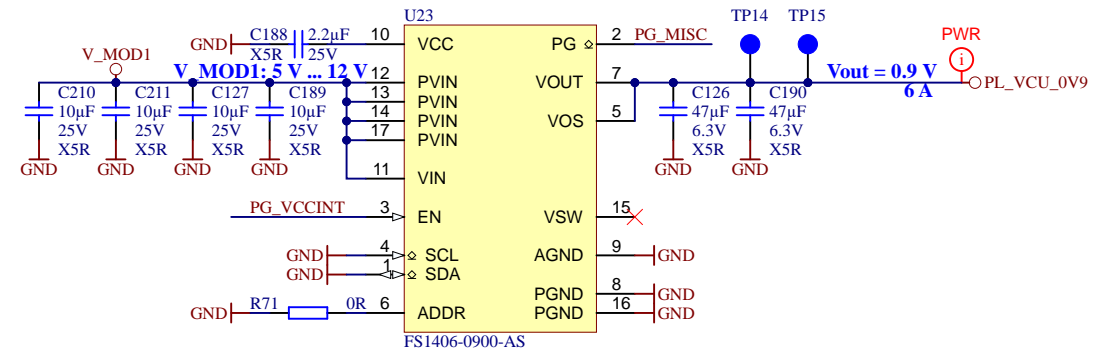
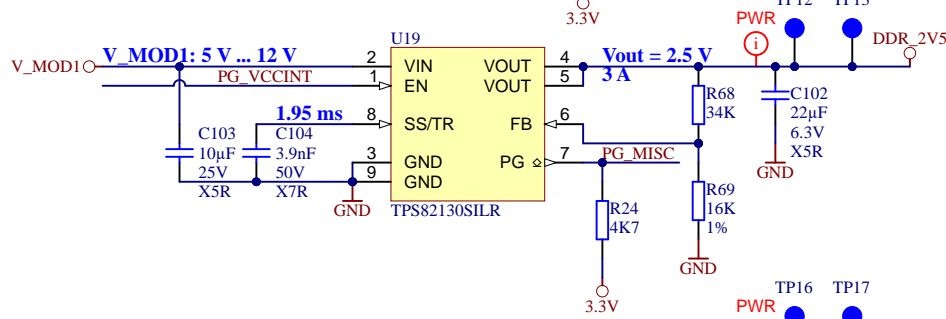
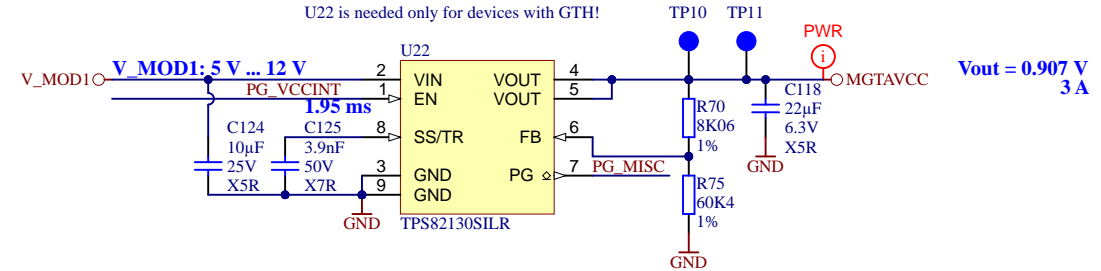
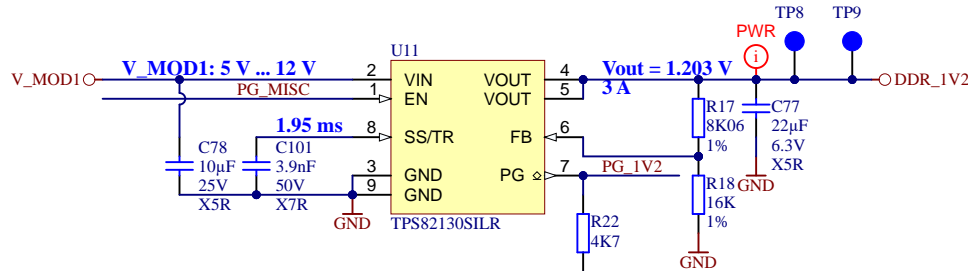
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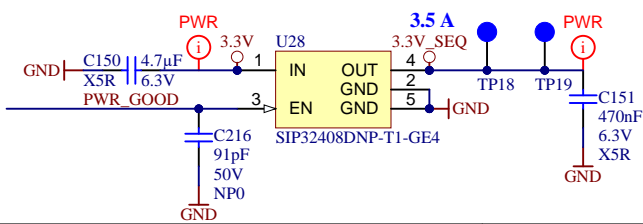
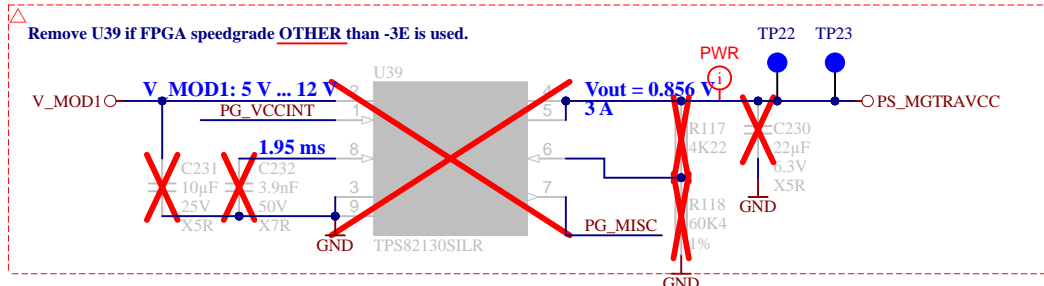
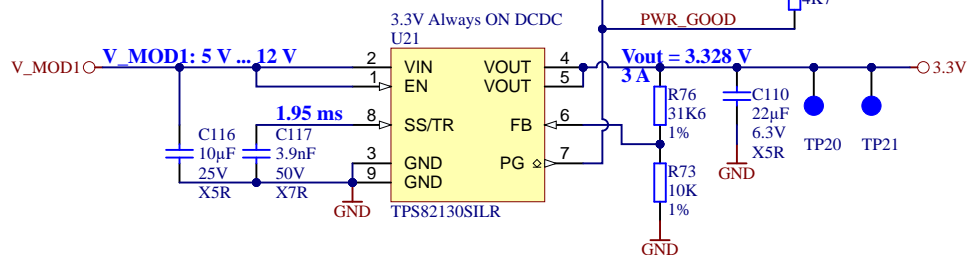


Remove L14 when FPGA speedgrade -3E is used

Speedgrade	L14	VCCINT
-1	L14	0.85 V
-2	L14	0.85 V
-3	DNP	0.9 V

VCCINT - L14 (3A, 120 Ohm@100 MHz) - PS\_MGTRAVCC

Vout\_max = 0.876V (+3%)  
 Vout\_nom = 0.85V  
 Vout\_min = 0.833V (-2%)



Title: AM0010 - POWER_2		
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