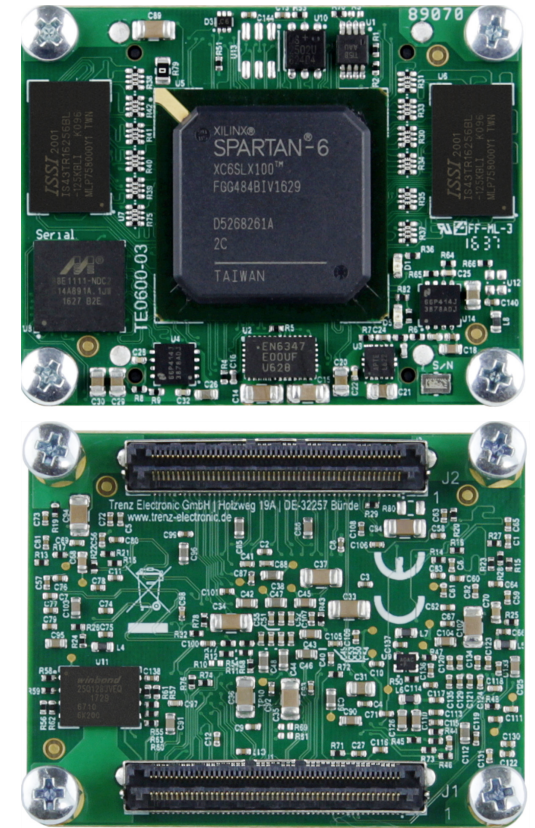




Regarding the usage of our schematics and alike documentation for Trenz module .

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0600 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: TE0600 - Legal Notices		
	A4	Number: TE0600 83I21-A	Rev. 04
	Date: 01-Sep-23	Copyright: Trenz Electronic GmbH	Page 1 of 13
	Filename: Legal_Notices.SchDoc		

1		2		3		4	
A	REV		Description				
	-01		Initial revision				
	-03		1) added NetTie (board revision 03) 2) optimized placement and routing pwr DCDC 3) added tespoints 4) changed OSC U9 (AN25008, SiT8008AI-73-XXS-25.000000E) 5) update Razorbeam Connectors, full update lib 6) added serial number (tracebility pad) 7) added thermal vias to mounting holes 8) changed SPI flash (AN26012,W25Q128FVEIG 3V 128MBit Serial Flash) 9) changed DDR3 (AN27202, AN27039) 10) U13 (DS2432P+) is not populated				
B	-04		1) Leds D1 , D5 were changed to SML-P11MTT86 2) R83 was added. R29 was changed from 2.2k to 100 3) D3 was changed from single BAT54VV,115 to pair BAT54A,215 4) U2 was changed from EN6347QI to MPM3860GQW-Z 5) U3 was changed from EP53F8QI to MPM3834CGPA 6) Stacked vias were removed 7) Net BR0 was connected to GND 8) B2B signal groups information was added 9) Field filename was renamed for all schematic pages 10) Legal Notices page was added 11) System overview and power-on sequencing were added for TE0600.SchDoc page 12) Testpoints TP11 - TP14 , TP23 - TP28 were added 13) R56 , R57 , R58 were changed from 2k2 to 2k4 14) U12 was fitted for all module assembly variants 15) R36 was changed from 120R to 240R, R84 and T1 were added 16) U4 and U14 were changed from LP3878SD-ADJ to TPS74601PBDRV1		MT		
C							
D							
1		2		3		4	



Title:TE0600 - Changes list

A4

Number:GigaBee FPGA Module83I21-A

Rev.04

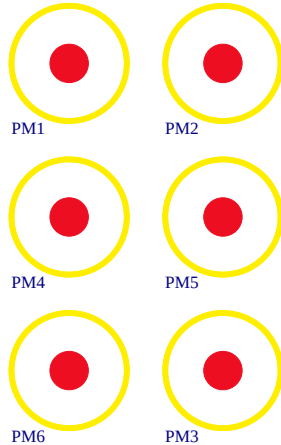
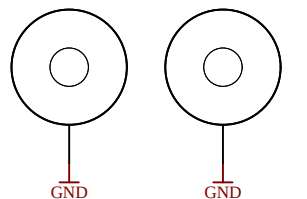
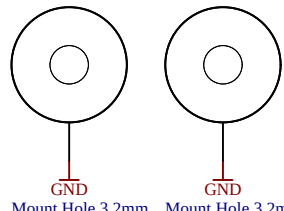
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Copyright: Trenz Electronic GmbH

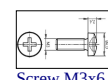
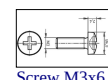
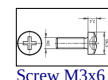
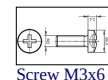
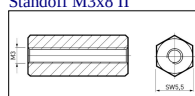
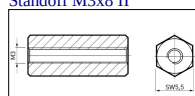
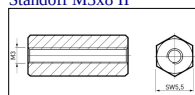
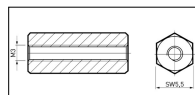
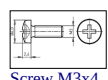
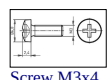
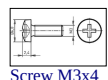
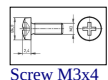
Page 2 of 13

Filename:Revision_Changes.SchDoc

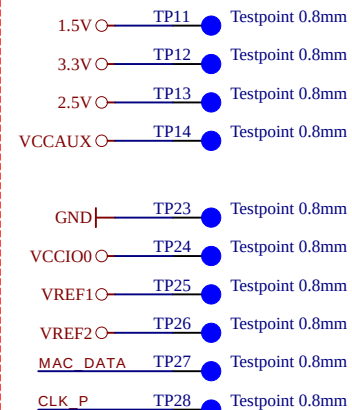
Mount.Hole 3.2mm Mount.Hole 3.2mm



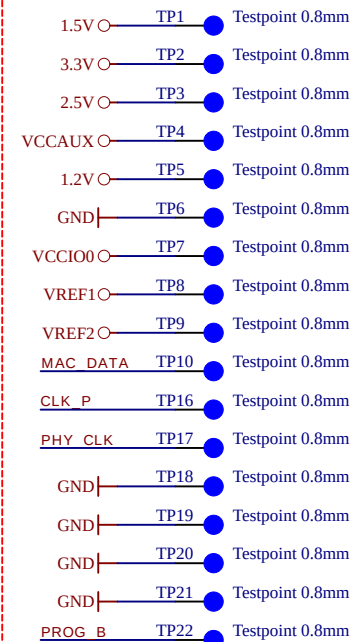
Top of Board



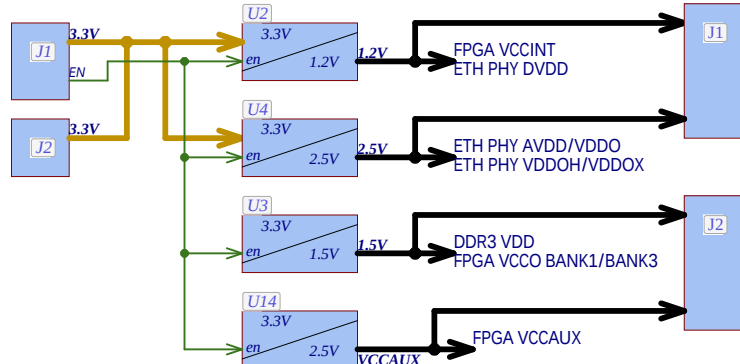
Top side testpoints:



Bottom side testpoints:



Power-on sequencing

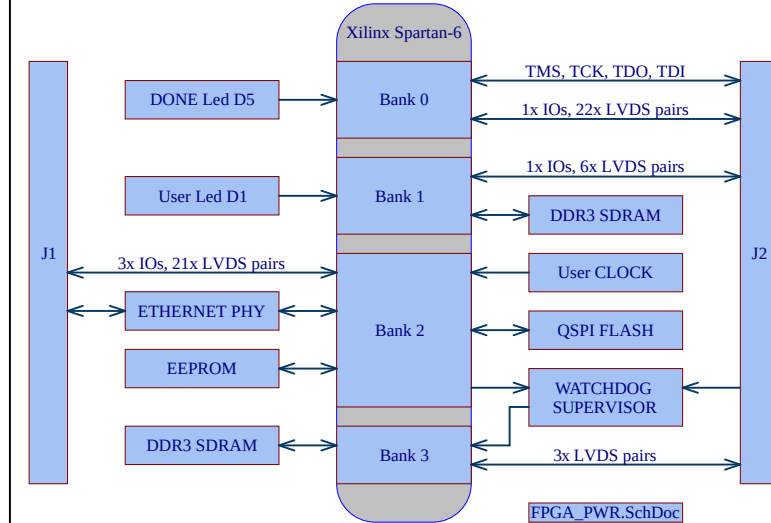


Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3V	IN	3.3V	+/-5%	Micromodule Power	-
VCCIO0	IN	1.1 - 3.45V	+/-5%	IO Bank0	-
1.2V	OUT	1.2V	+/-3%	Power for Carrier	-
1.5V	OUT	1.5V	+/-3%	Power for Carrier	-
2.5V	OUT	2.5V	+/-3%	Power for Carrier	-
VCCAUX	OUT	2.5V	+/-3%	Power for Carrier	-

Special notes:

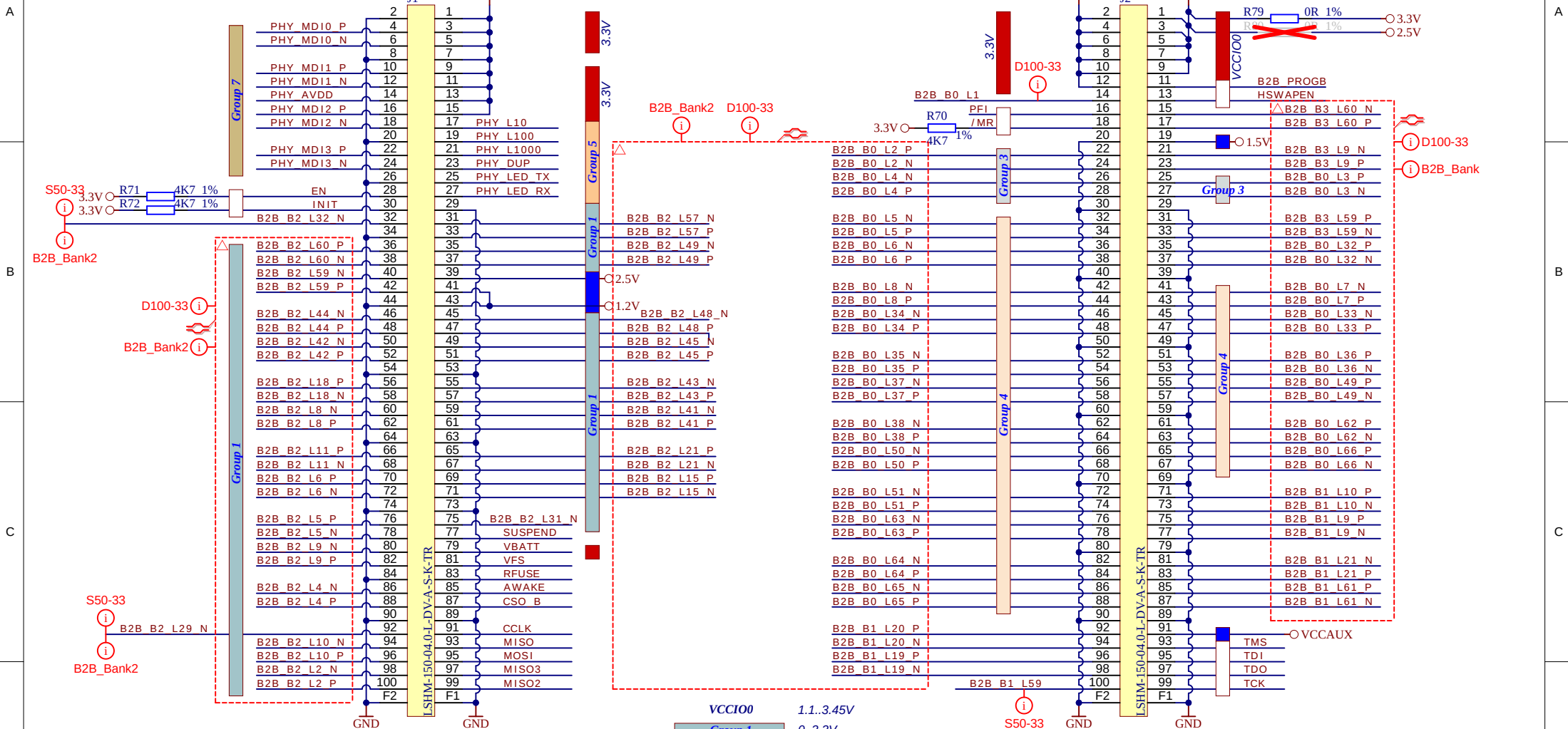
System Overview



Title: TE0600		
A4	Number: GigaBee FPGA Module 83I21-A	Rev. 04
Date: 04-Dec-23	Copyright: Trenz Electronic GmbH / TT	Page 3 of 13
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B2: 45 Pins: 21 Differential; 3.3V Fixed VCCIO
ETHERNET PHY 10/100/1G

B0: 45 Pins: 22 Differential; variable VCCIO
B1: 13 Pins: 6 Differential; 1.5V Fixed
B3: 6 Pins: 3 Differential; 1.5V Fixed
JTAG: 3.3V Level



VCCIO0	1.1...3.45V
Group 1	0..3.3V
Group 3	0..VCCIO0
Group 4	0..VCCIO0
Group 5	
Group 7	ETHERNET
Special	
	PWR_in
	PWR_out



Title: TE0600 - B2B Connectors		
A4	Number: GigaBee FPGA Module 83I21-A	Rev. 04
Date: 29-Nov-23	Copyright: Trenz Electronic GmbH / TT	Page 4 of 13
Filename: B2B.SchDoc		

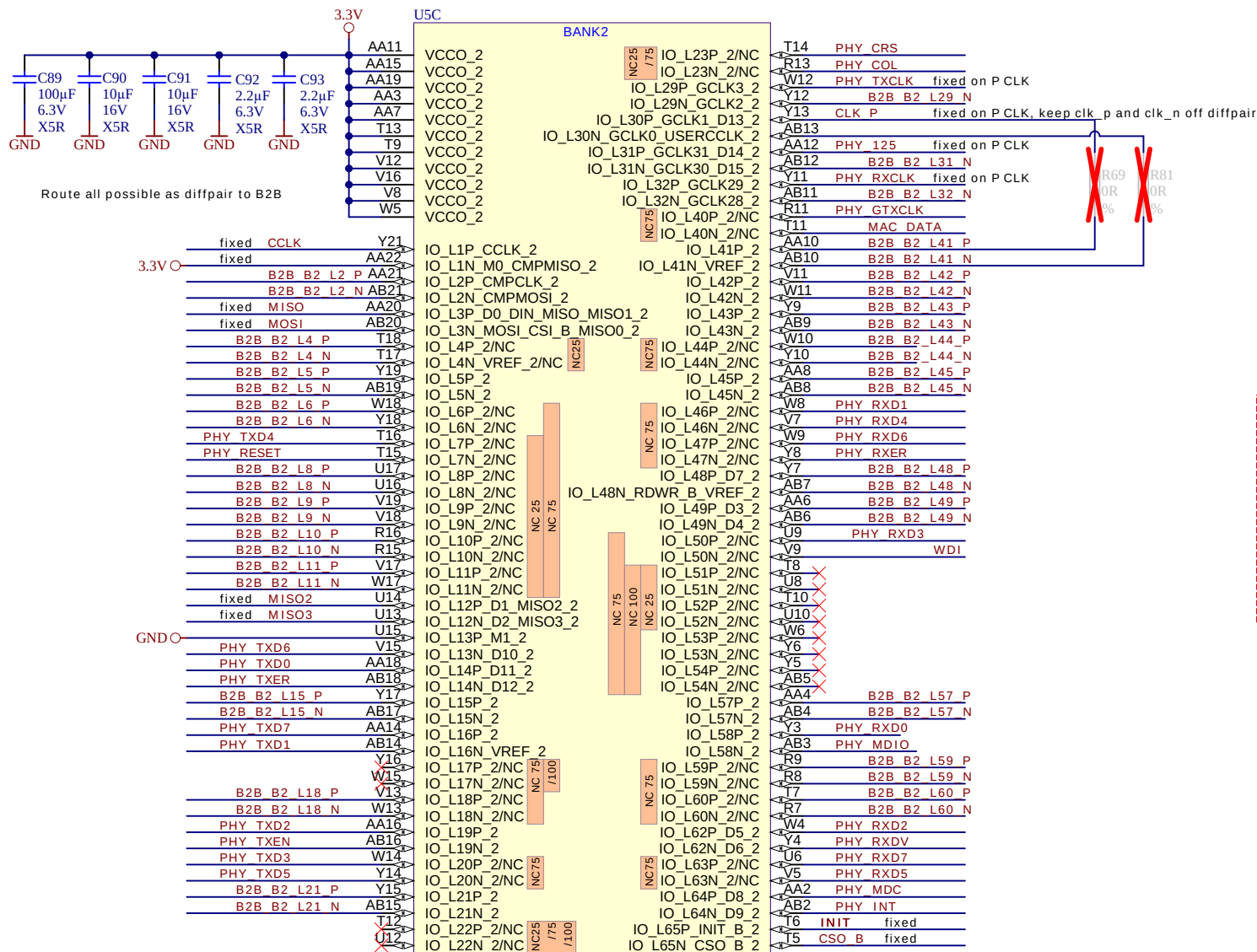
1

2

3

4

B2B_Bank2 S50-33



Don't use pins, which are marked NC100



Title: TE0600 - FPGA BANK2		
A4	Number: GigaBee FPGA Module 83I21-A	Rev. 04
Date: 30-Nov-23	Copyright: Trenz Electronic GmbH / TT	Page 7 of 13
Filename: BANK2.SchDoc		

1

2

3

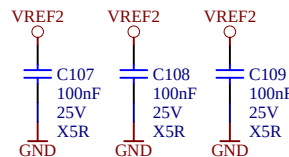
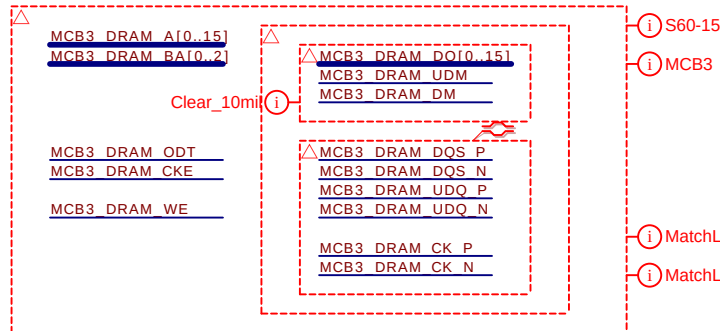
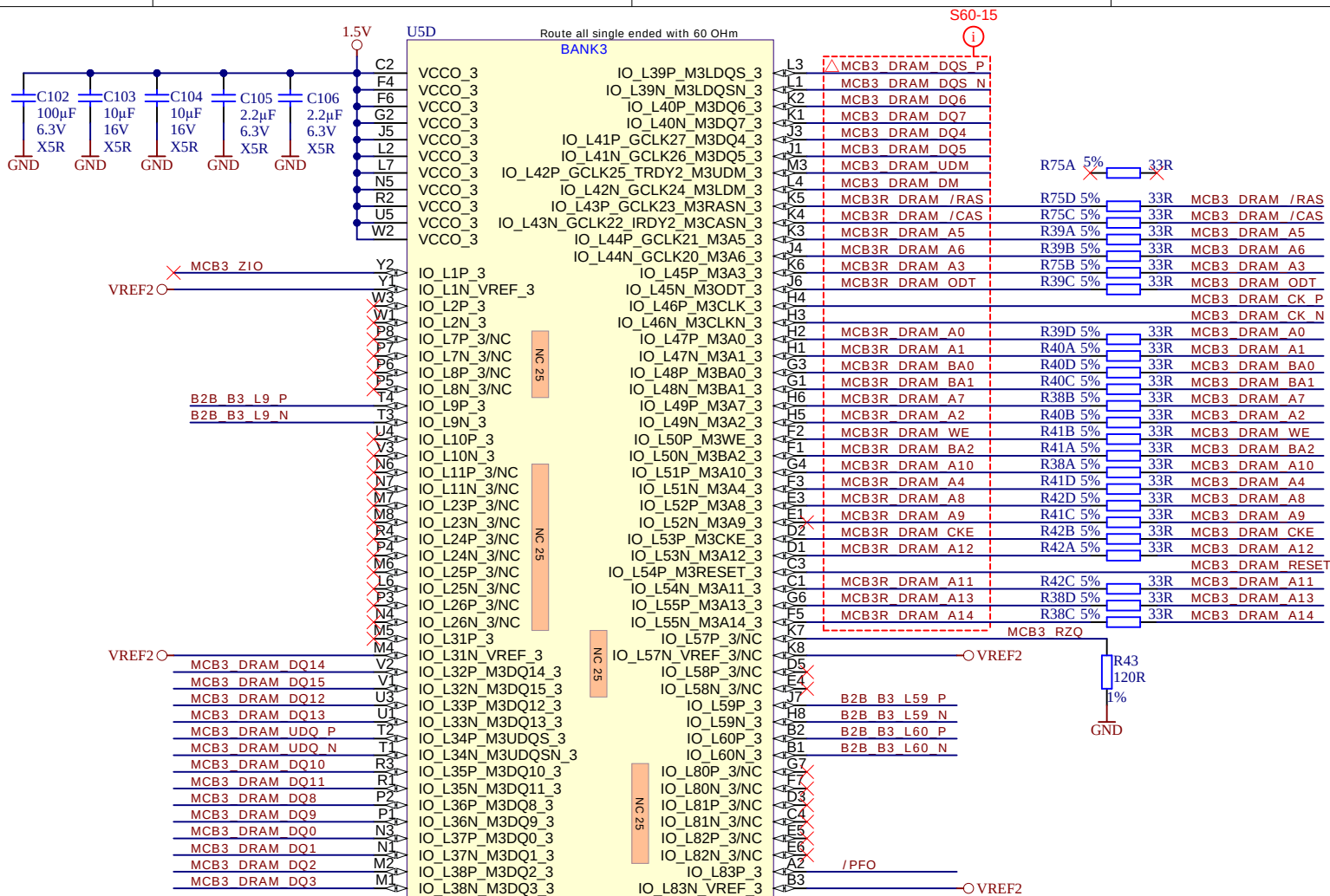
4

1

2

3

4



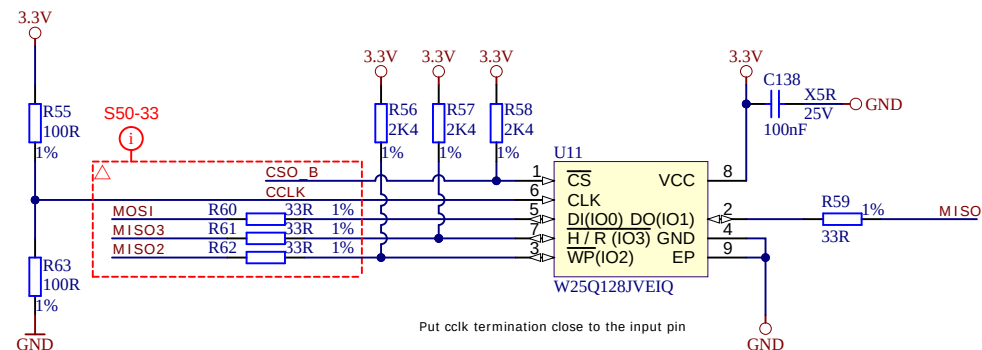
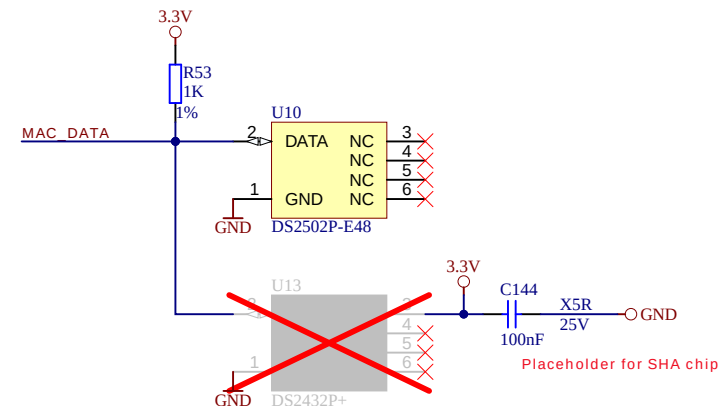
Title: TE0600 - FPGA BANK3 DDR		
A4	Number: GigaBee FPGA Module 83I21-A	Rev. 04
Date: 30-Nov-23	Copyright: Trenz Electronic GmbH / TT	Page 8 of 13
Filename: BANK3_DDR.SchDoc		

1

2

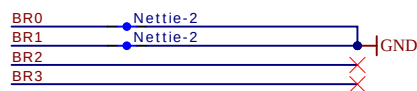
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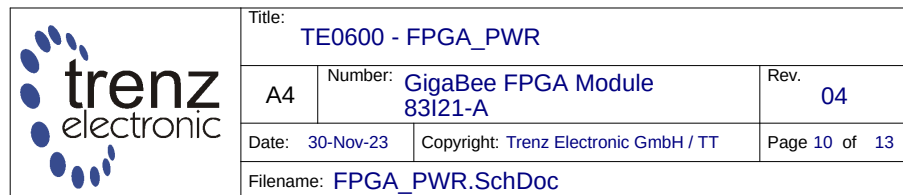


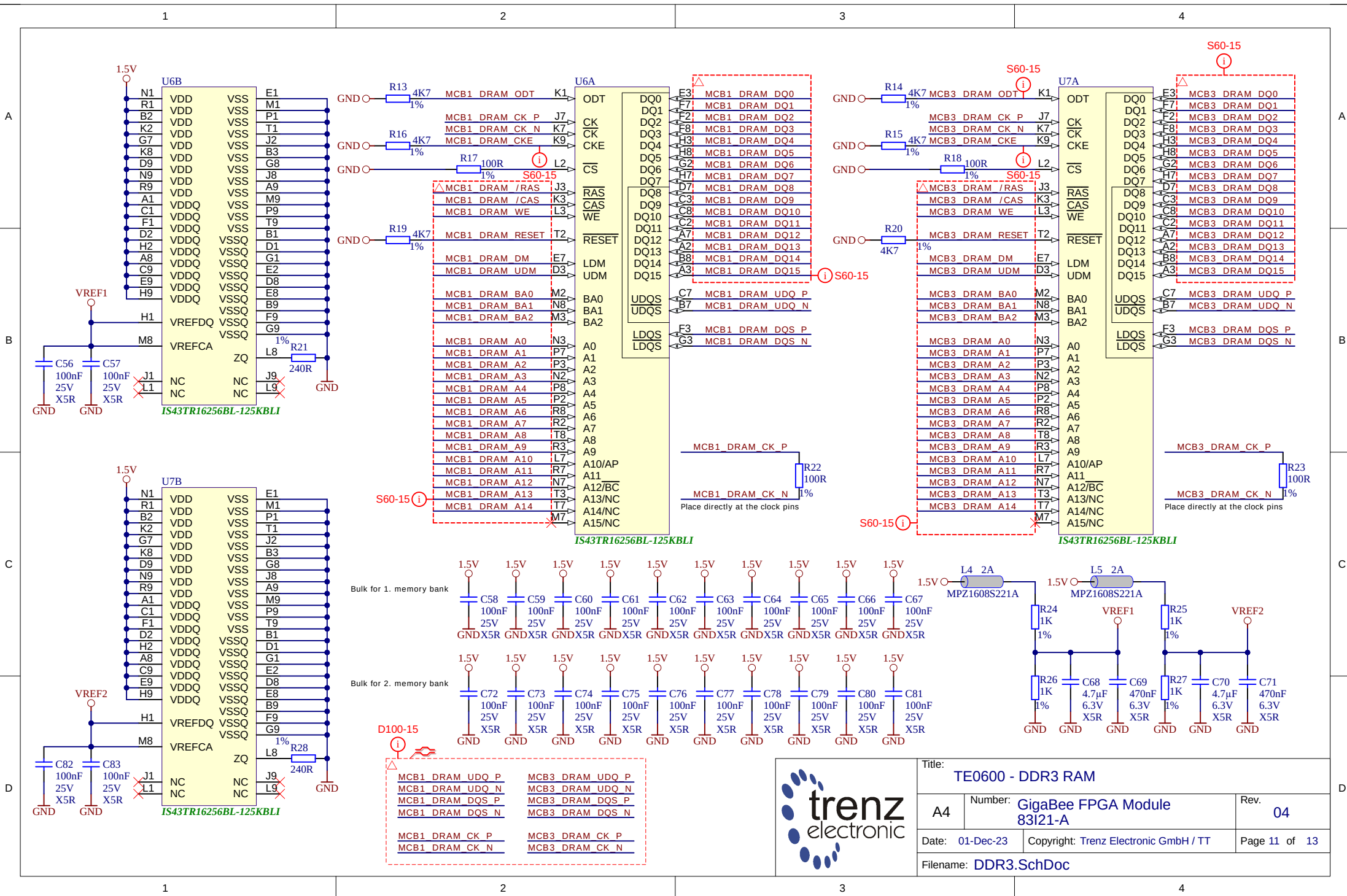
BR3	BR2	BR1	BR0	
1	1	1	1	-01 Initial revision
1	1	1	0	-02
1	1	0	1	-03
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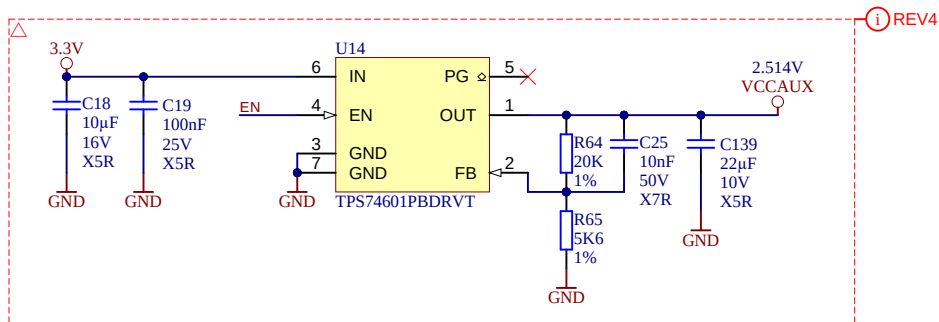
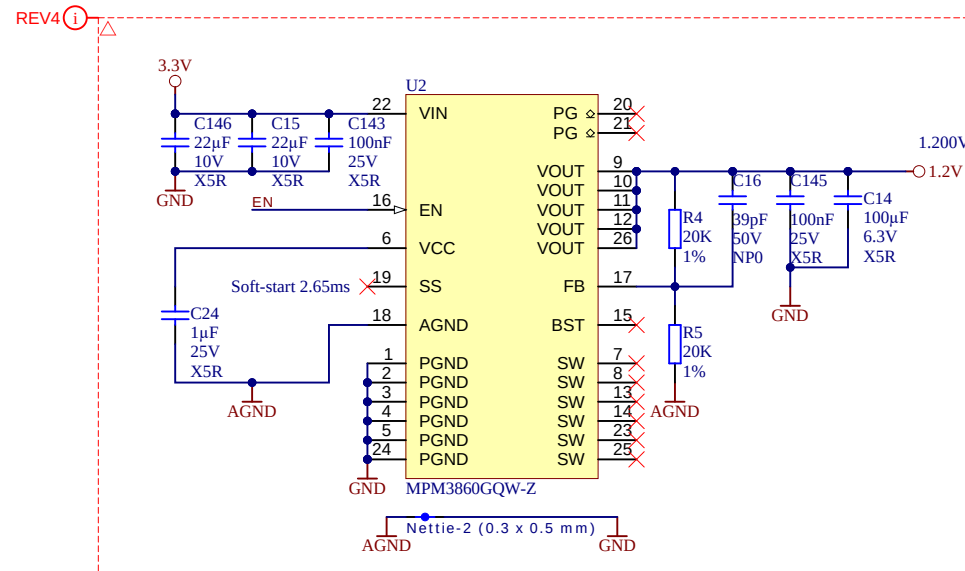
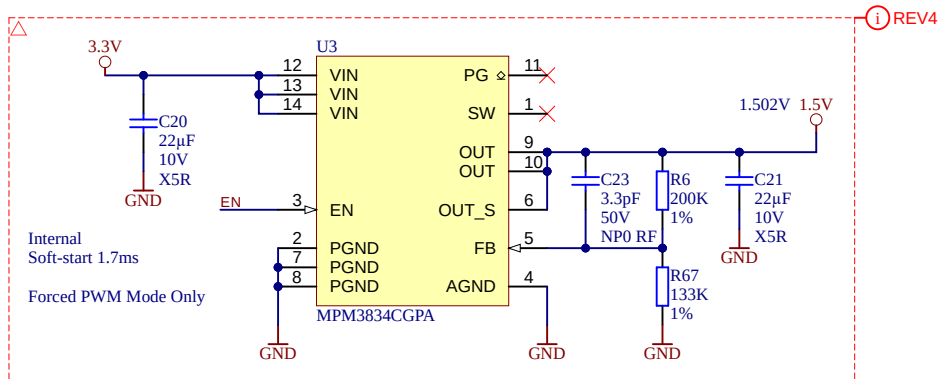
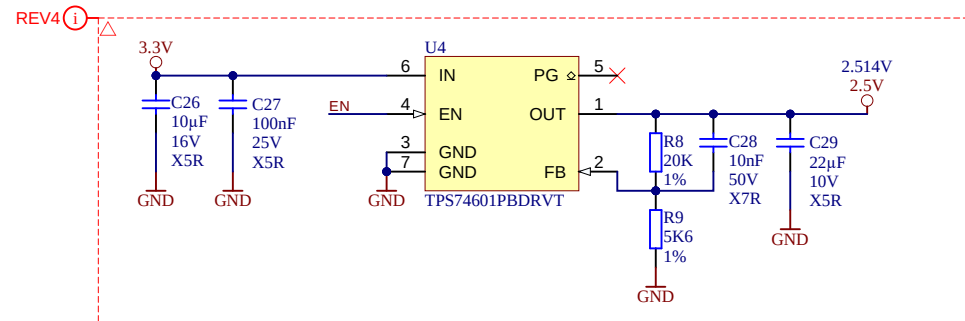
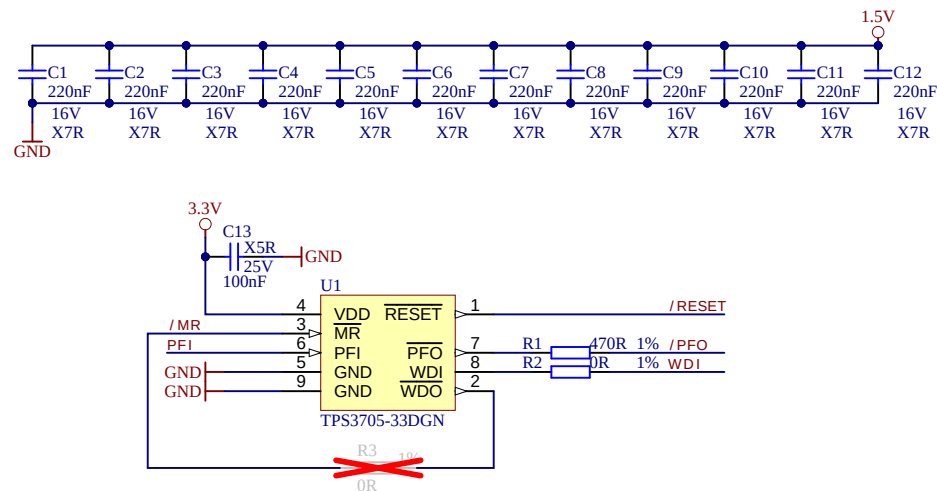
Board Revisions



Title: TE0600 - FPGA CFG			
A4	Number: GigaBee FPGA Module 83I21-A	Rev. 04	
Date: 29-Nov-23	Copyright: Trenz Electronic GmbH / TT		Page 9 of 13
Filename: FPGA CFG.SchDoc			







Title: TE0600 - POWER		
A4	Number: GigaBee FPGA Module 83I21-A	Rev. 04
Date: 05-Dec-23	Copyright: Trenz Electronic GmbH / TT	Page 13 of 13
Filename: POWER.SchDoc		

