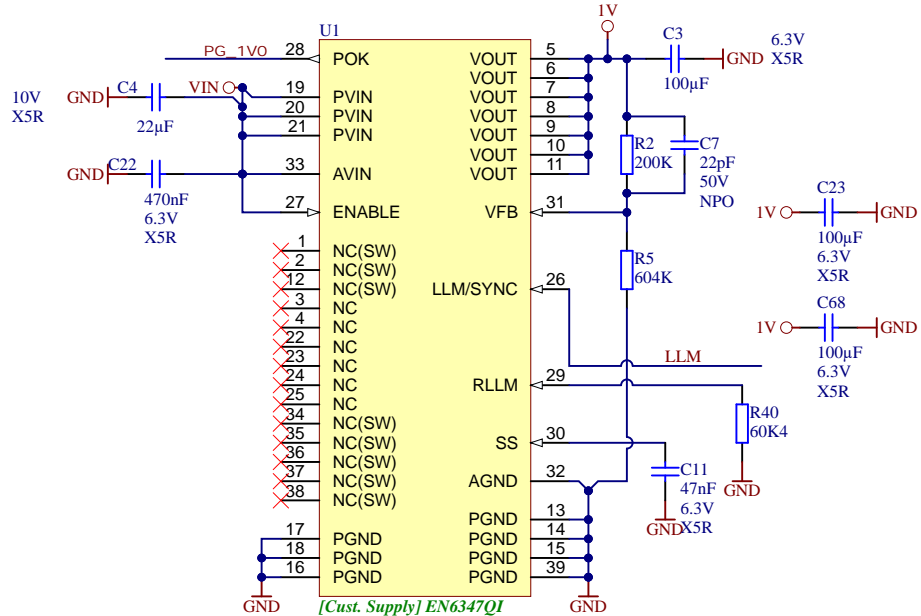
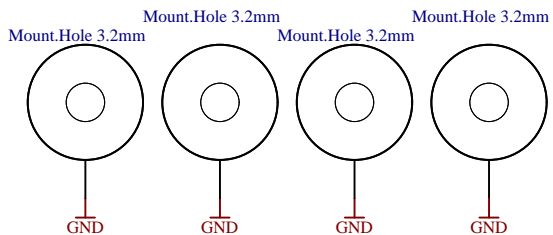
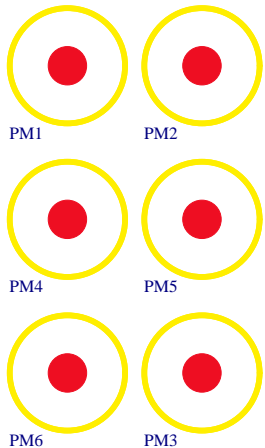
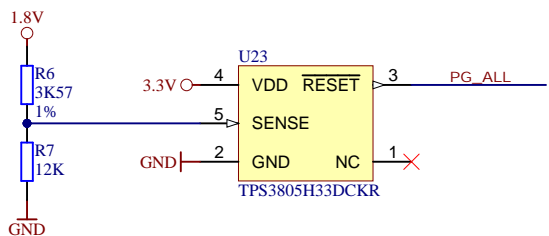
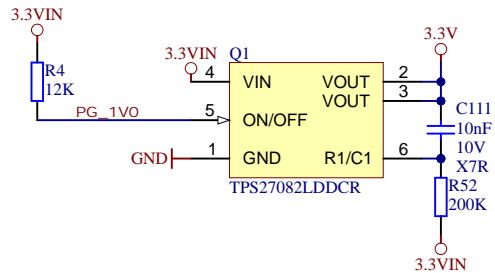
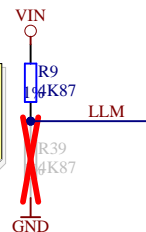


U_B2B_Connector	U_PLL
B2B_Connector.SchDoc	PLL.SchDoc
U_B14_B16	U_POWER
B14_B16.SchDoc	POWER.SchDoc
U_B15	
B15.SchDoc	
U_B34	
B34.SchDoc	
U_B35-RAM	
B35-RAM.SchDoc	
U_DDR3-MEM	
DDR3-MEM.SchDoc	
U_ETHERNET	
ETHERNET.SchDoc	
U_FPGA_CFG	
FPGA_CFG.SchDoc	
U_FPGA_PWR_MISC	
FPGA_PWR_MISC.SchDoc	

LOGO1
TE Logo PRINT Layer
LOGO PRINT

Select which resistor to mount with assembly variant!
Pullup switch DCDC to light load mode



Top of Board



Assembly variant	100-2CFV
Created by	VY
Modified by	VY
Modified at	2021-03-03
SVN Revision	8563



Title: TE0710		
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Dual 10/100 Ethernet Interface
 4 system controller IO Pins; 3.3V VCCIO
 B14 8 Pins Single ended IO; 3.3V Fixed VCCIO; replacing MIO0 pins on TE0720
 B16 6 Pins; 3 Differential; 3.3V Fixed VCCIO; TE0720 SD Card compatible
 B15: 48 Pins; 24 Differential; variable VCCIO

Total maximum I/O: 112
 JM2 total I/O: 50
 JM1 total I/O: 62

B34: 50 Pins; 24 Differential; variable VCCIO
 JTAG or IO (4 pins); 3.3V Levels

A

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C

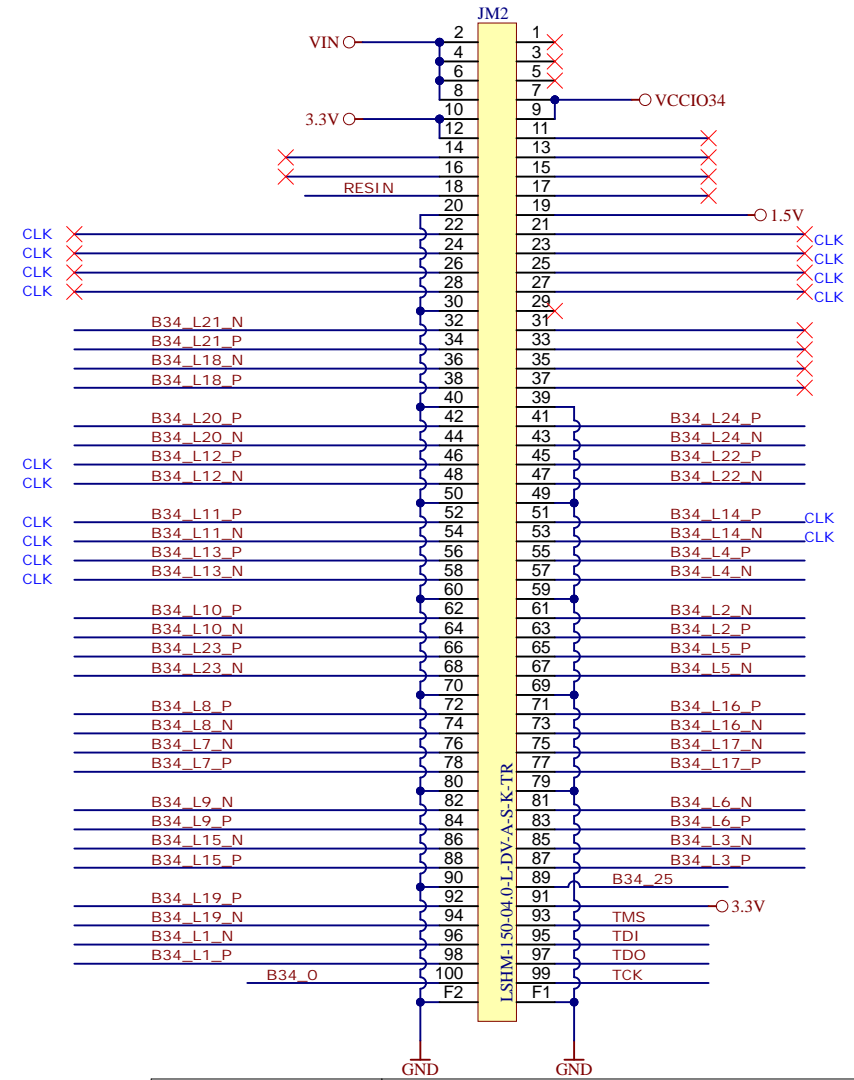
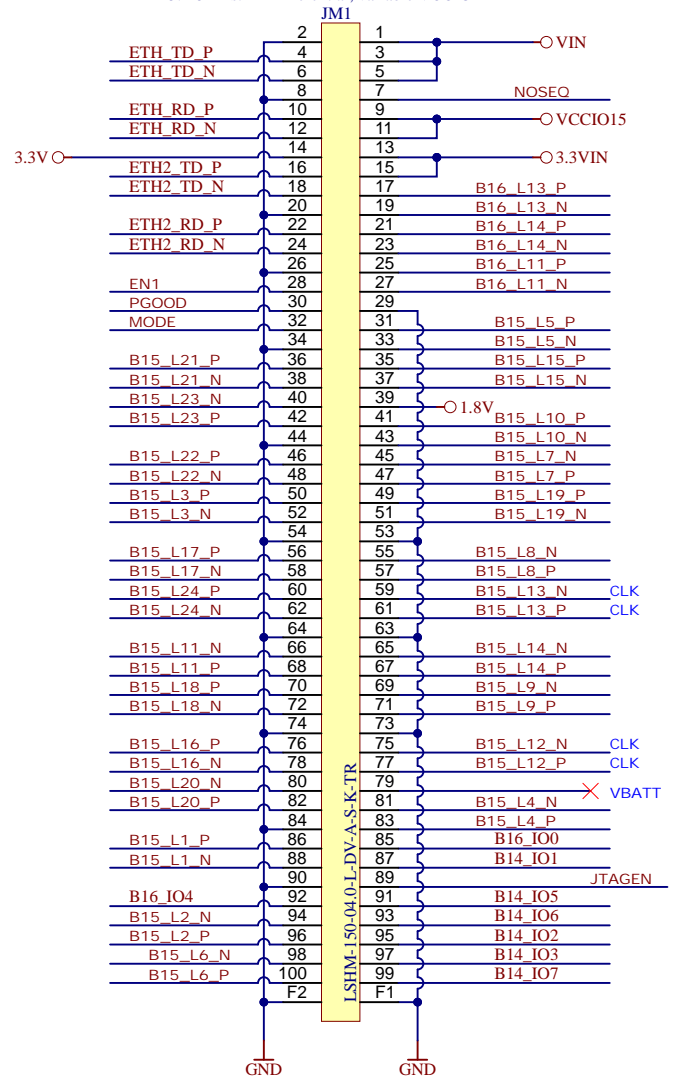
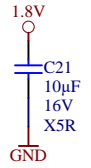
D

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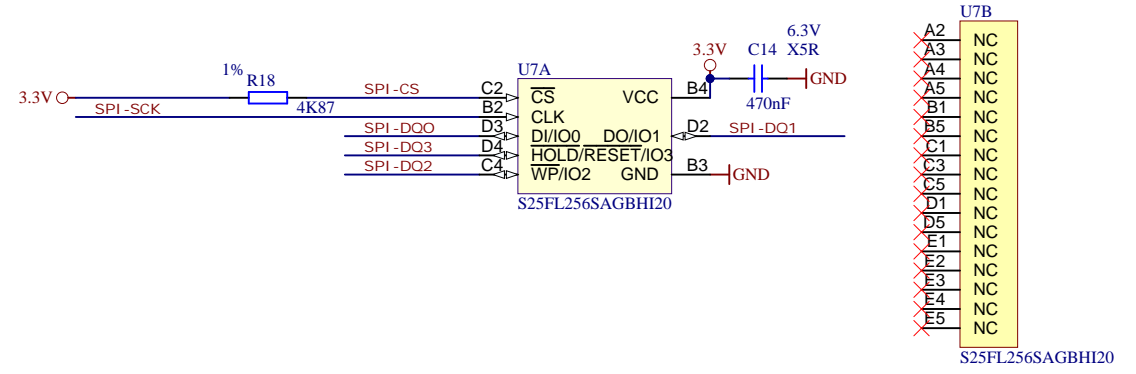
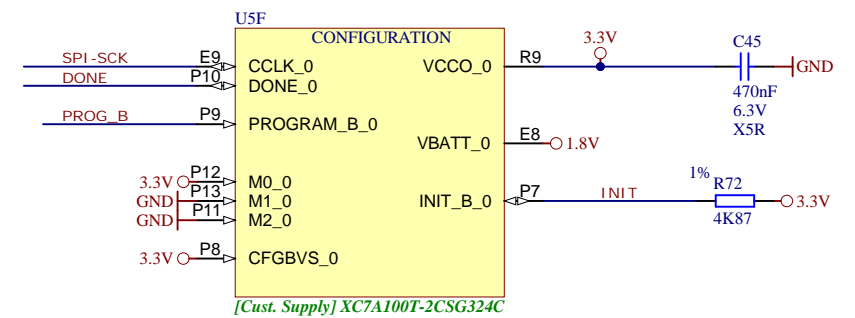
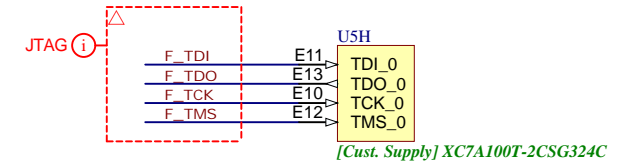
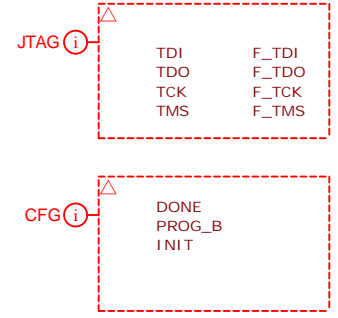
B

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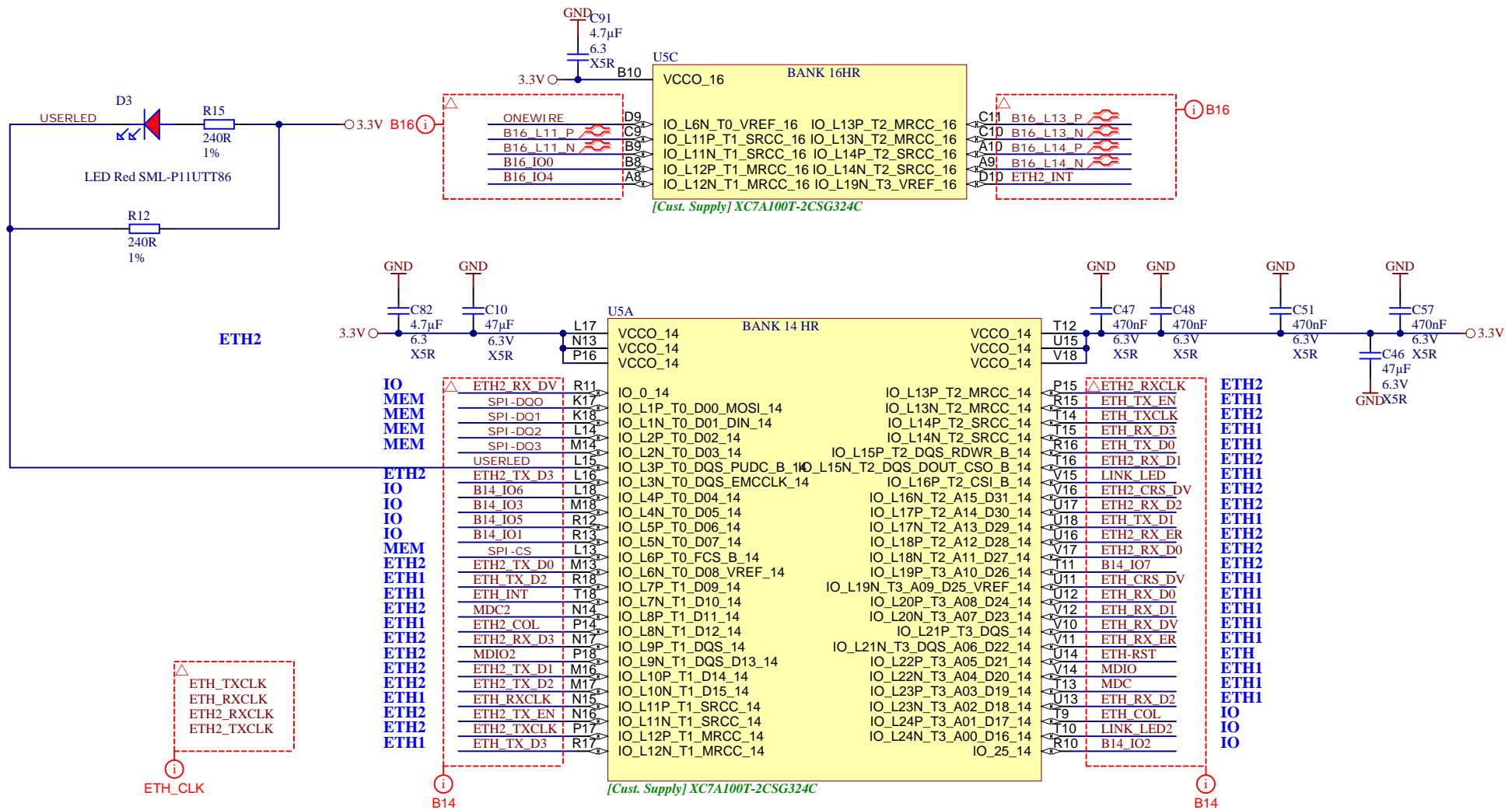
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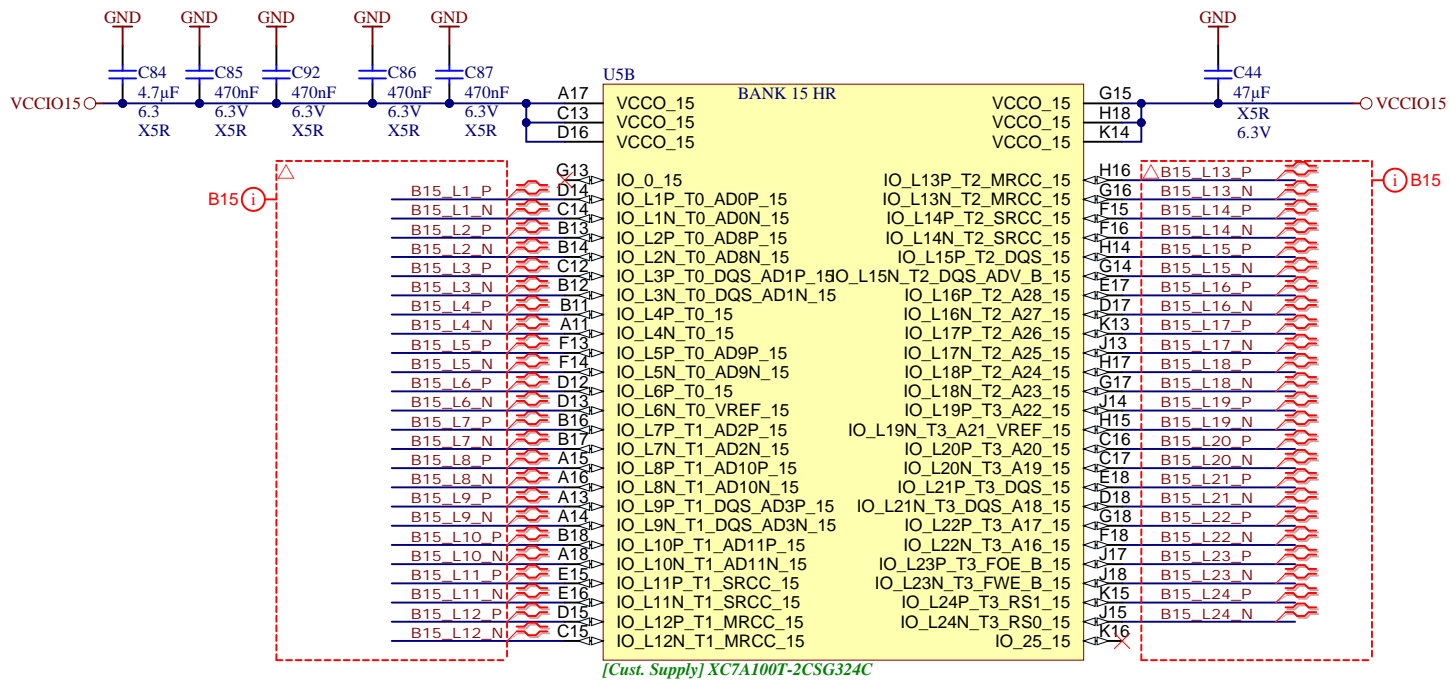
Title: TE0710		
A4	Number: TE0710 100-2CFV	Rev. 02
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Filename: B2B_Connector.SchDoc		



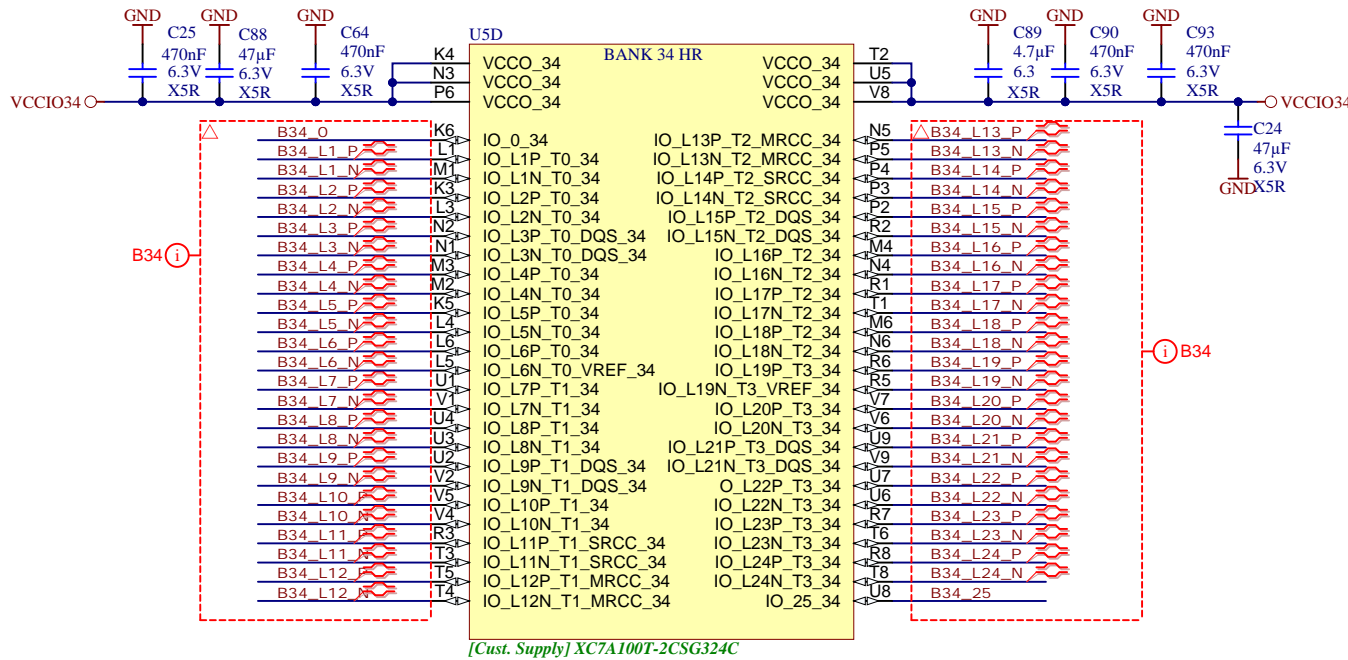
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	A4	Number: TE0710 100-2CFV	Rev. 02
	Date: 2014-03-07	Copyright: Trenz Electronic GmbH / TT	Page 3 of 13
	Filename: FPGA_CFG.SchDoc		



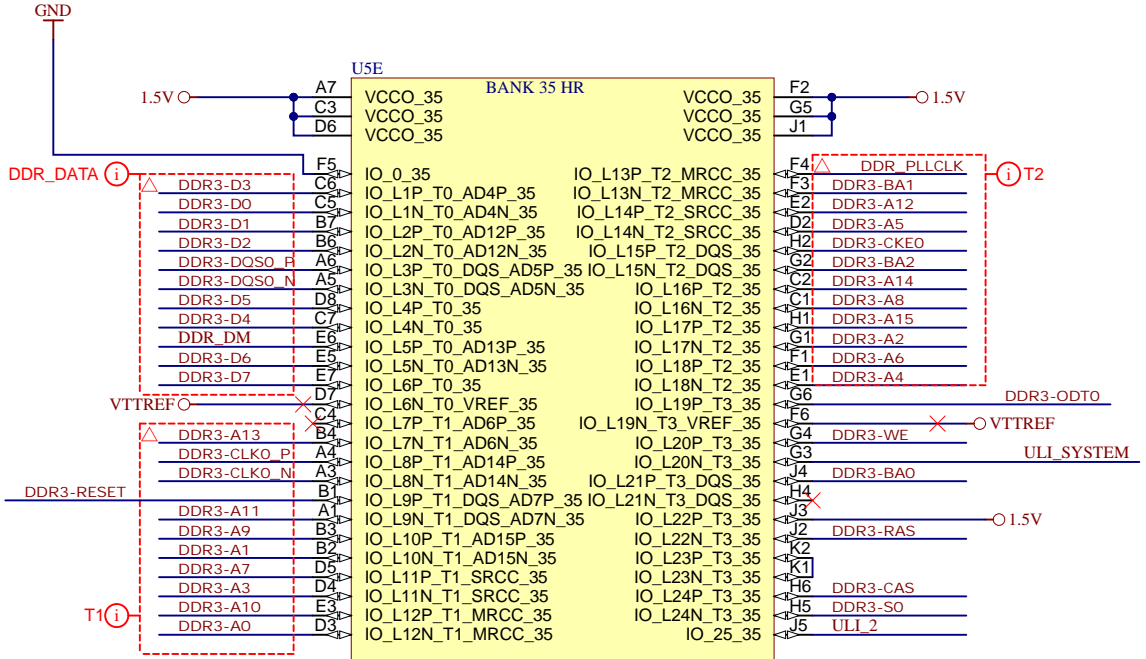
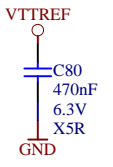
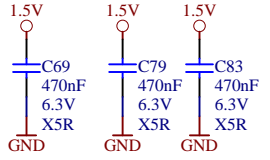
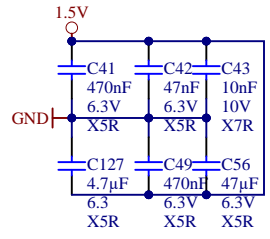
Title: TE0710		
A4	Number: TE0710 100-2CFV	Rev. 02
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Filename: B14_B16.SchDoc		



Title: TE0710		
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Filename: B15.SchDoc		



Title: TE0710		
A4	Number: TE0710 100-2CFV	Rev. 02
Date: 2014-03-07	Copyright: Trenz Electronic GmbH / TT	Page 6 of 13
Filename: B34.SchDoc		



[Cust. Supply] XC7A100T-2CSG324C



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Filename: B35-RAM.SchDoc		

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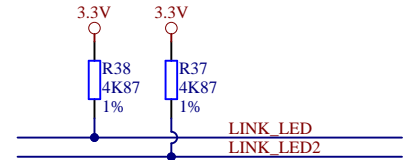
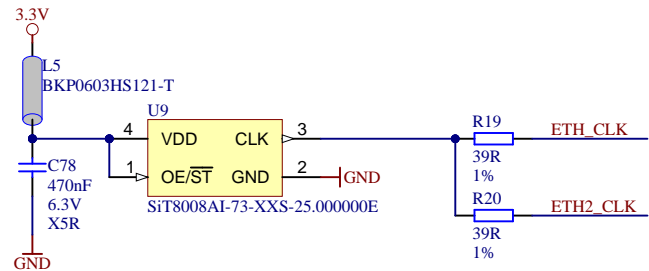
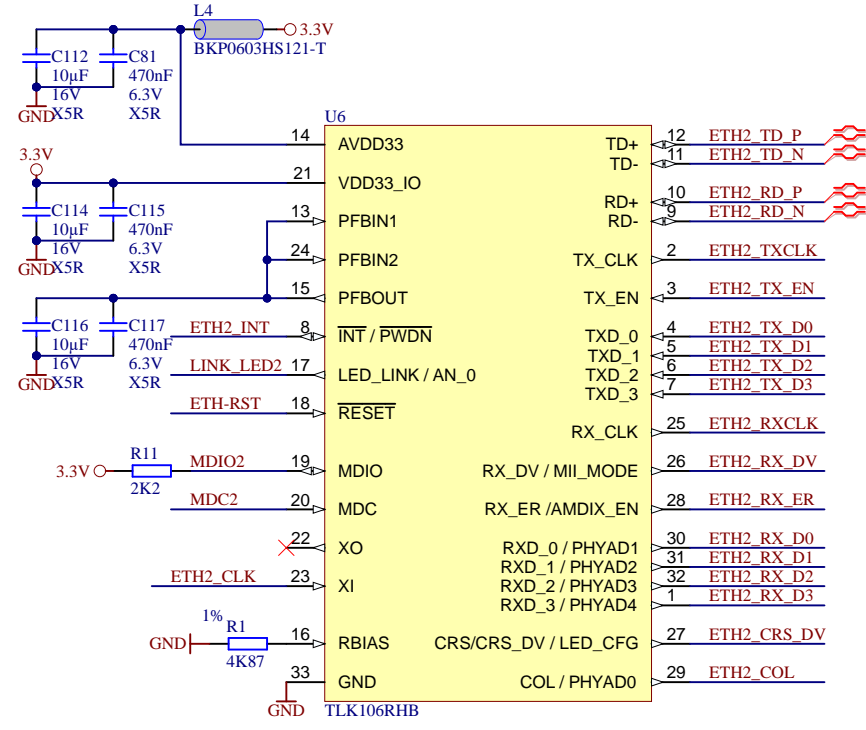
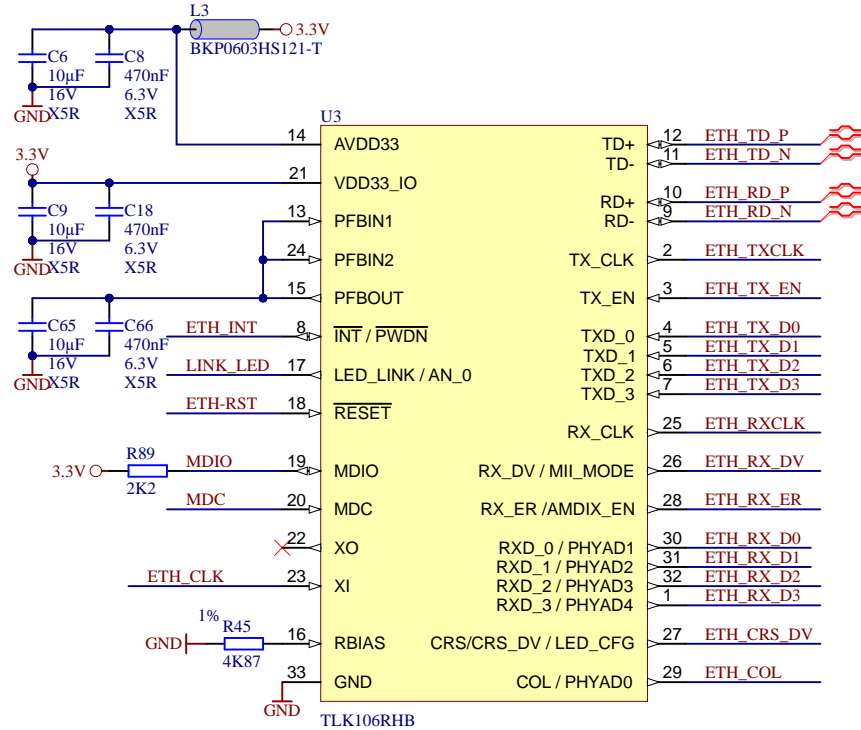
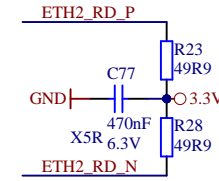
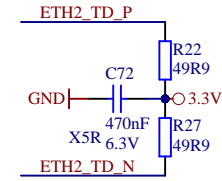
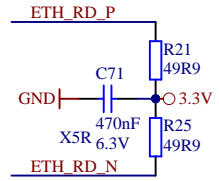
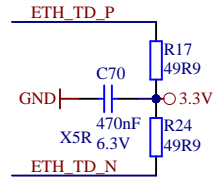
B

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Title: TE0710		
A4	Number: TE0710 100-2CFV	Rev. 02
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Filename: ETHERNET.SchDoc		

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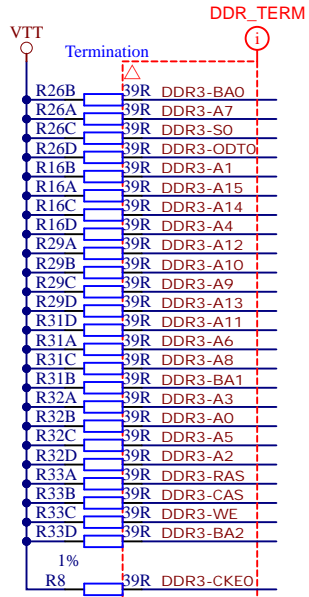
D

A

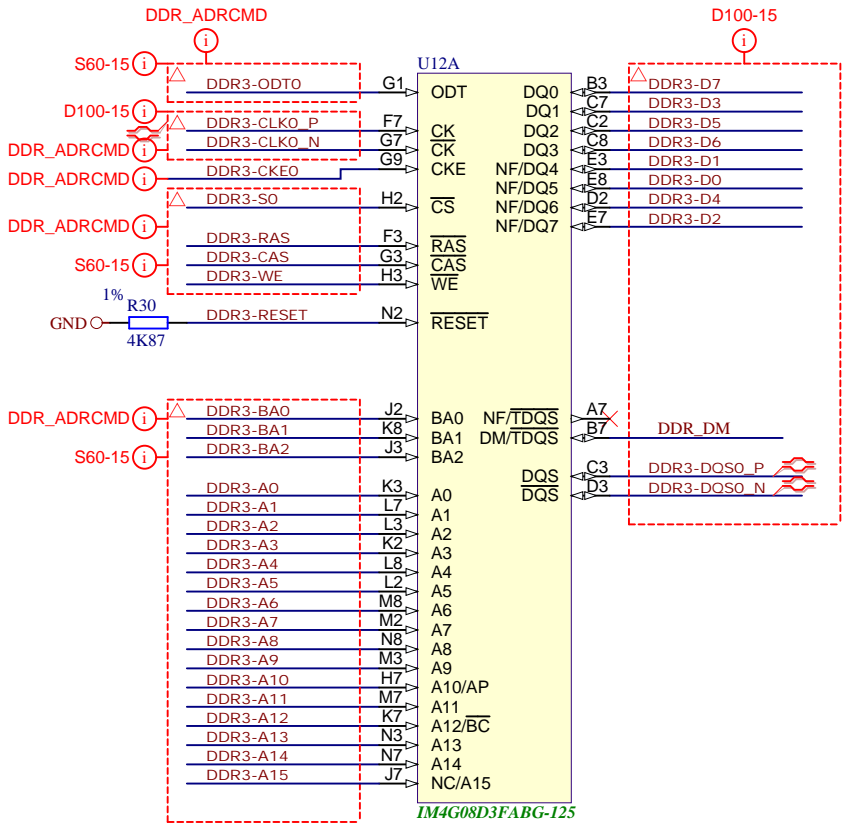
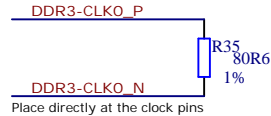
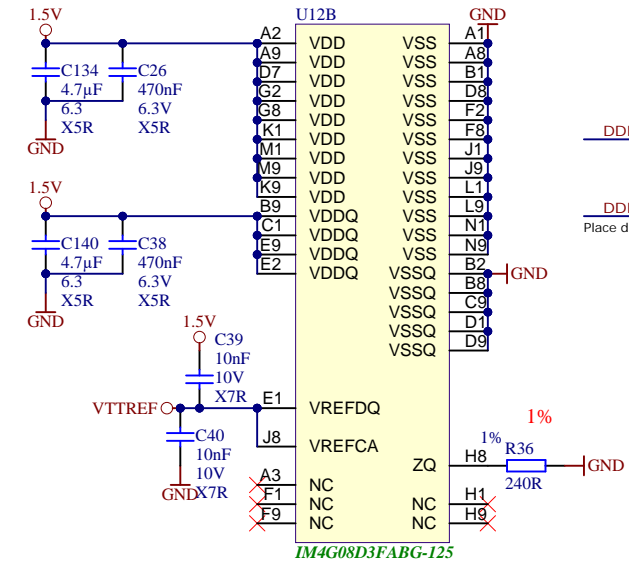
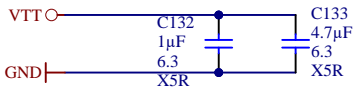
B

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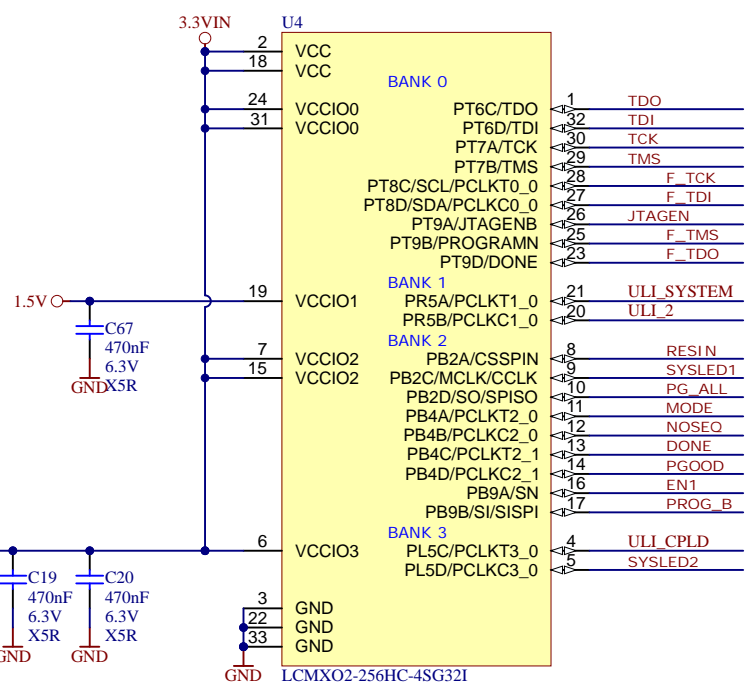
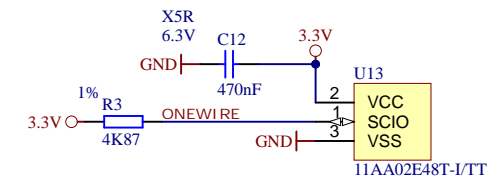
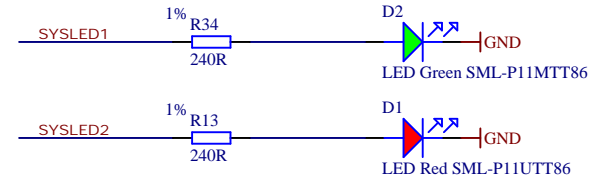
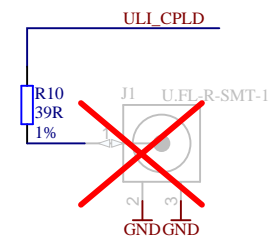
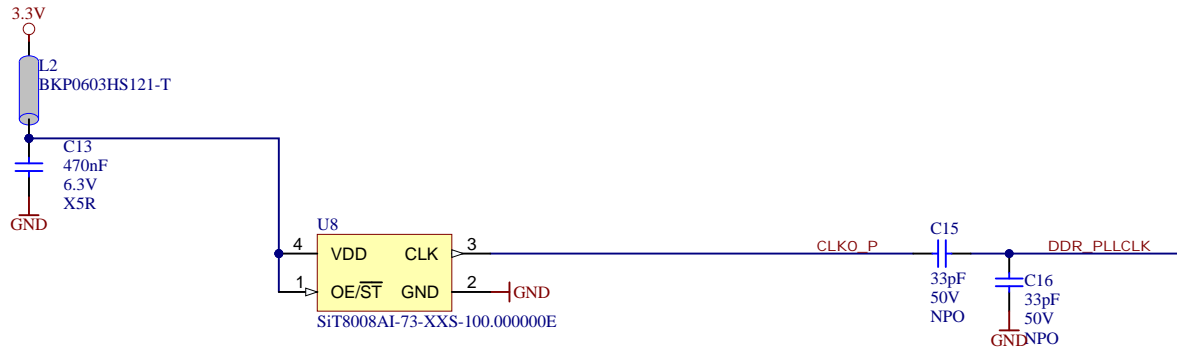
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Resistors can be swap to better routing



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A4	Number: TE0710 100-2CFV	Rev. 02
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Filename: DDR3-MEM.SchDoc		



	Title: TE0710	
	A4	Number: TE0710 100-2CFV
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	Filename: PLL.SchDoc	Page 11 of 13

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Revision changes REV02.a (15.03.19):

- 1) Schematic: nets B14_IO0 and B14_IO4 renamed to B16_IO0 and B16_IO4 accordingly
- 2) Schematic: changed value of R12 and R15 to 240R

Revision changes REV02.b (19.07.19):

- 3) VY: Replaced capacitors C39, C40, C43, C111 from 10nF 6.3V X5R to 10nF 10V X7R

A

A

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B

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C

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D

	Title: TEC0049		
	A4	Number: TE0710 100-2CFV	Rev. 02
	Date: 2017-10-09	Copyright: Trenz Electronic GmbH / TT	Page 13 of 13
	Filename: RevisionChanges.SchDoc		