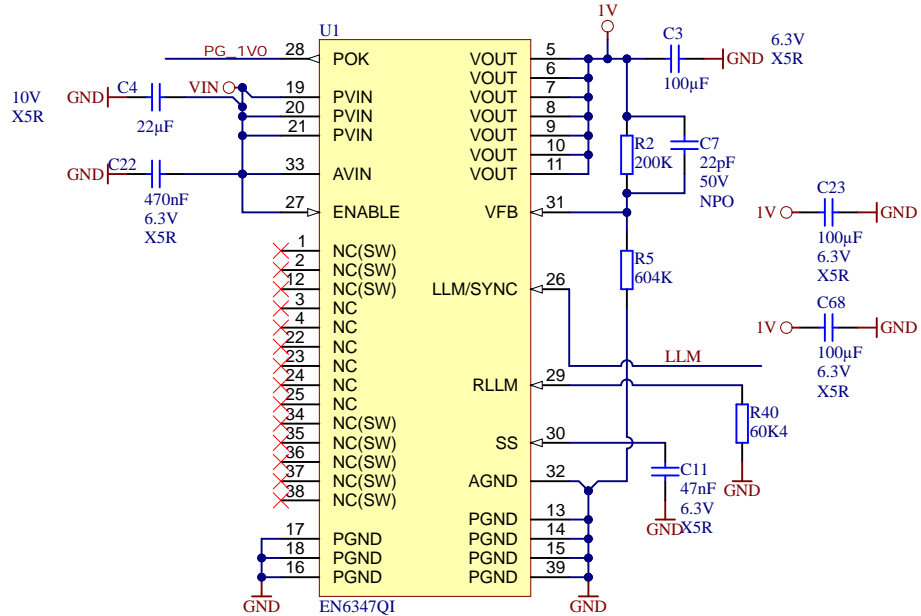
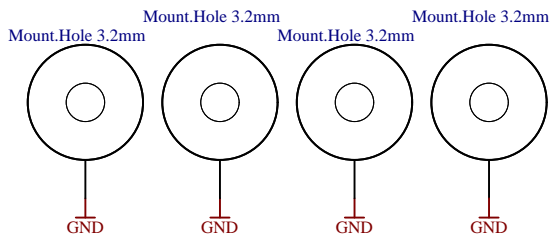
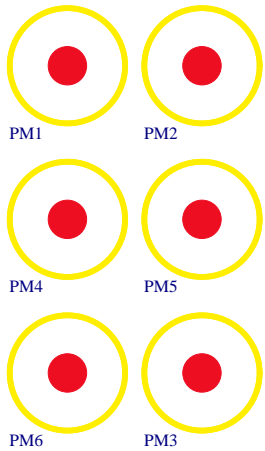
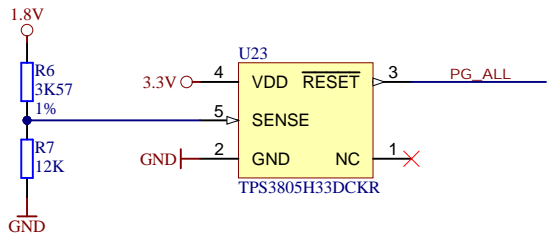
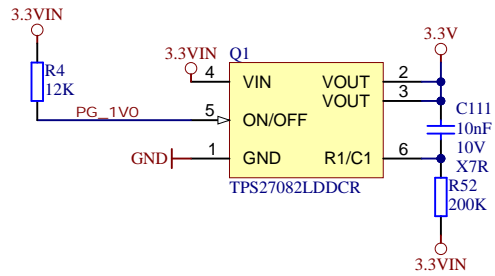
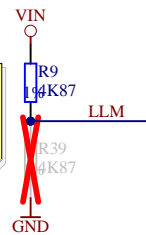


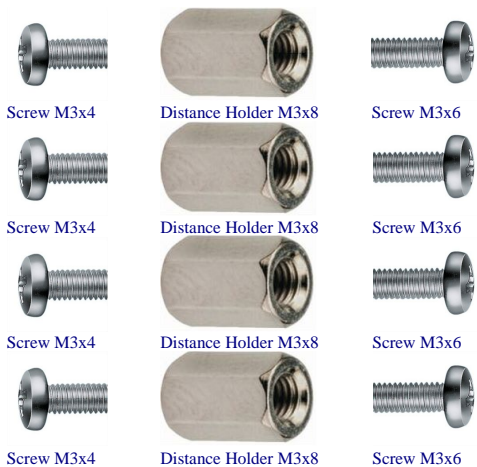
U_B2B_Connector	U_PLL
B2B_Connector.SchDoc	PLL.SchDoc
U_B14_B16	U_POWER
B14_B16.SchDoc	POWER.SchDoc
U_B15	
B15.SchDoc	
U_B34	
B34.SchDoc	
U_B35-RAM	
B35-RAM.SchDoc	
U_DDR3-MEM	
DDR3-MEM.SchDoc	
U_ETHERNET	
ETHERNET.SchDoc	
U_FPGA_CFG	
FPGA_CFG.SchDoc	
U_FPGA_PWR_MISC	
FPGA_PWR_MISC.SchDoc	

LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

Select which resistor to mount with assembly variant!  
Pullup switch DCDC to light load mode



Top of Board



Assembly variant	35-21F
Created by	TT
Modified by	VY
Modified at	2019-07-25
SVN Revision	8563

Title: TE0710		
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Dual 10/100 Ethernet Interface  
 4 system controller IO Pins; 3.3V VCCIO  
 B14 8 Pins Single ended IO; 3.3V Fixed VCCIO; replacing MIO0 pins on TE0720  
 B16 6 Pins; 3 Differential; 3.3V Fixed VCCIO; TE0720 SD Card compatible  
 B15: 48 Pins; 24 Differential; variable VCCIO

Total maximum I/O: 112  
 JM2 total I/O: 50  
 JM1 total I/O: 62

B34: 50 Pins; 24 Differential; variable VCCIO  
 JTAG or IO (4 pins); 3.3V Levels

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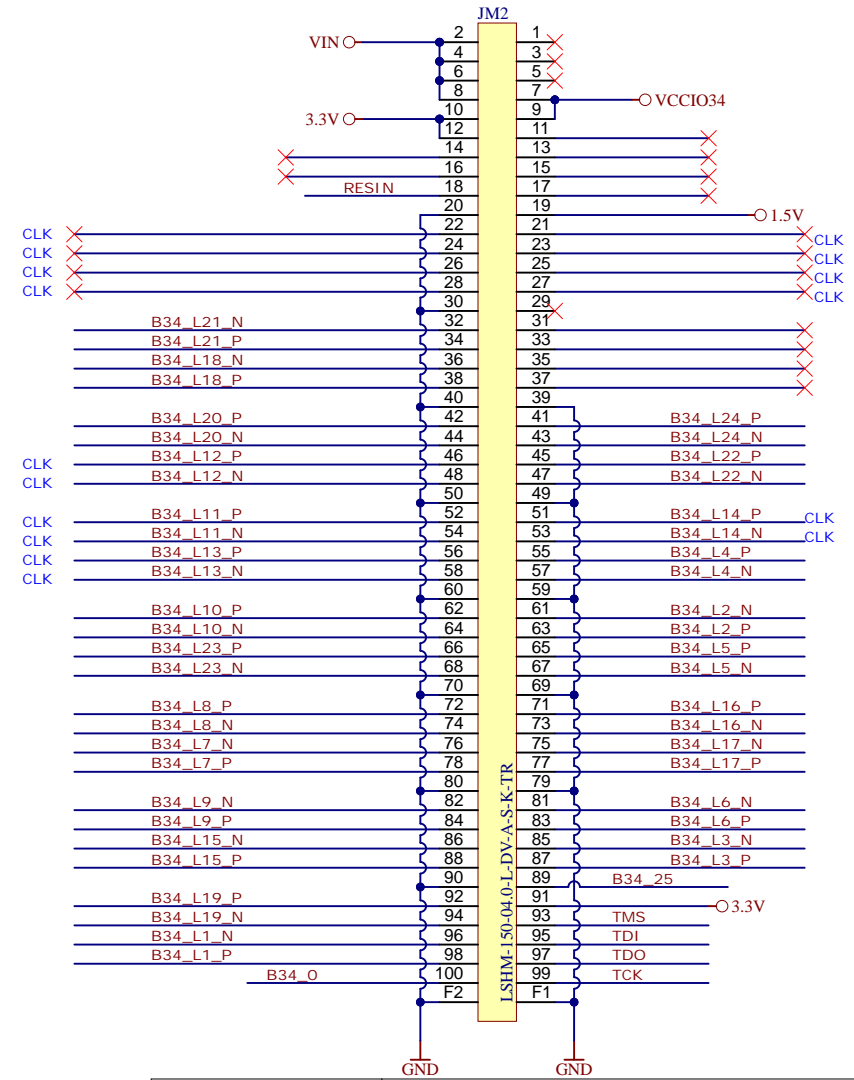
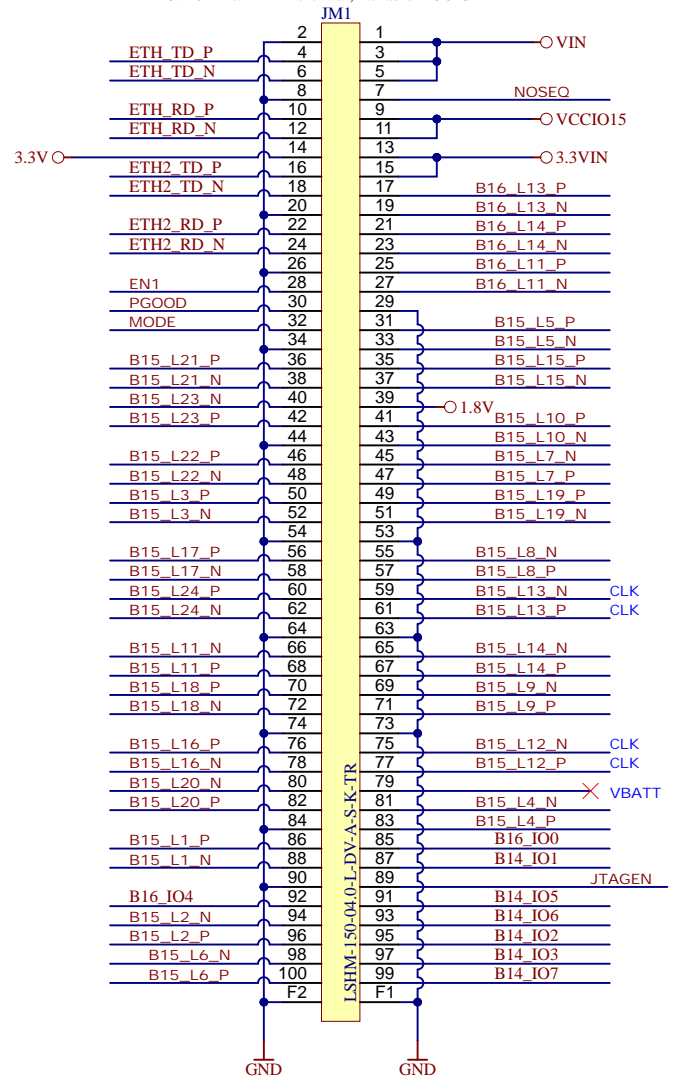
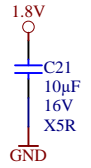
D

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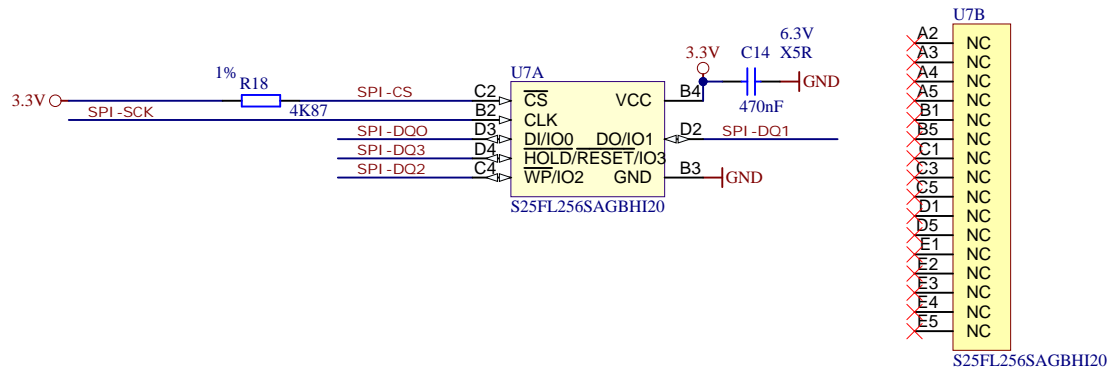
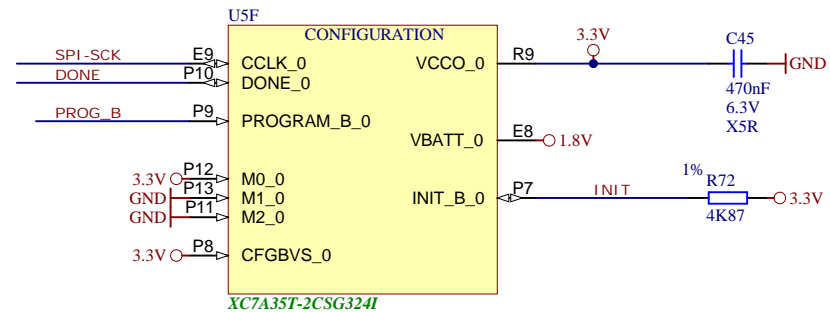
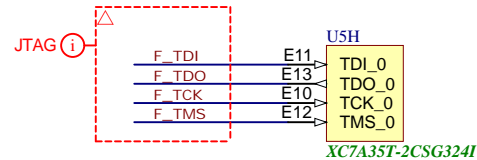
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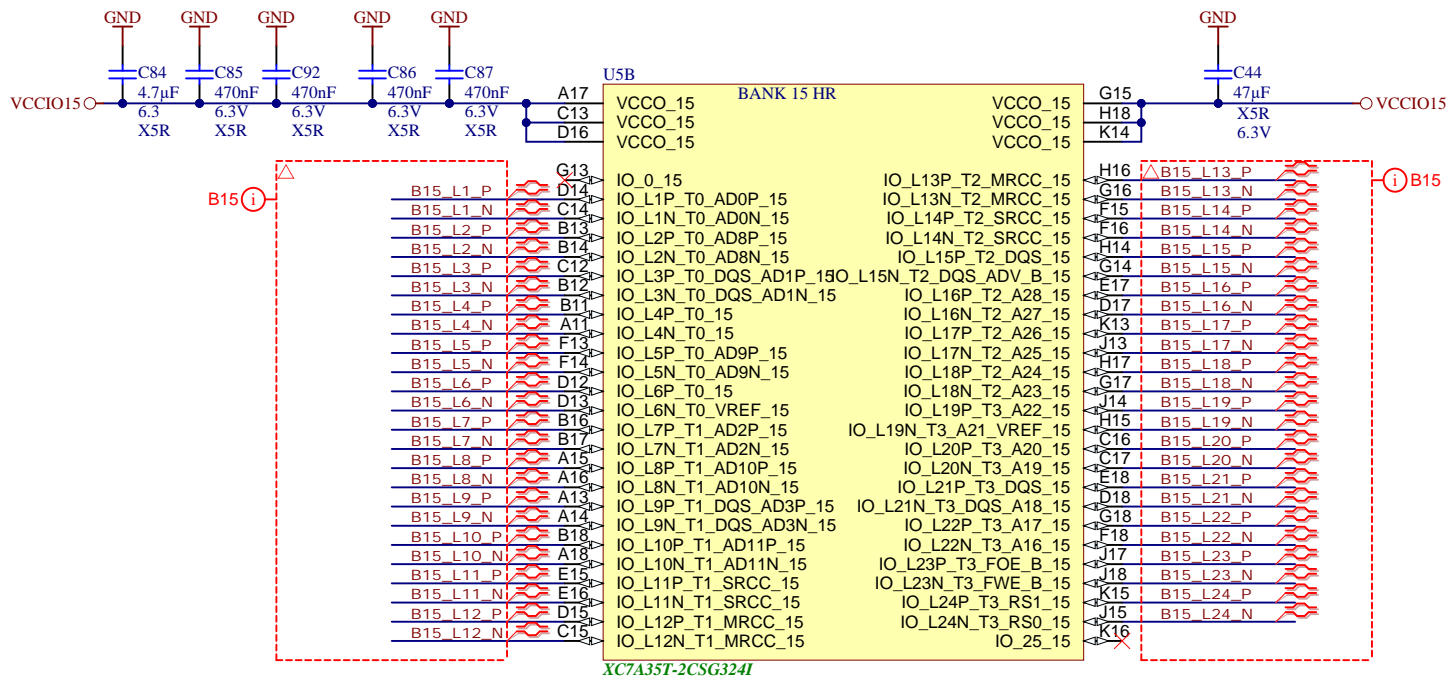


Title: TE0710		
A4	Number: TE0710 35-21F	Rev. 02
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Filename: B2B_Connector.SchDoc		

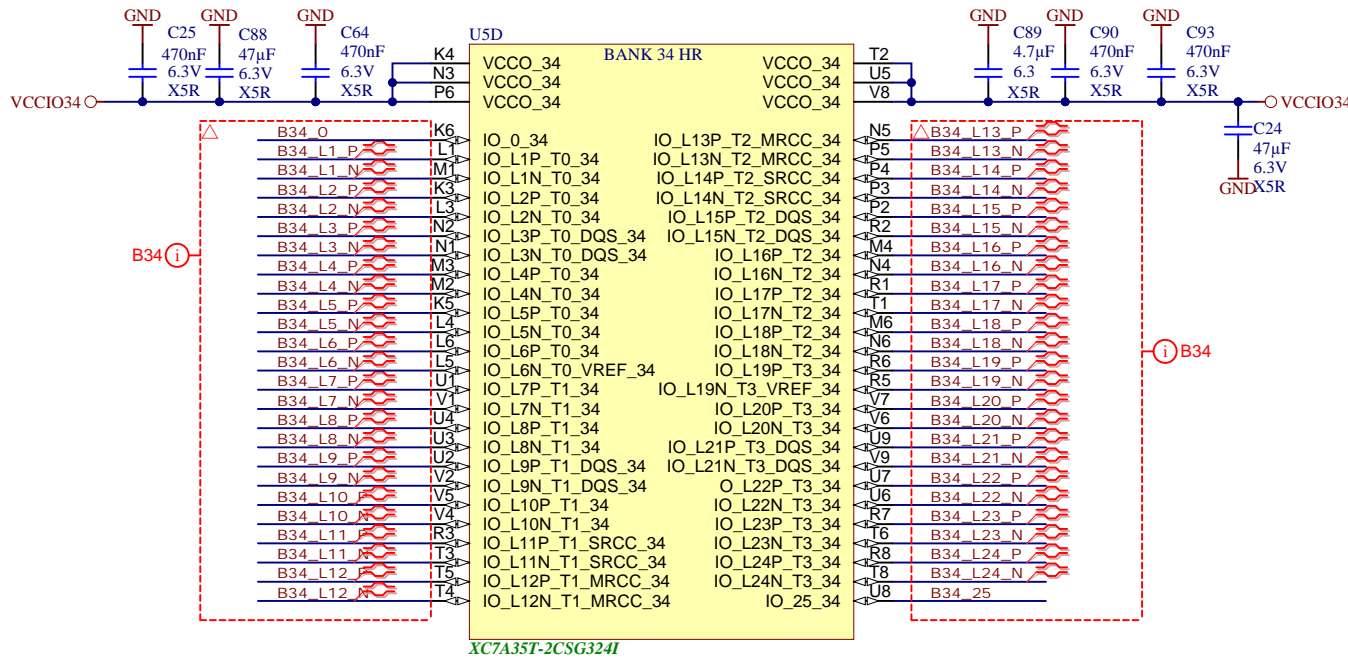


		Title: TE0710	
		A4	Number: TE0710 35-2IF
Date: 2014-03-07		Copyright: Trenz Electronic GmbH / TT	
Page 3		of 13	
Filename: FPGA_CFG.SchDoc			

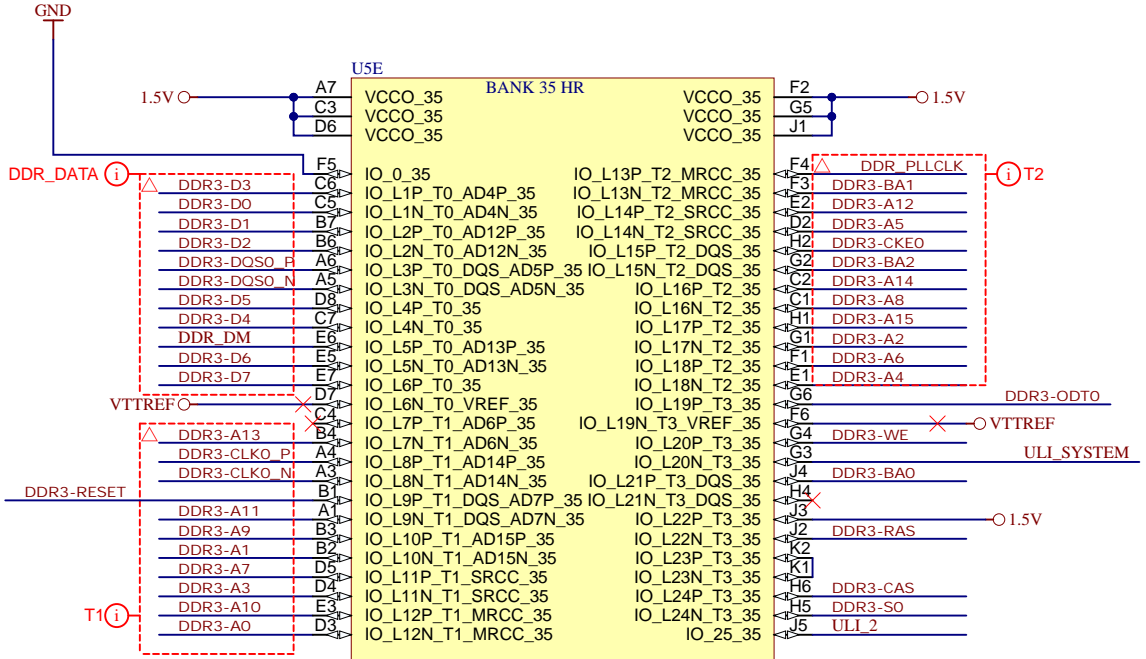
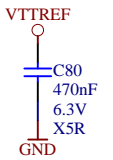
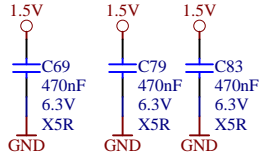
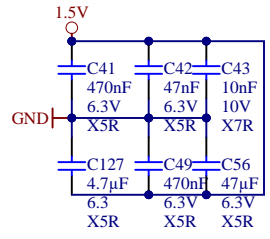




Title: <b>TE0710</b>		
A4	Number: <b>TE0710 35-2IF</b>	Rev. <b>02</b>
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Filename: <b>B15.SchDoc</b>		



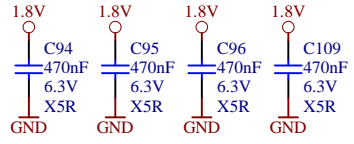
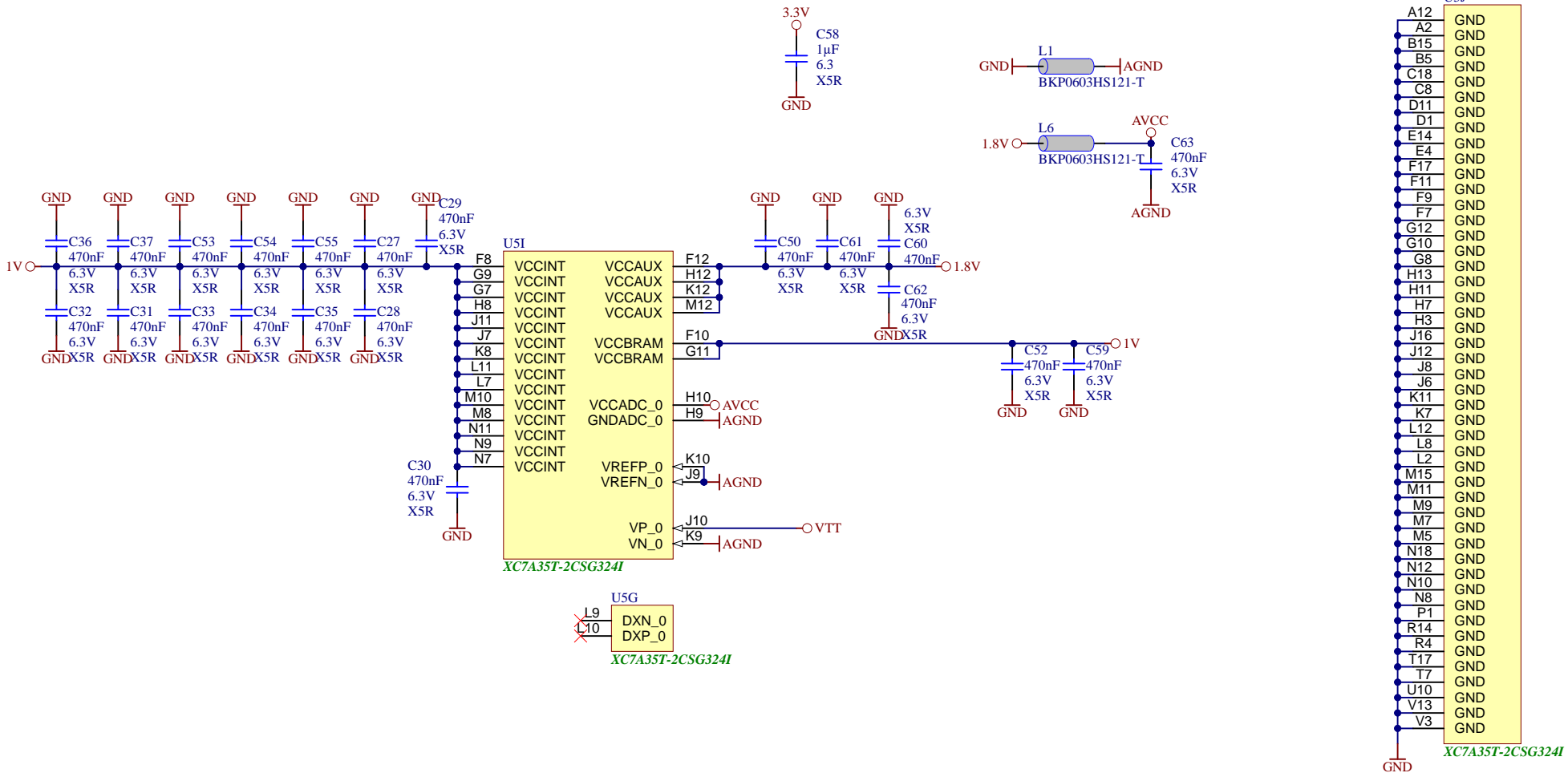
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A4	Number: <b>TE0710 35-2IF</b>	Rev. <b>02</b>
Date: <b>2014-03-07</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>6</b> of <b>13</b>
Filename: <b>B34.SchDoc</b>		



XC7A35T-2CSG324I



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Title: TE0710		
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Filename: FPGA_PWR_MISC.SchDoc		

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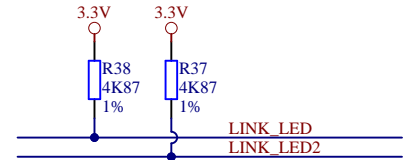
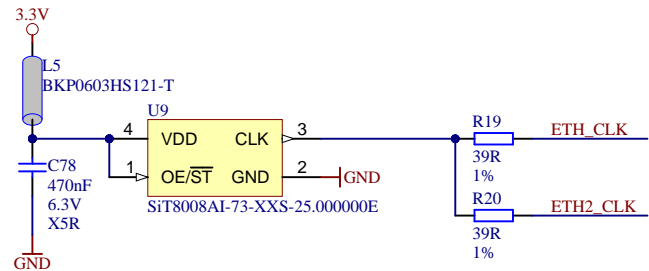
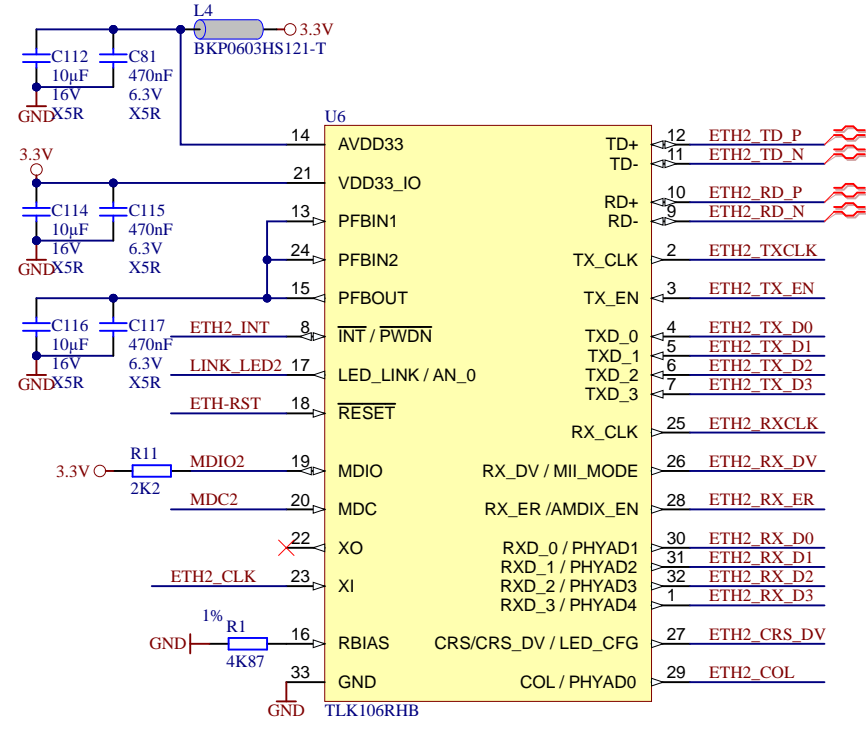
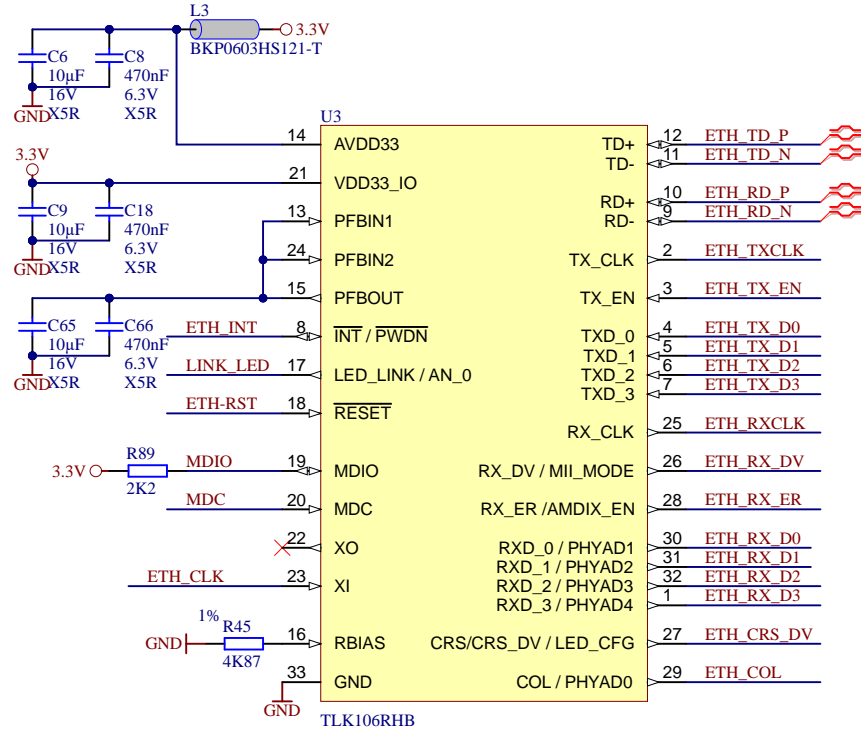
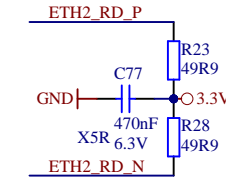
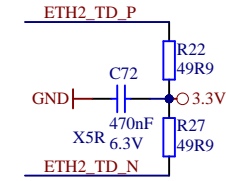
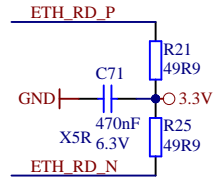
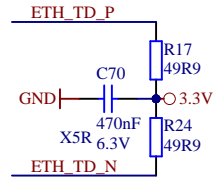
B

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			Title: TE0710	
			A4	Number: TE0710 35-2IF
Date: 22.10.2013		Copyright: Trenz Electronic GmbH / TT		Page9 of 13
Filename: ETHERNET.SchDoc				

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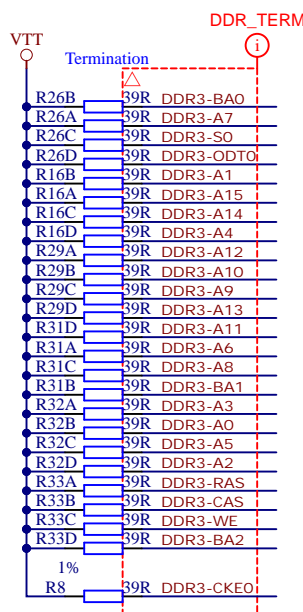
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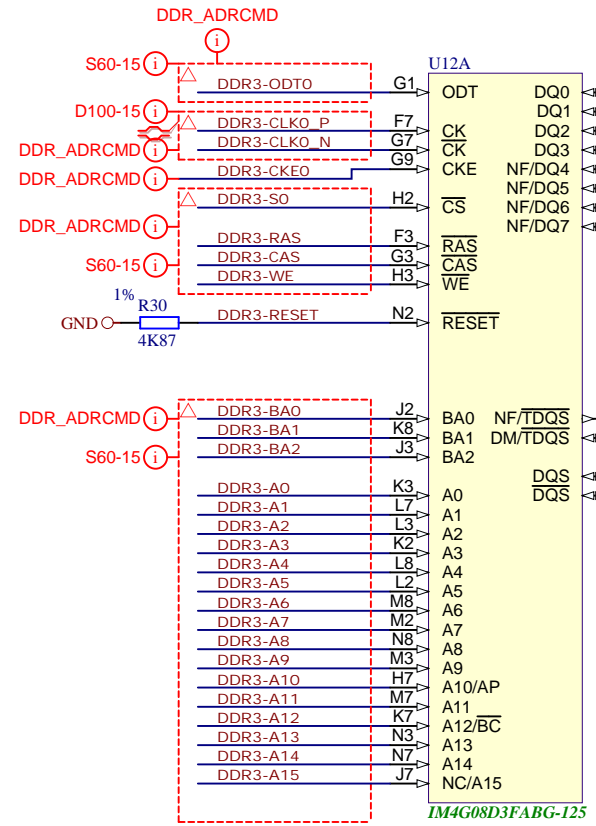
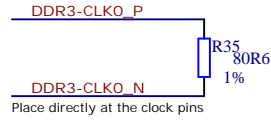
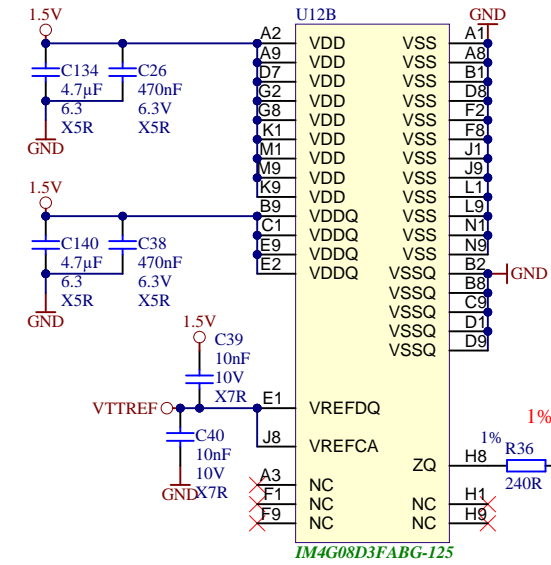
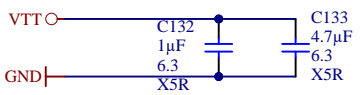
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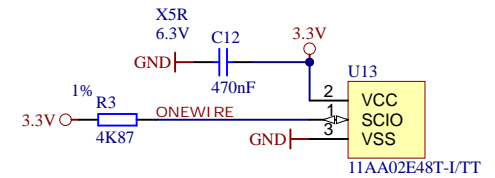
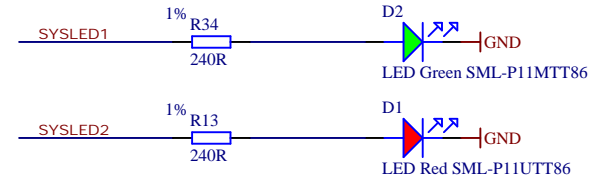
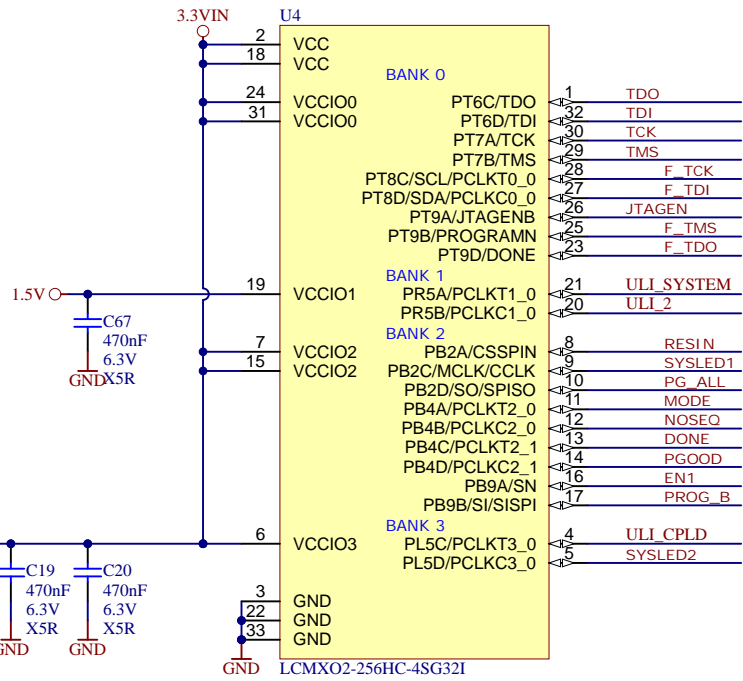
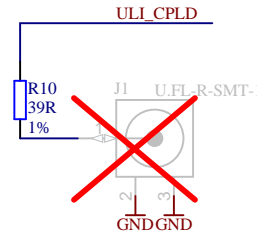
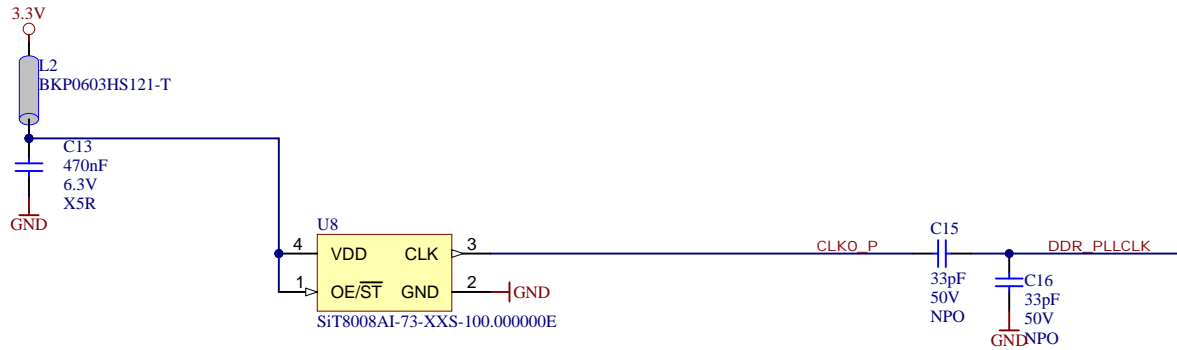
D



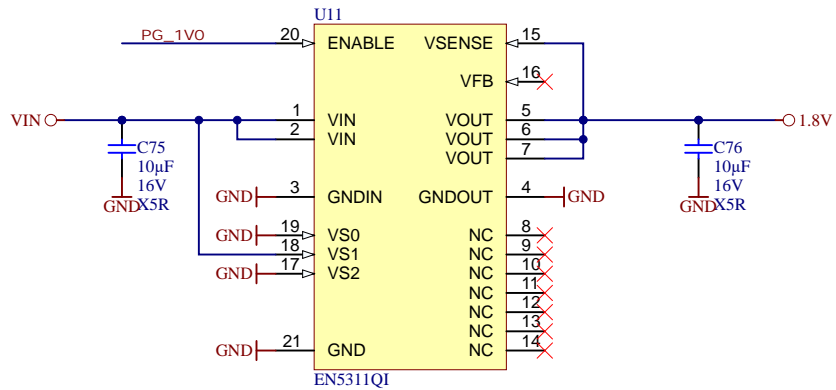
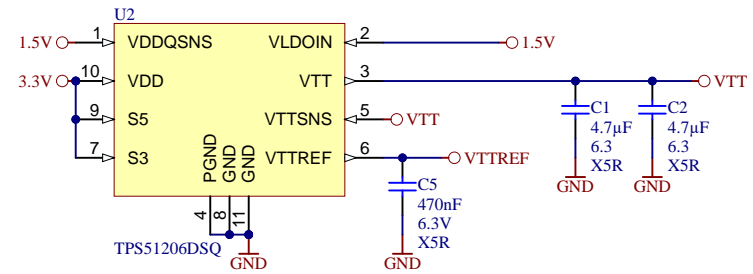
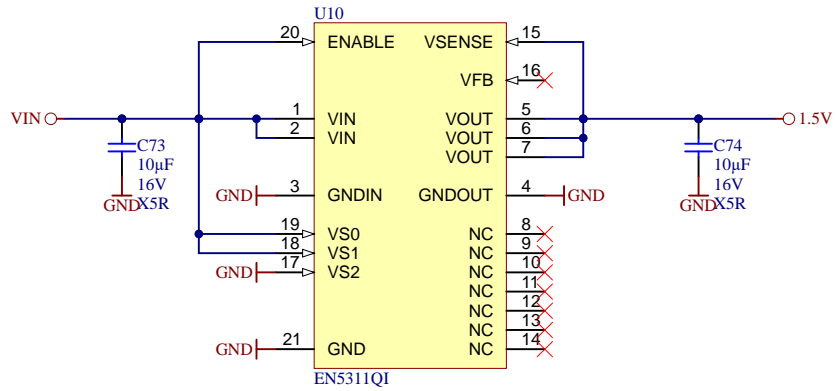
Resistors can be swap to better routing




Title: <b>TE0710</b>		
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Filename: <b>DDR3-MEM.SchDoc</b>		



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	A4	Number: <b>TE0710 35-2IF</b>
	Date: <b>2014-03-07</b>	Copyright: <b>Trenz Electronic GmbH</b>
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Filename: <b>PLL.SchDoc</b>		



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Revision changes REV02.a (15.03.19):

- 1) Schematic: nets B14\_IO0 and B14\_IO4 renamed to B16\_IO0 and B16\_IO4 accordingly
- 2) Schematic: changed value of R12 and R15 to 240R

Revision changes REV02.b (19.07.19):

- 3) VY: Replaced capacitors C39, C40, C43, C111 from 10nF 6.3V X5R to 10nF 10V X7R

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	Title: <b>TEC0049</b>		
	A4	Number: <b>TE0710 35-2IF</b>	Rev. <b>02</b>
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