TE0710 Test Board

Revision v.5

Exported on 2022-02-04

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0710+Test+Board

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4 Overview

Microblaze Design with linux example.

Refer to http://trenz.org/te0710-info for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2019.2
- PetaLinux
- MicroBlaze
- SREC
- Flash
- MIG
- ETH (ETH1)
- LED

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-04-21	2019.2	TE0710-test_board-vivado_2019.2-build_10_20200421063949.zip TE0710-test_board_noprebuilt-vivado_2019.2-build_10_20200421064005.zip	John Hartfiel	• 2019.2 update
2018-03-29	2017.4	te0710-test_board-vivado_2017.4-build_07_20180329130739.zip te0710-test_board_noprebuilt-vivado_2017.4-build_07_20180329130757.zip	John Hartfiel	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
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Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2019.2	• needed • Vivado is included into Vitis installation
PetaLinux	2019.2	• needed

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[1]

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0710-02-35-2CF	35_2cf_512mb	REV02	512MB	32MB	NA	NA	less IOs
TE0710-02-35-2IF	35_2if_512mb	REV02	512MB	32MB	NA	NA	less IOs
TE0710-02-100-2CF	100_2cf_512mb	REV02	512MB	32MB	NA	NA	NA
TE0710-02-100-2IF	100_2if_512mb	REV02	512MB	32MB	NA	NA	NA

Table 4: Hardware Modules
Design supports following carriers:

Carrier Model	Notes
TE0701	
TE0703	used as reference carrier

1 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Carrier Model	Notes
TE0705	
TE0706	
TEBA0841	

Table 5: Hardware Carrier
Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct typ
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Table 6: Additional Hardware

4.5 Content

For general structure and of the reference design, see Project Delivery - Xilinx devices[2]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

2 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

Type	Location	Notes
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Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems
SREC-File	*.srec	Converted Software Application for MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebult content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0710 "Test Board" Reference Design[3]

3 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0710/Reference_Design/2019.2/test_board

5 Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

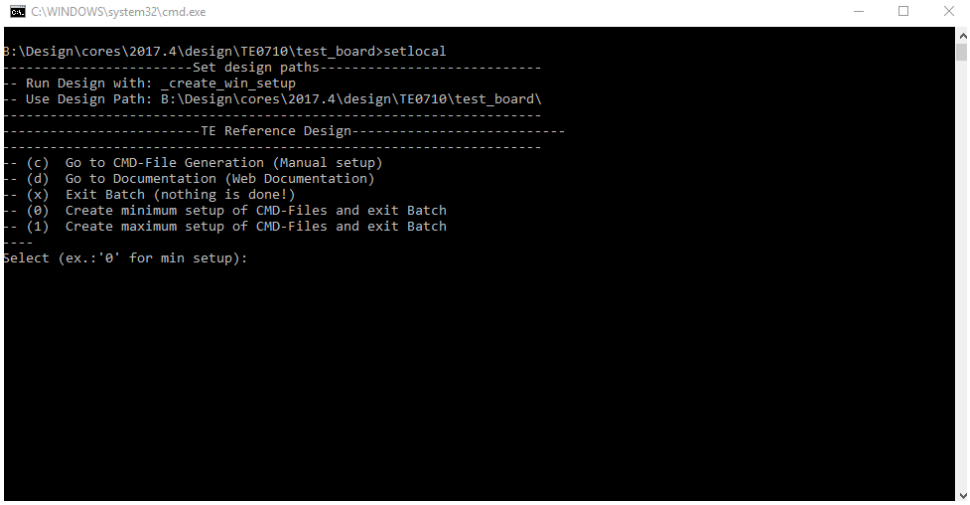
See also:Xilinx Development Tools[4]

- Xilinx Development Tools[5]
- Vivado Projects - TE Reference Design[6]
- Project Delivery.[7]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[8]

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
   a. optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
   Note: Select correct one, see TE Board Part Files[9]
5. Create XSA and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
   Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (uboot.elf and image.ub) with exported XSA

4 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
5 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
6 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
8 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality
9 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

   a. XSA is exported to "prebuilt\hardware\<short name>"
      Note: HW Export from Vivado GUI create another path as default workspace.
      Create Linux images on VM, see PetaLinux KICKstart[10]
      i. Use TE Template from /os/petalinux
         Important Note: Select correct Flash partition offset on petalinux-config: Subsystem Auto HW Settings → Flash Settings, FPGA+Boot+bootenv=0x900000 (increase automatically generate Boot partition), increase image size to A:, see TE0710 Test Board#Config(see page 19)
7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalinux\<ddr size>" or "prebuilt\os\petalinux\<short name>"
      Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise "prebuilt\os\petalinux\<DDR size>" of the selected device
8. Generate Programming Files with Vitis
   a. Run on Vivado TCL: TE::sw_run_vitis -all
      Note: Depending of PC performance this can take several minutes. Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv" and open Vitis
   b. (alternative) Start Vitis with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
      Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used. See Vitis[11]
9. Copy "\prebuilt\software\<short name>\srec_spi_bootloader.elf" into "\firmware\microblaze_0\"
10. Regenerate Vivado Project or Update Bitfile only with "srec_spi_bootloader.elf"

10 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
11 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging[12]

6.1.1 Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder
   Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

6.1.2 QSPI

1. Connect JTAG and power on PCB
2. (if not done) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" or open with "vivado_open_project_guimode.cmd", if generated.
3. Type on Vivado Console: TE::pr_program_flash -swapp u-boot
   Note: Alternative use SDK or setup Flash on Vivado manually
4. Reboot (if not done automatically)

6.1.3 SD

Not used on this Example.

6.1.4 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming(see page 14)
2. Connect UART USB (most cases same as JTAG)
3. Power on PCB
   Note: FPGA Loads Bitfile from Flash, SREC Bootloader from Bitfile Firmware loads U-Boot into DDR (This takes a while), U-boot loads Linux from QSPI Flash into DDR

Boot process takes a while, please wait.

12 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging

```
SREC SPI Bootloader
Loading SREC image from flash @ address: 00400000
Bootloader: Processed (0x)00001000 S-records
Bootloader: Processed (0x)00002000 S-records
Bootloader: Processed (0x)00003000 S-records
Bootloader: Processed (0x)00004000 S-records
Please wait...
Executing program starting at address: 80100000
```

6.2.1 Linux

Note: Linux boot process is slower on Microblaze.

1. Open Serial Console (e.g. putty)
   a. Speed: 9600
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root
3. You can use Linux shell now.
   a. ETH0 works with udhcpc

6.2.2 Vivado HW Manager:

- Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).
- Control:
  - User LED Control
  - ETH Power Down
- Monitoring
  - ETH Link Status
  - MicroBlaze Reset Status

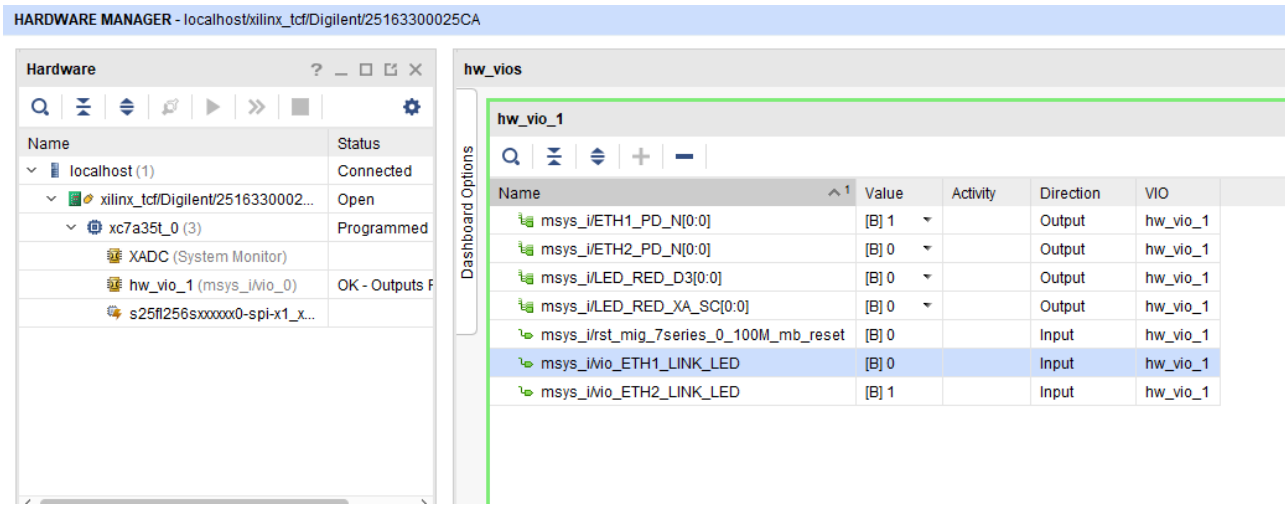


Figure 1: Vivado Hardware Manager

7 System Design - Vivado

7.1 Block Design

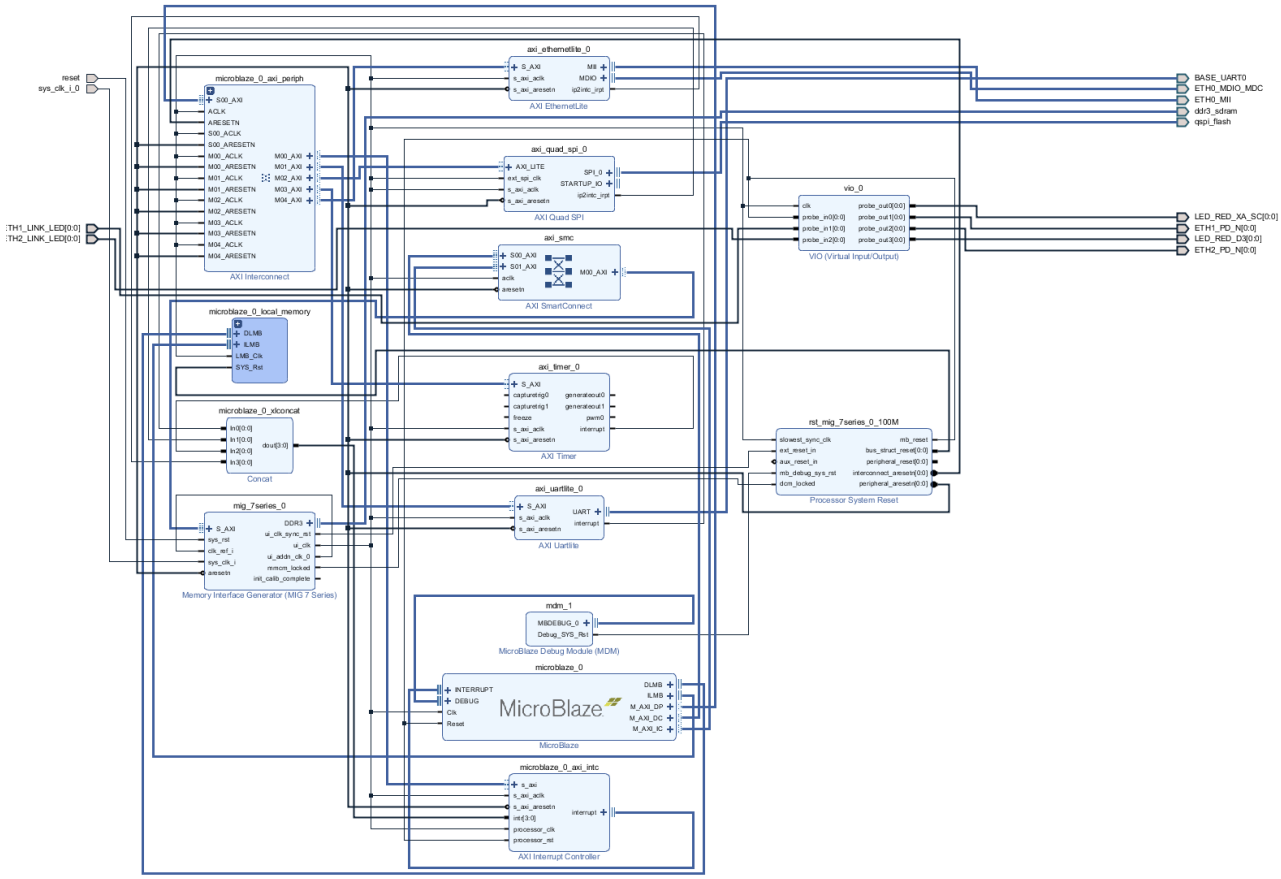


Figure 2: Block Design PCB REV02

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
```

```
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

_i_bitgen.xdc

```
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLDOWN [current_design]
```

7.2.2 Design specific constrain

_i_io.xdc

```
set_property PACKAGE_PIN G3 [get_ports {LED_RED_XA_SC[0]}]
set_property IOSTANDARD LVCMOS15 [get_ports {LED_RED_XA_SC[0]}]

set_property PACKAGE_PIN T10 [get_ports {ETH2_LINK_LED[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {ETH2_LINK_LED[0]}]
set_property PACKAGE_PIN V15 [get_ports {ETH1_LINK_LED[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {ETH1_LINK_LED[0]}]
set_property PACKAGE_PIN T18 [get_ports {ETH1_PD_N[0]}]
set_property PACKAGE_PIN D10 [get_ports {ETH2_PD_N[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {ETH2_PD_N[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {ETH1_PD_N[0]}]

set_property PACKAGE_PIN L15 [get_ports {LED_RED_D3[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LED_RED_D3[0]}]
```

8 Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis[13]

8.1 Application

8.1.1 srec_spi_bootloader

TE modified 2019.2 SREC

Bootloader to load app or second bootloader from flash into DDR

Descriptions:

- Modified Files: blconfig.h, bootloader.c
- Changes:
  - Add some console outputs and changed bootloader read address.
  - Add bugfix for 2018.2 qspi flash (some reinitialisation)

8.1.2 xilisf_v5_14

TE modified 2019.2 xilisf_v5_14

- Changed default Flash type to 5.

8.1.3 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate u-boot.srec. Vivado to generate *.mcs

13 https://wiki.trenz-electronic.de/display/PD/Vitis

9 Software Design - PetaLinux

- PetaLinux KICKstart[14]

Description currently not available.

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- SUBSYSTEM_FLASH_AXI_QUAD_SPI_0_BANKLESS_PART0_SIZE = 0x5E0000
- SUBSYSTEM_FLASH_AXI_QUAD_SPI_0_BANKLESS_PART1_SIZE = 0x300000
- SUBSYSTEM_FLASH_AXI_QUAD_SPI_0_BANKLESS_PART2_SIZE = 0x20000
- SUBSYSTEM_FLASH_AXI_QUAD_SPI_0_BANKLESS_PART3_SIZE = 0xA00000
    - (Set kernel flash Address to 0x900000 and Kernel size to 0xA00000)

9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set
- # CONFIG_PHY_ATHEROS is not set
- # CONFIG_PHY_BROADCOM is not set
- # CONFIG_PHY_DAVICOM is not set
- # CONFIG_PHY_LXT is not set
- # CONFIG_PHY_MICREL_KSZ90X1 is not set
- # CONFIG_PHY_MICREL is not set
- # CONFIG_PHY_NATSEMI is not set
- # CONFIG_PHY_REALTEK is not set
- CONFIG_RGMII=y

Change platform-top.h:

9.3 Device Tree

```
/include/ "system-conf.dtsi"
/ {
};

/* QSPI PHY */

&axi_quad_spi_0 {
    #address-cells = <1>;
    #size-cells = <0>;
```

14 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart

```
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        spi-tx-bus-width=<1>;
        spi-rx-bus-width=<4>;
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
        spi-max-frequency = <25000000>;
    };
};


/* ETH PHY */
&axi_ethernetlite_0 {
    phy-handle = <&phy0>;
    mdio {
        #address-cells = <1>;
        #size-cells = <0>;
        phy0: phy@0 {
            device_type = "ethernet-phy";
            reg = <1>;
        };
    };
};
```

9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- No changes.

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- # CONFIG_dropbear is not set
- # CONFIG_dropbear-dev is not set
- # CONFIG_dropbear-dbg is not set
- # CONFIG_packagegroup-core-ssh-dropbear is not set
- # CONFIG_packagegroup-core-ssh-dropbear-dev is not set
- # CONFIG_packagegroup-core-ssh-dropbear-dbg is not set
- # CONFIG_imagefeature-ssh-server-dropbear is not set

9.6 Applications

No changes.

10 Additional Software

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2020-04-21	v.5(see page 6)	@ John Hartfiel[15]	• Release 2019.2 • Docu update
2019-03-29	v.4	John Hartfiel	• Release 2017.4
2019-03-29	v.1	@ John Hartfiel[16]	• Initial release
---	All	@ John Hartfiel[17]	---

Table 10: Document change history.

11.2 Legal Notices

11.3 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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15 https://wiki.trenz-electronic.de/display/~j.hartfiel
16 https://wiki.trenz-electronic.de/display/~j.hartfiel
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18 http://guidance.echa.europa.eu/
19 https://echa.europa.eu/candidate-list-table
20 http://www.echa.europa.eu/

necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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2019-06-07