

Image is for illustrative purposes only

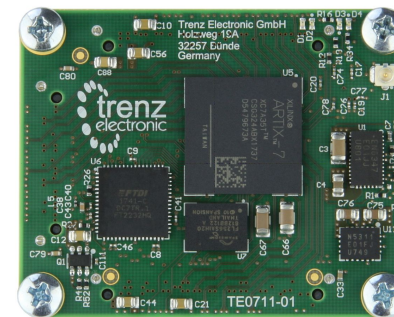


Image is for illustrative purposes only

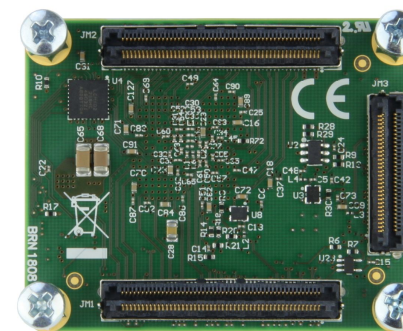



Image is for illustrative purposes only

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Schematics and other handouts serve for informational purposes only!

	Title: TE0711 - Legal Notices Modules		
	A4	Number: TE0711 42C-1-A	Rev. 02
	Date: 25-Jul-23	Copyright: Trenz Electronic GmbH	Page 1 of 15
	Filename: Legal_Notices.SchDoc		

1

2

3

4

A

A

B

B


C

C

D

D

REV	Description	
-01	Initial revision	
-02	1) Pages "Legal_Notices.SchDoc", "Revision_Changes.SchDoc", "Overview.SchDoc" and "Power_Diagram.SchDoc" were added 2) Signal groups tables and colors were added on page "B2B_Connector.SchDoc" 3) L1 - L6 were replaced from BKP0603HS121-T to MPZ0603S121HT000 4) All SCH and PCB components were updated 5) Fiducials were updated 6) Serial number was updated 7) D5 was added 8) U1 was updated from EN6347QI to MPM3860GQW-Z 9) Q1 was updated from TPS27082LDDCR to MP5077GG-Z 10) U11 was updated from EN5311QI to MPM3834CGPA 11) U23 was updated from TPS3805H33DCKR to STM6710LWB6F 12) R25 pullup was added 13) TP1 - TP19 were added 14) UKCA and CE logos were added 15) Fiducials on top and bottom were moved to same positions 16) R15 was changed from 2.2k to 470R 17) R22 was added 18) PCB net lengths were changed to improve routing	MT

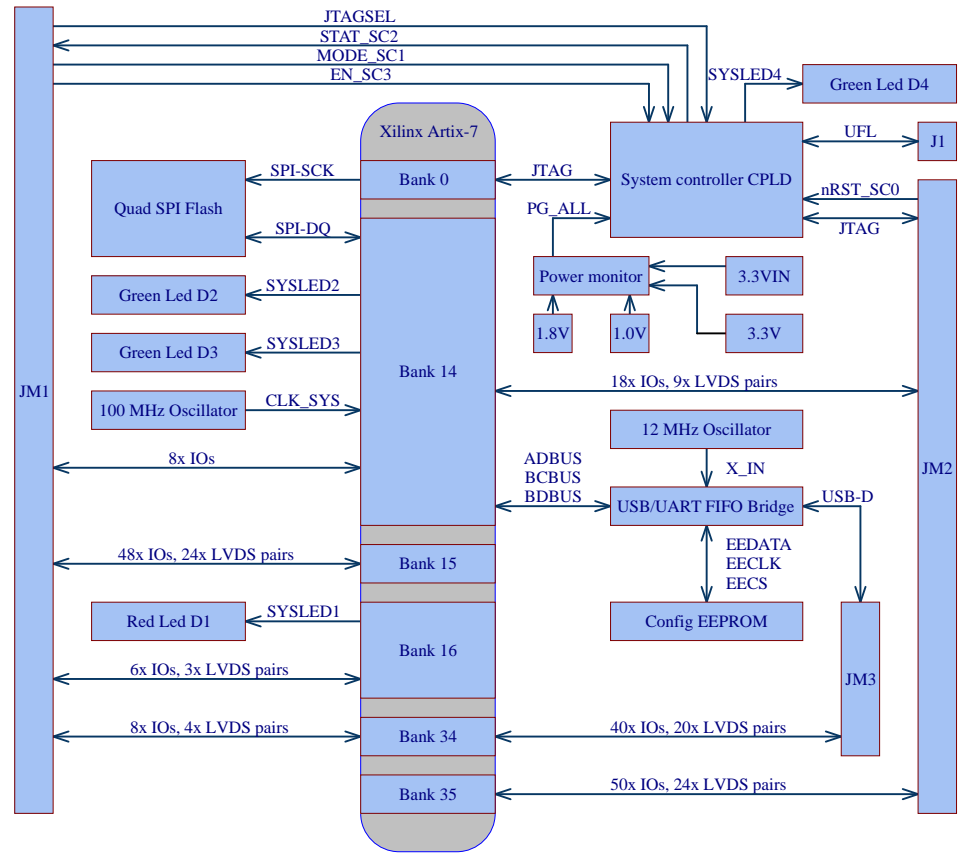
	Title: TE0711 - Changes list		
	A4	Number: TE0711 42C-1-A	Rev. 02
	Date: 04-Sep-23	Copyright: Trenz Electronic GmbH	Page 2 of 15
	Filename: Revision_Changes.SchDoc		

1

2

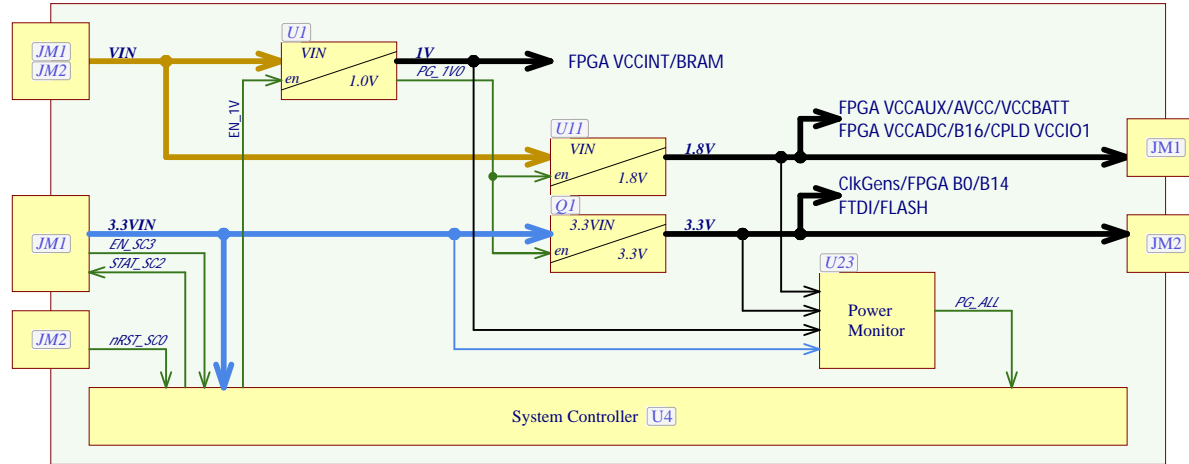
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4



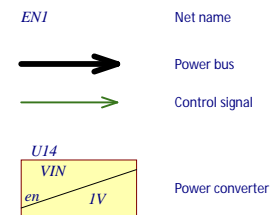
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	A4	Number: TE0711 42C-1-A	Rev. 02
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	Filename: Overview.SchDoc		

Power-on sequencing:



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5.0V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCIO15	IN	1.2 - 3.3V	+/-3%	HR IO Bank15	-
VCCIO34	IN	1.2 - 3.3V	+/-3%	HR IO Bank34	-
VCCIO35	IN	1.2 - 3.3V	+/-3%	HR IO Bank35	-
3.3V	OUT	3.3V	+/-5%	Power for Carrier	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-



Title: TE0711 - Power Diagram		
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U_FPGA_PWR_MISC
FPGA_PWR_MISC.SchDoc

U_FPGA_CFG
FPGA_CFG.SchDoc

U_B14_B16
B14_B16.SchDoc

U_B15
B15.SchDoc

U_B34
B34.SchDoc

U_B35
B35.SchDoc

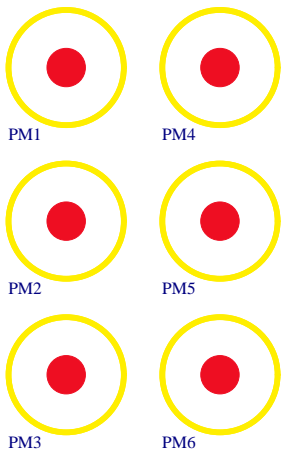
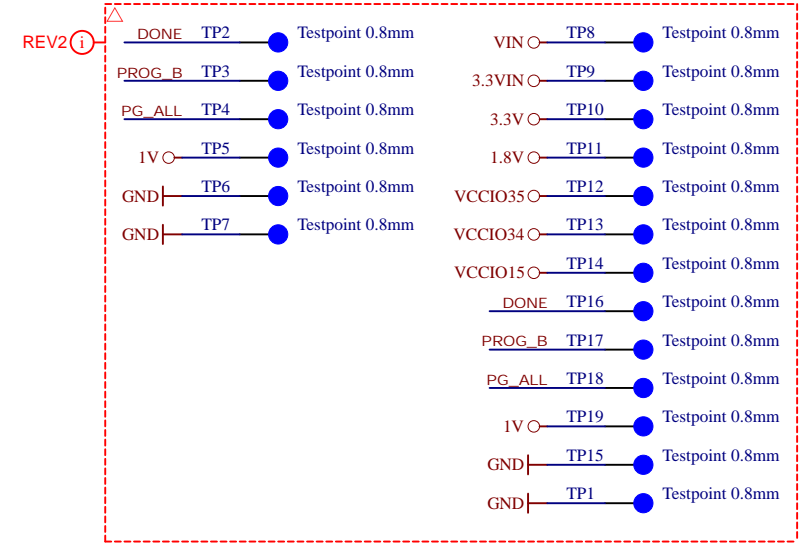
U_SystemController
SystemController.SchDoc

U_FTDI
FTDI.SchDoc

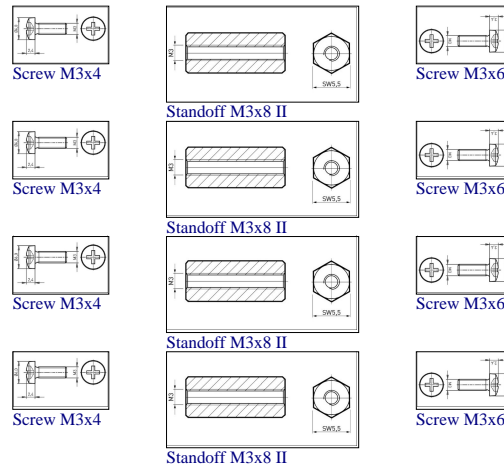
U_POWER
POWER.SchDoc

U_B2B_Connector
B2B_Connector.SchDoc

Special notes:



Top of Board



Serial
Serialnumber 6,3 x 6.3mm

LOGO1
TE Logo PRINT Layer

LOGO PRINT

UKCA1
UKCA Logo on Top Overlay

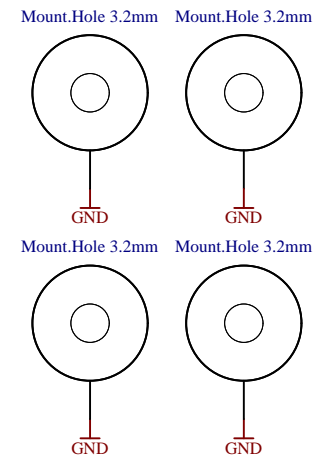
UKCA-TOPOVERLAY

CE1
CE Logo on Top Overlay

CE-TOPOVERLAY



Title: TE0711		
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B14: 8 Pins: 8 Single ended; 3.3V Fixed VCCIO
 B15: 48 Pins: 24 Differential; variable VCCIO
 B16: 6 Pins: 3 Differential; 1.8V Fixed VCCIO
 B34: 8 Pins: 4 Differential; variable VCCIO

B34: 40 Pins: 20 Differential; variable VCCIO
 USB Device

B14: 18 Pins: 9 Differential; 3.3V Fixed VCCIO
 B35: 50 Pins: 24 Differential; variable VCCIO
 JTAG: 3.3V Levels

A

A

B

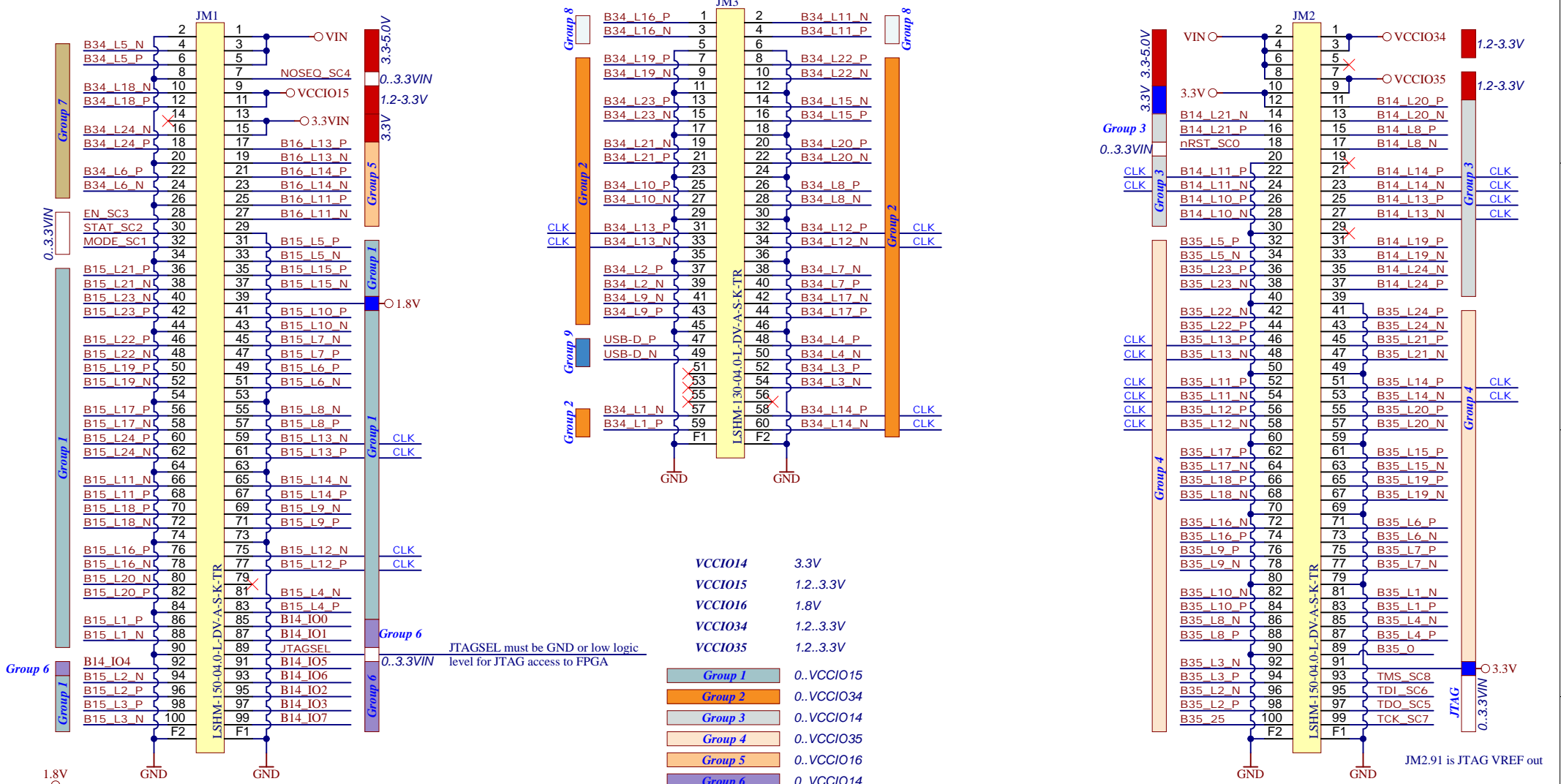
B

C

C

D

D



- VCCIO14 3.3V
- VCCIO15 1.2..3.3V
- VCCIO16 1.8V
- VCCIO34 1.2..3.3V
- VCCIO35 1.2..3.3V
- Group 1 0..VCCIO15
- Group 2 0..VCCIO34
- Group 3 0..VCCIO14
- Group 4 0..VCCIO35
- Group 5 0..VCCIO16
- Group 6 0..VCCIO14
- Group 7 0..VCCIO34
- Group 8 0..VCCIO34
- Group 9 USB_OTG
- Special PWR_in
- PWR_out

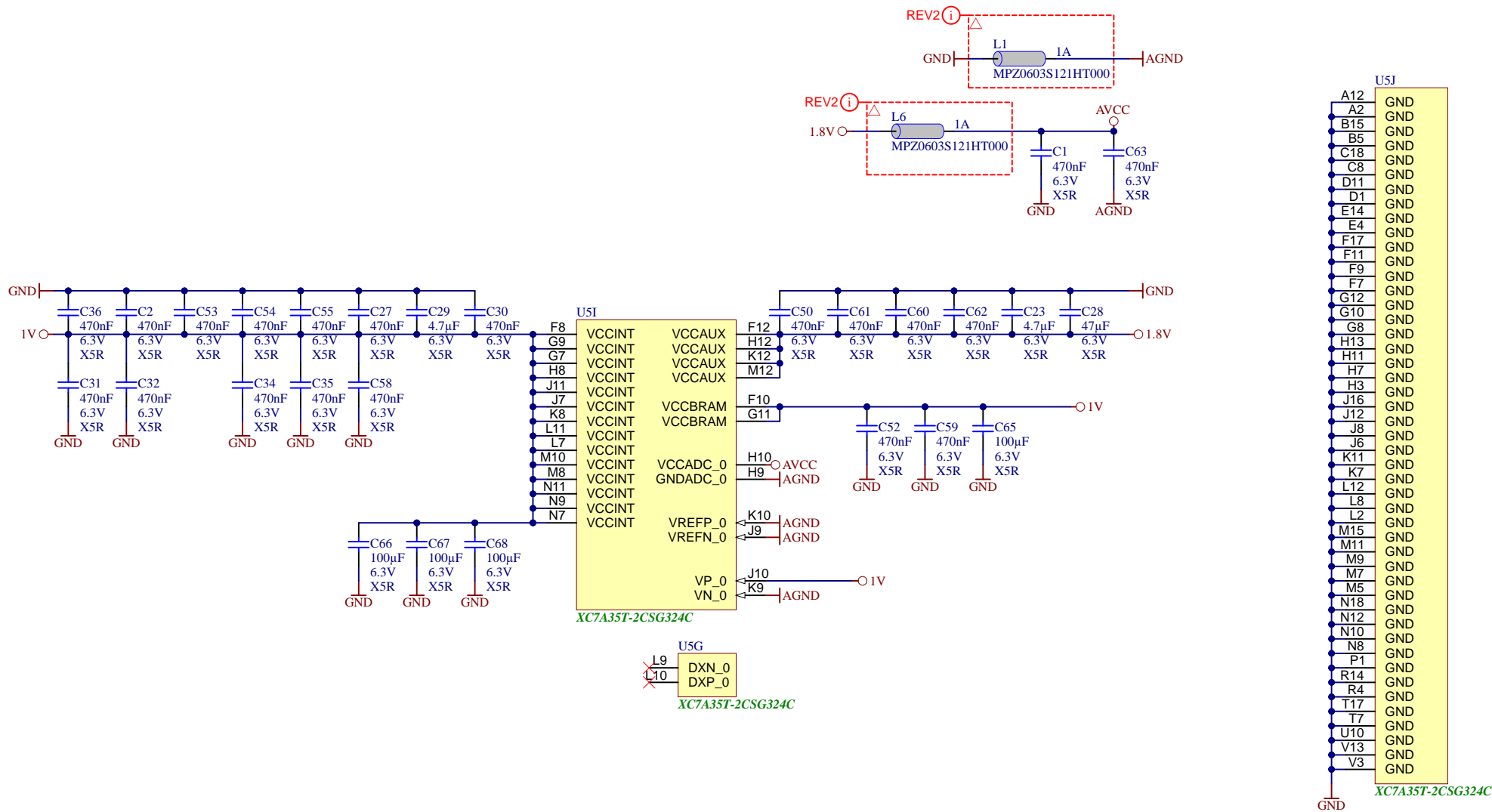
JTAGSEL must be GND or low logic level for JTAG access to FPGA

JM2.91 is JTAG VREF out

Some information about Trenz modules compatibility and differences [here](#)



Title: TE0711 - B2B-Connectors		
A4	Number: TE0711 42C-1-A	Rev. 02
Date: 23-Aug-23	Copyright: Trenz Electronic GmbH / TT	Page 6 of 15
Filename: B2B_Connector.SchDoc		



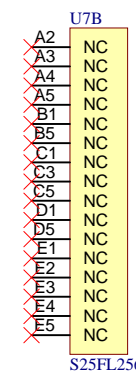
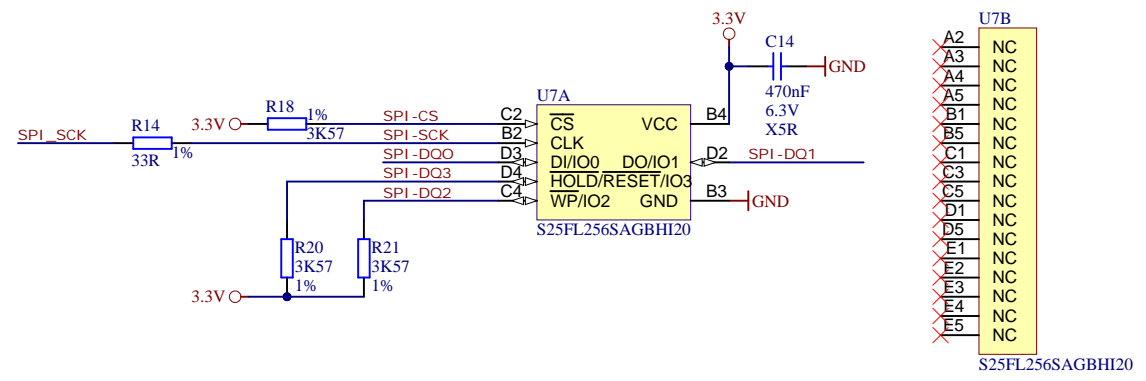
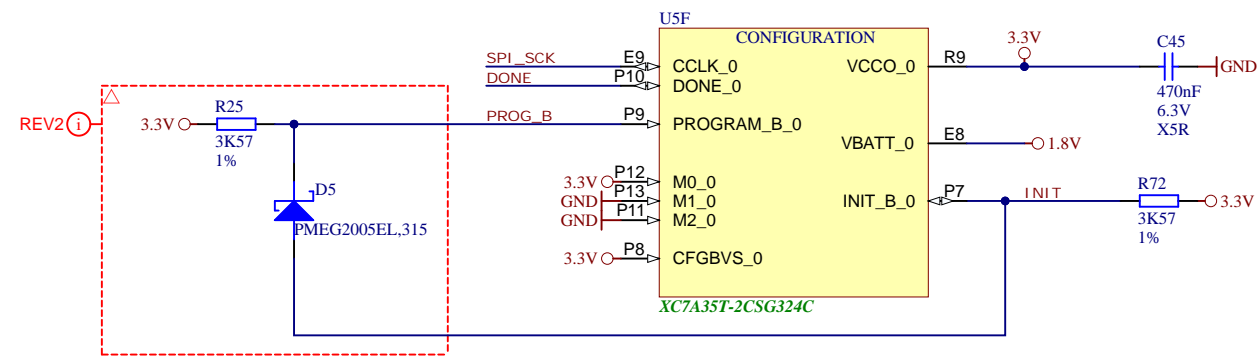
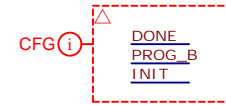
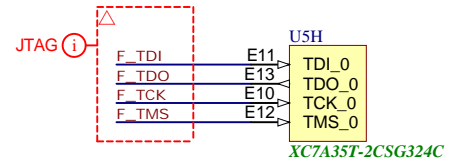
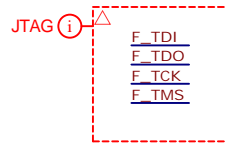
U5J

A12	GND
A2	GND
B15	GND
B5	GND
C18	GND
C8	GND
D11	GND
D1	GND
E14	GND
E4	GND
F17	GND
F11	GND
F9	GND
F7	GND
G12	GND
G10	GND
G8	GND
H13	GND
H11	GND
H7	GND
H3	GND
J16	GND
J12	GND
J8	GND
J6	GND
K11	GND
K7	GND
L12	GND
L8	GND
L2	GND
M15	GND
M11	GND
M9	GND
M7	GND
M5	GND
N18	GND
N12	GND
N10	GND
N8	GND
P1	GND
R14	GND
R4	GND
T17	GND
T7	GND
U10	GND
V13	GND
V3	GND

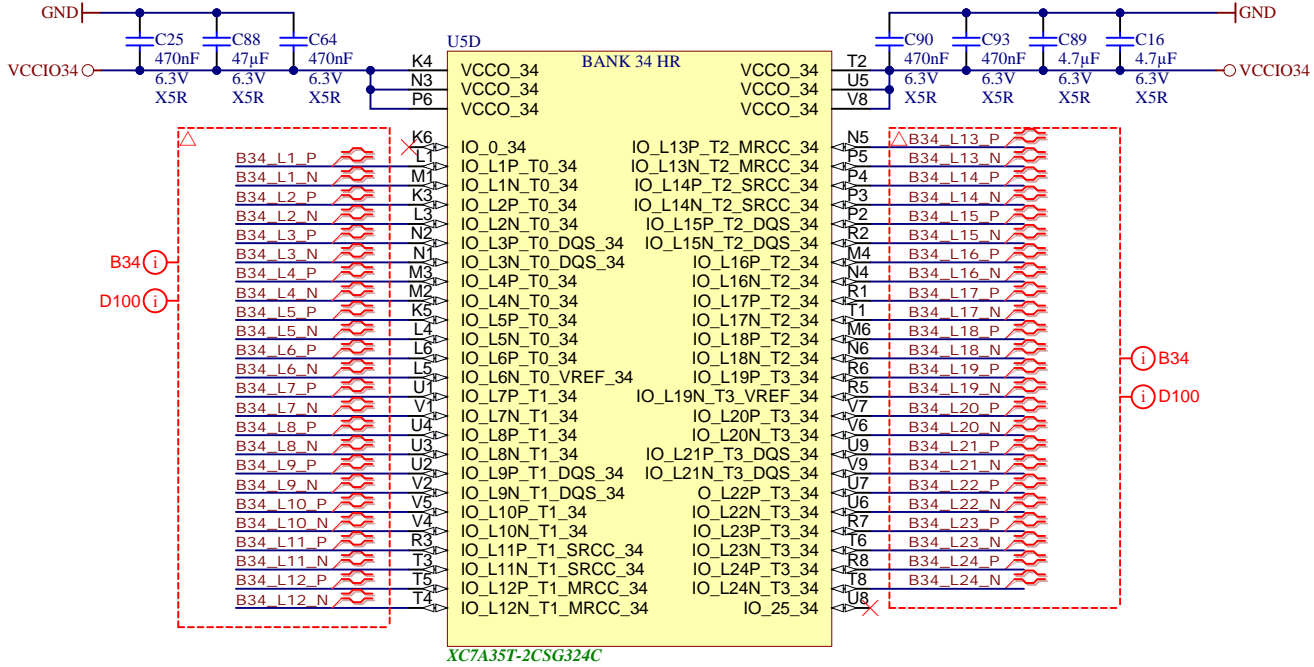
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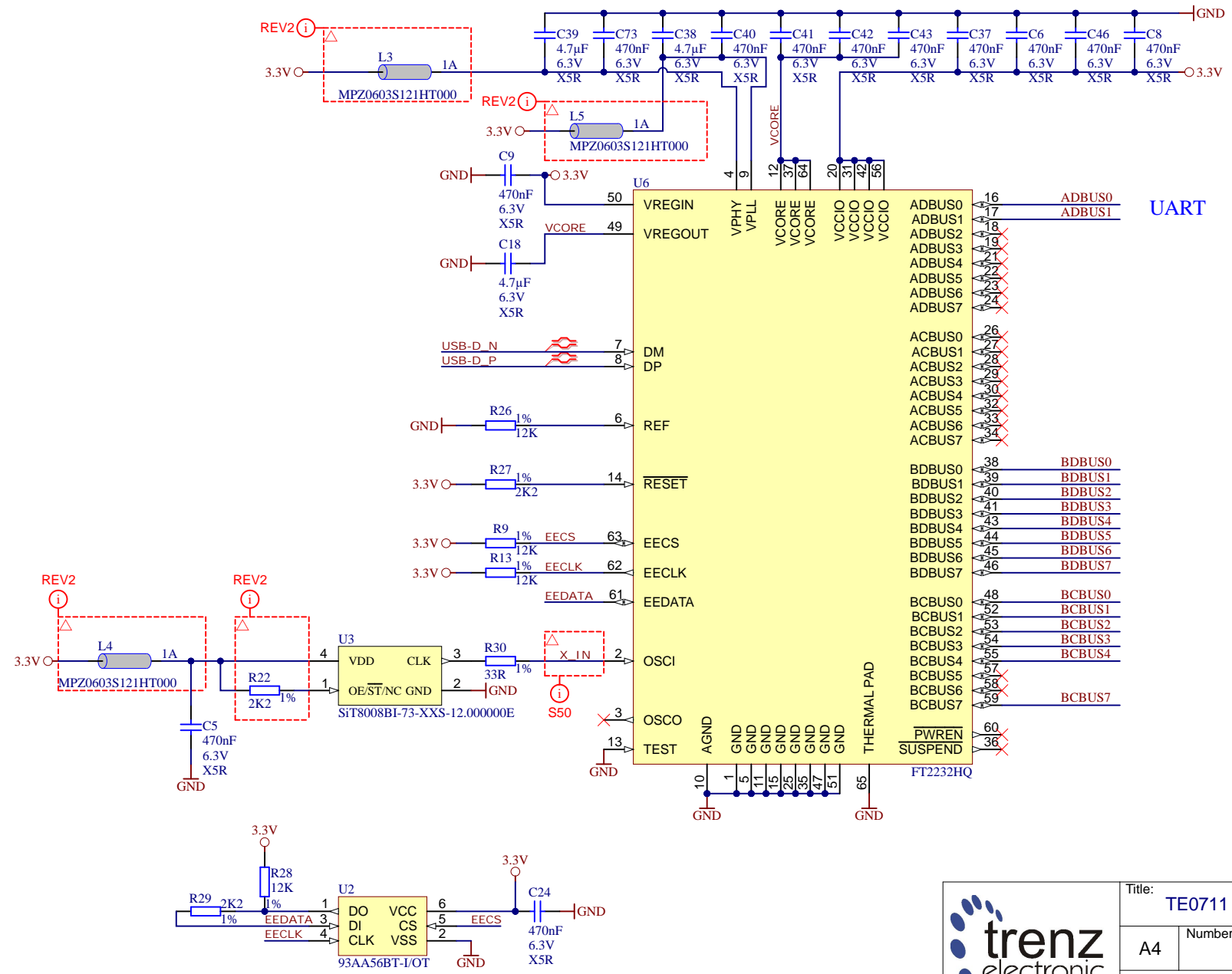
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A4	Number: TE0711 42C-1-A	Rev. 02
Date: 27-Jul-23	Copyright: Trenz Electronic GmbH / TT	Page 7 of 15
Filename: FPGA_PWR_MISC.SchDoc		



	Title: TE0711 - FPGA Configuration		
	A4	Number: TE0711 42C-1-A	Rev. 02
	Date: 28-Jul-23	Copyright: Trenz Electronic GmbH / TT	
	Page 8 of 15		
Filename: FPGA_CFG.SchDoc			



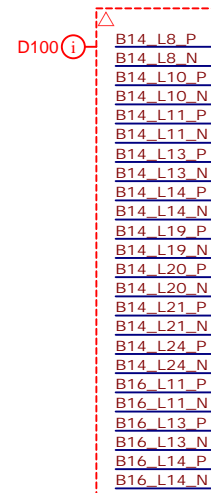
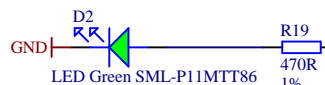
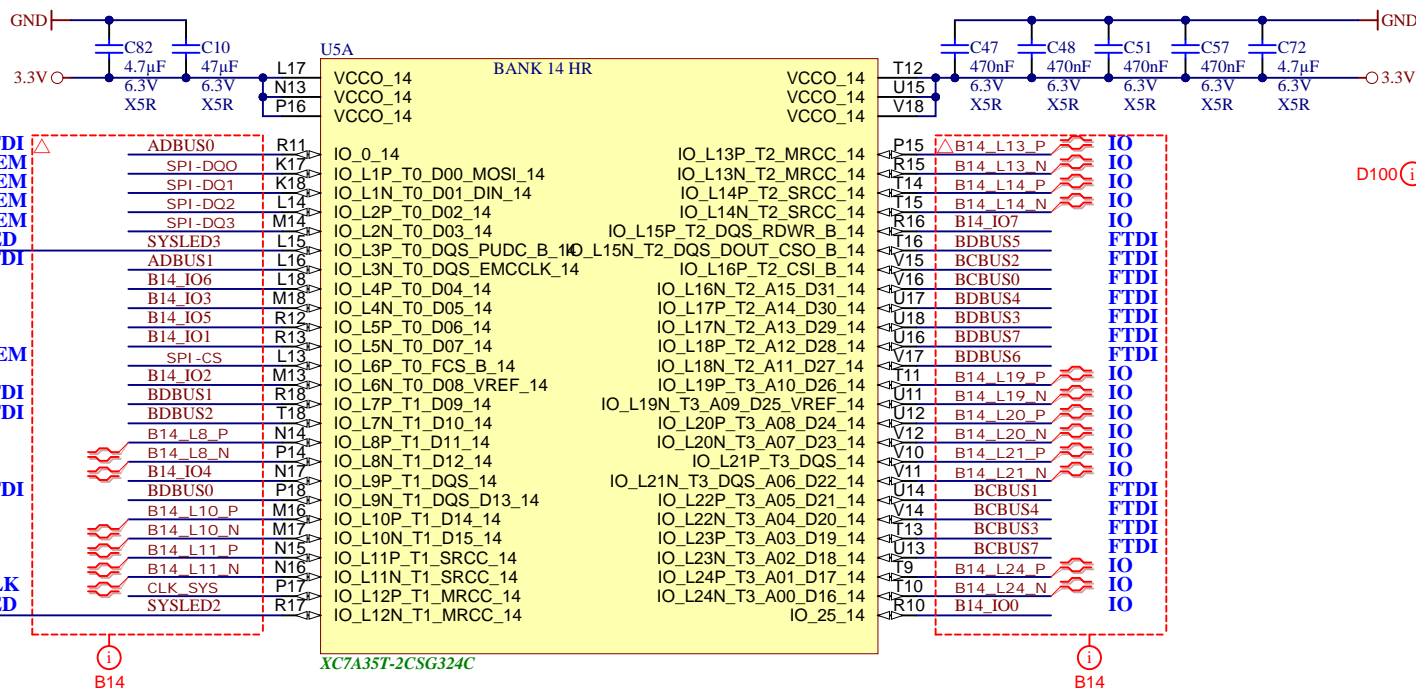
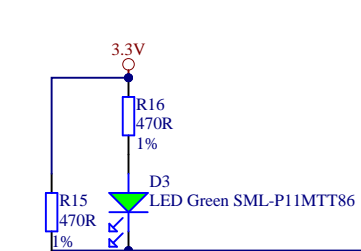
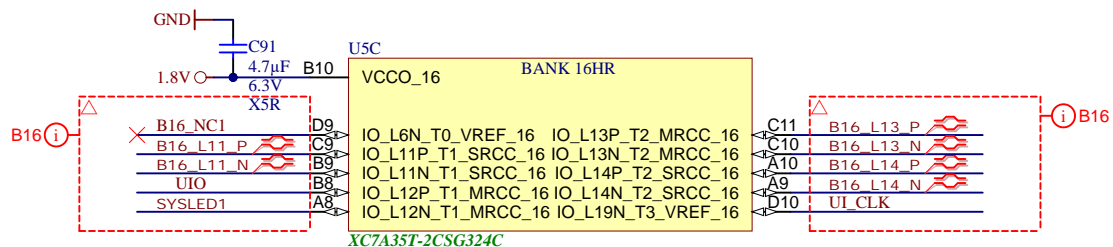
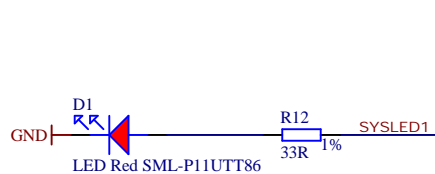
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Date: 24-Aug-23		Copyright: Trenz Electronic GmbH / TT	
Filename: B34.SchDoc			



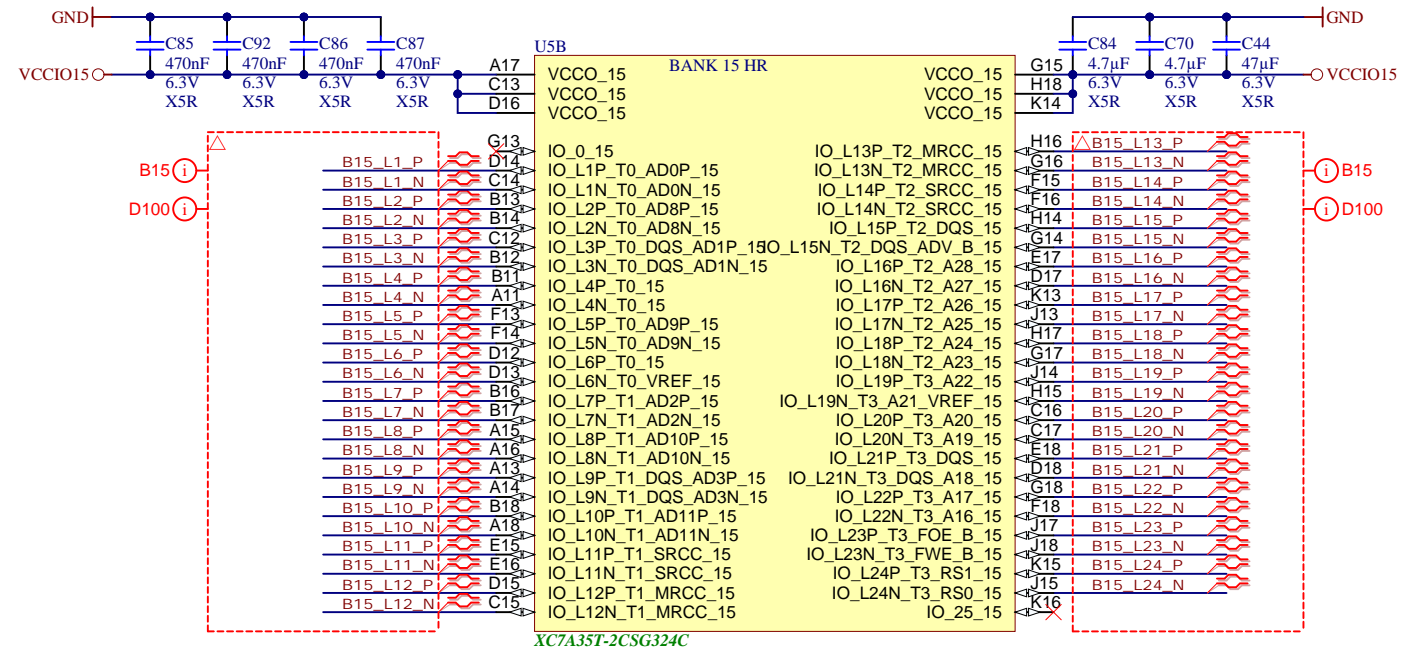
UART



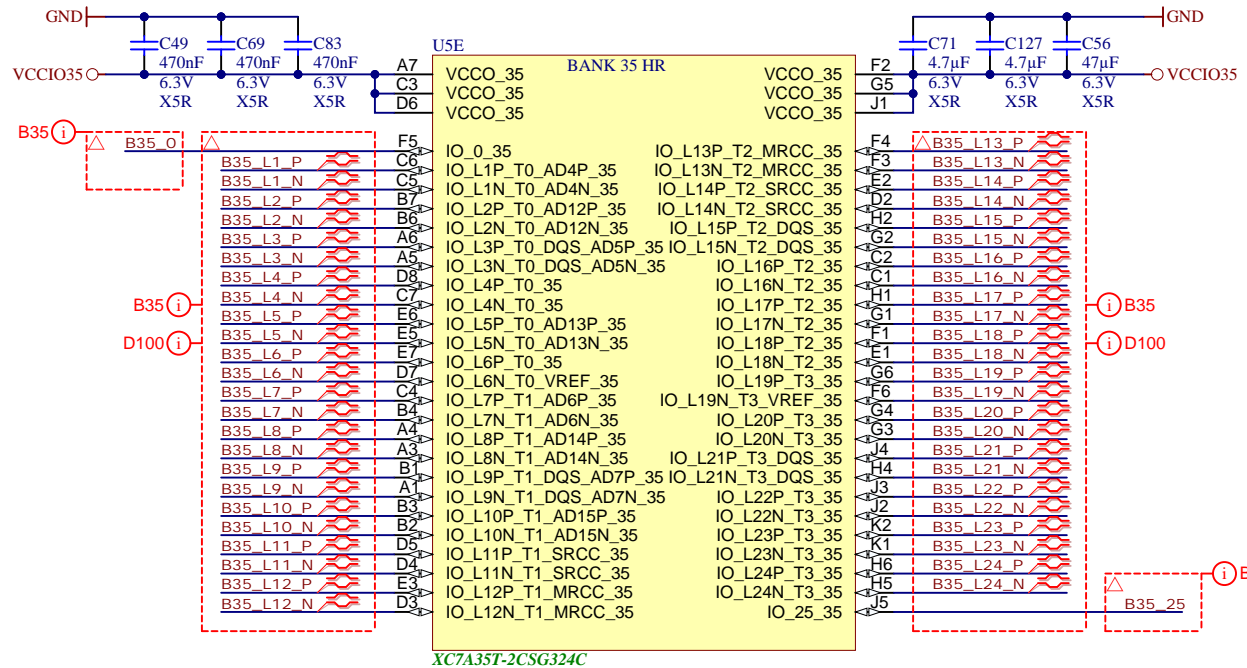
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Filename: FTDI.SchDoc		




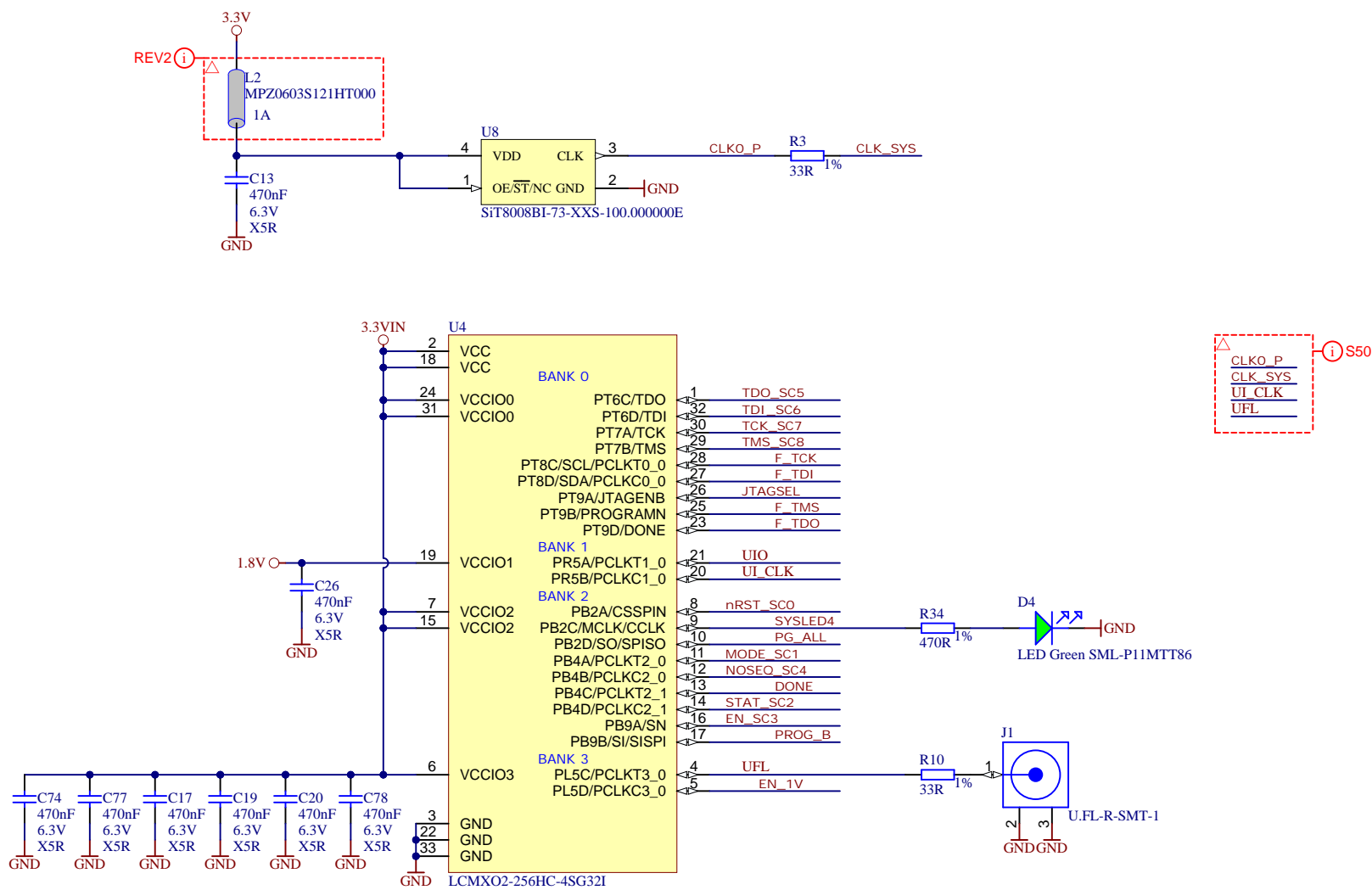
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A4	Number: TE0711 42C-1-A	Rev. 02
Date: 24-Aug-23	Copyright: Trenz Electronic GmbH / TT	Page 11 of 15
Filename: B14_B16.SchDoc		




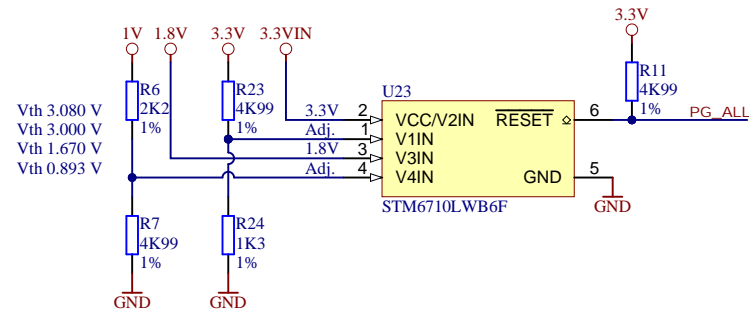
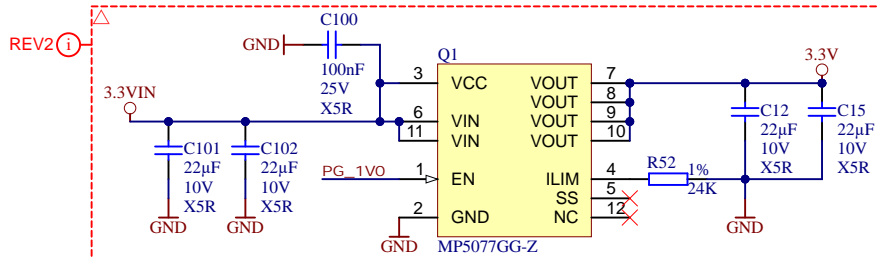
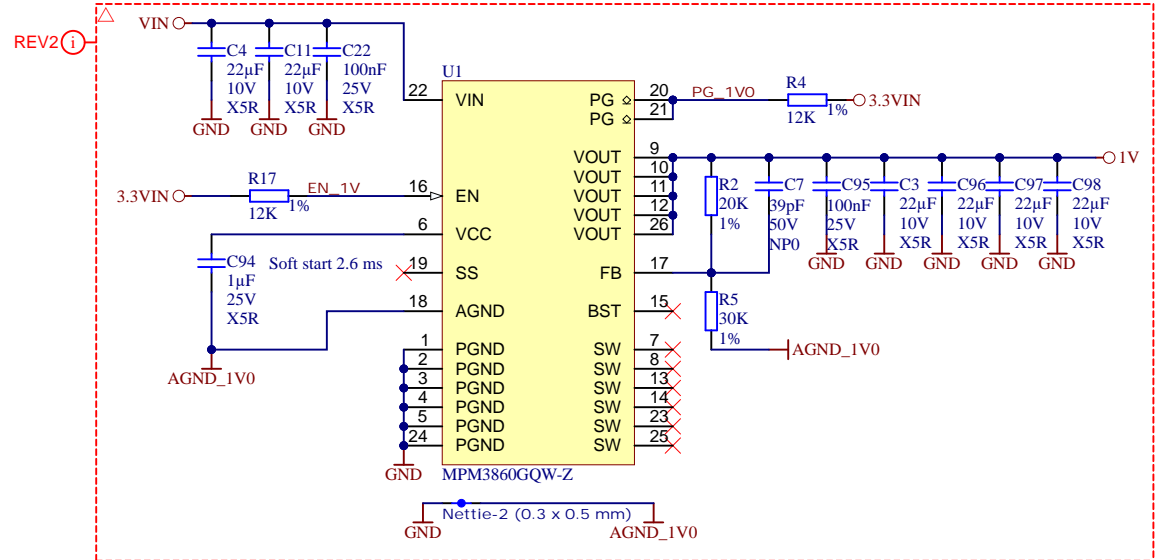
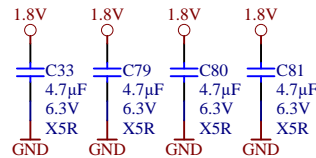
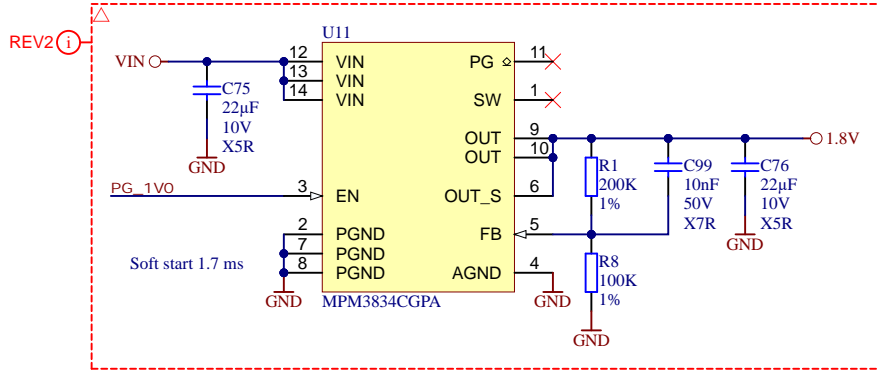
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	Date: 23-Aug-23	Copyright: Trenz Electronic GmbH / TT	Page 12 of 15
	Filename: B15.SchDoc		



		Title: TE0711 - FPGA B35	
		A4	Number: TE0711 42C-1-A
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Filename: B35.SchDoc			
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		Title: TE0711 - System Controller	
		A4	Number: TE0711 42C-1-A
Date: 24-Aug-23		Copyright: Trenz Electronic GmbH	
Filename: SystemController.SchDoc		Page 14 of 15	



Title: TE0711 - POWER		
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