

A

A

B

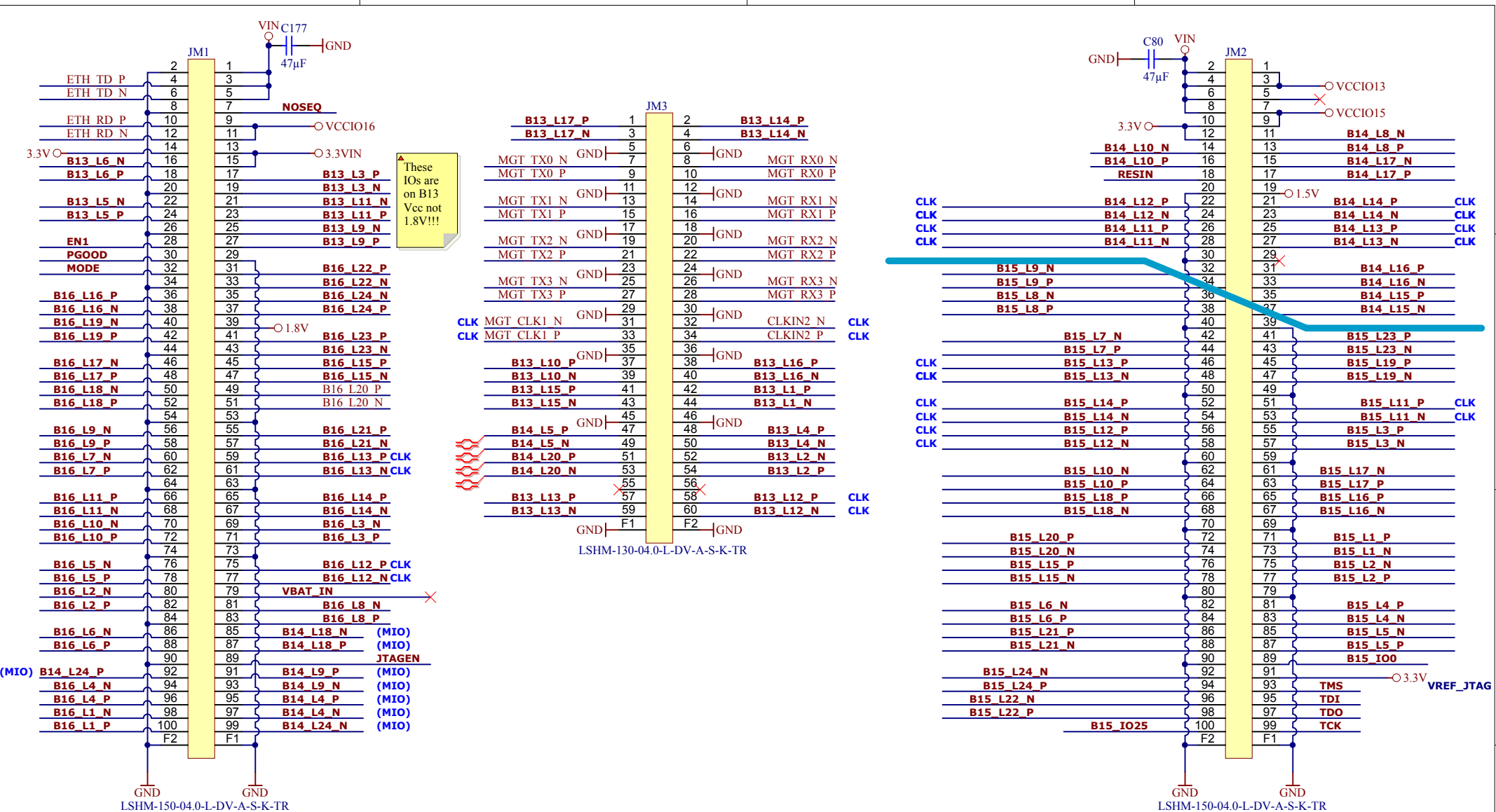
B

C

C

D

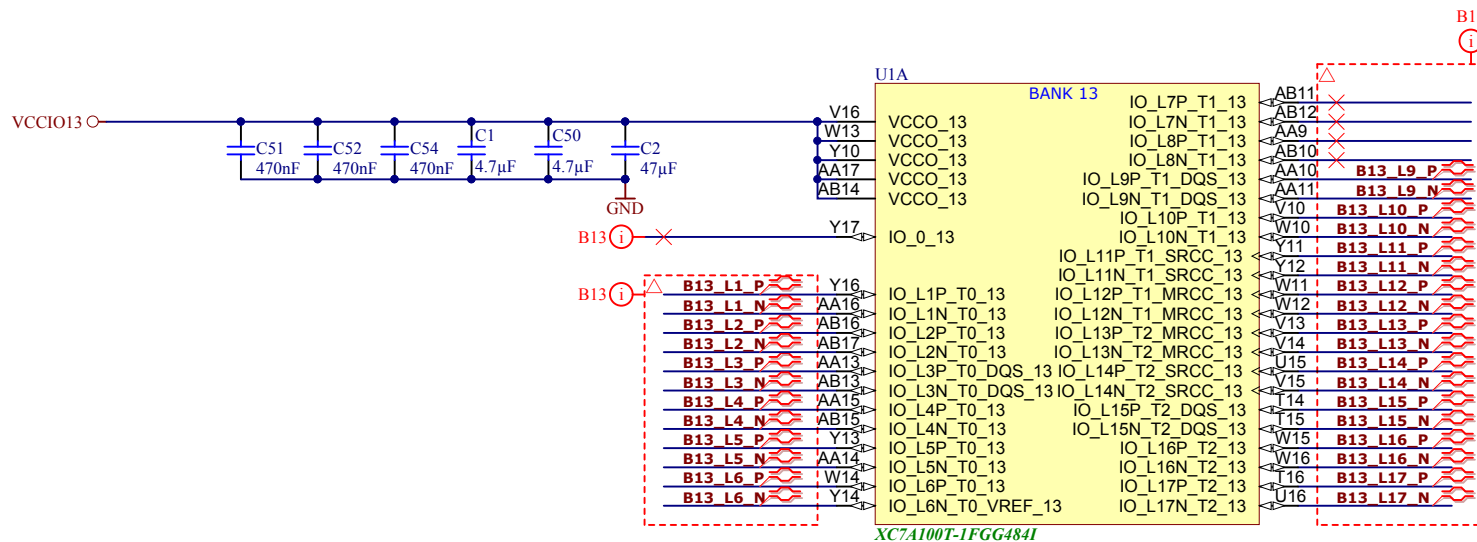
D



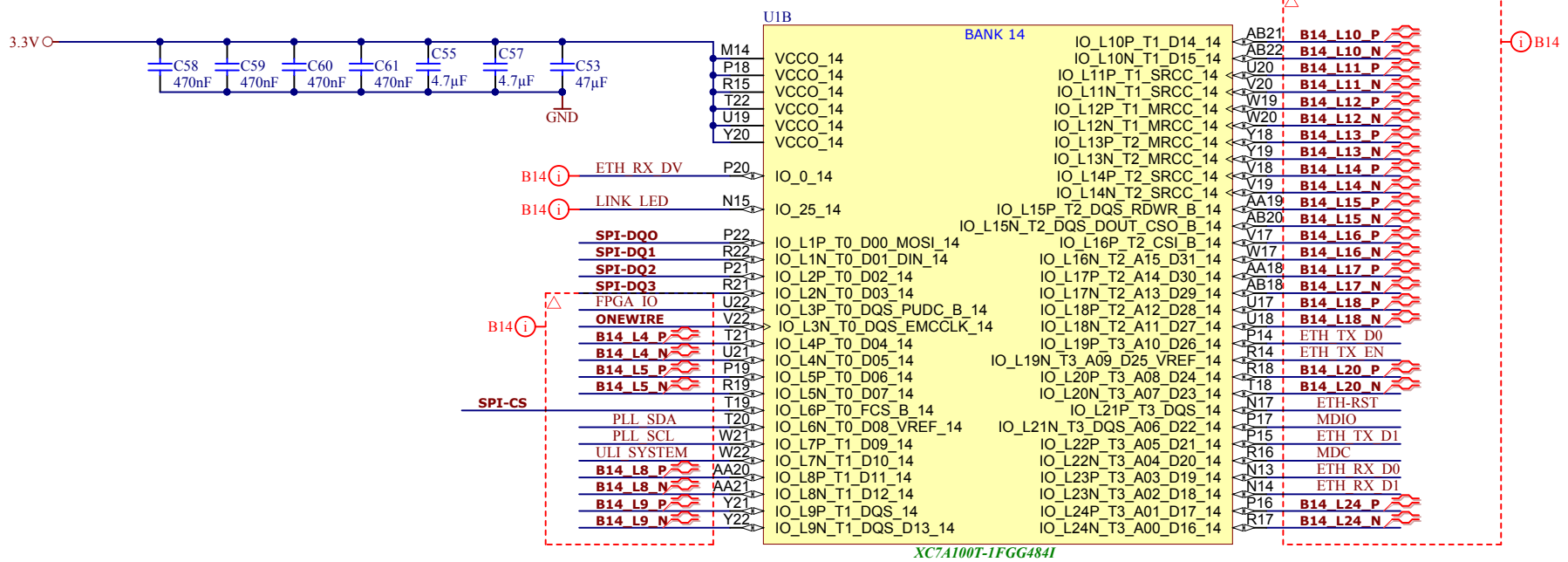
These IOs are on B13 Vcc not 1.8V!!!



Title: B2B		
A4	Number: TE0712 100_11	Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page1 of 16
Filename: B2B-Connectors.SchDoc		



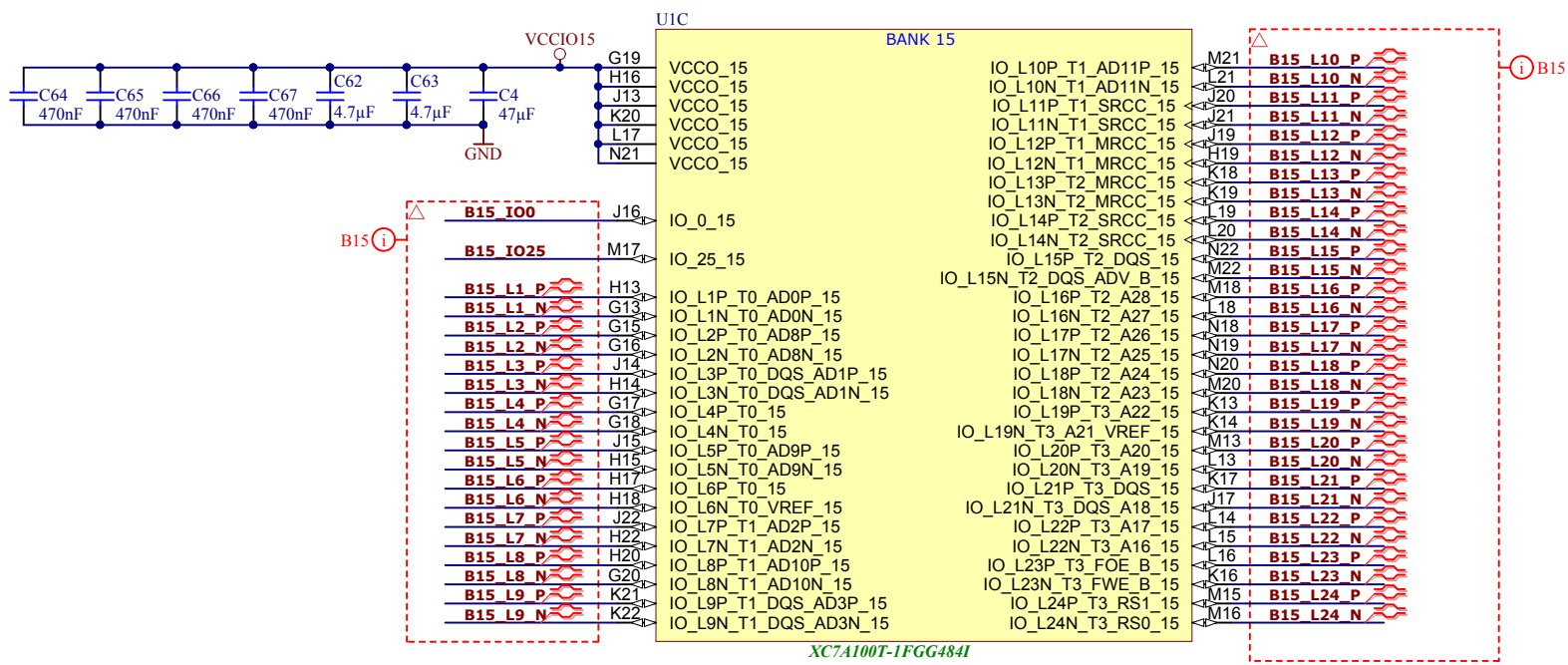
Title: B13		
A4	Number: TE0712 100_11	Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page2 of 16
Filename: B13.SchDoc		



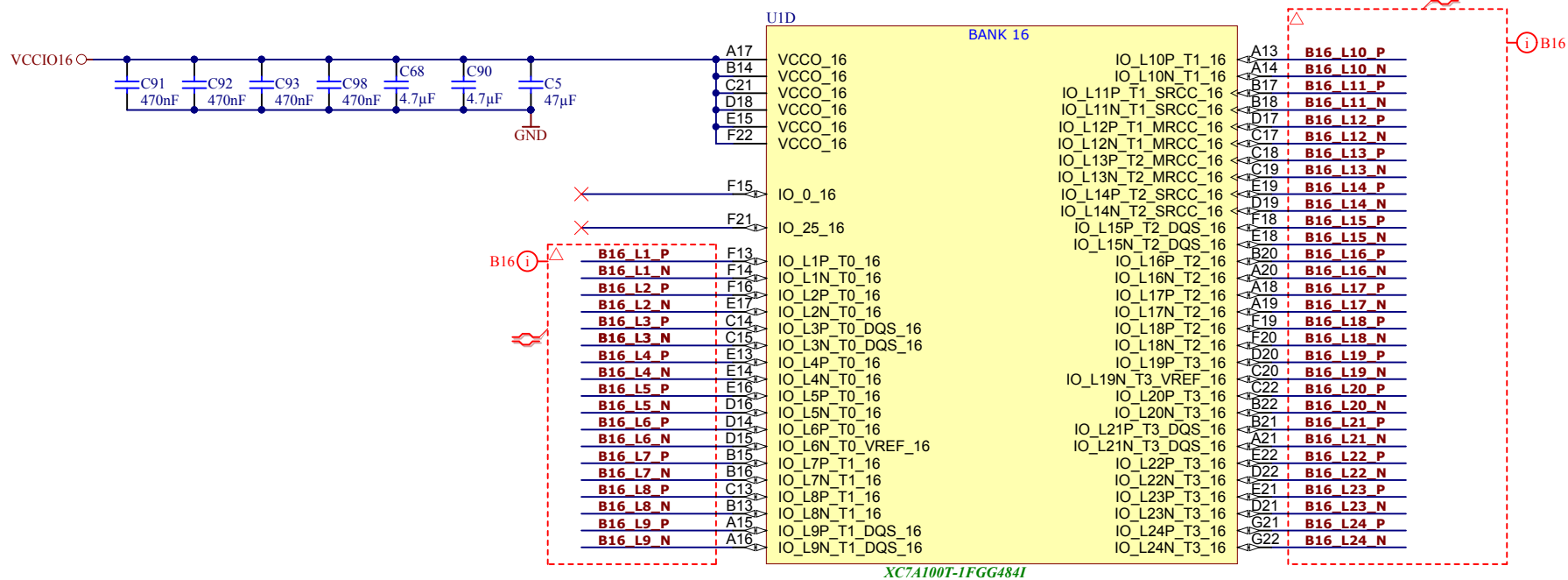
XC7A100T-1FGG484I



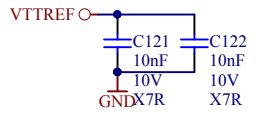
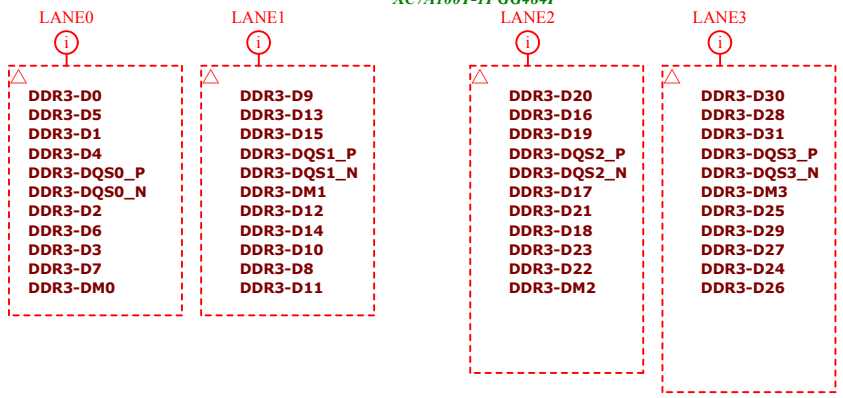
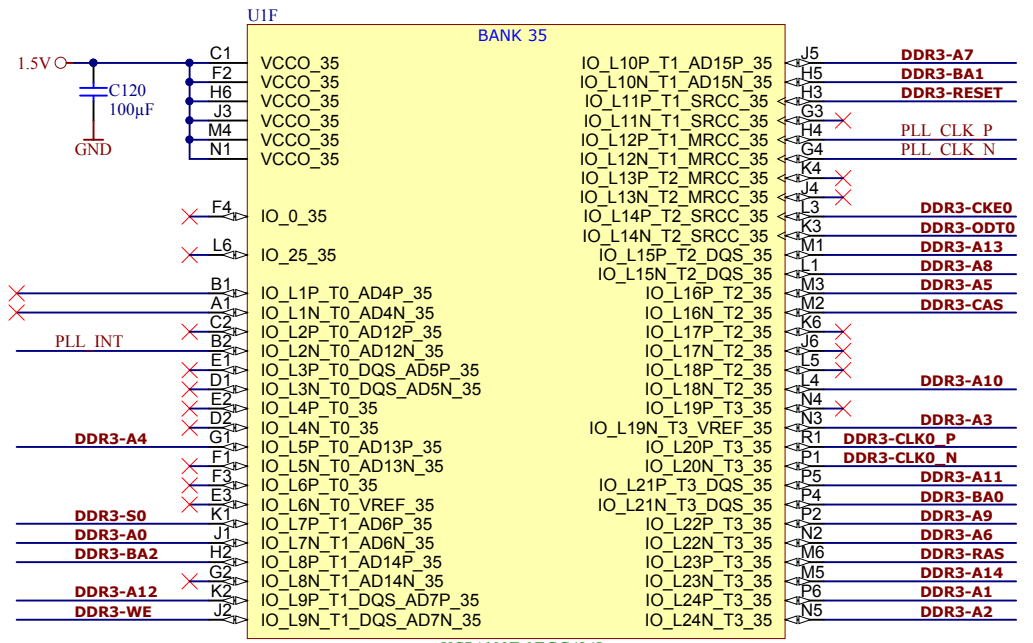
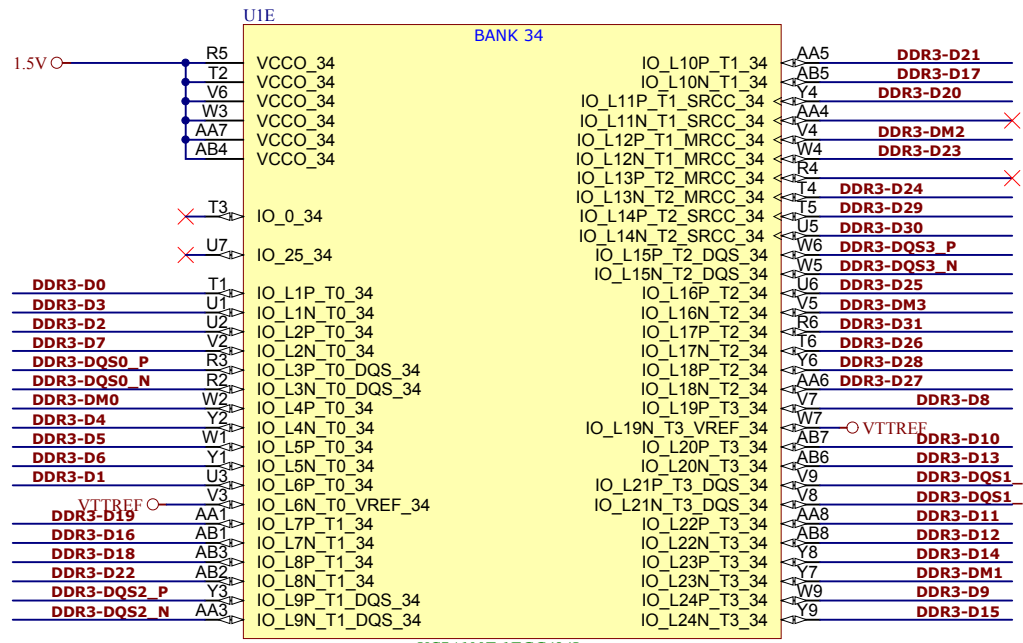
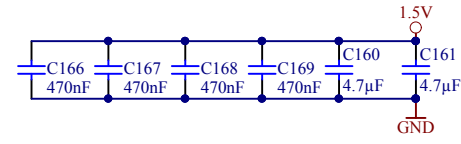
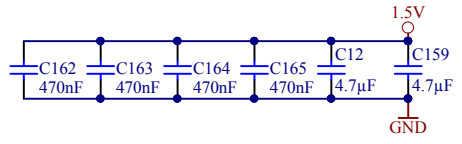
Title: <b>B14</b>		
A4	Number: <b>TE0712 100_11</b>	Rev. <b>01</b>
Date: <b>2014-06-23</b>	Copyright: <b>2014 Trenz Electronic GmbH</b>	Page <b>3</b> of <b>16</b>
Filename: <b>B14.SchDoc</b>		



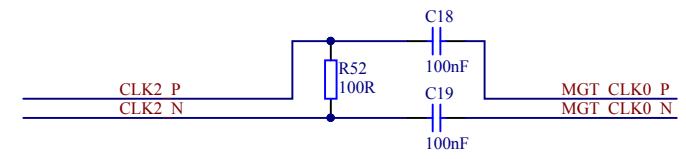
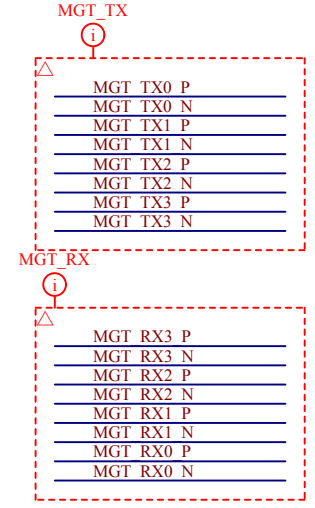
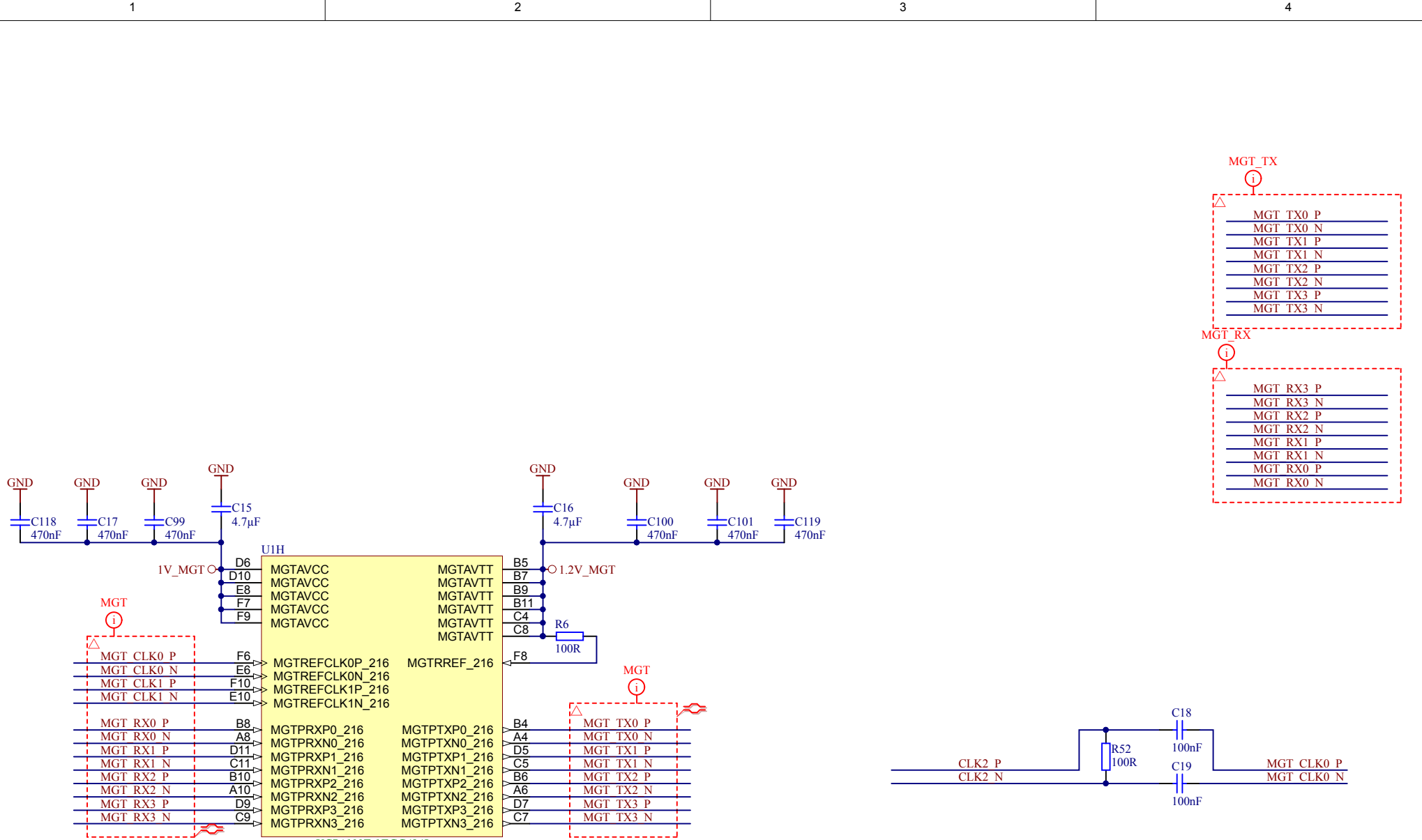
Title: <b>B15</b>		
A4	Number: <b>TE0712 100_11</b>	Rev. <b>01</b>
Date: <b>2014-06-23</b>	Copyright: <b>2014 Trenz Electronic GmbH</b>	Page <b>4</b> of <b>16</b>
Filename: <b>B15.SchDoc</b>		




Title: <b>B16</b>		
A4	Number: <b>TE0712 100_11</b>	Rev. <b>01</b>
Date: <b>2014-06-23</b>	Copyright: <b>2014 Trenz Electronic GmbH</b>	Page <b>5</b> of <b>16</b>
Filename: <b>B16.SchDoc</b>		



Title: B34		
A4	Number: TE0712 100_11	Rev: 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page6 of 16
Filename: B34.SchDoc		



		Title: MGT	
		A4	Number: TE0712 100_11
Date: 2014-06-23		Copyright: 2014 Trenz Electronic GmbH	
Page 7		of 16	
Filename: FPGA-MGT.SchDoc			

1

2

3

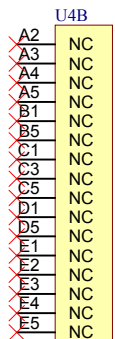
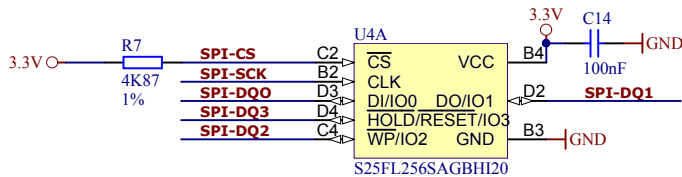
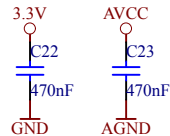
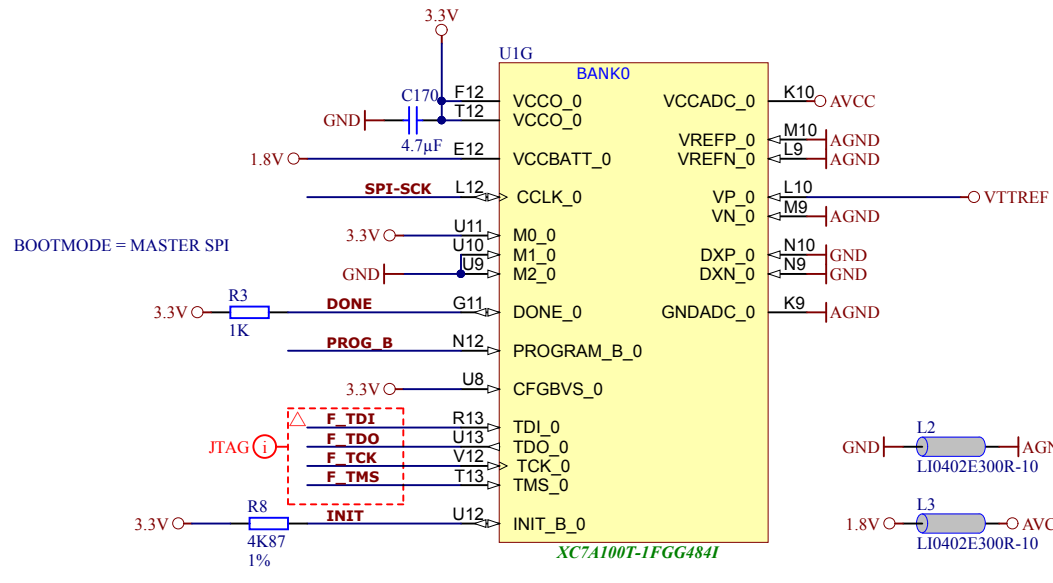
4

1

2

3

4



Title: CFG		
A4	Number: TE0712 100_11	Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page 8 of 16
Filename: FPGA-CFG.SchDoc		



1

2

3

4

A

A

B

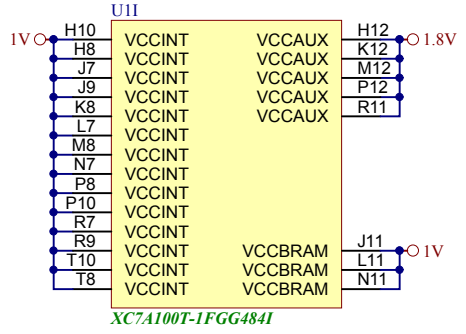
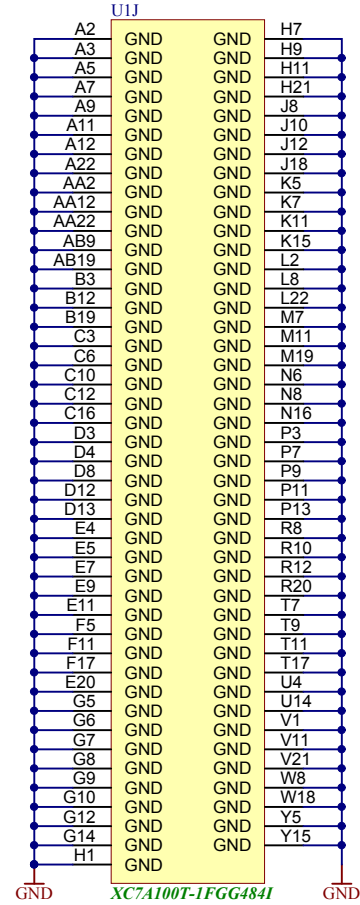
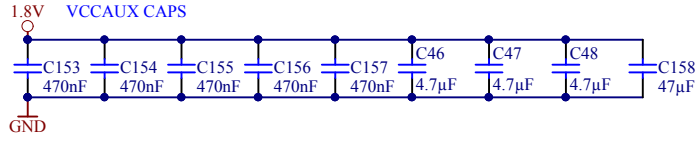
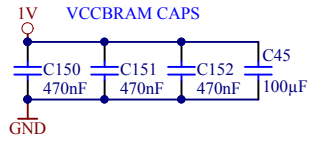
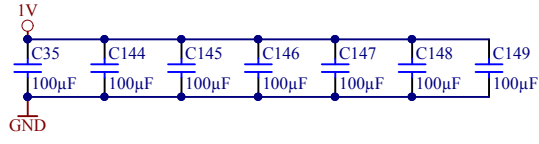
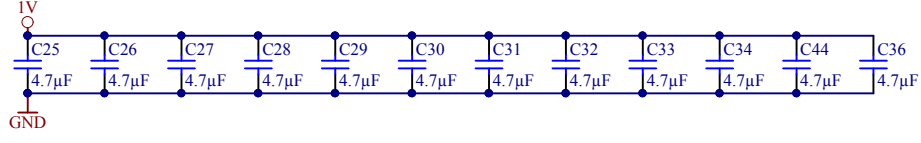
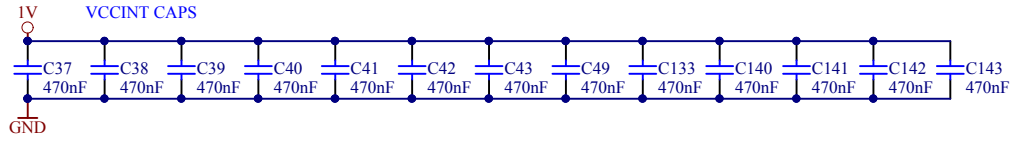
B

C

C

D

D



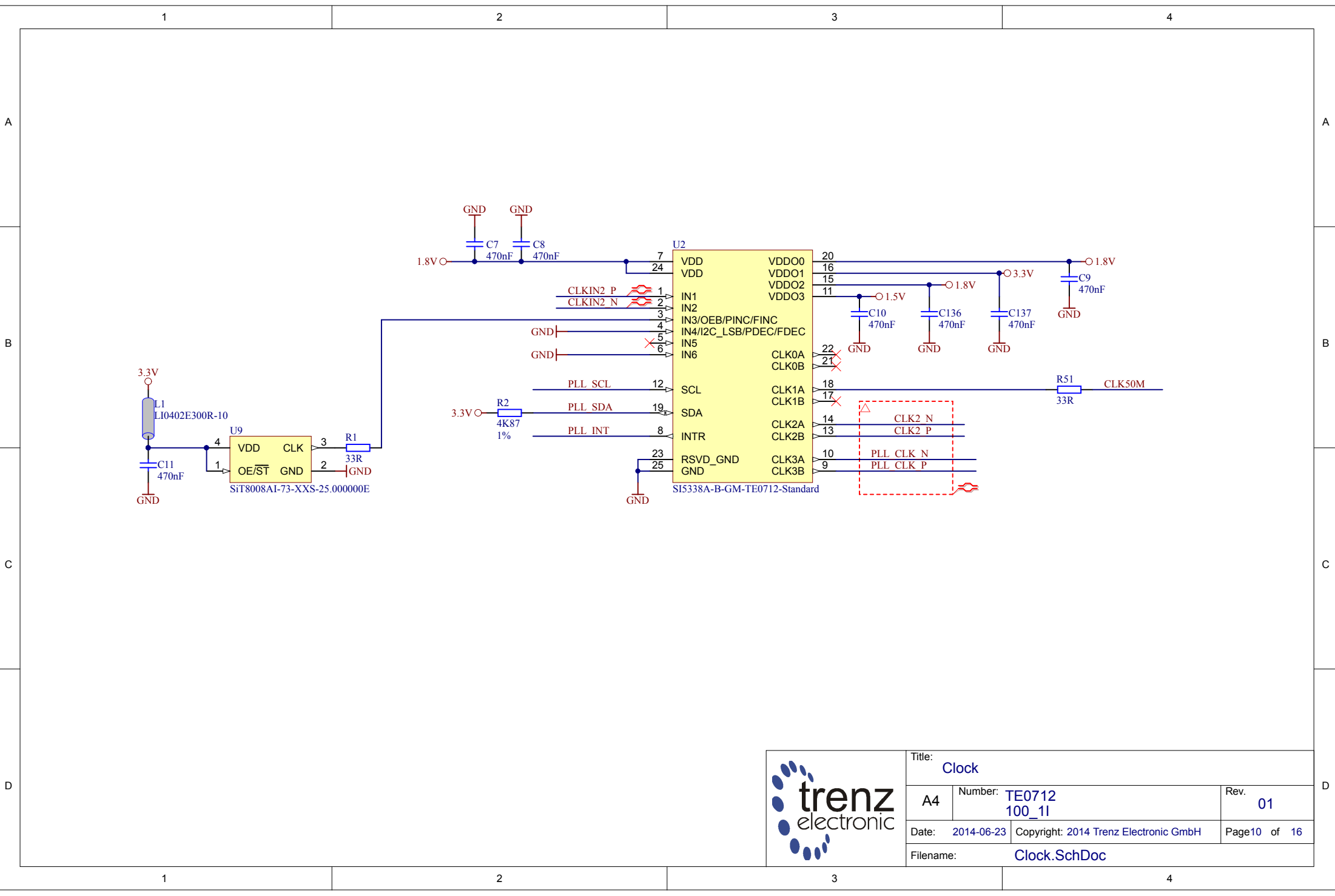
Title: PWR		
A4	Number: TE0712 100_11	Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page9 of 16
Filename: FPGA-PWR.SchDoc		


1

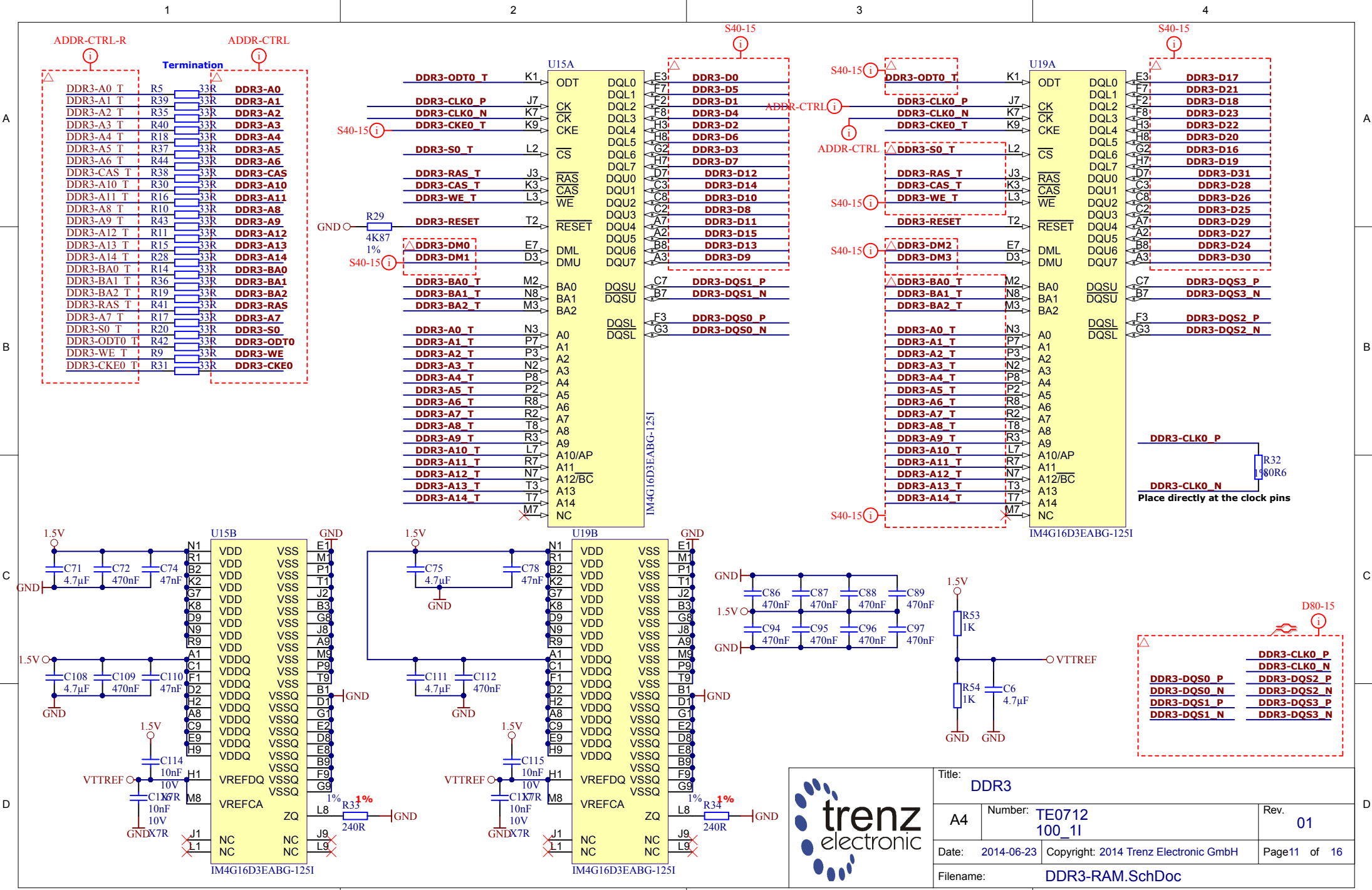
2

3

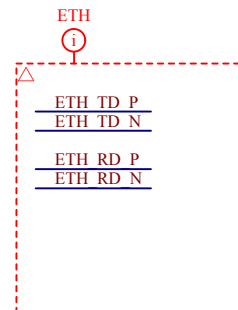
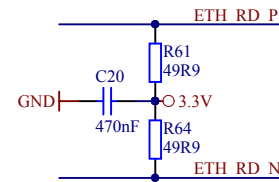
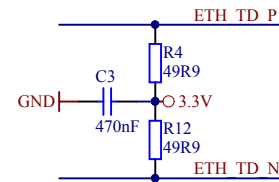
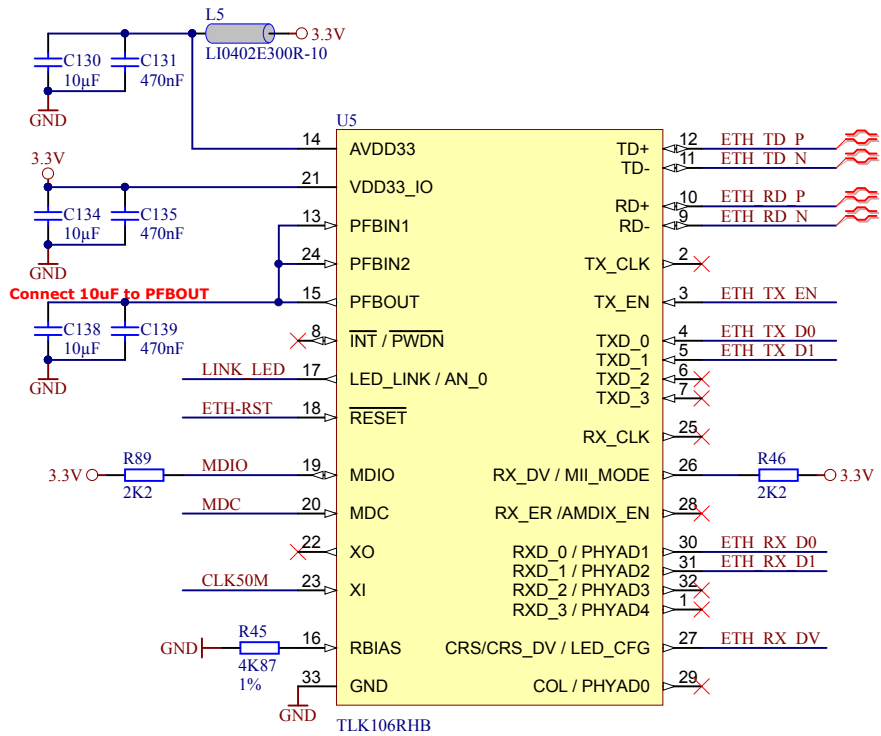
4




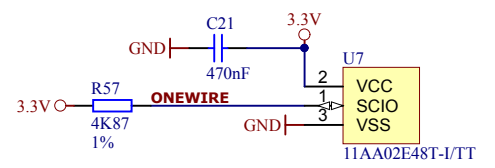
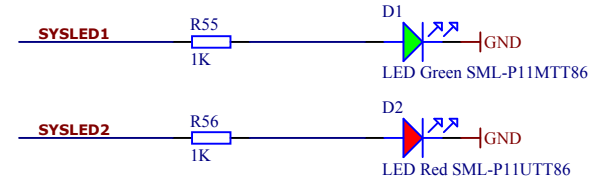
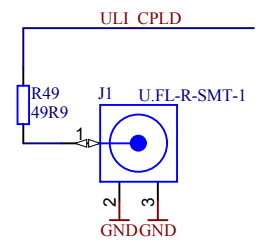
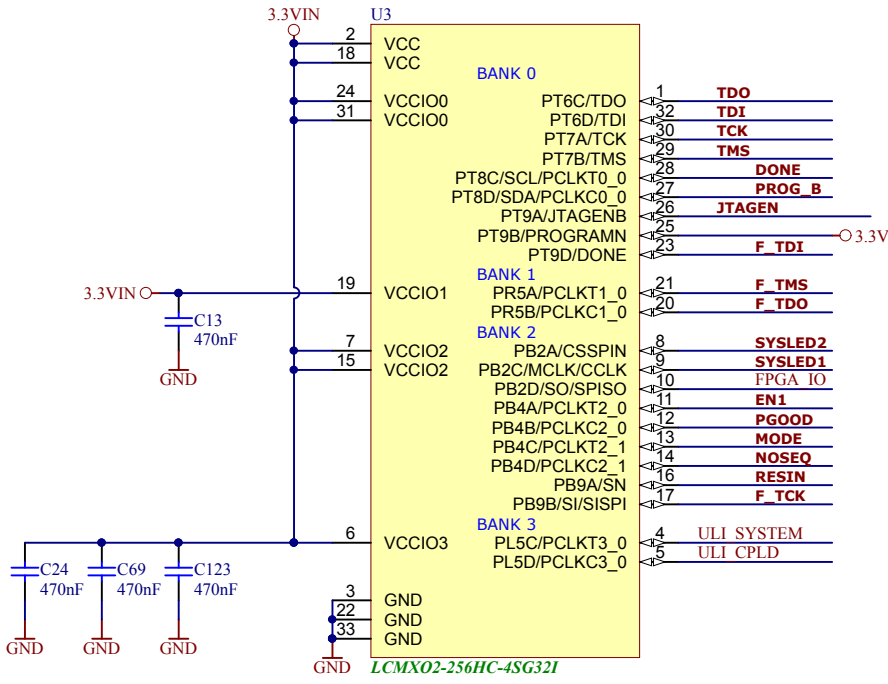
			Title: <b>Clock</b>	
			A4	Number: <b>TE0712 100_11</b>
Date: 2014-06-23		Copyright: 2014 Trenz Electronic GmbH		Page 10 of 16
Filename: <b>Clock.SchDoc</b>				



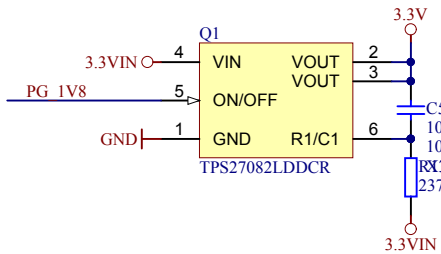
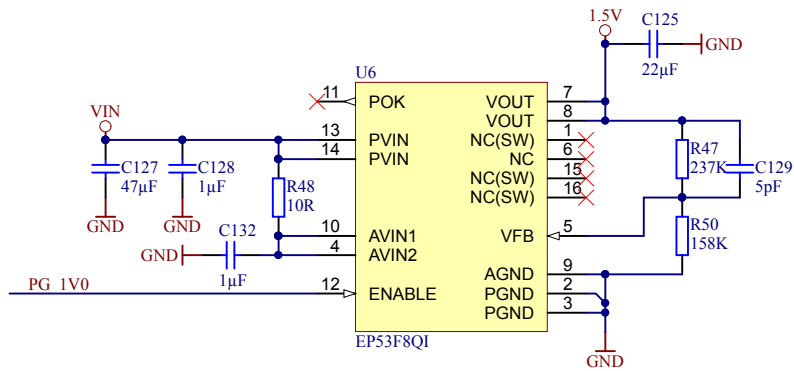
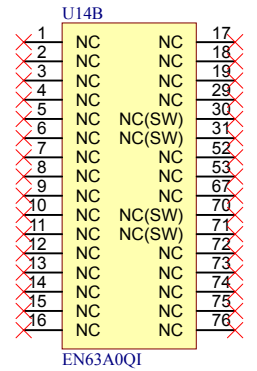
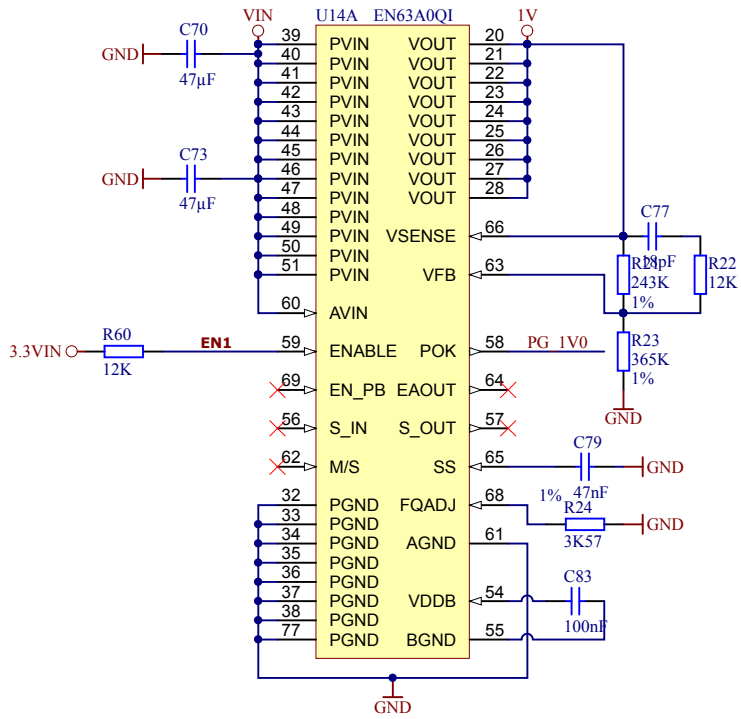
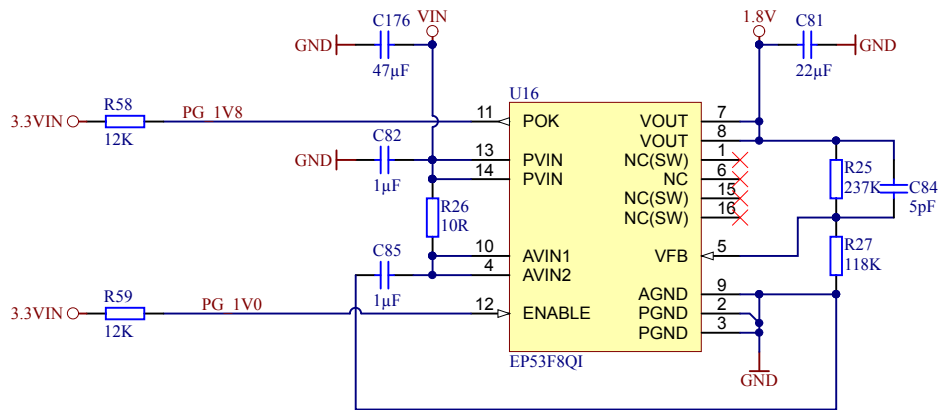
Title: <b>DDR3</b>		
A4	Number: <b>TE0712 100_11</b>	Rev. <b>01</b>
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page 11 of 16
Filename: <b>DDR3-RAM.SchDoc</b>		



	Title: <b>ETH</b>		
	A4	Number: <b>TE0712 100_11</b>	Rev. <b>01</b>
	Date: <b>2014-06-23</b>	Copyright: <b>2014 Trenz Electronic GmbH</b>	Page <b>12</b> of <b>16</b>
	Filename: <b>ETHERNET.SchDoc</b>		



Title: CPLD		
A4	Number: TE0712 100_11	Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page 13 of 16
Filename: CPLD.SchDoc		



Title: PWR		
A4	Number: TE0712 100_11	Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page 14 of 16
Filename: PWR1.SchDoc		

1

2

3

4

A

A

B

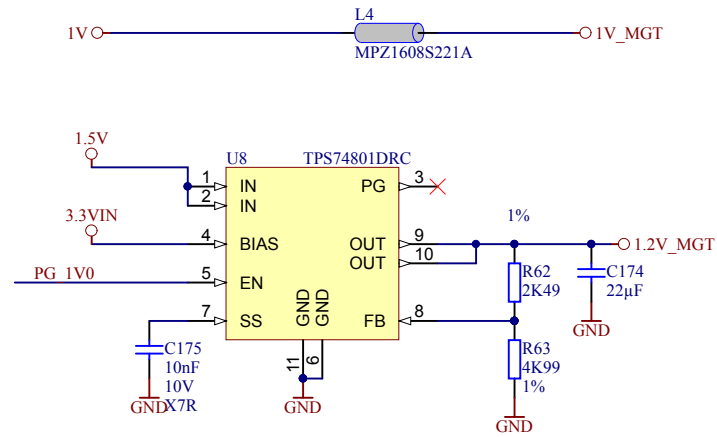
B


C

C

D

D



		Title: PWR	
		A4	Number: TE0712 100_11
Date: 2014-06-23		Copyright: 2014 Trenz Electronic GmbH	
Filename: PWR2.SchDoc		Page 15 of 16	

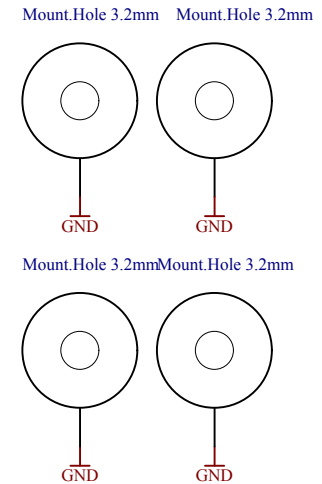
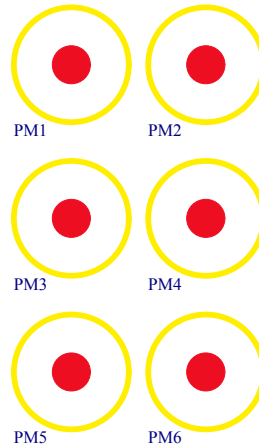
1

2

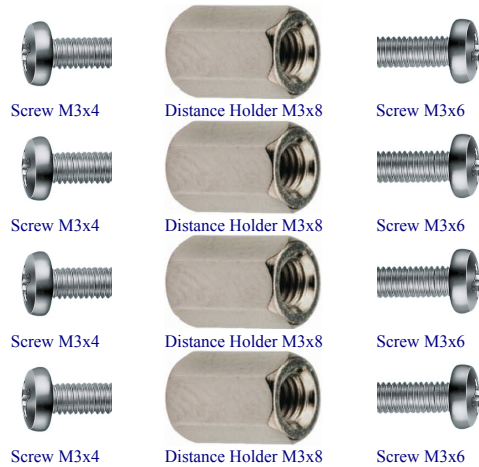
3

4

U_B2B-Connectors
B2B-Connectors.SchDoc
U_B13
B13.SchDoc
U_B14
B14.SchDoc
U_B15
B15.SchDoc
U_B16
B16.SchDoc
U_B34
B34.SchDoc
U_FPGA-MGT
FPGA-MGT.SchDoc
U_FPGA-CFG
FPGA-CFG.SchDoc
U_FPGA-PWR
FPGA-PWR.SchDoc
U_Clock
ClOCK.SchDoc
U_DDR3-RAM
DDR3-RAM.SchDoc
U_ETHERNET
ETHERNET.SchDoc
U_CPLD
CPLD.SchDoc
U_PWR1
PWR1.SchDoc
U_PWR2
PWR2.SchDoc



**Top of Board**



	Title: <b>TE0712</b>		
	A4	Number: <b>TE0712 100_11</b>	Rev. <b>01</b>
	Date: <b>2014-06-23</b>	Copyright: <b>2014 Trenz Electronic GmbH</b>	Page <b>16</b> of <b>16</b>
	Filename: <b>TE0712.SchDoc</b>		