

A

B

C

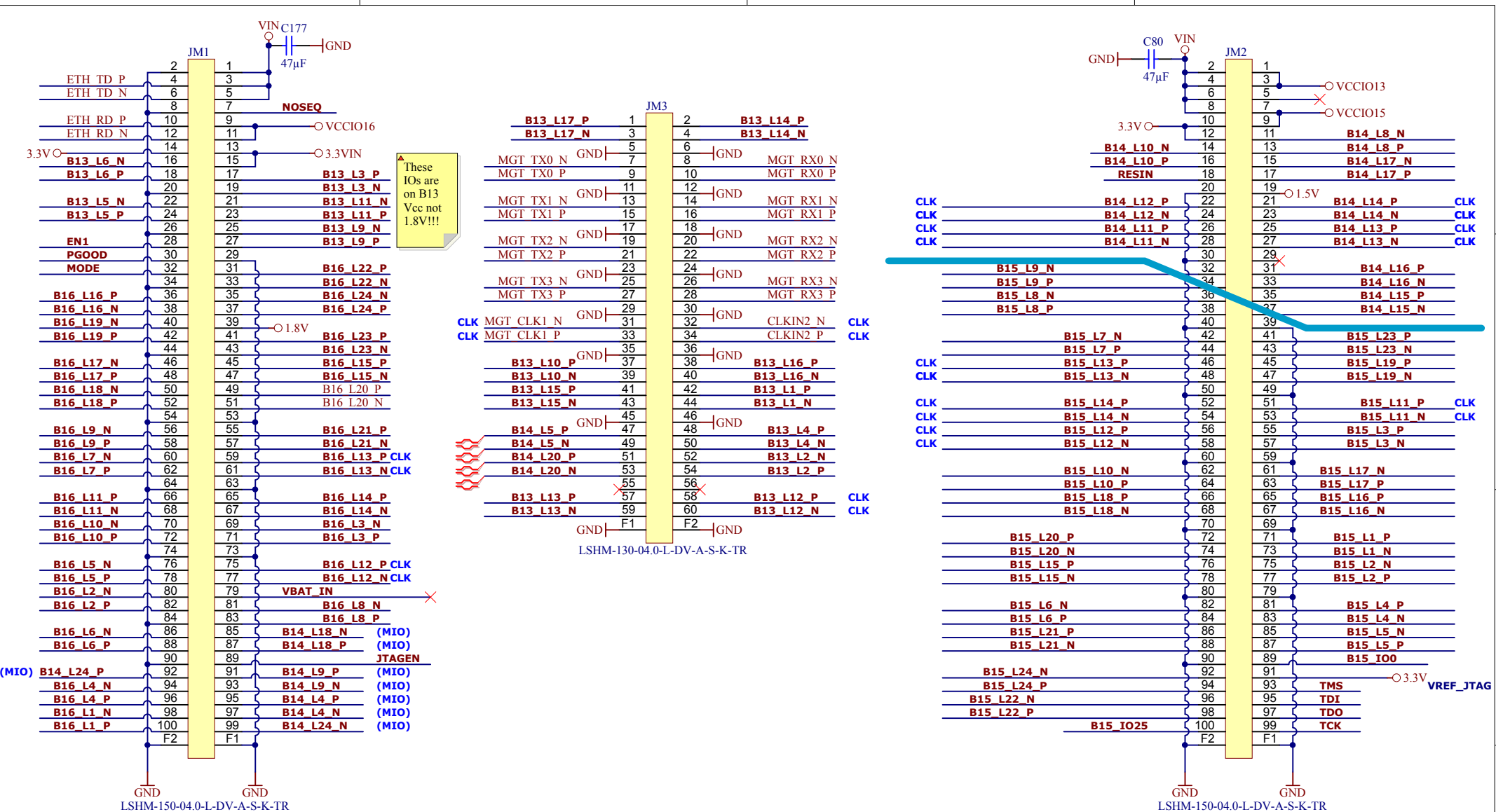
D


A

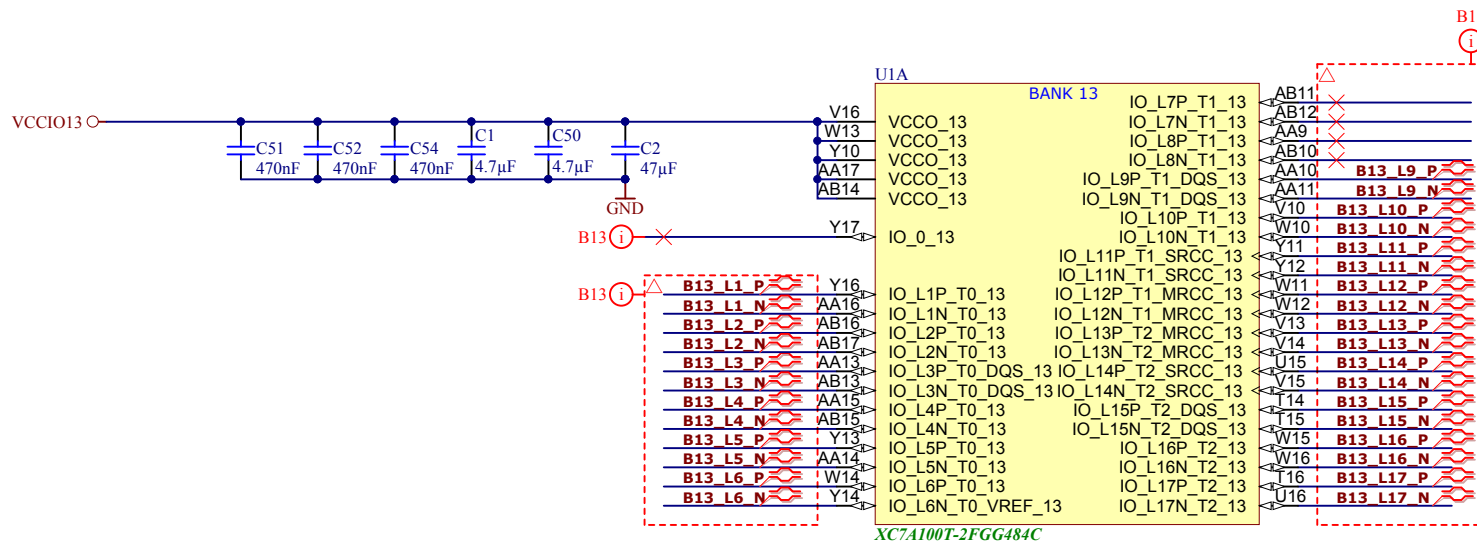
B

C

D

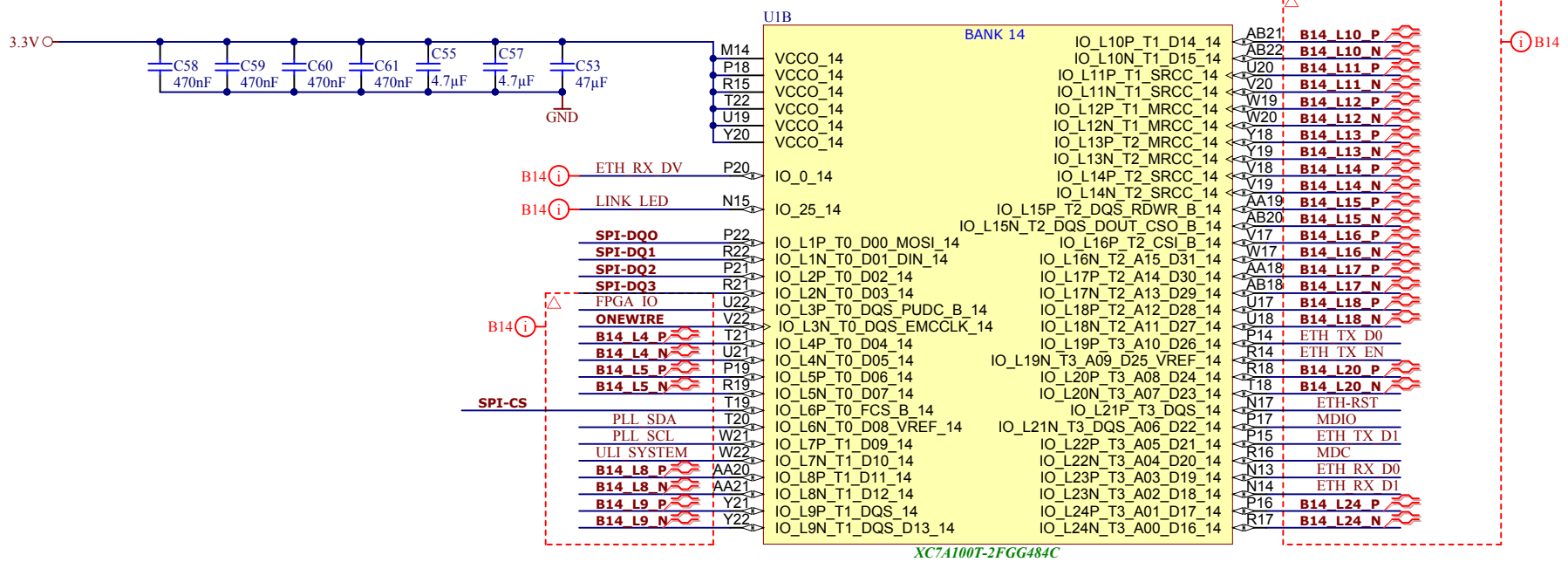


			Title: <b>B2B</b>	
			A4	Number: <b>TE0712 100_2C</b>
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XC7A100T-2FGG484C

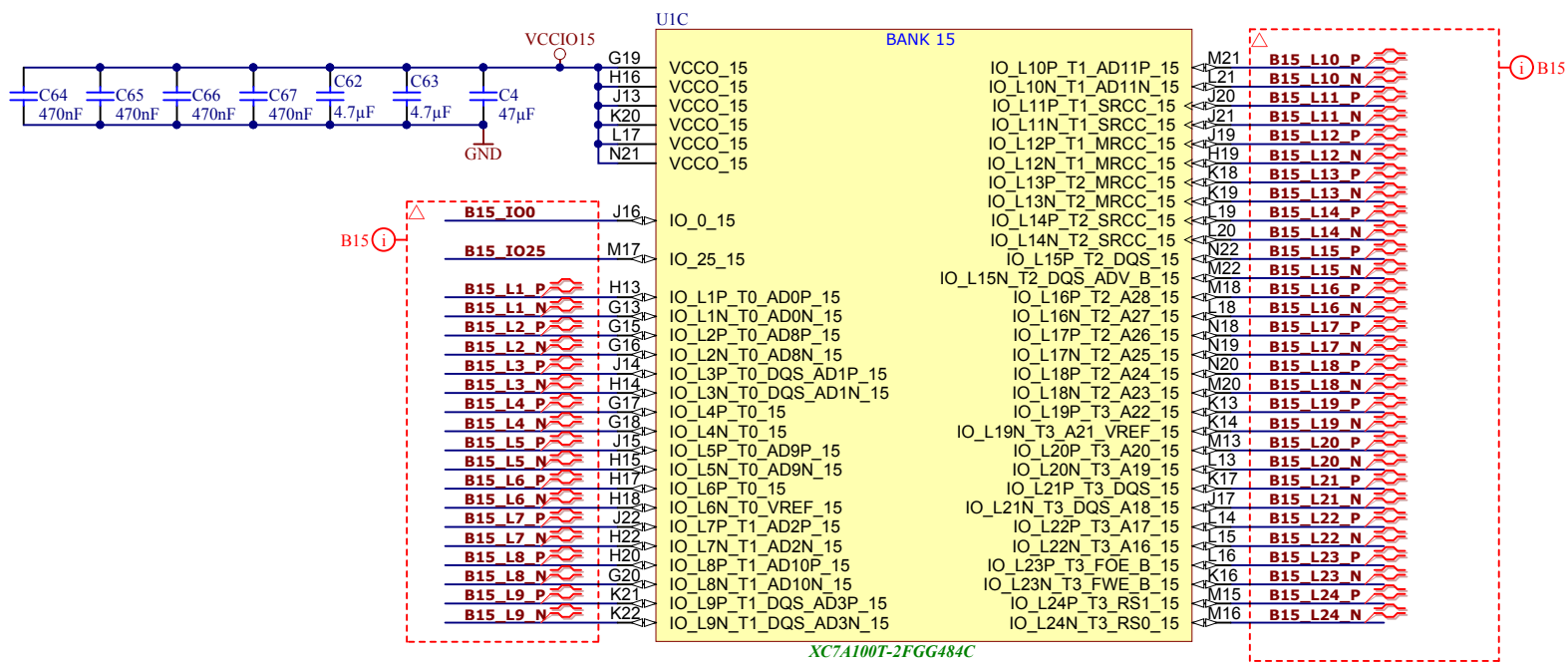
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	A4	Number: <b>TE0712 100_2C</b>
	Date: <b>2014-06-23</b>	Copyright: 2014 Trenz Electronic GmbH
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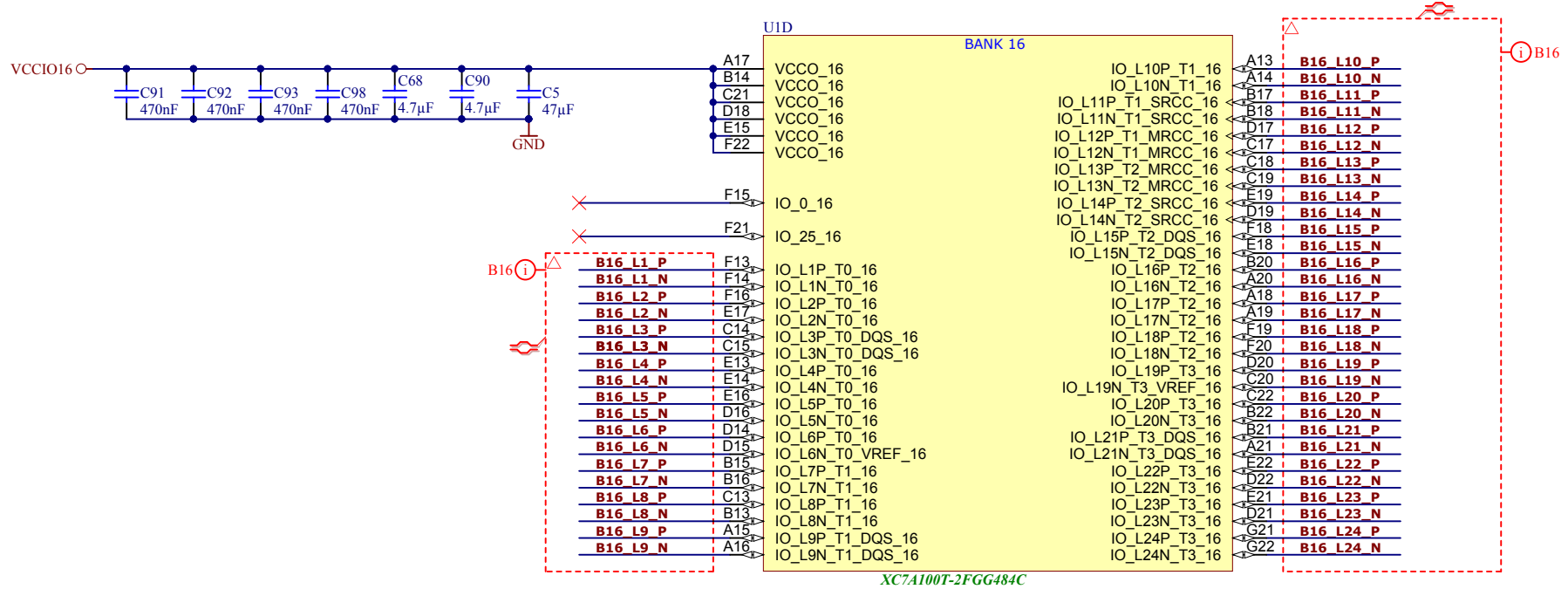
XC7A100T-2FGG484C



Title: <b>B14</b>		
A4	Number: <b>TE0712 100_2C</b>	Rev. <b>01</b>
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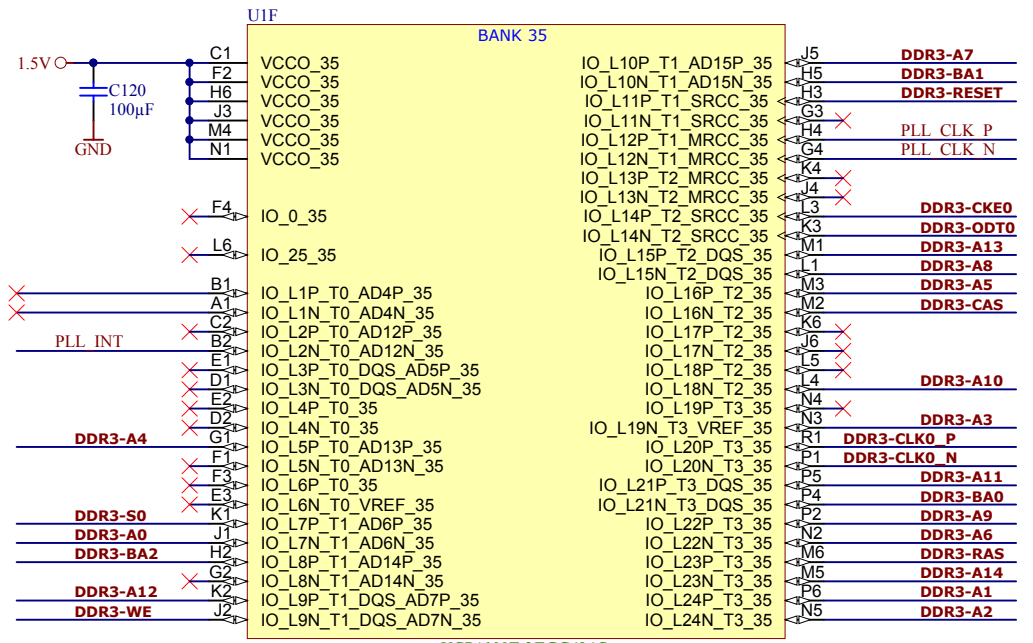
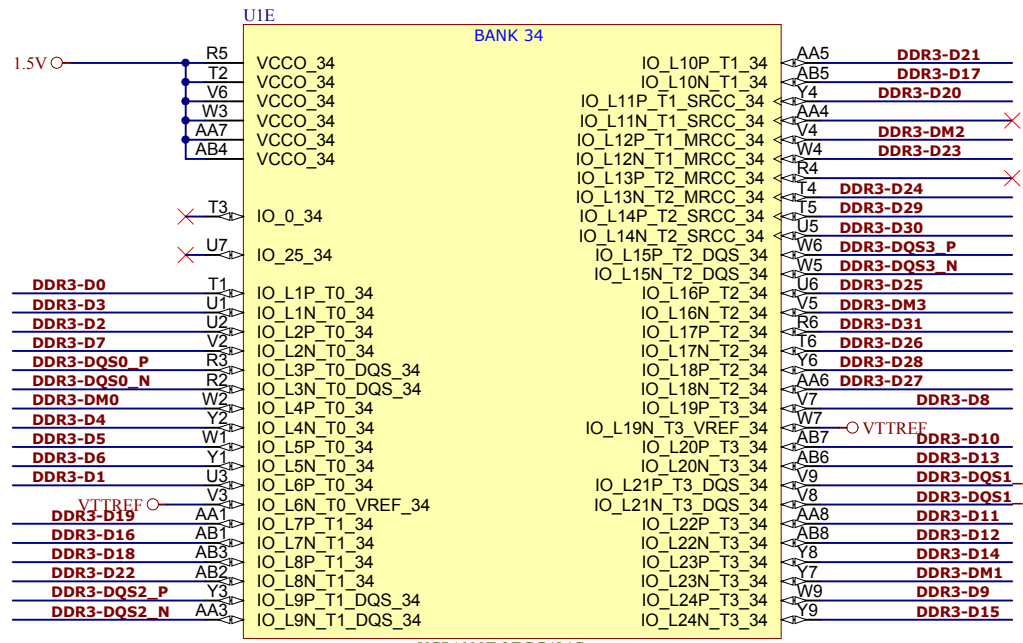
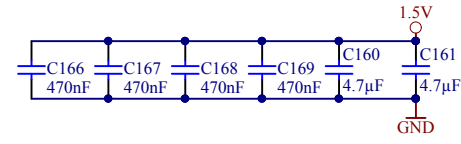
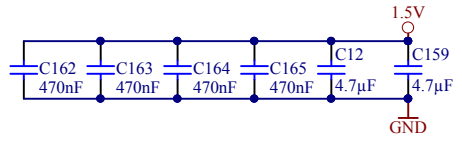
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A4	Number: <b>TE0712 100_2C</b>	Rev. <b>01</b>
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Filename: <b>B15.SchDoc</b>		



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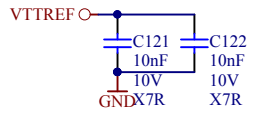
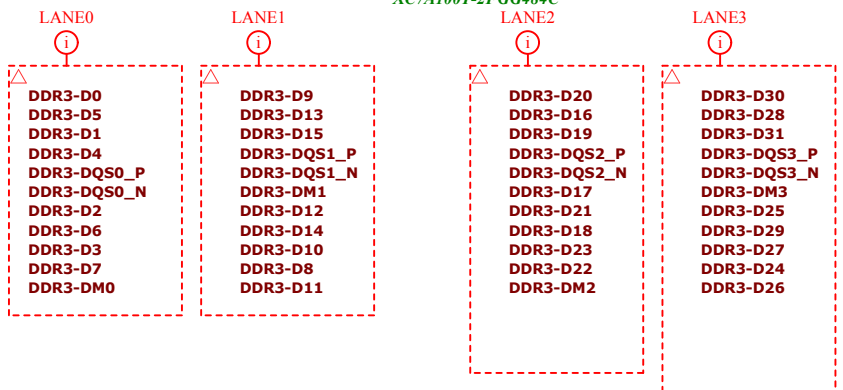


Title: <b>B16</b>		
A4	Number: <b>TE0712 100_2C</b>	Rev. <b>01</b>
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Filename: <b>B16.SchDoc</b>		

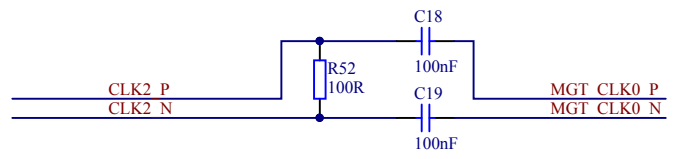
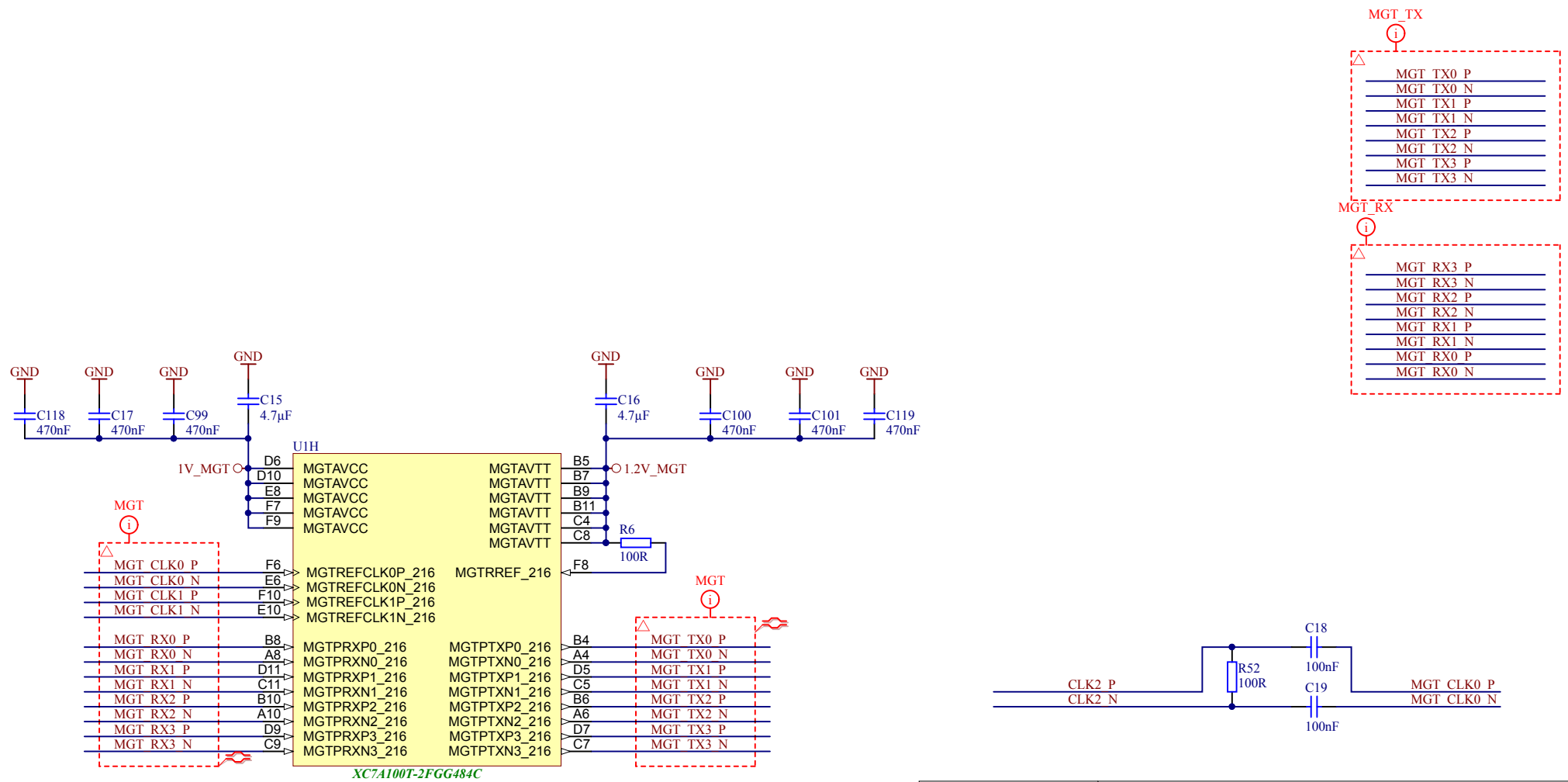



XC7A100T-2FGG484C

XC7A100T-2FGG484C



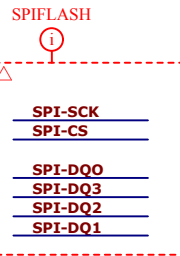
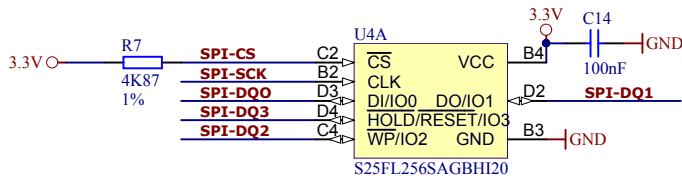
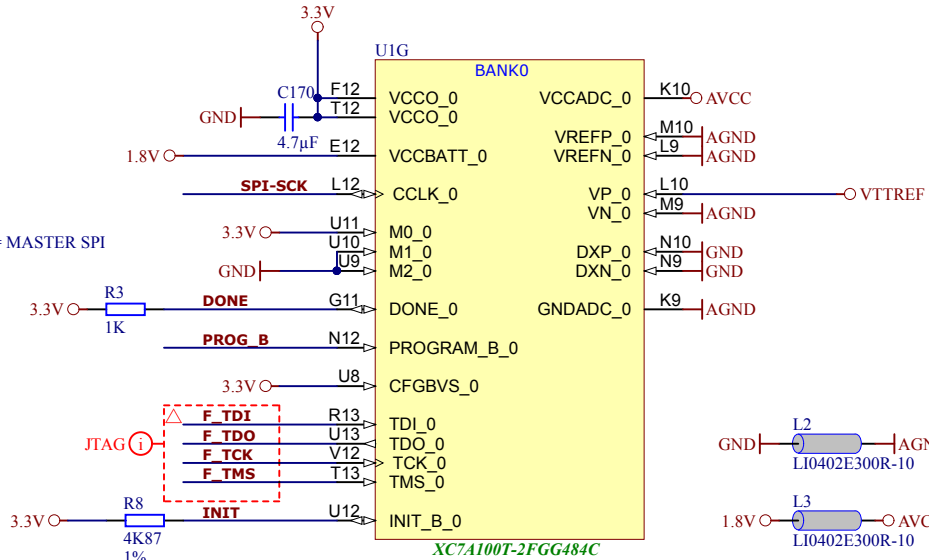
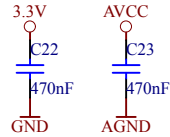
Title: B34		
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		Title: MGT	
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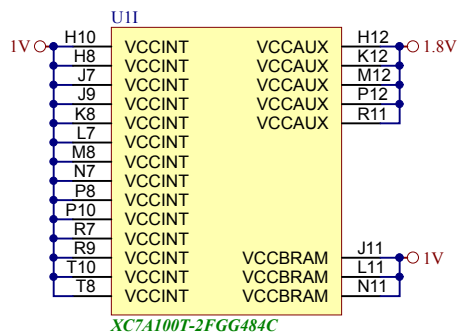
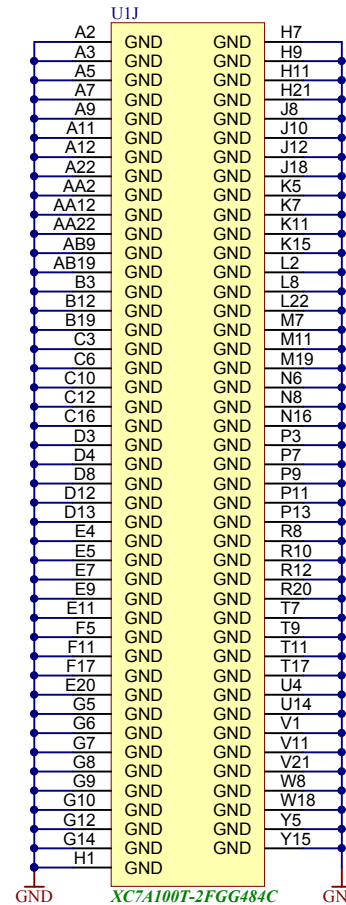
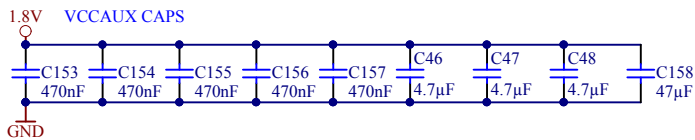
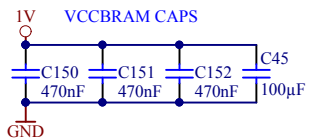
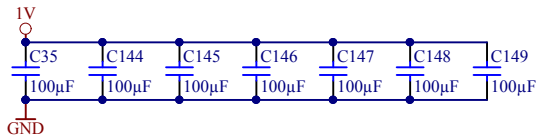
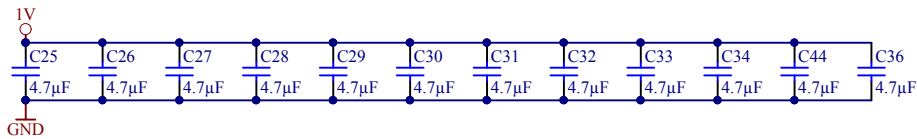
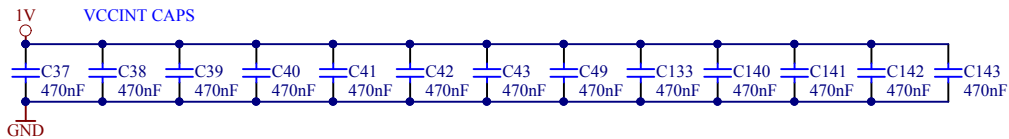
BOOTMODE = MASTER SPI



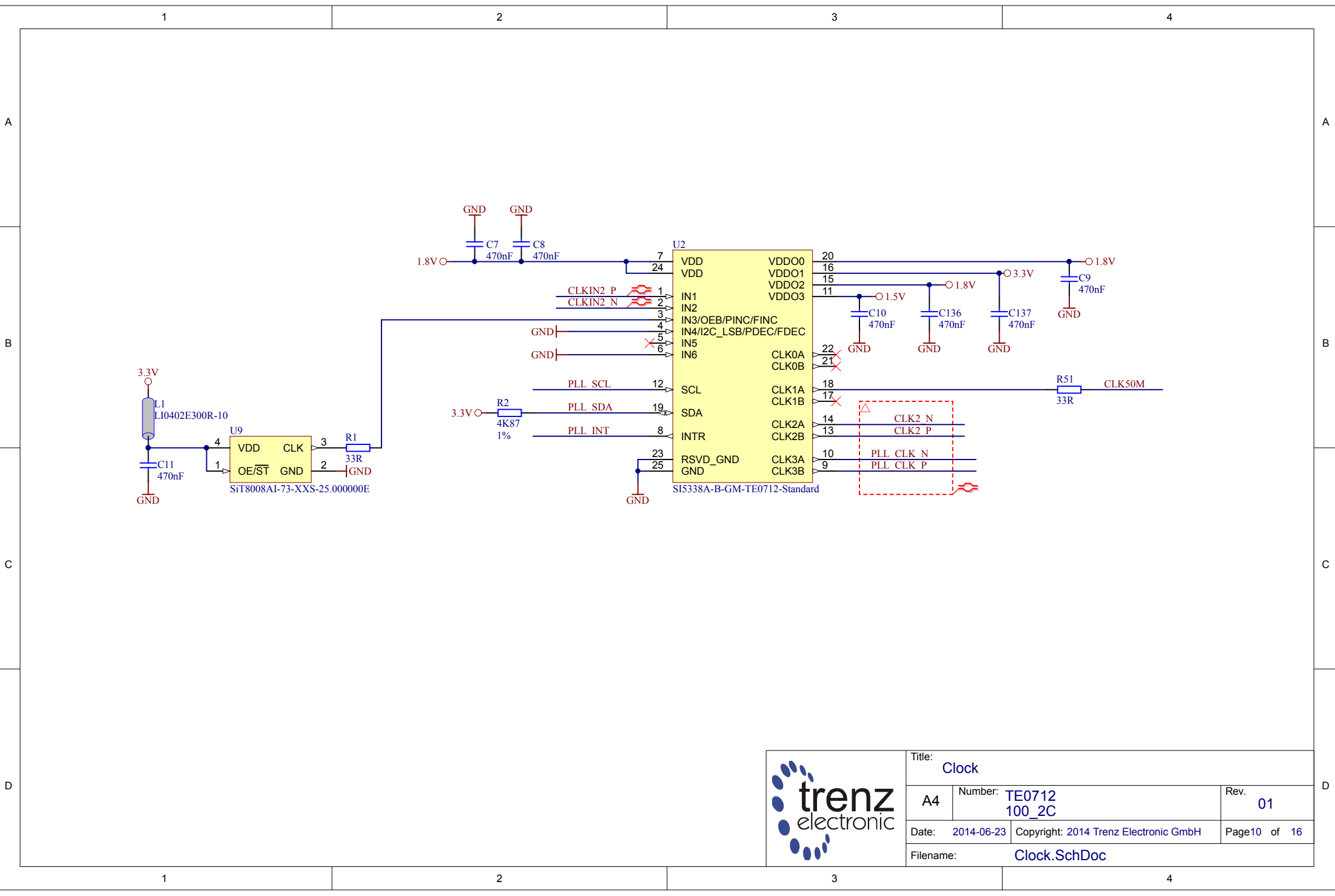
Title: CFG


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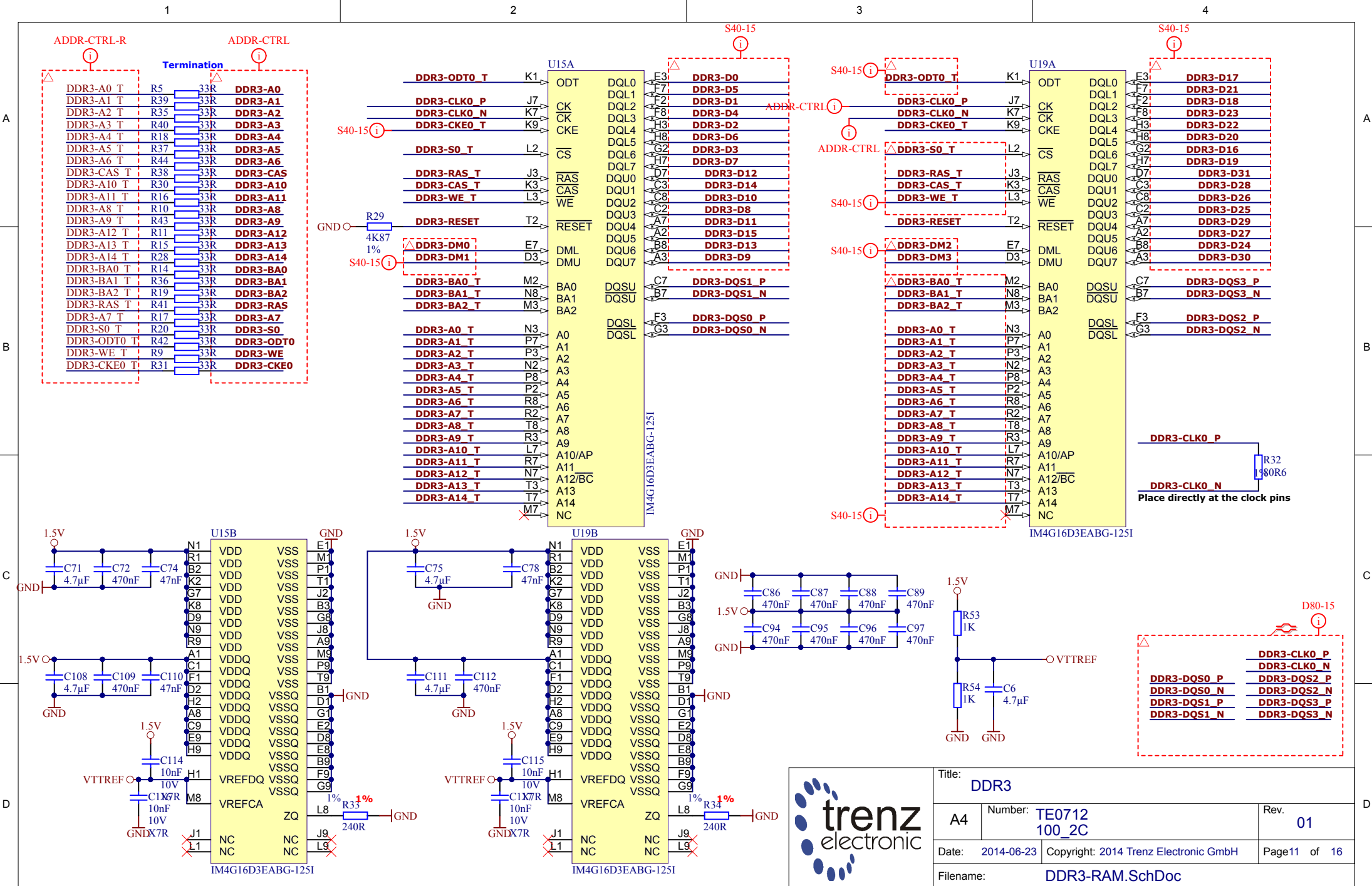


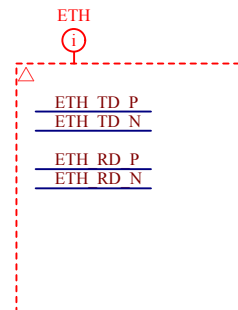
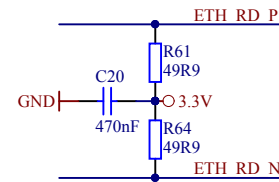
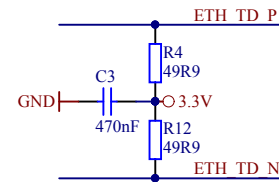
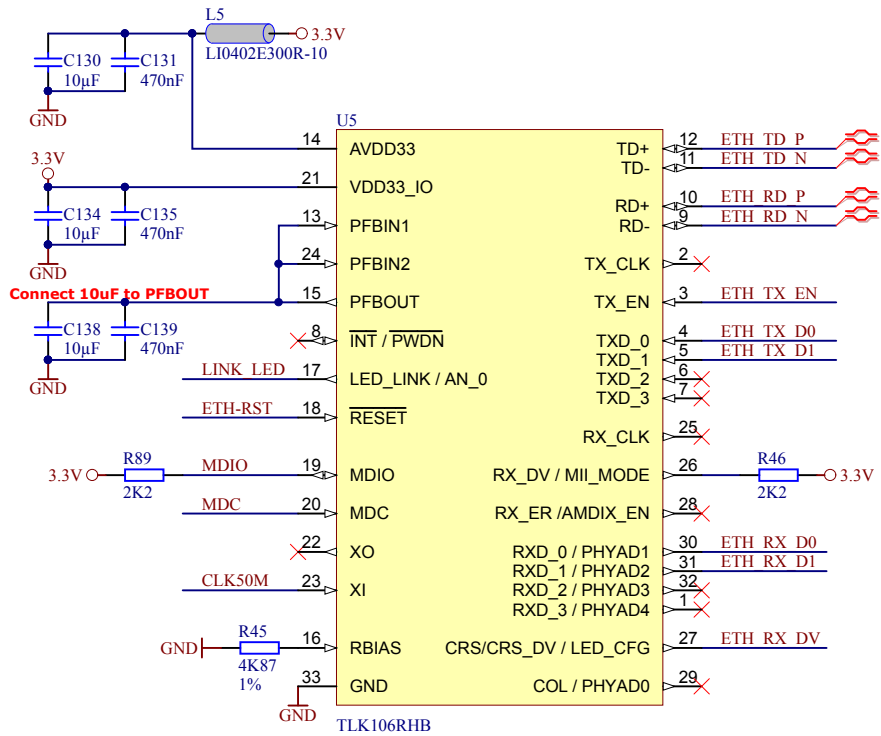



Title: PWR		
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			Title: <b>Clock</b>	
			A4	Number: <b>TE0712 100_2C</b>
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Filename: <b>Clock.SchDoc</b>				





		Title: ETH	
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1

2

3

4

A

A

B

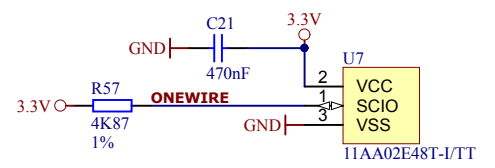
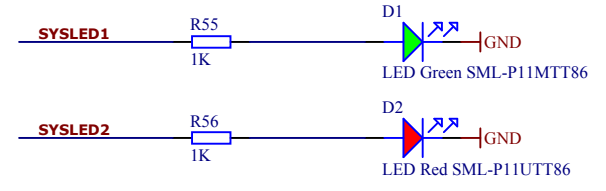
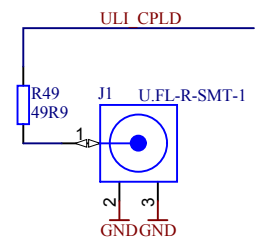
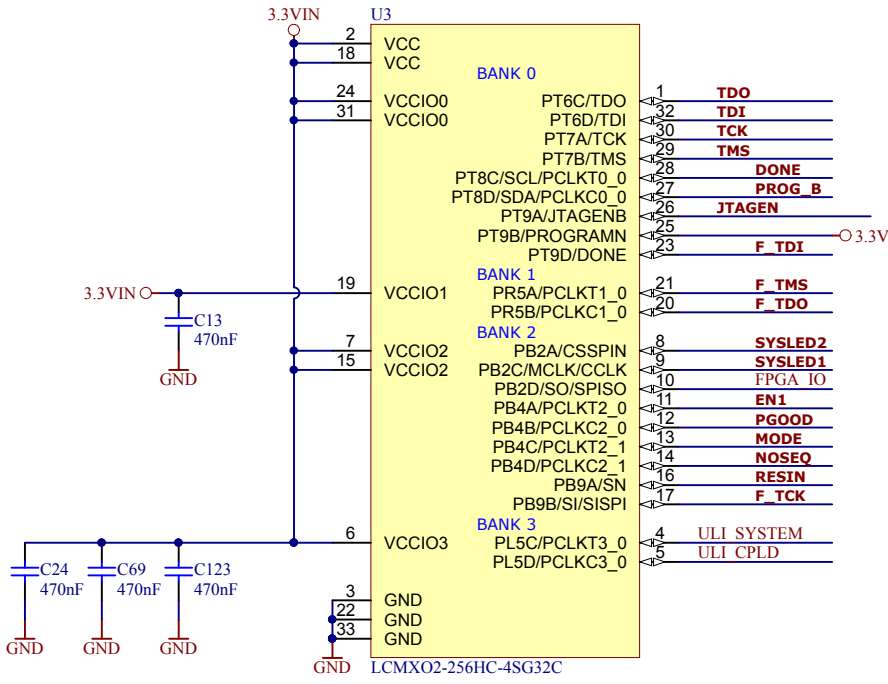
B

C

C

D

D



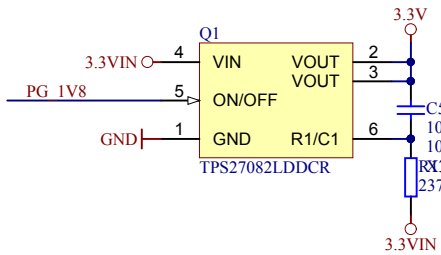
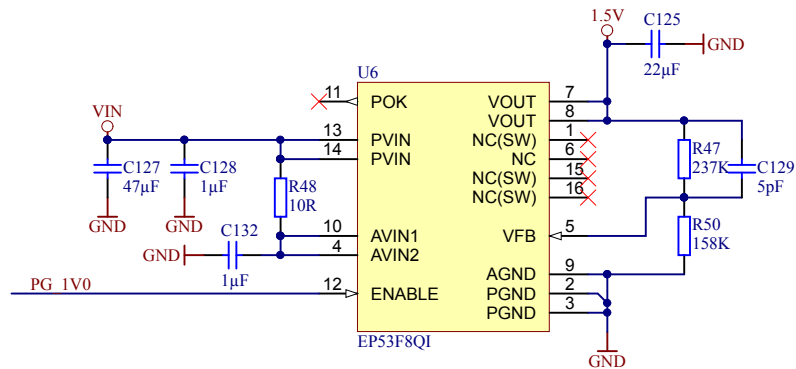
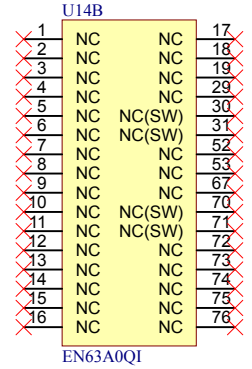
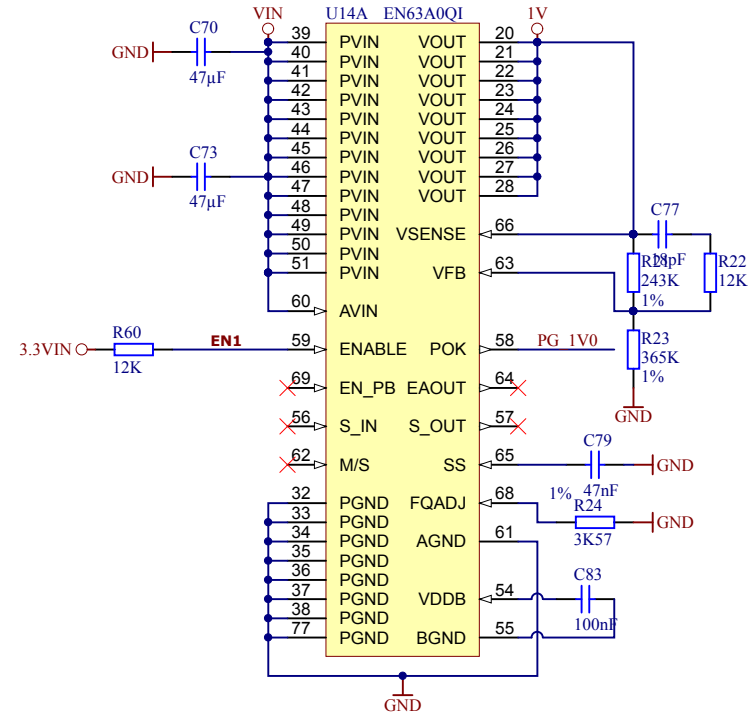
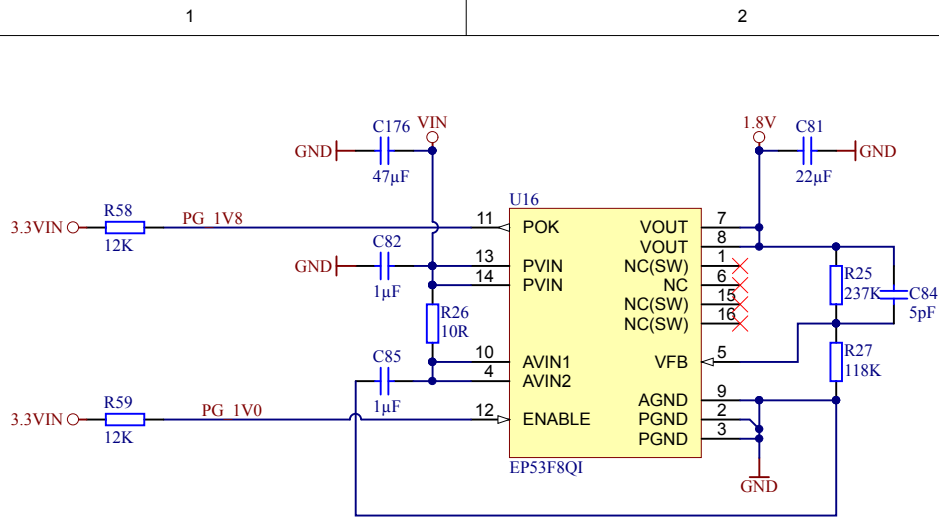
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A4	Number: <b>TE0712 100_2C</b>	Rev. <b>01</b>
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Filename: <b>CPLD.SchDoc</b>		

1

2

3

4



Title: PWR		
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1

2

3

4

A

A

B

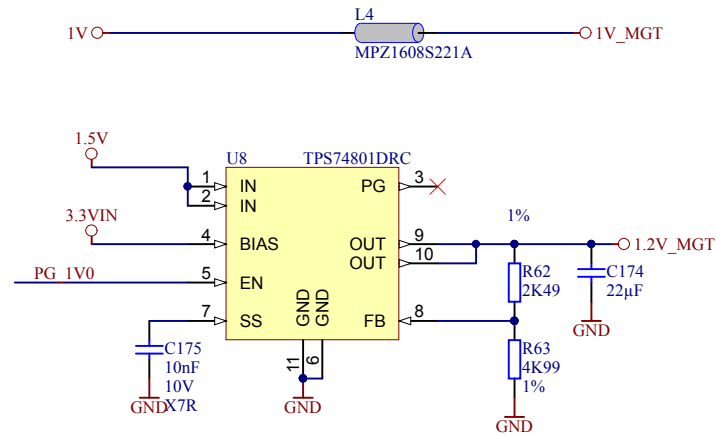
B


C

C

D

D



		Title: PWR	
		A4	Number: TE0712 100_2C
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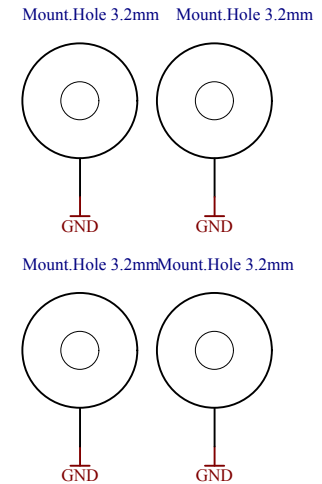
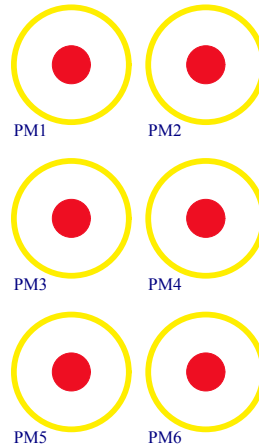
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2

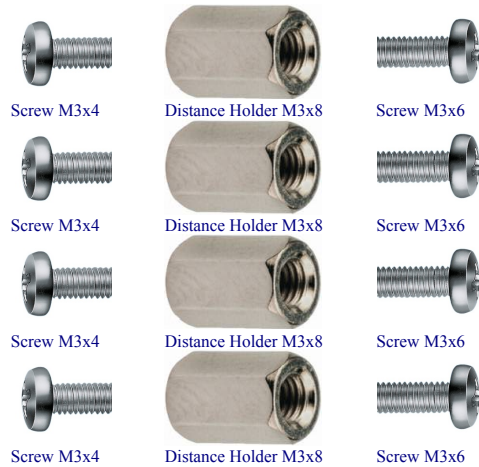
3


4

U_B2B-Connectors
B2B-Connectors.SchDoc
U_B13
B13.SchDoc
U_B14
B14.SchDoc
U_B15
B15.SchDoc
U_B16
B16.SchDoc
U_B34
B34.SchDoc
U_FPGA-MGT
FPGA-MGT.SchDoc
U_FPGA-CFG
FPGA-CFG.SchDoc
U_FPGA-PWR
FPGA-PWR.SchDoc
U_Clock
ClOCK.SchDoc
U_DDR3-RAM
DDR3-RAM.SchDoc
U_ETHERNET
ETHERNET.SchDoc
U_CPLD
CPLD.SchDoc
U_PWR1
PWR1.SchDoc
U_PWR2
PWR2.SchDoc



**Top of Board**



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