

A

A

B

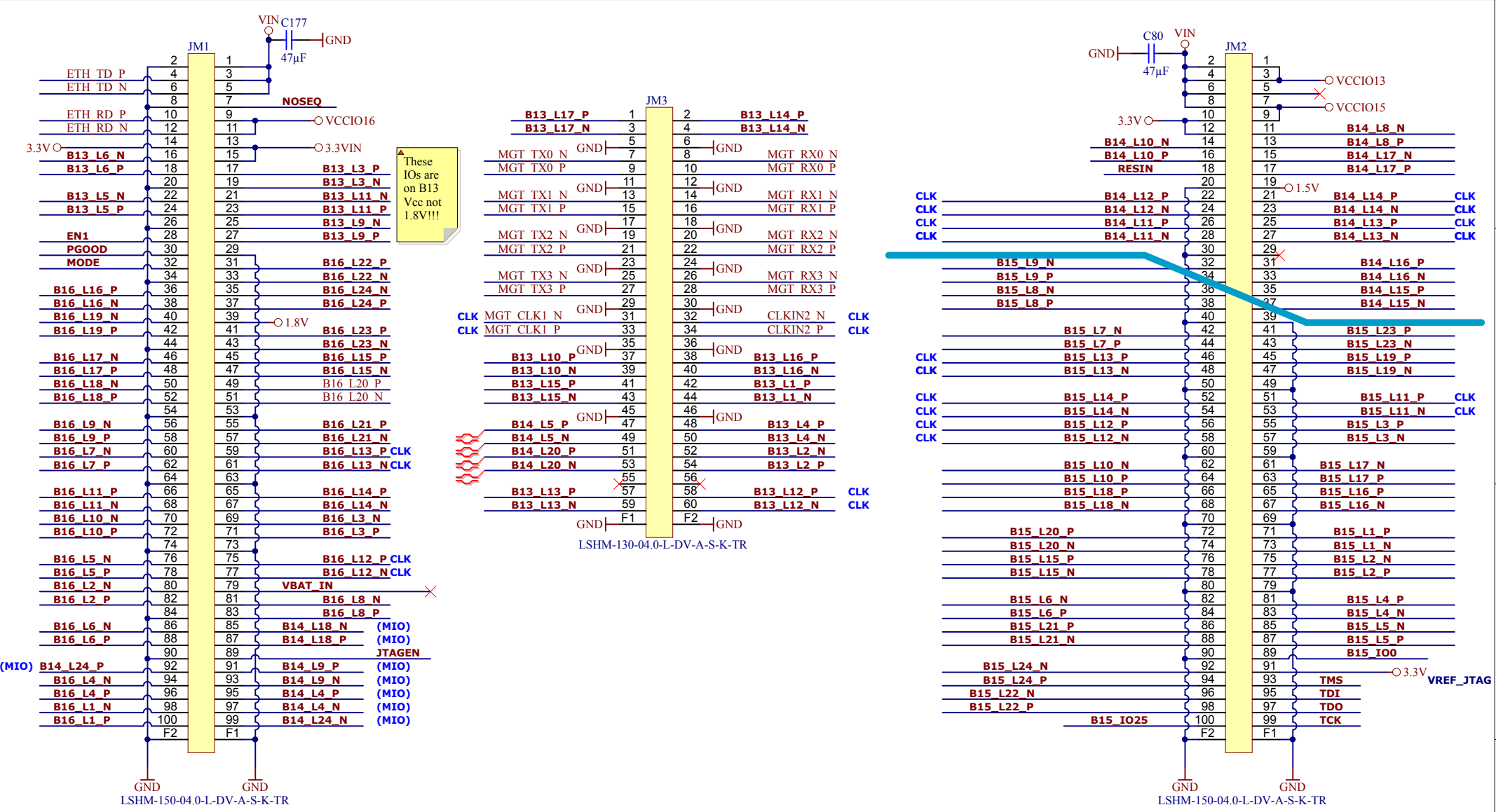
B

C

C

D

D

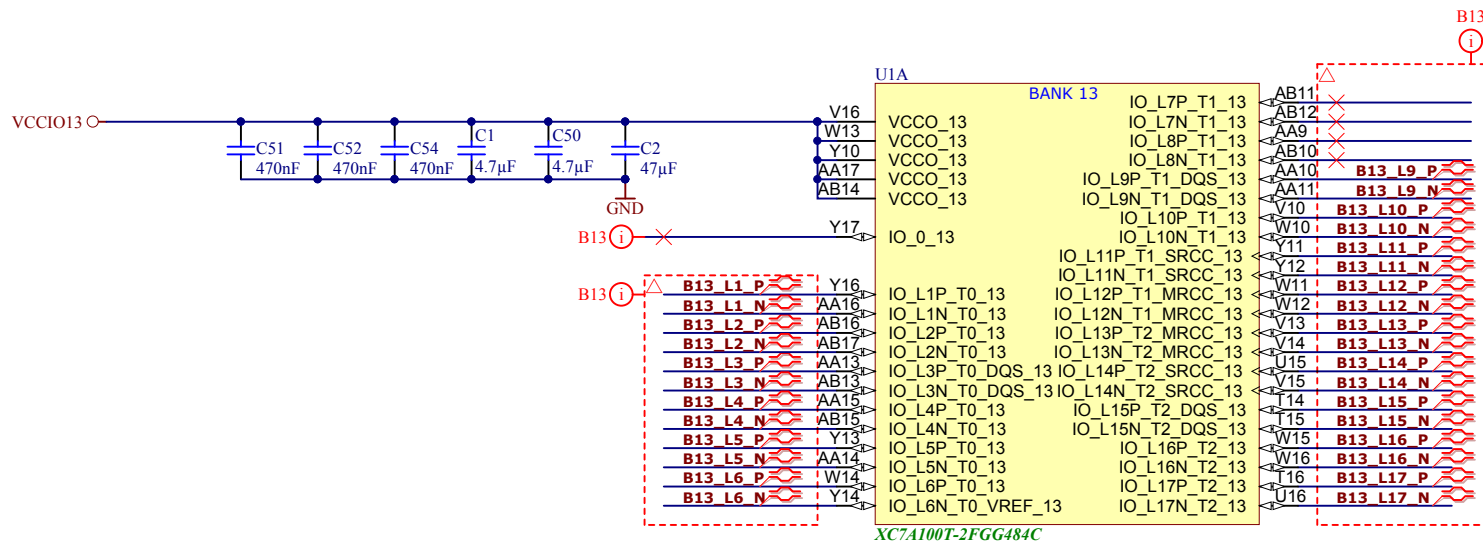


These IOs are on B13 Vcc not 1.8V!!!


CLK MGT CLK1 N CLK MGT CLK1 P

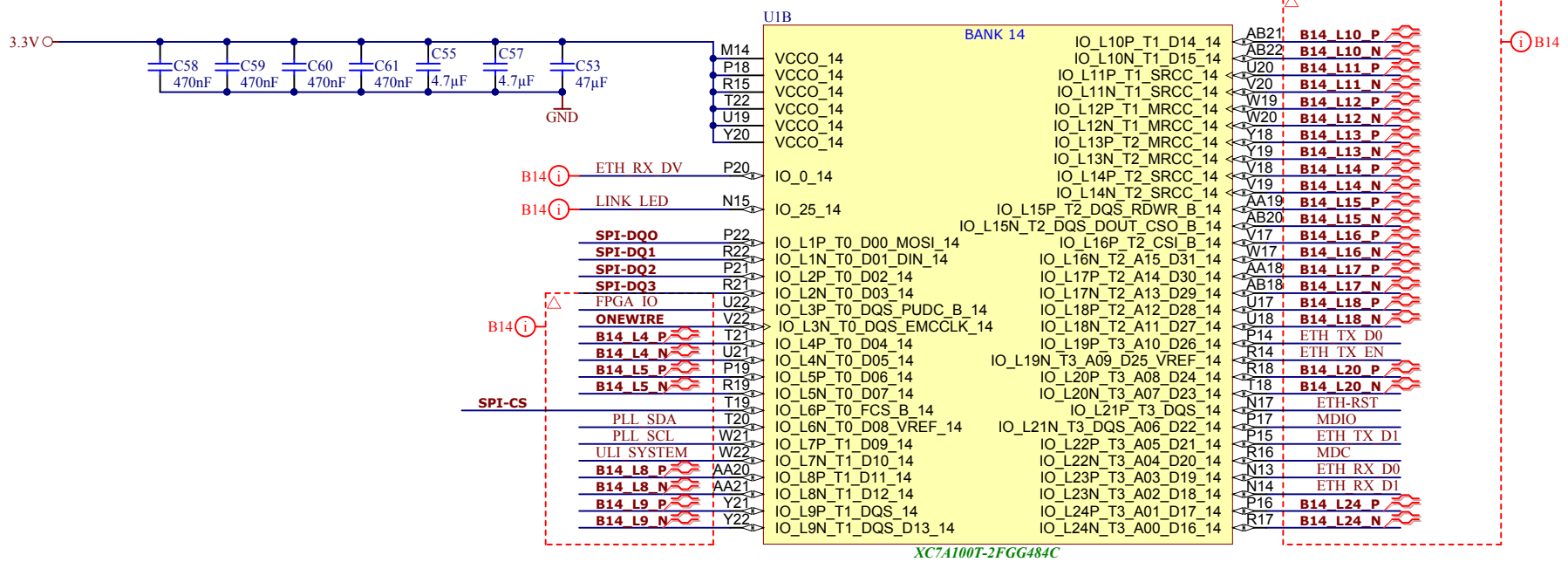


| | | |
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| Title: B2B | | |
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| Filename: B2B-Connectors.SchDoc | | |

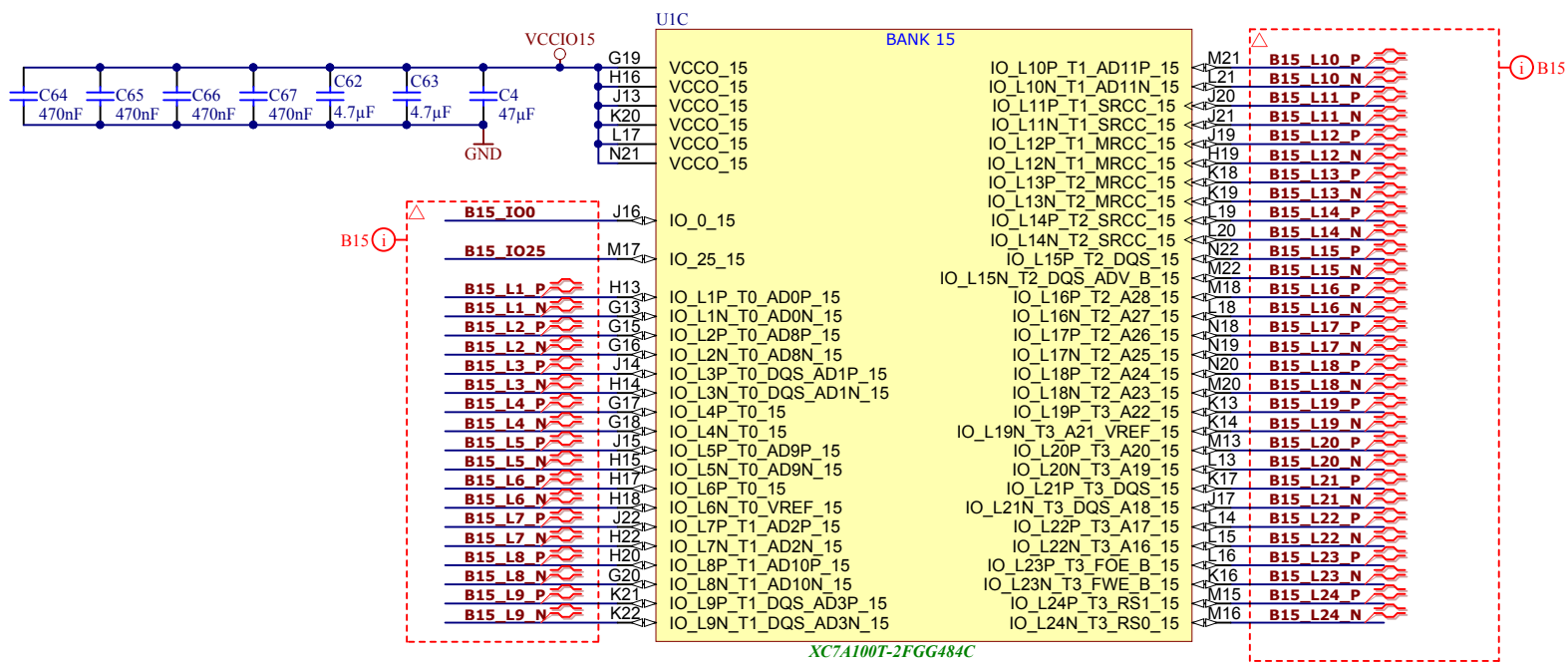


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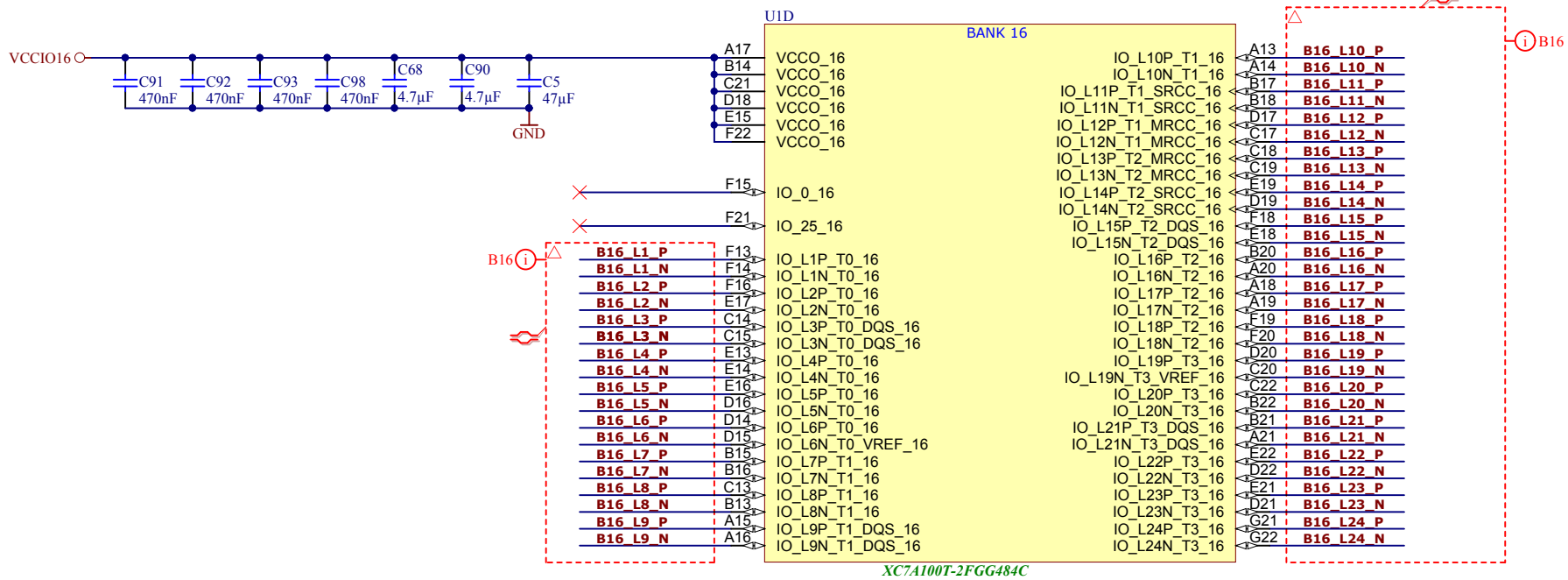
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|  | Title: B13 | |
| | A4 | Number: TE0712 100_2C2 |
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| Filename: B13.SchDoc | | |



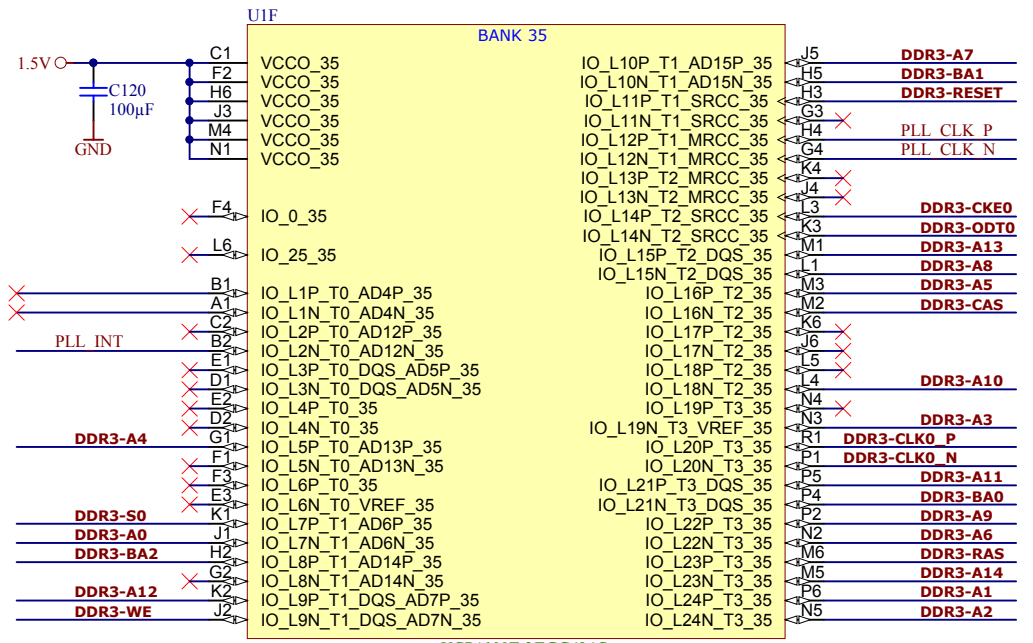
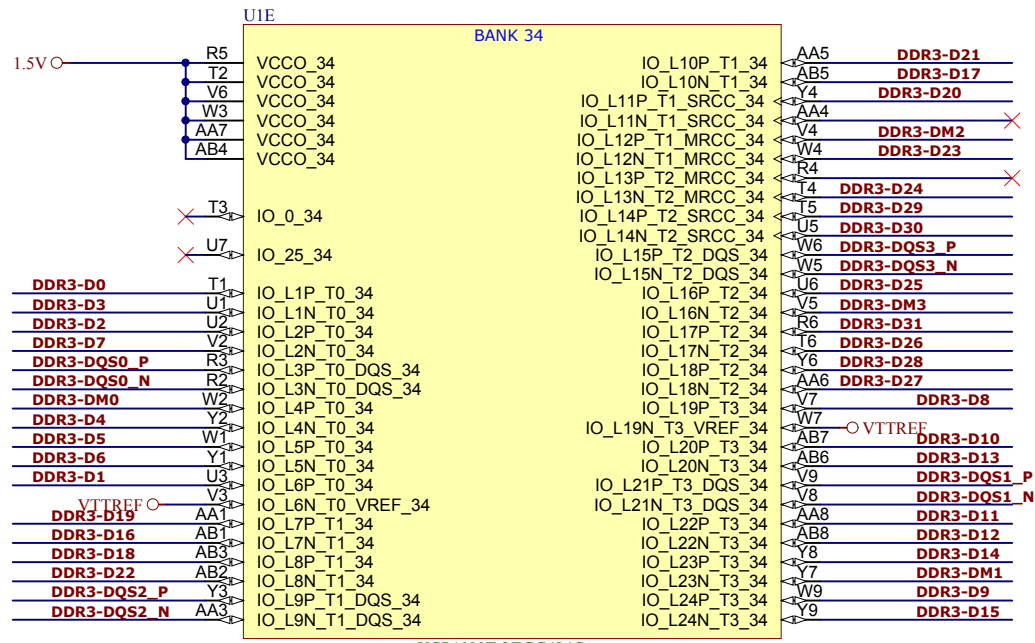
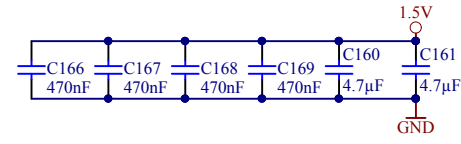
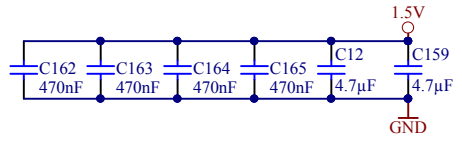
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| Title: B14 | | |
| A4 | Number: TE0712 100_2C2 | Rev. 01 |
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| Title: B15 | | |
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| Filename: B15.SchDoc | | |

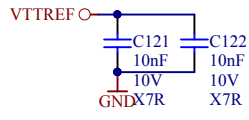
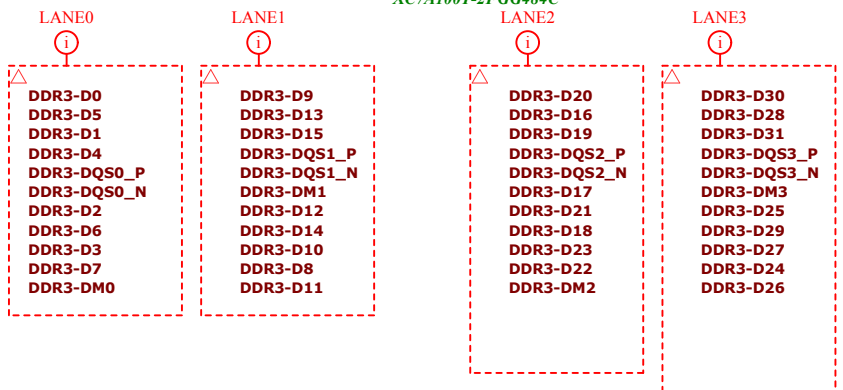


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| Title: B16 | | |
| A4 | Number: TE0712 100_2C2 | Rev. 01 |
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| Filename: B16.SchDoc | | |

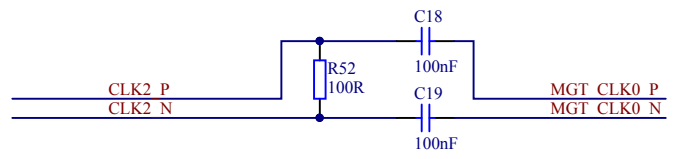
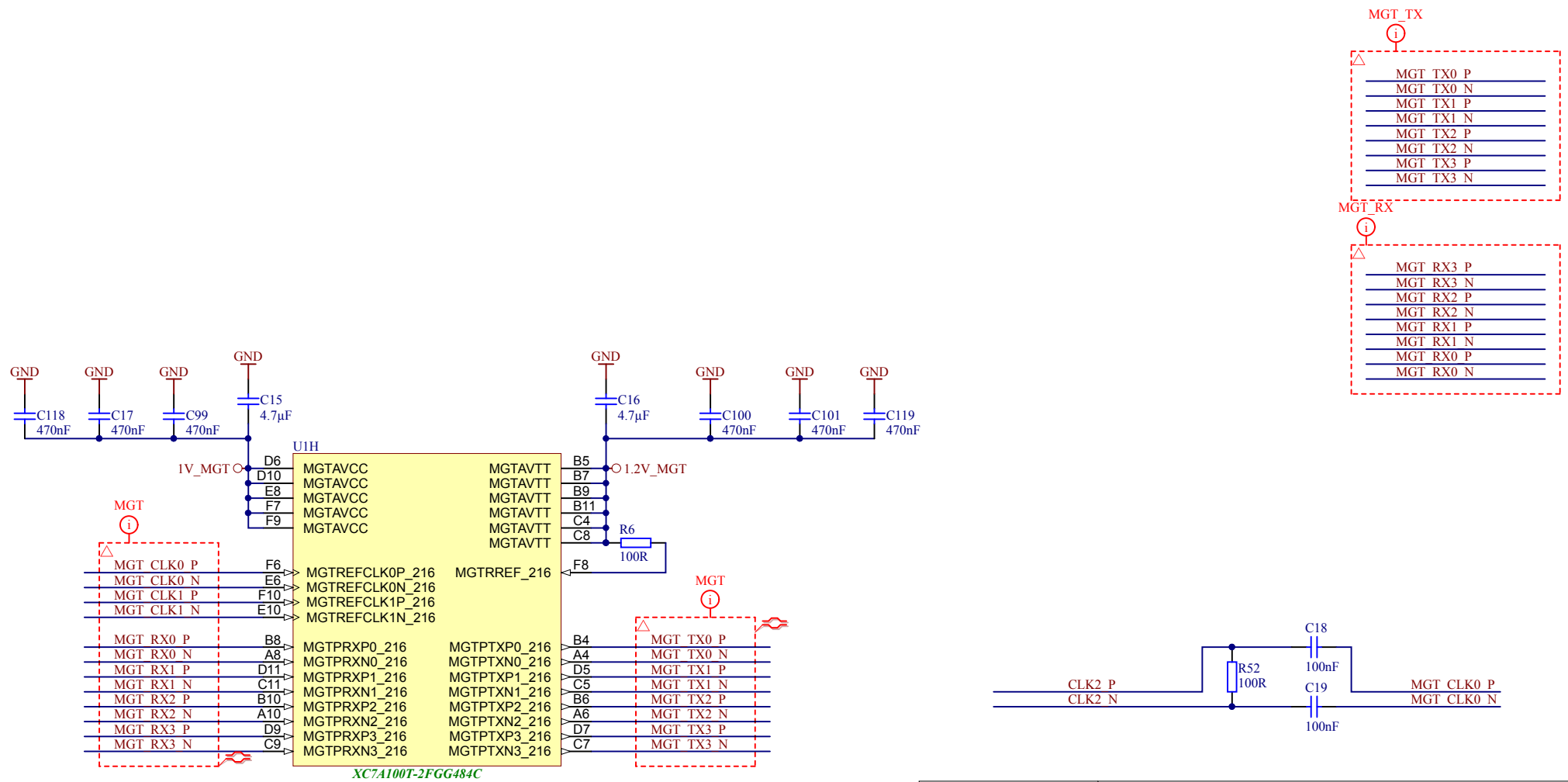



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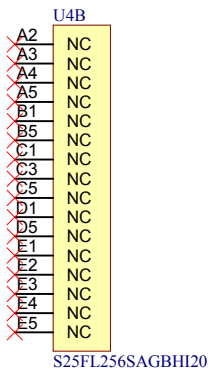
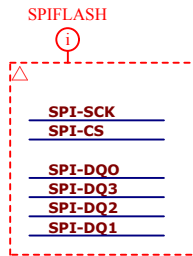
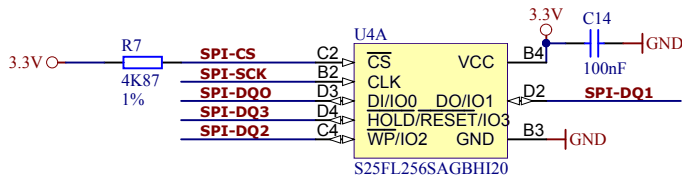
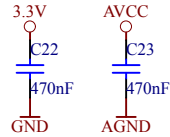
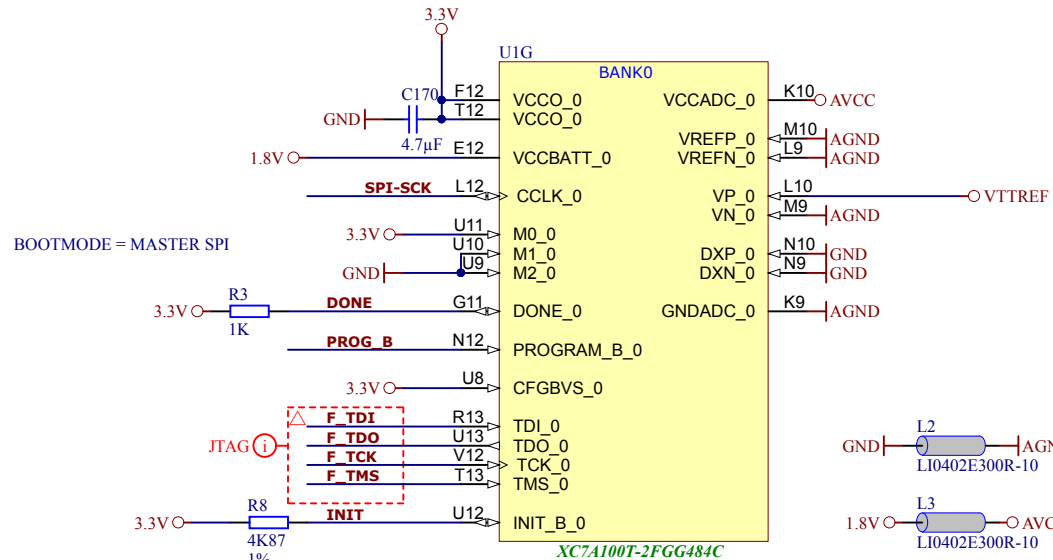
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| Title: B34 | | |
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|---|--|---------------------------------------|---------------------------|
|  | | Title: MGT | |
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|---------------------------|--|---------------------------------------|---------------------------|
| | | Title: CFG | |
| | | A4 | Number: TE0712 100_2C2 |
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| Filename: FPGA-CFG.SchDoc | | | |

1

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A

A

B

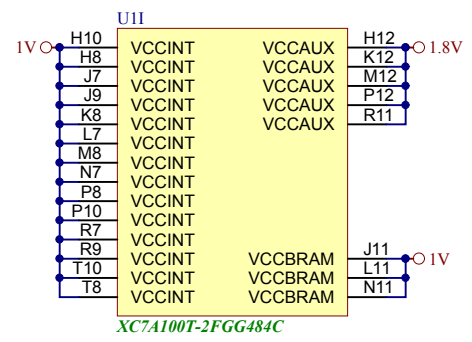
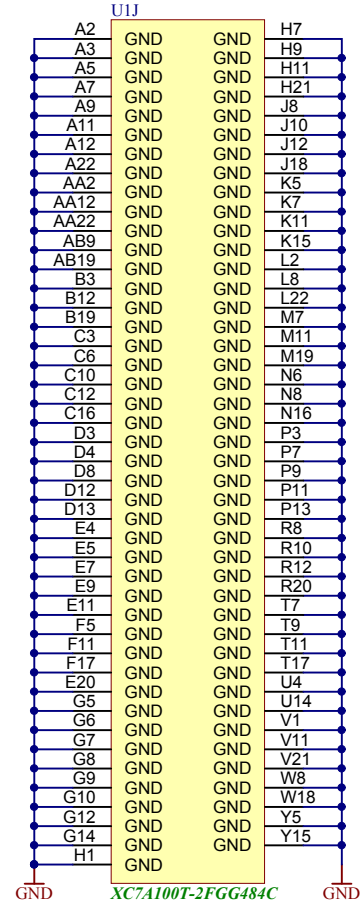
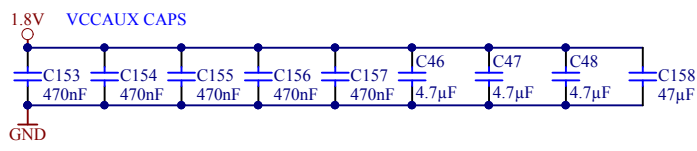
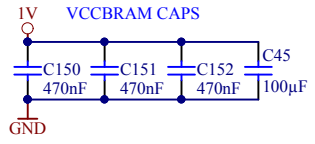
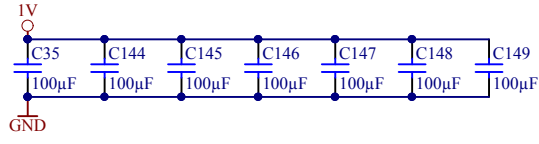
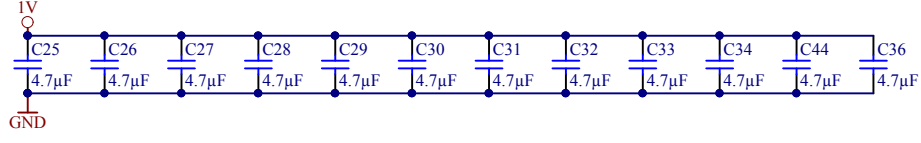
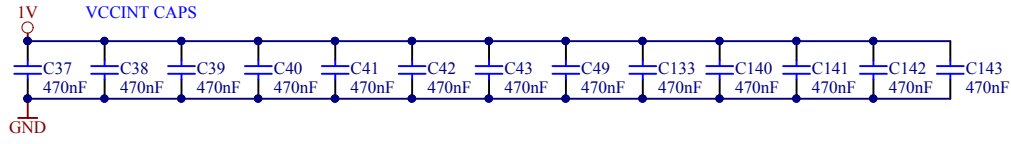
B

C

C

D

D



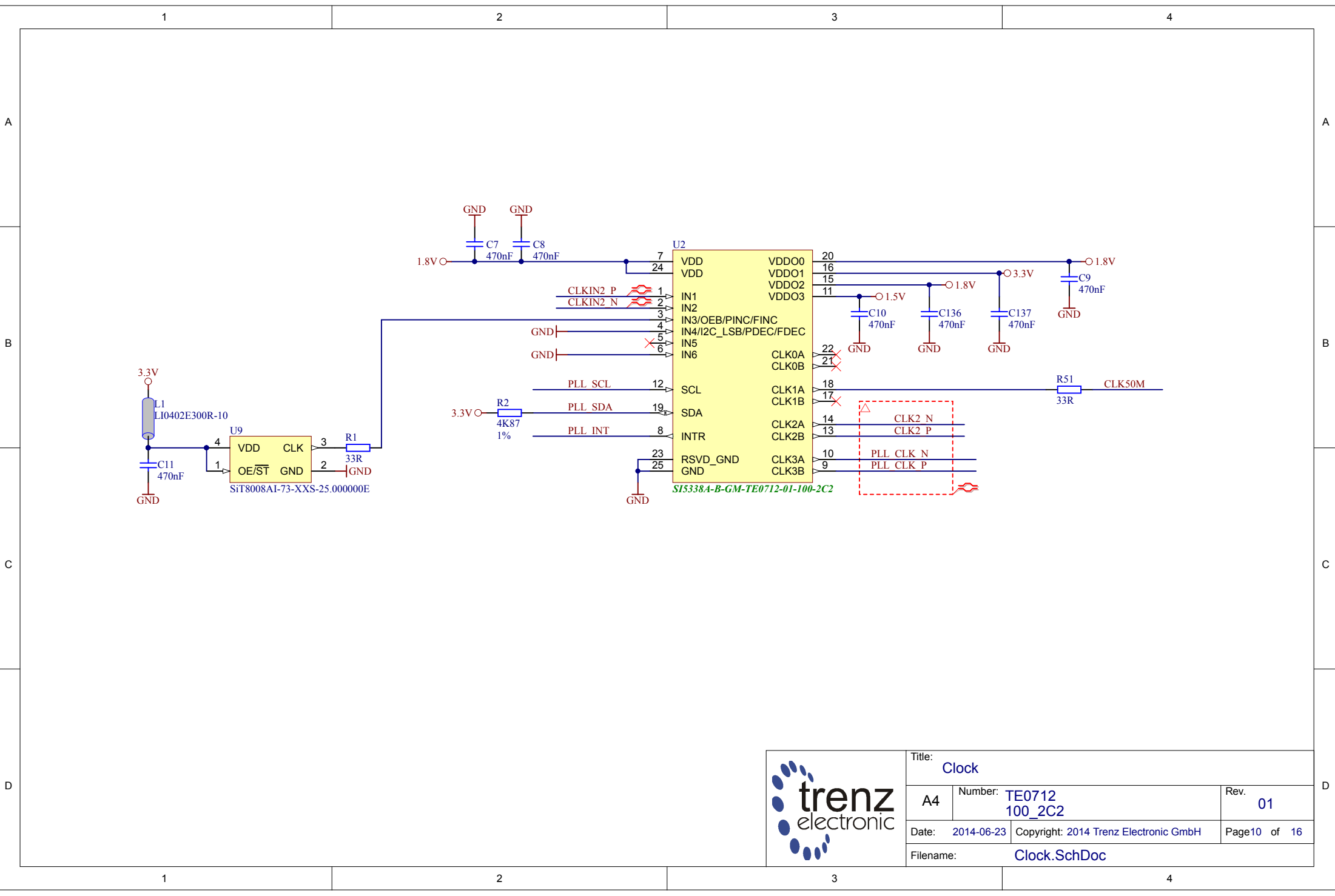
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| Title: PWR | | |
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1

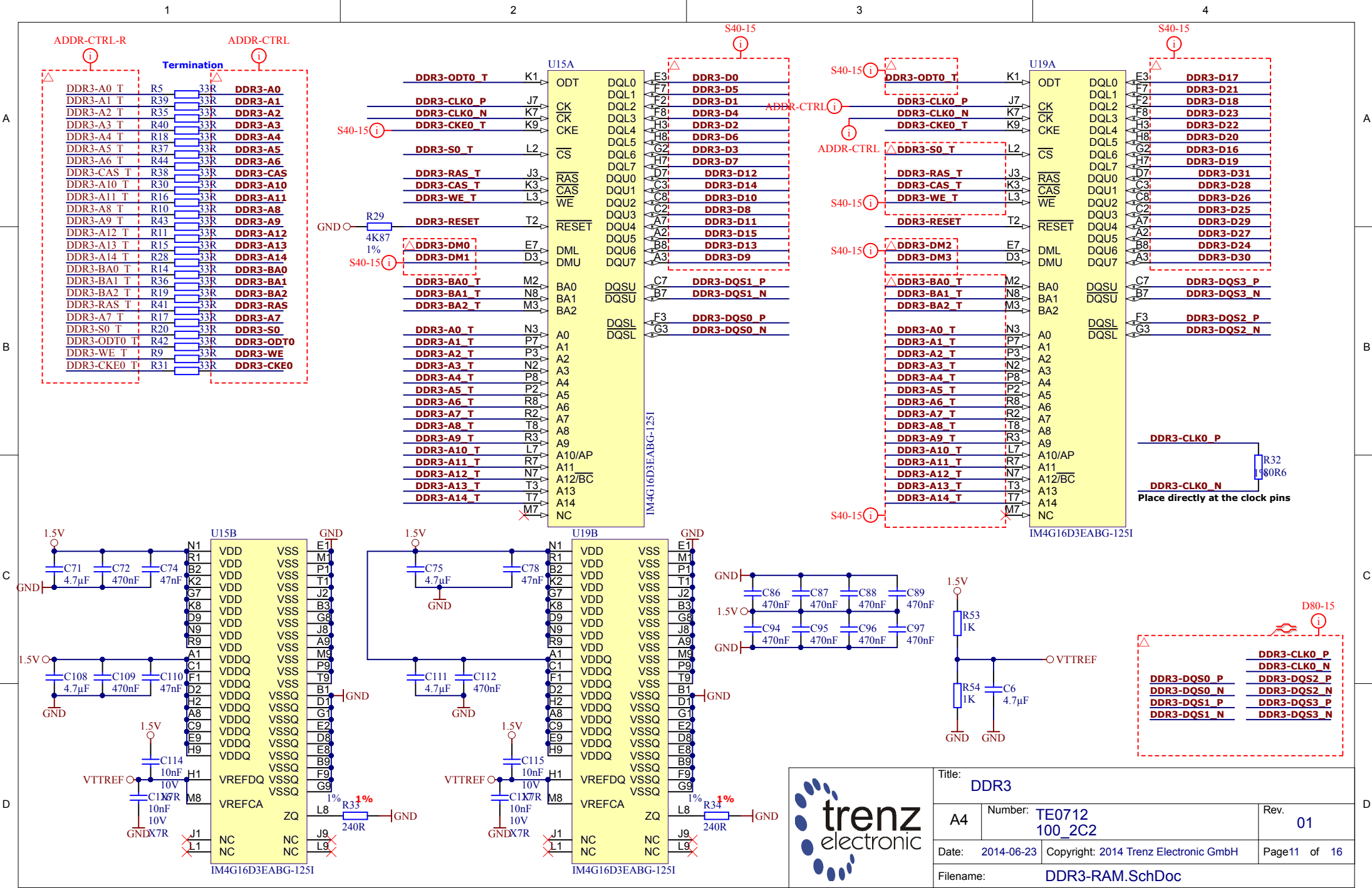
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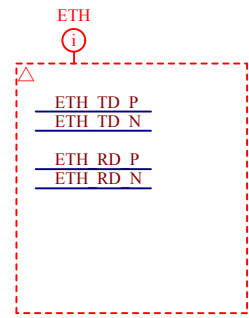
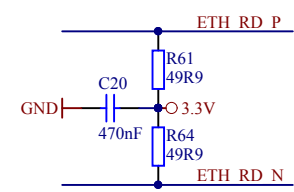
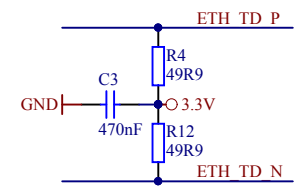
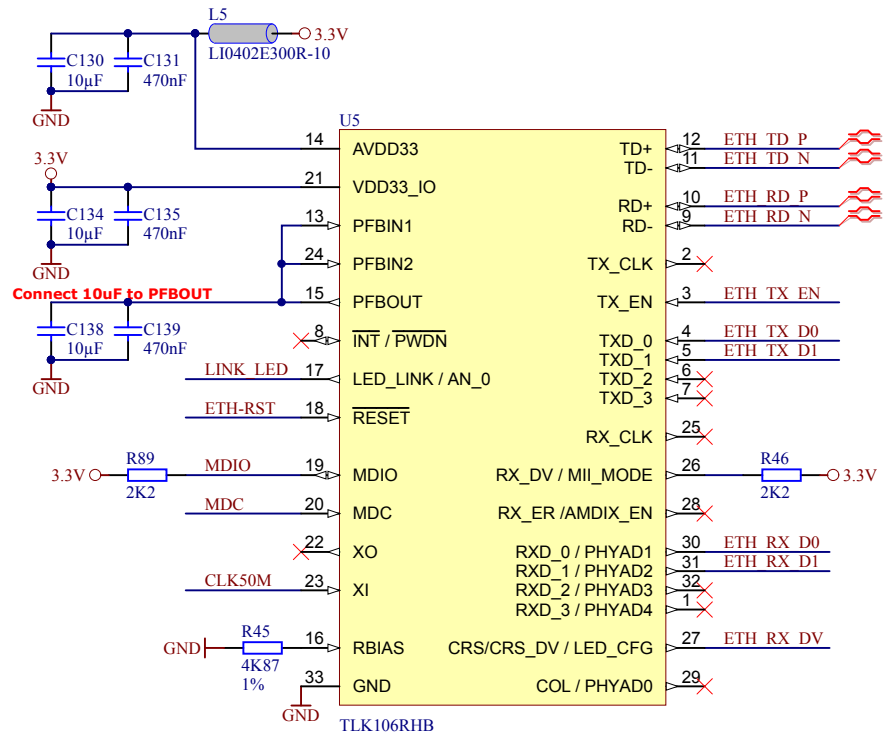
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4

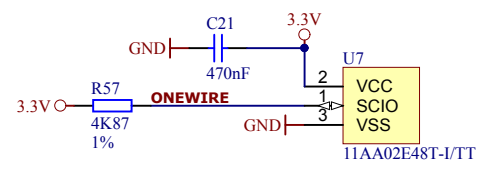
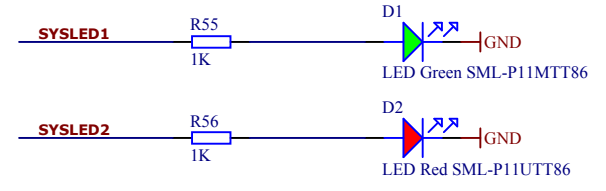
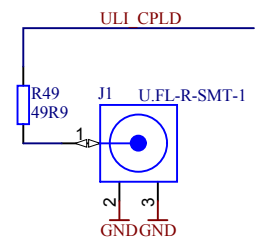
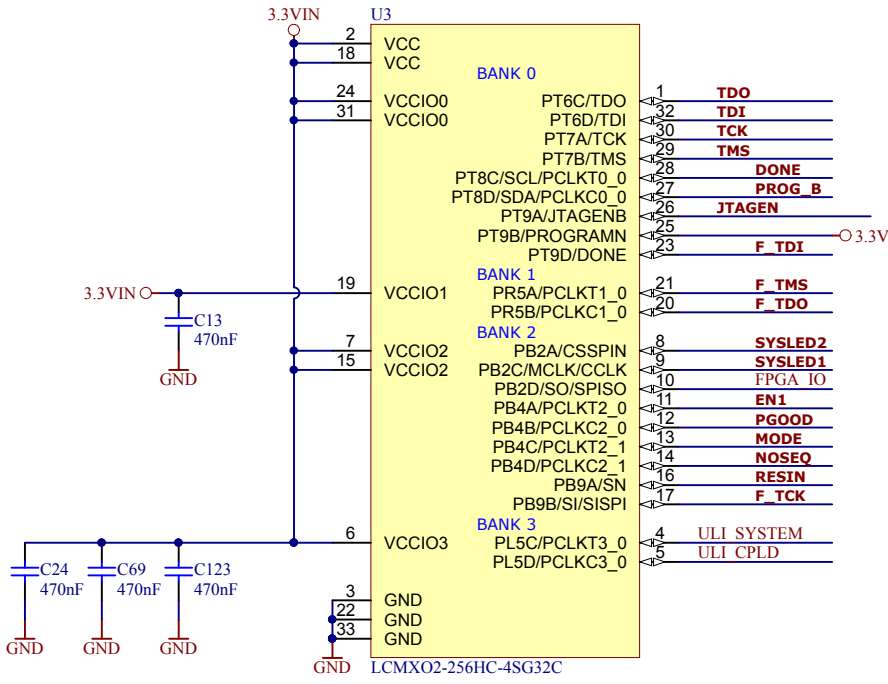


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|  | | | Title: Clock | |
| | | | A4 | Number: TE0712 100_2C2 |
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| Filename: Clock.SchDoc | | | | |

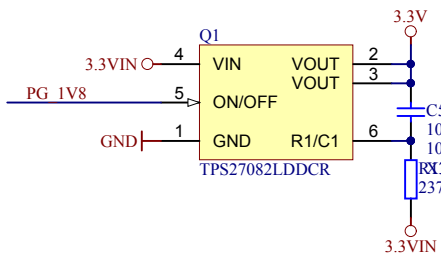
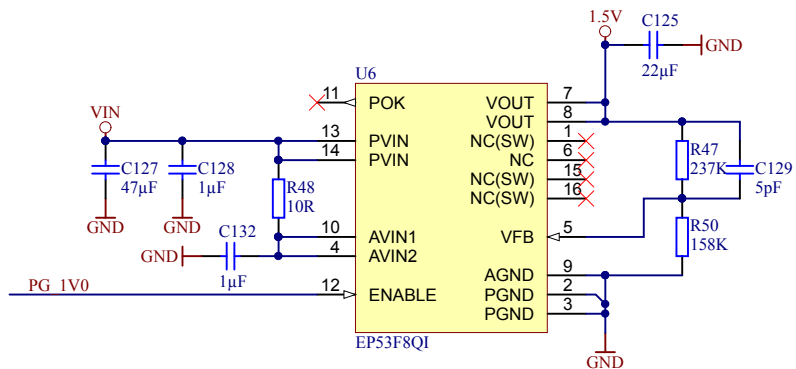
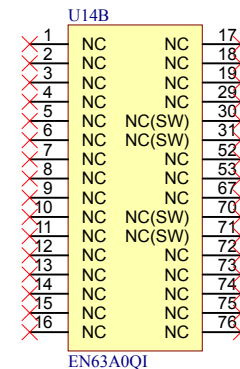
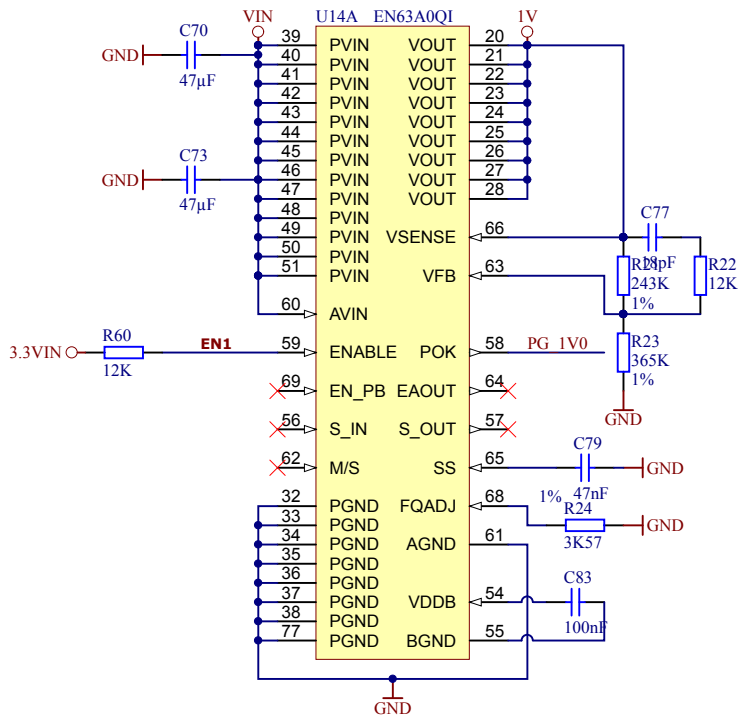
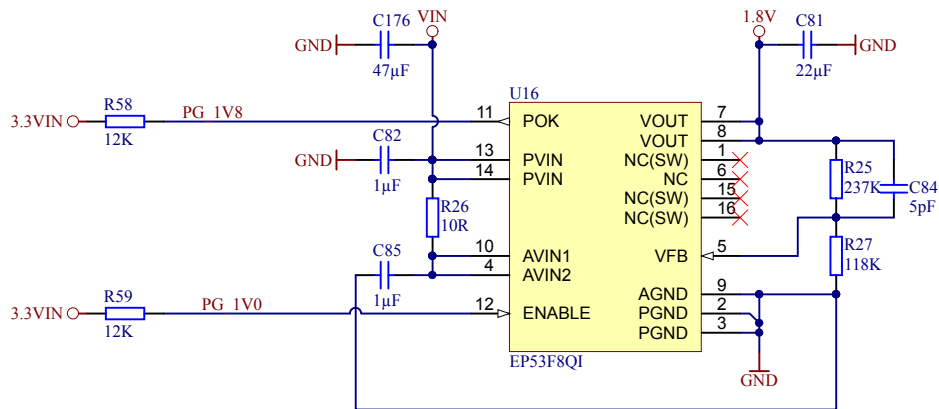




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|  | | | Title: ETH | |
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| | | |
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| Filename: PWR1.SchDoc | | |

1

2

3

4

A

A

B

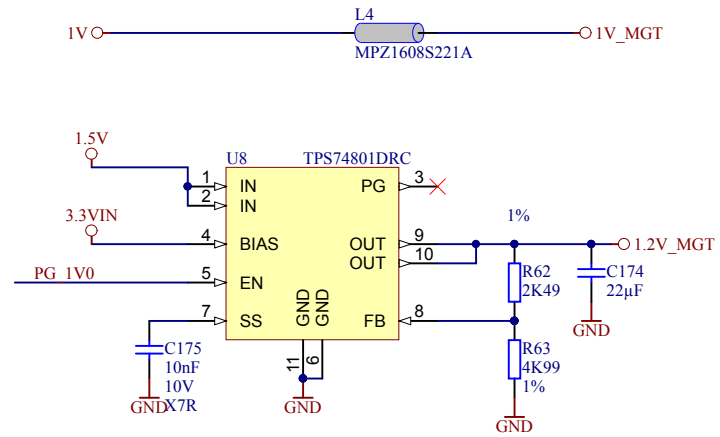
B


C

C

D

D



| | | | |
|---|-----------------------|---------------------------------------|---------------|
|  | Title: PWR | | |
| | A4 | Number: TE0712 100_2C2 | Rev. 01 |
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| | Filename: PWR2.SchDoc | | |

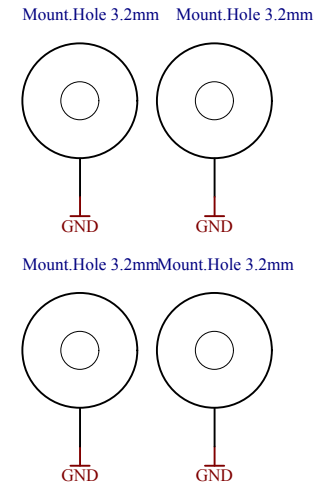
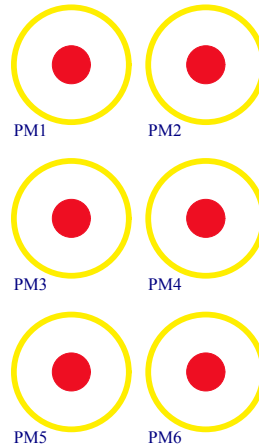
1

2

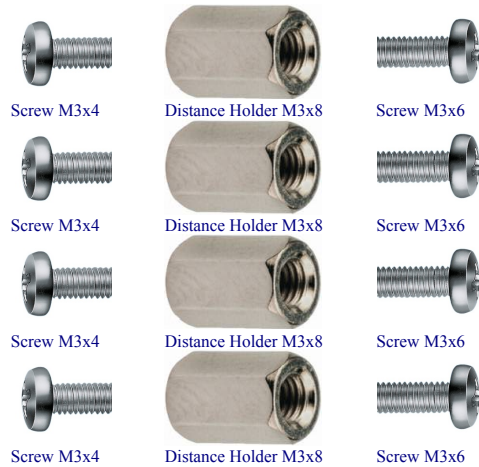
3


4

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|---|
| U_B2B-Connectors B2B-Connectors.SchDoc |
| U_B13 B13.SchDoc |
| U_B14 B14.SchDoc |
| U_B15 B15.SchDoc |
| U_B16 B16.SchDoc |
| U_B34 B34.SchDoc |
| U_FPGA-MGT FPGA-MGT.SchDoc |
| U_FPGA-CFG FPGA-CFG.SchDoc |
| U_FPGA-PWR FPGA-PWR.SchDoc |
| U_Clock Clock.SchDoc |
| U_DDR3-RAM DDR3-RAM.SchDoc |
| U_ETHERNET ETHERNET.SchDoc |
| U_CPLD CPLD.SchDoc |
| U_PWR1 PWR1.SchDoc |
| U_PWR2 PWR2.SchDoc |



Top of Board



| | | | | |
|---|--|---------------------------------------|----------------------|-----------------------------------|
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