

A

A

B

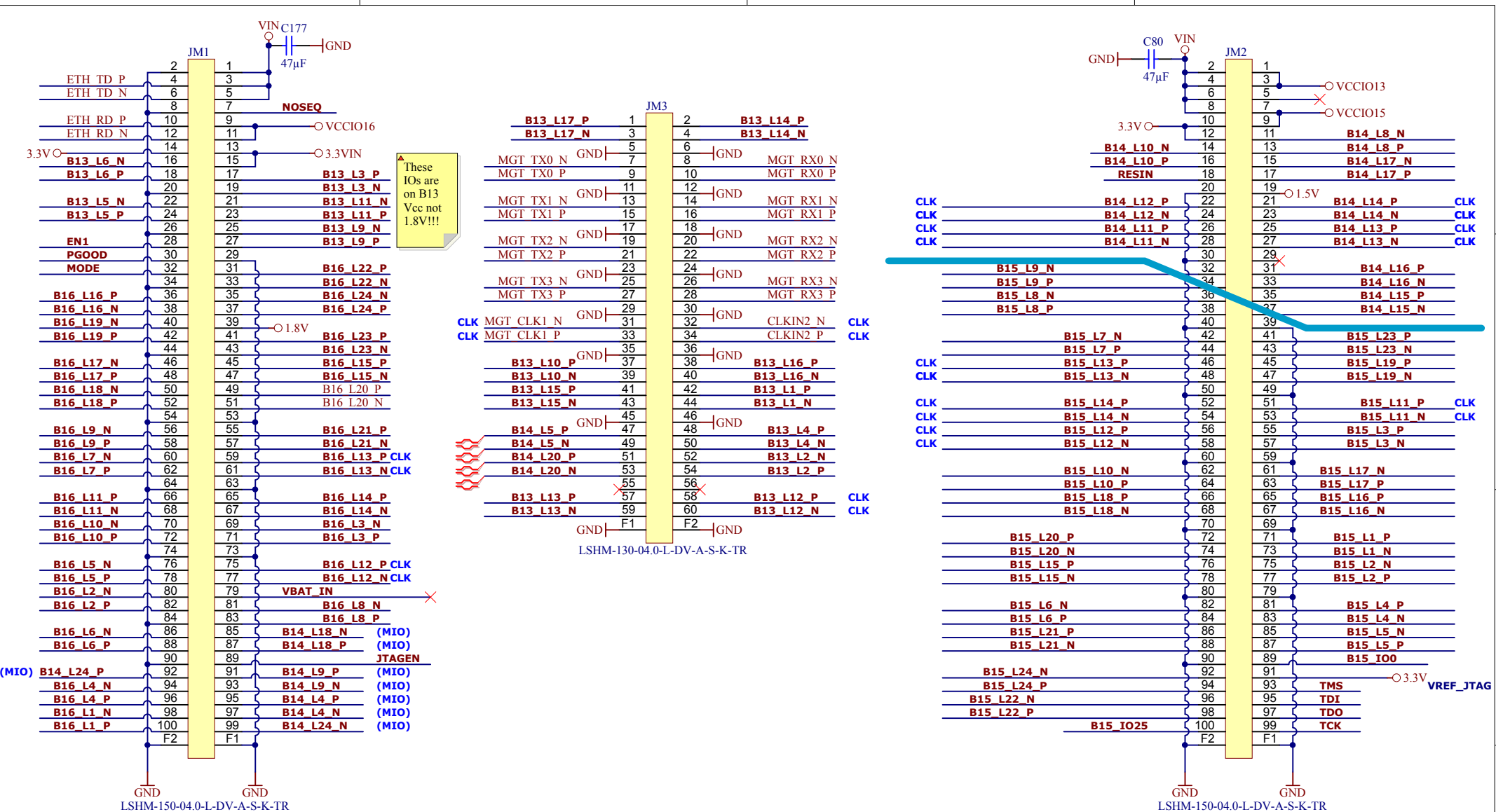
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C

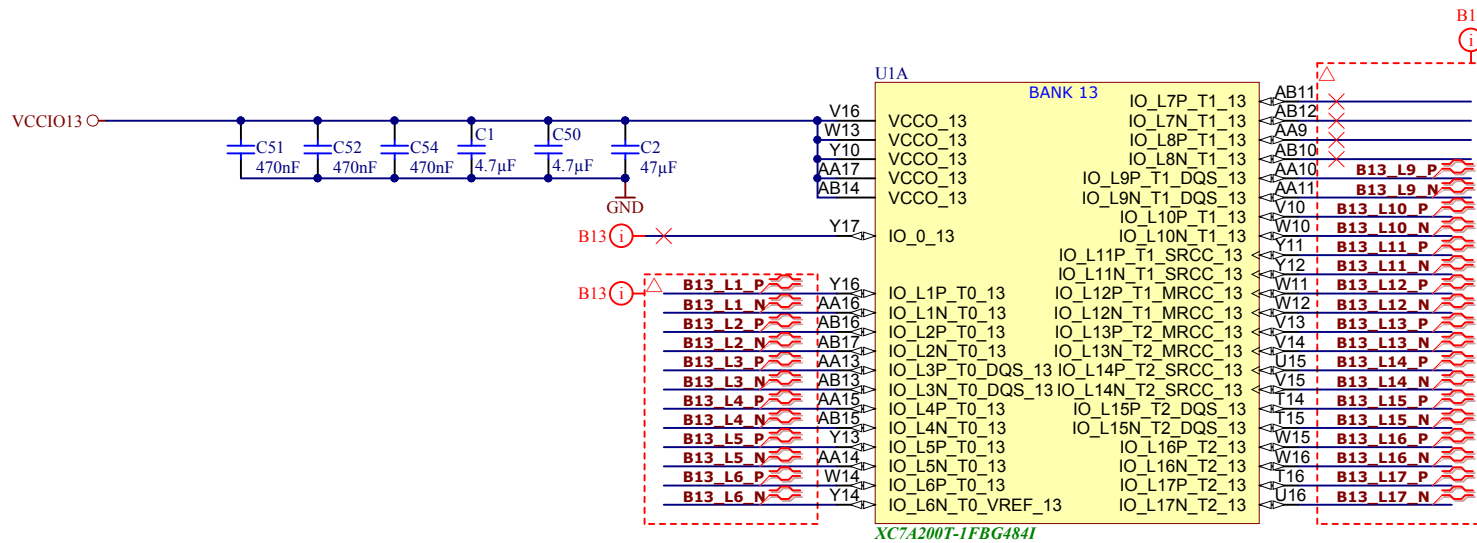
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D

D



	Title: B2B		
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	Filename: B2B-Connectors.SchDoc		



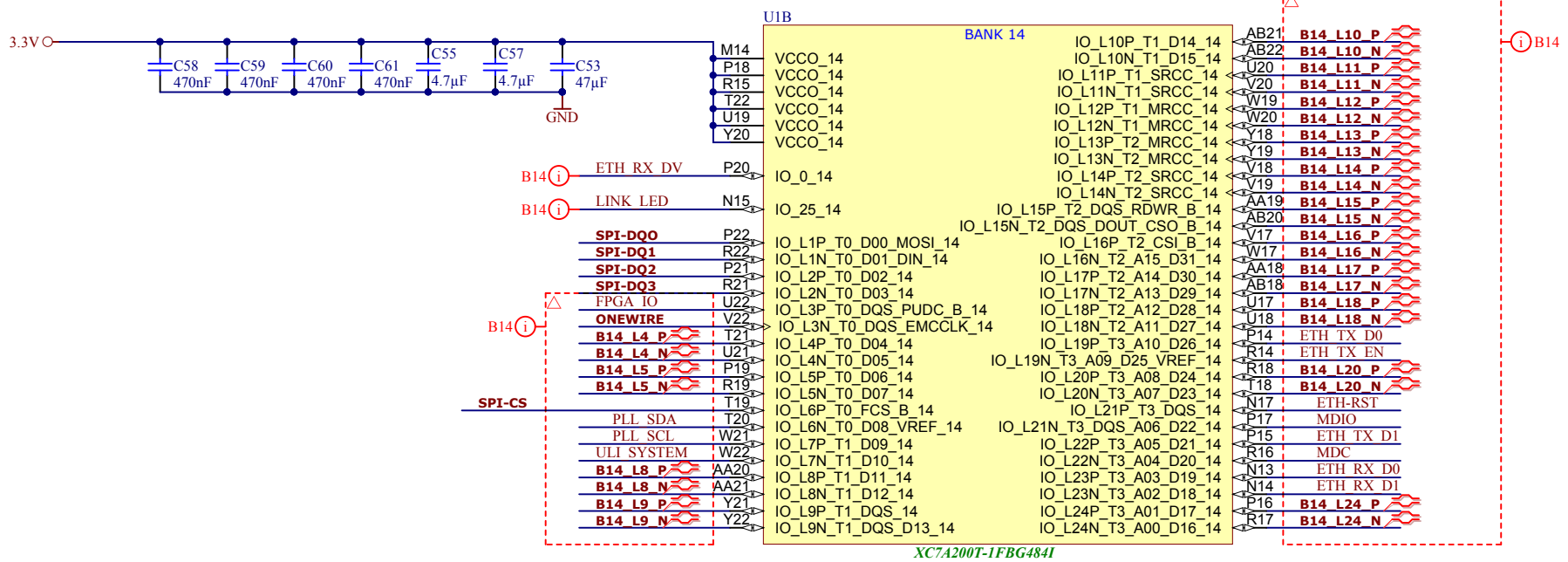
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BANK 13

XC7A200T-1FBG484I



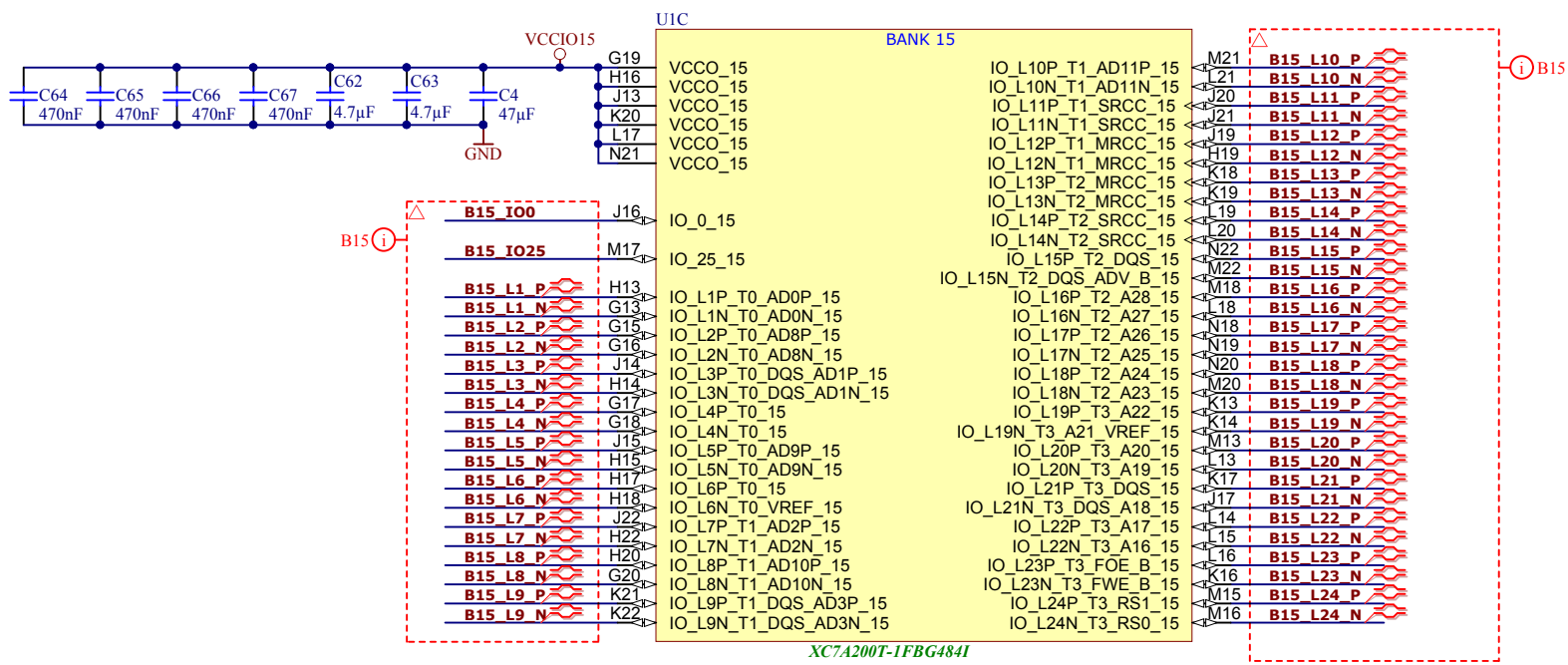
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A4	Number: TE0712 200_11	Rev. 01
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XC7A200T-1FBG484I



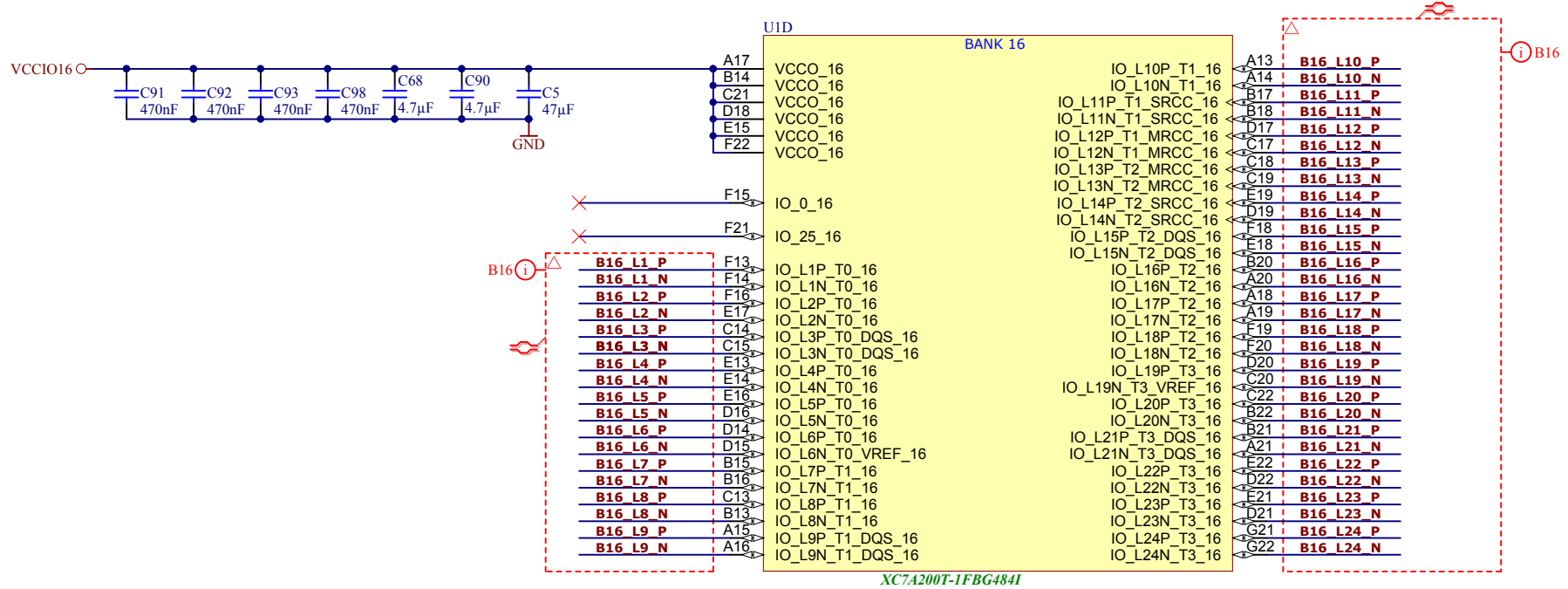
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A4	Number: TE0712 200_11	Rev. 01
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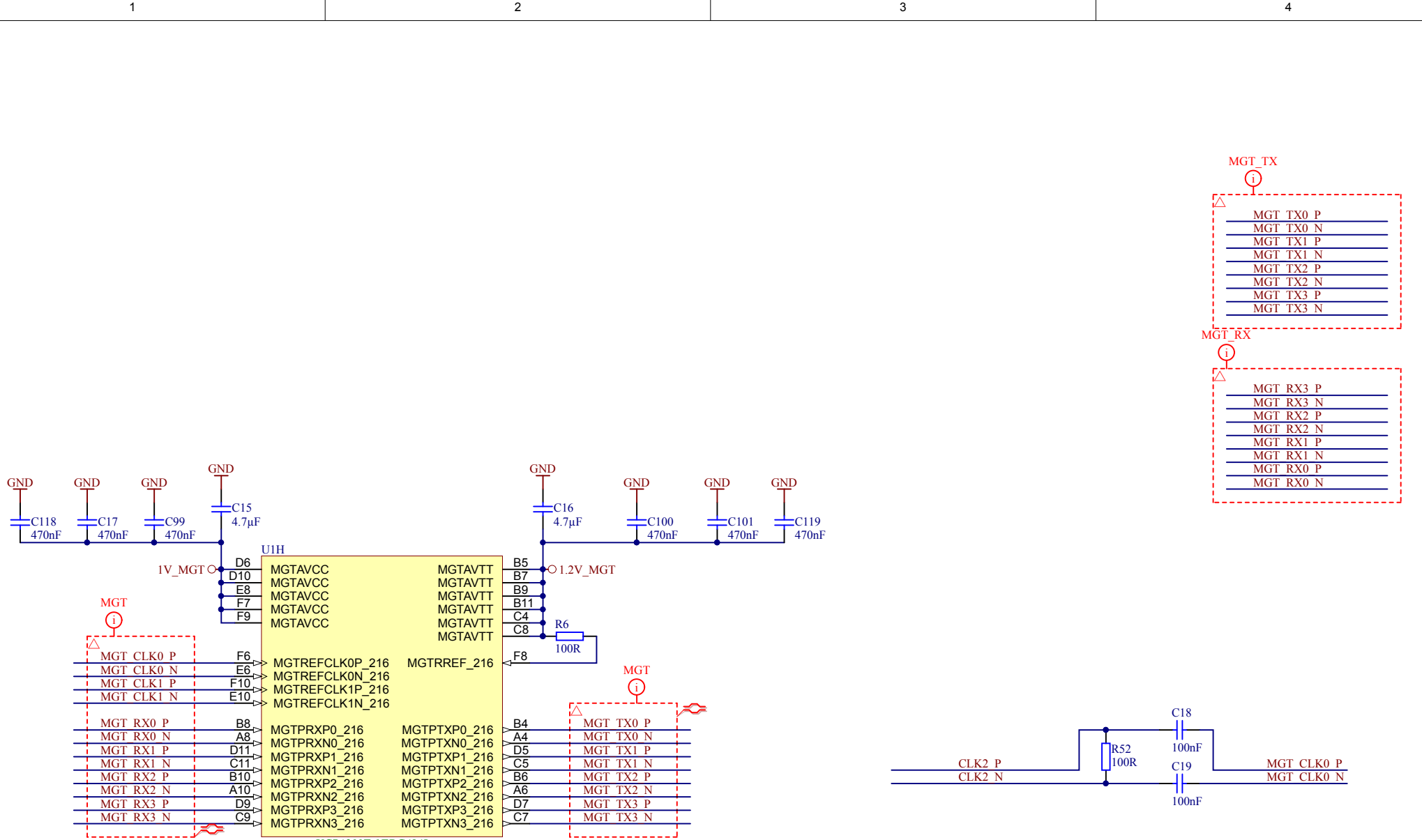
XC7A200T-1FBG484I




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		Title: MGT	
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1

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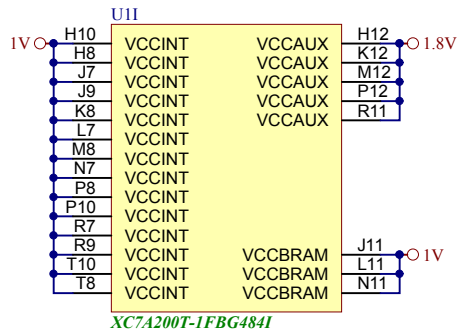
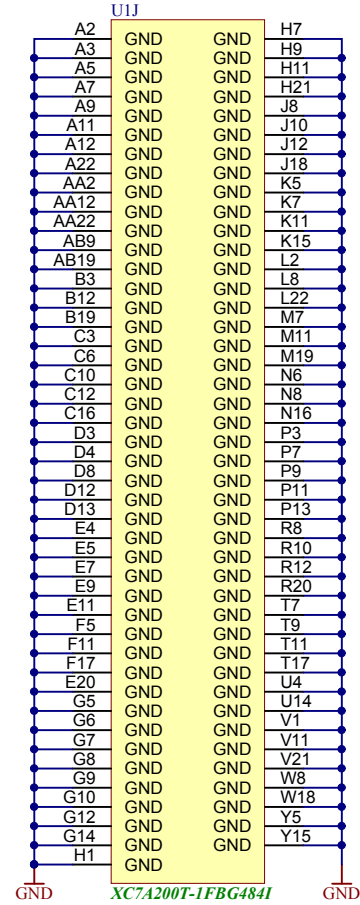
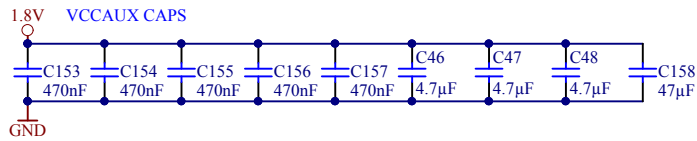
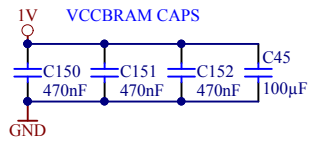
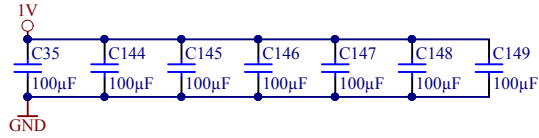
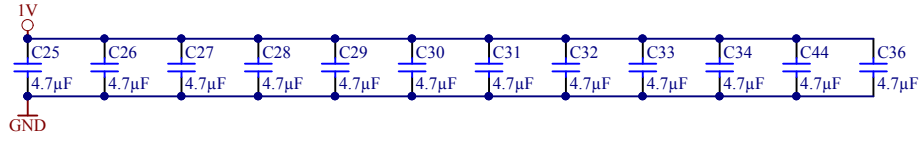
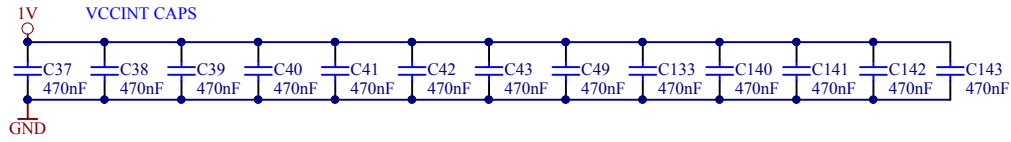
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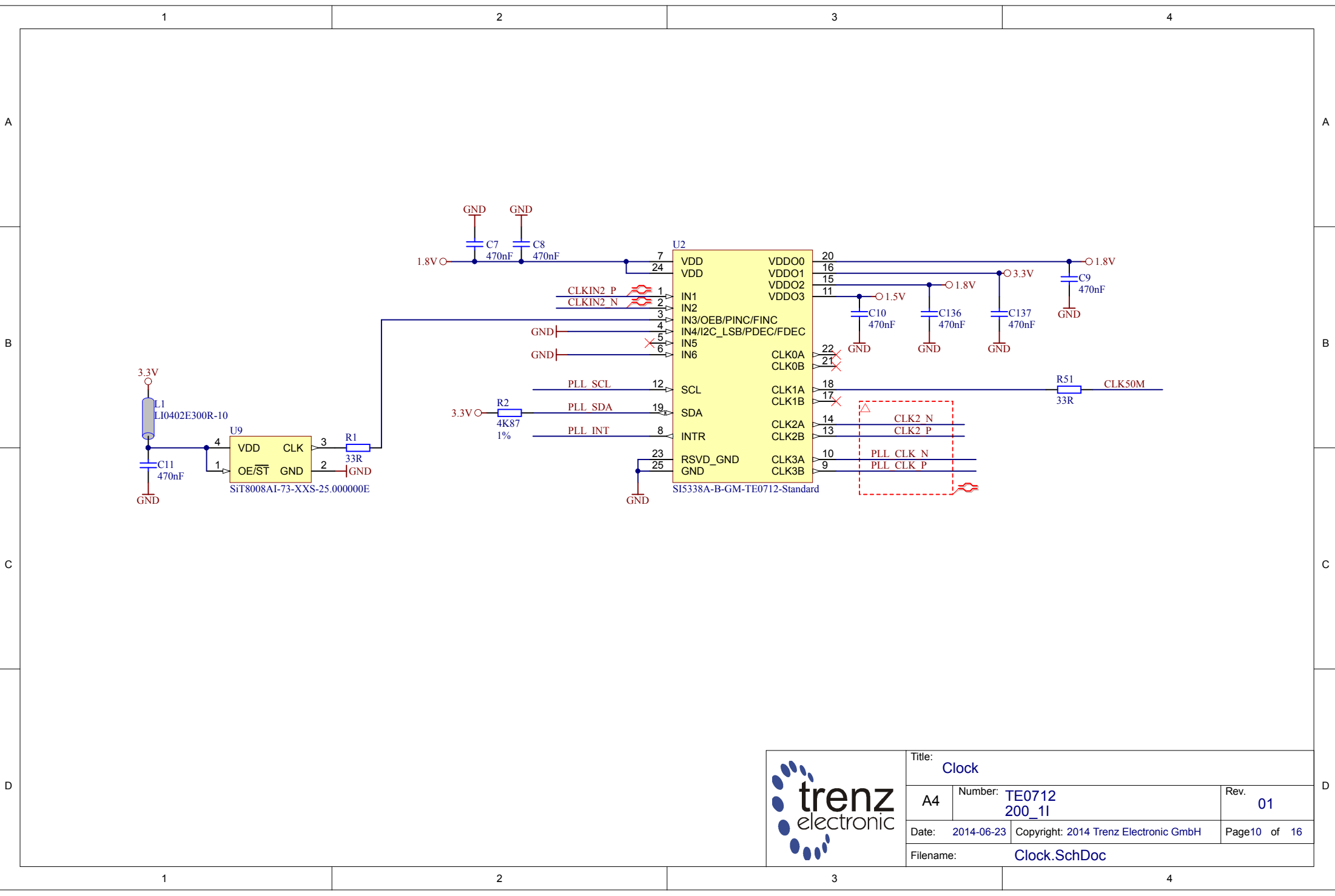
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4



Title: PWR		
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			Title: Clock	
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A

B

C

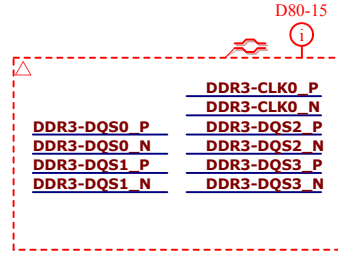
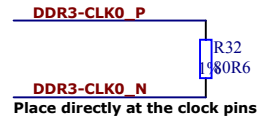
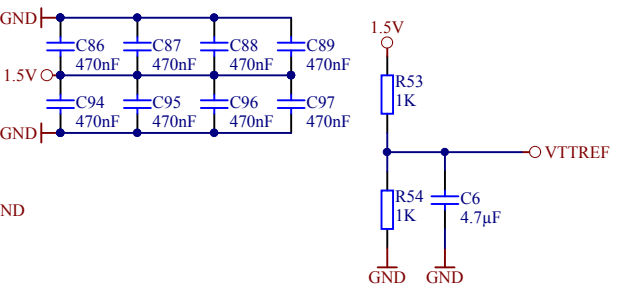
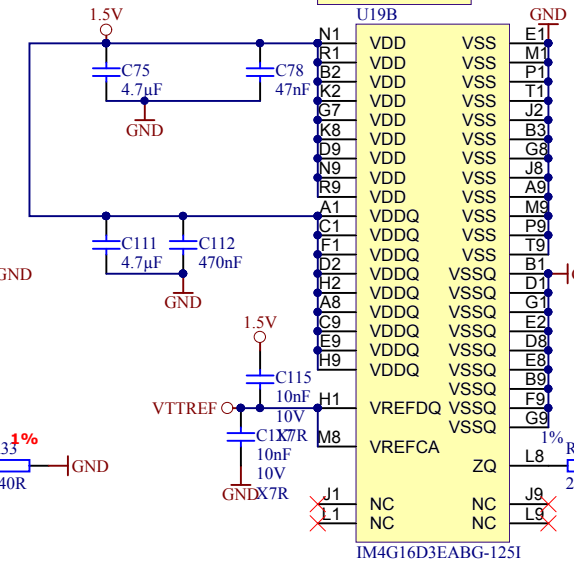
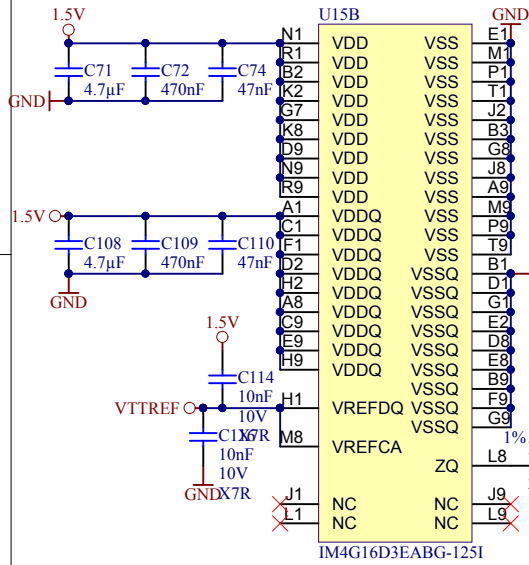
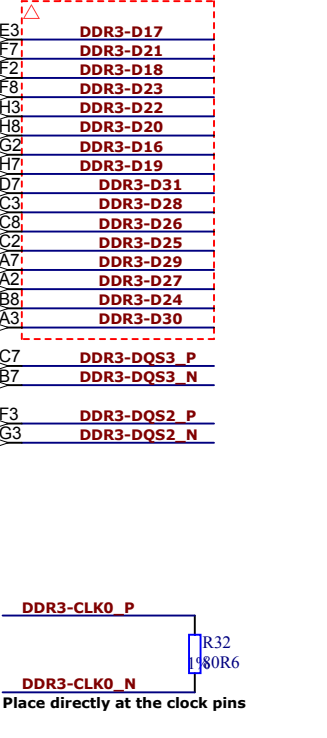
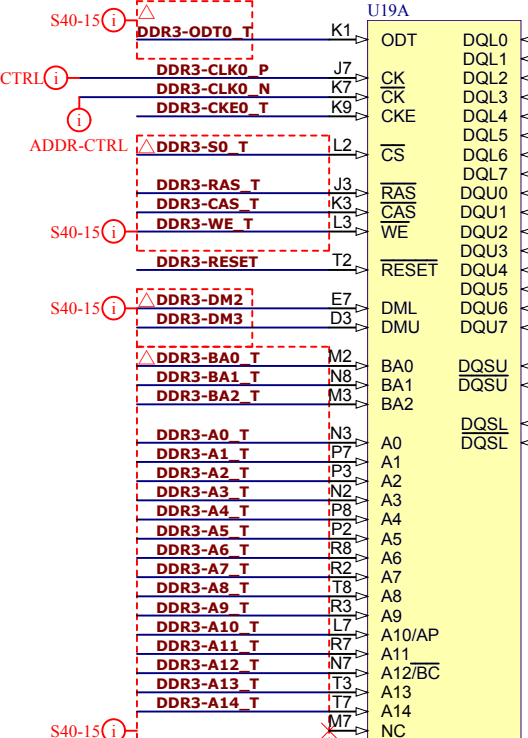
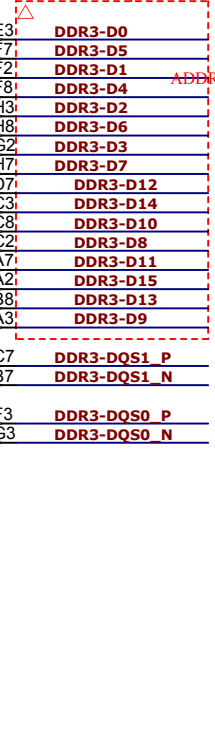
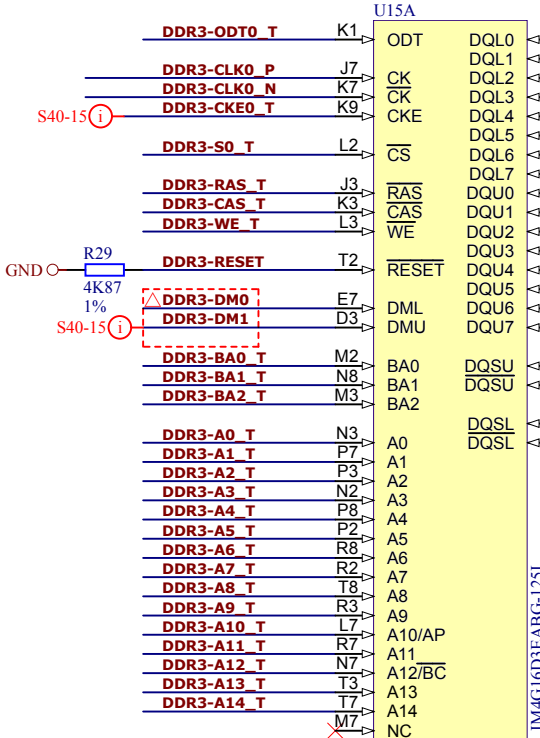
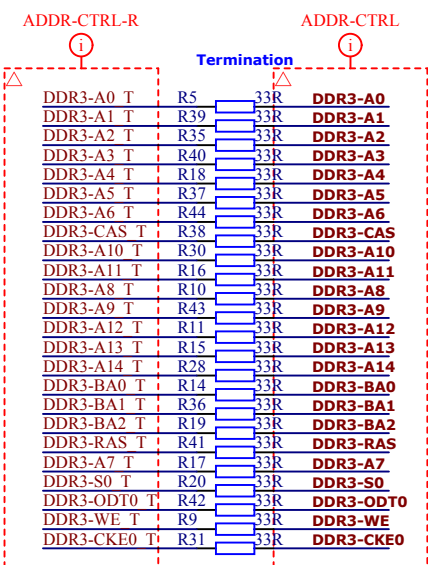
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A

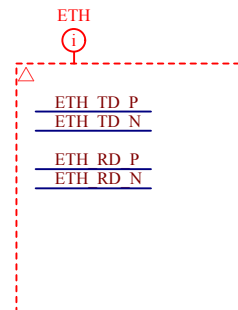
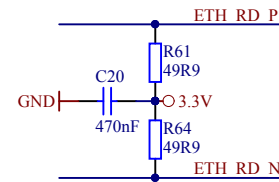
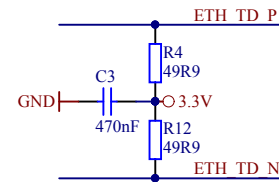
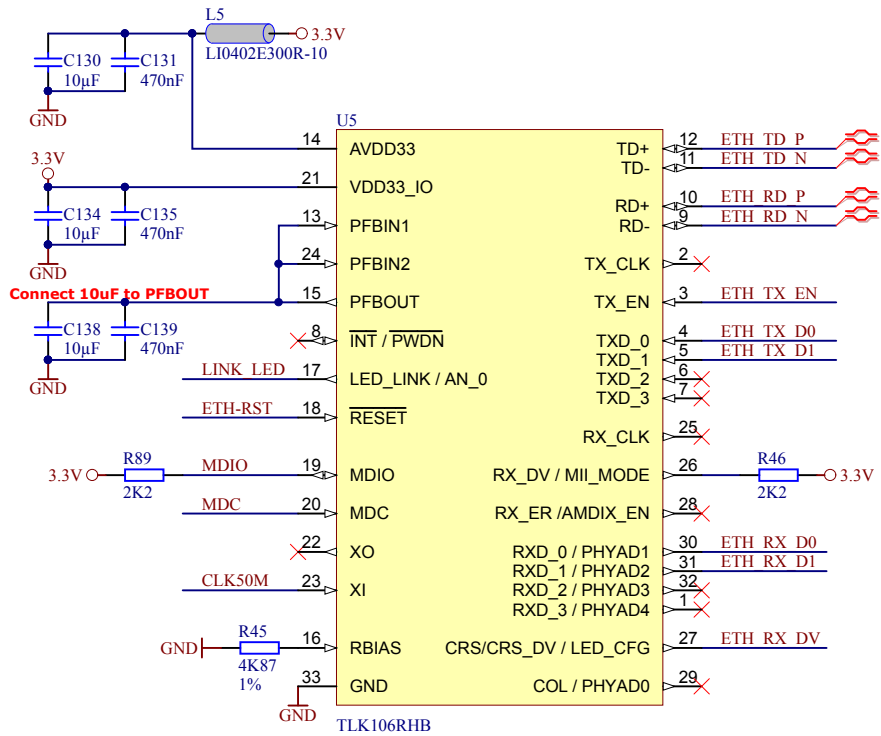
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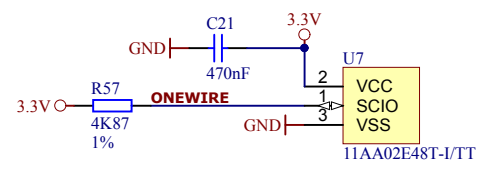
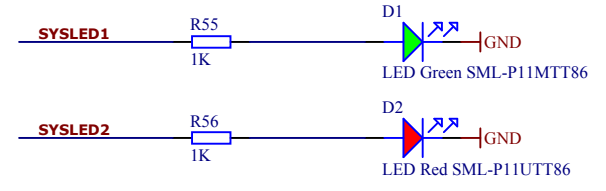
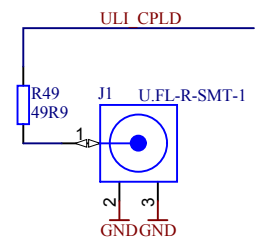
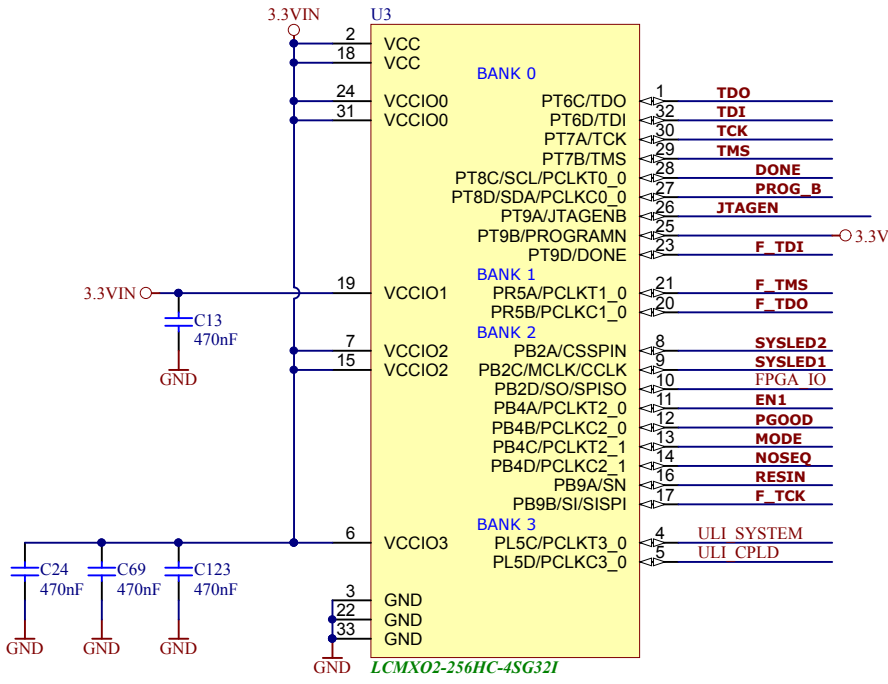
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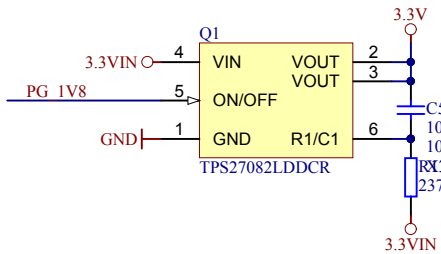
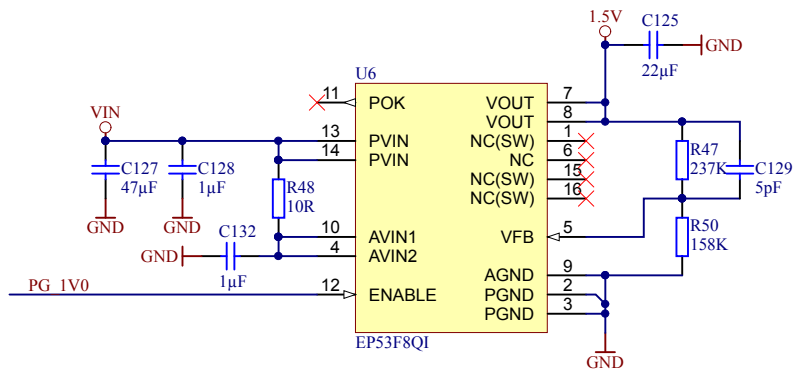
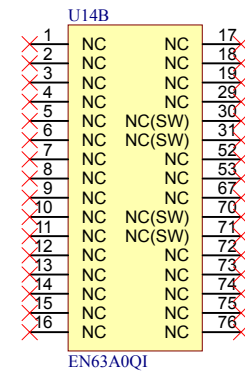
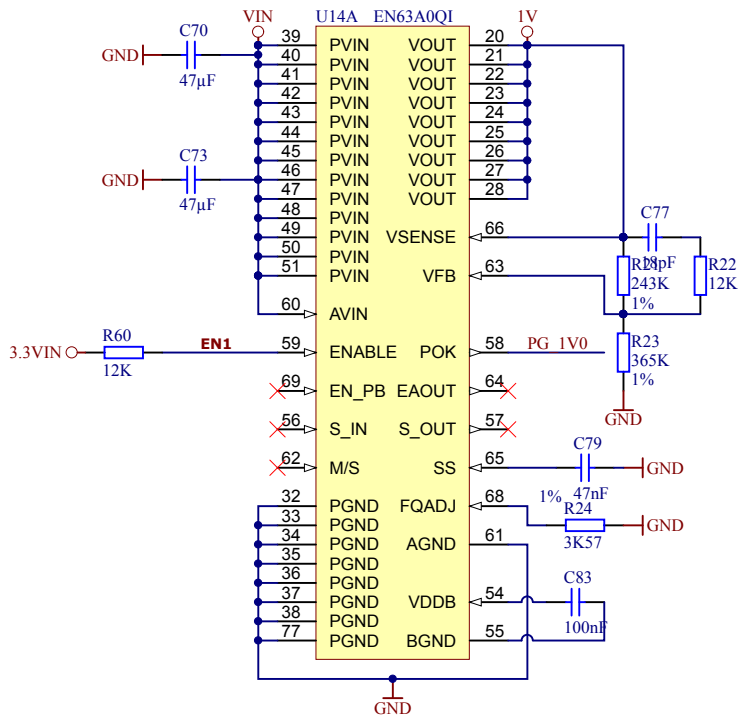
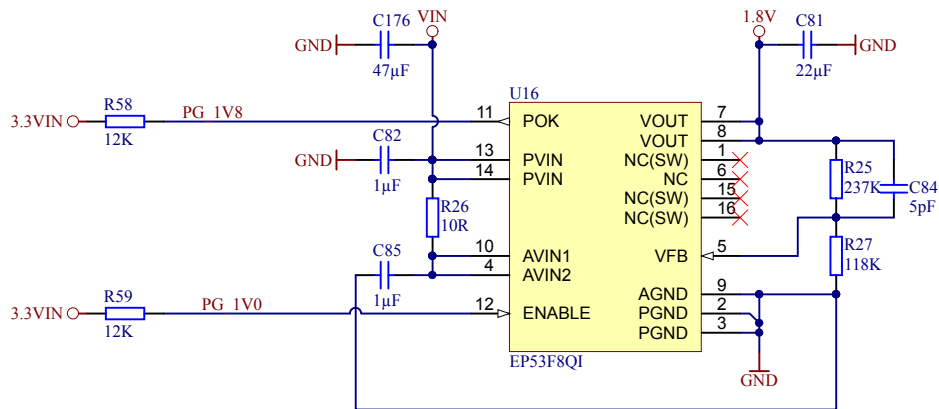
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Title: PWR		
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Filename: PWR1.SchDoc		

1

2

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A

A

B

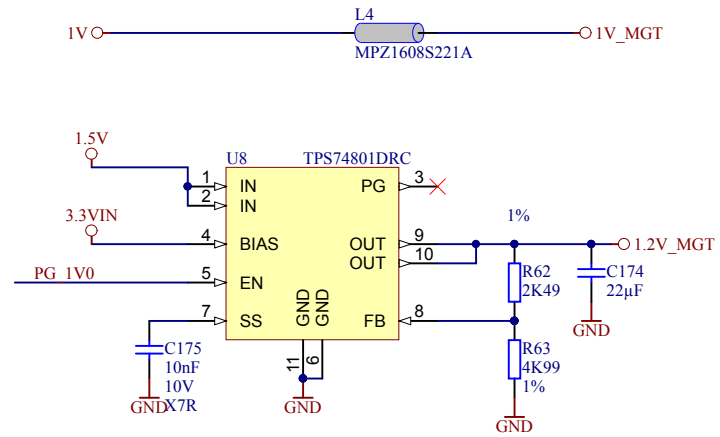
B


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C

D

D



		Title: PWR	
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Filename: PWR2.SchDoc		Page 15 of 16	

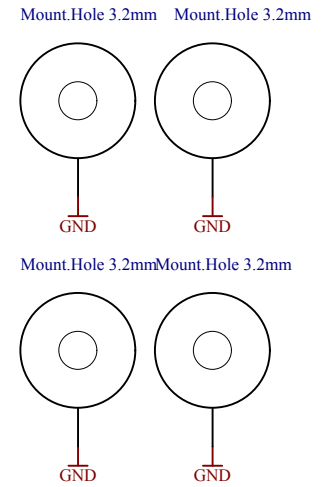
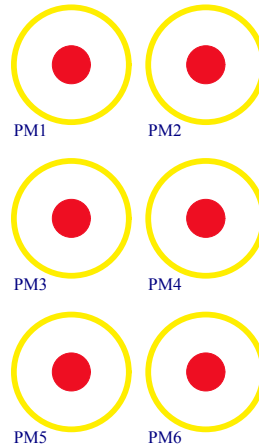
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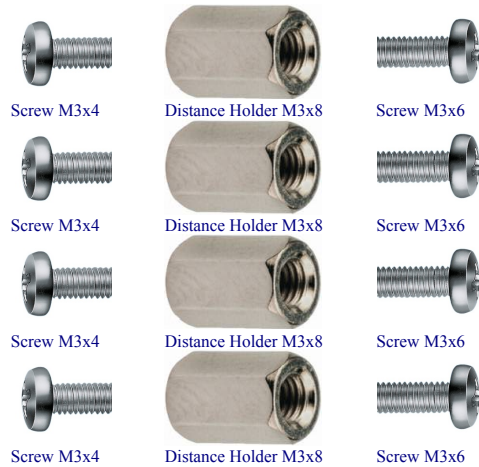
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4

U_B2B-Connectors
B2B-Connectors.SchDoc
U_B13
B13.SchDoc
U_B14
B14.SchDoc
U_B15
B15.SchDoc
U_B16
B16.SchDoc
U_B34
B34.SchDoc
U_FPGA-MGT
FPGA-MGT.SchDoc
U_FPGA-CFG
FPGA-CFG.SchDoc
U_FPGA-PWR
FPGA-PWR.SchDoc
U_Clock
Clock.SchDoc
U_DDR3-RAM
DDR3-RAM.SchDoc
U_ETHERNET
ETHERNET.SchDoc
U_CPLD
CPLD.SchDoc
U_PWR1
PWR1.SchDoc
U_PWR2
PWR2.SchDoc



Top of Board



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