

A

A

B

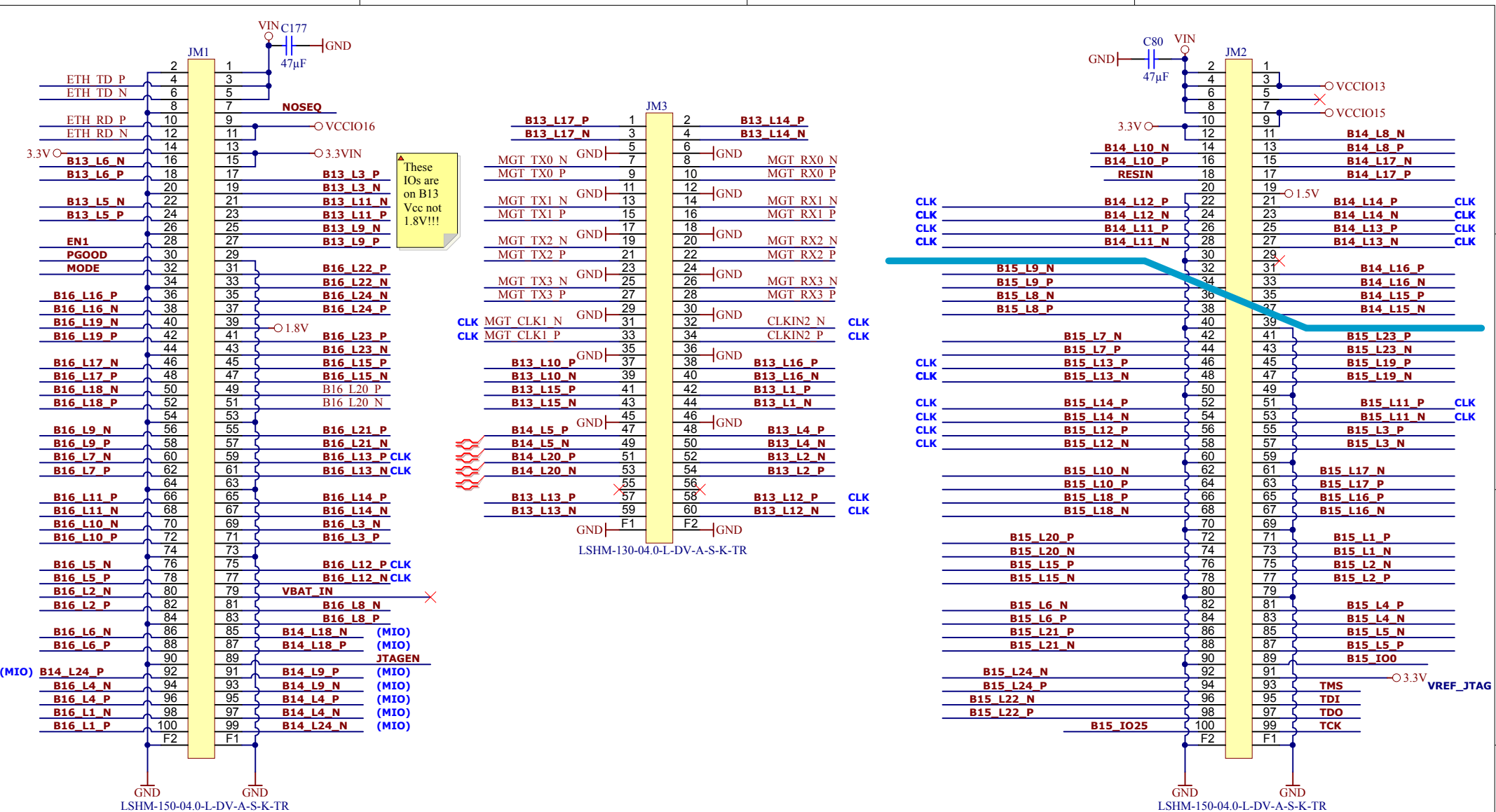
B

C

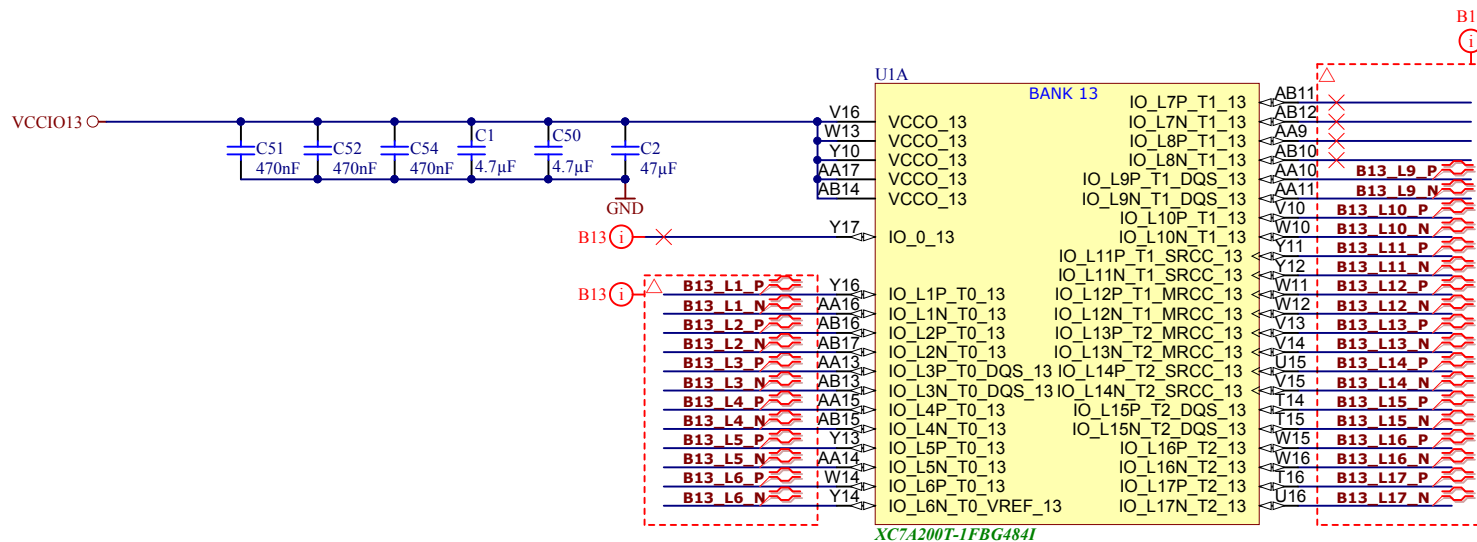
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D

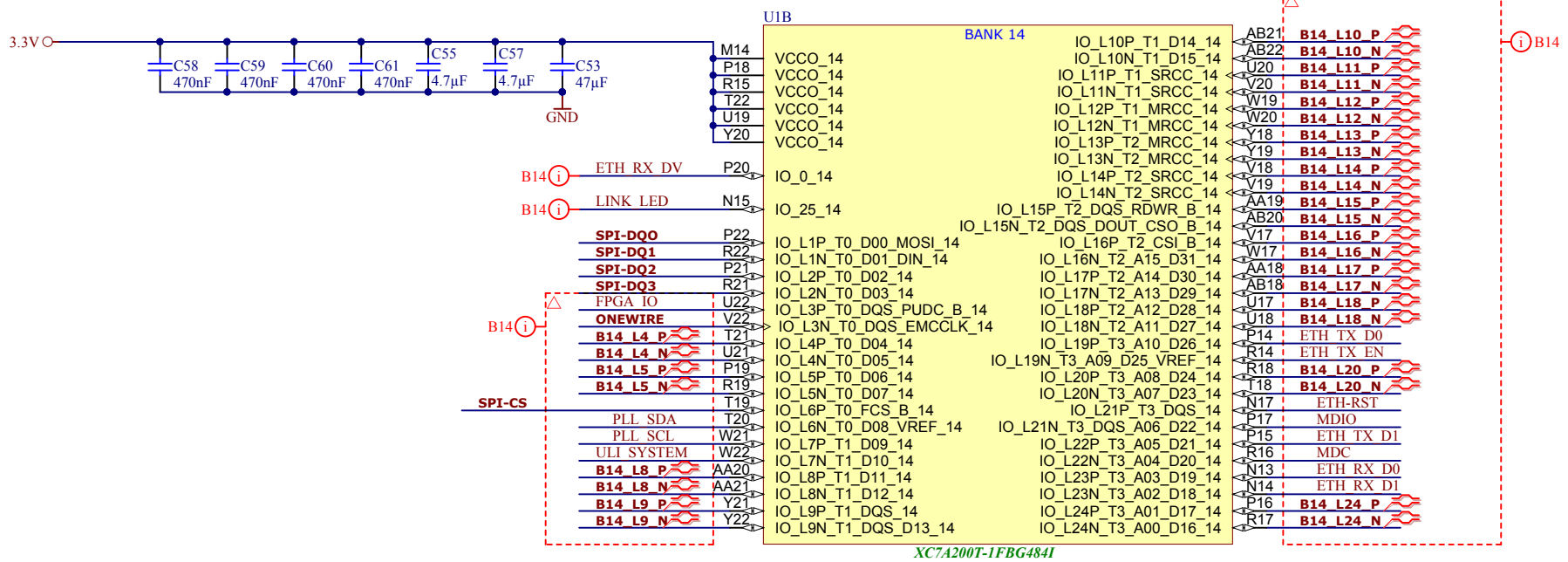


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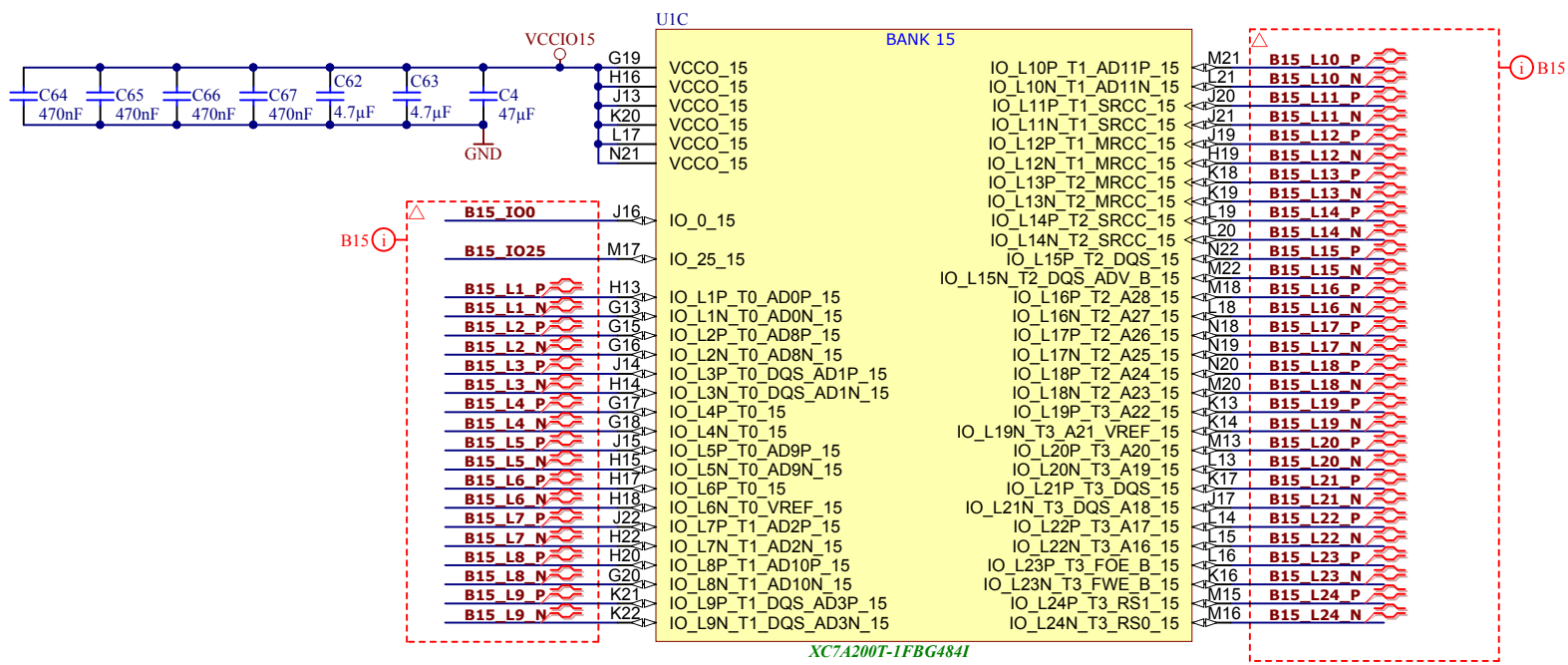


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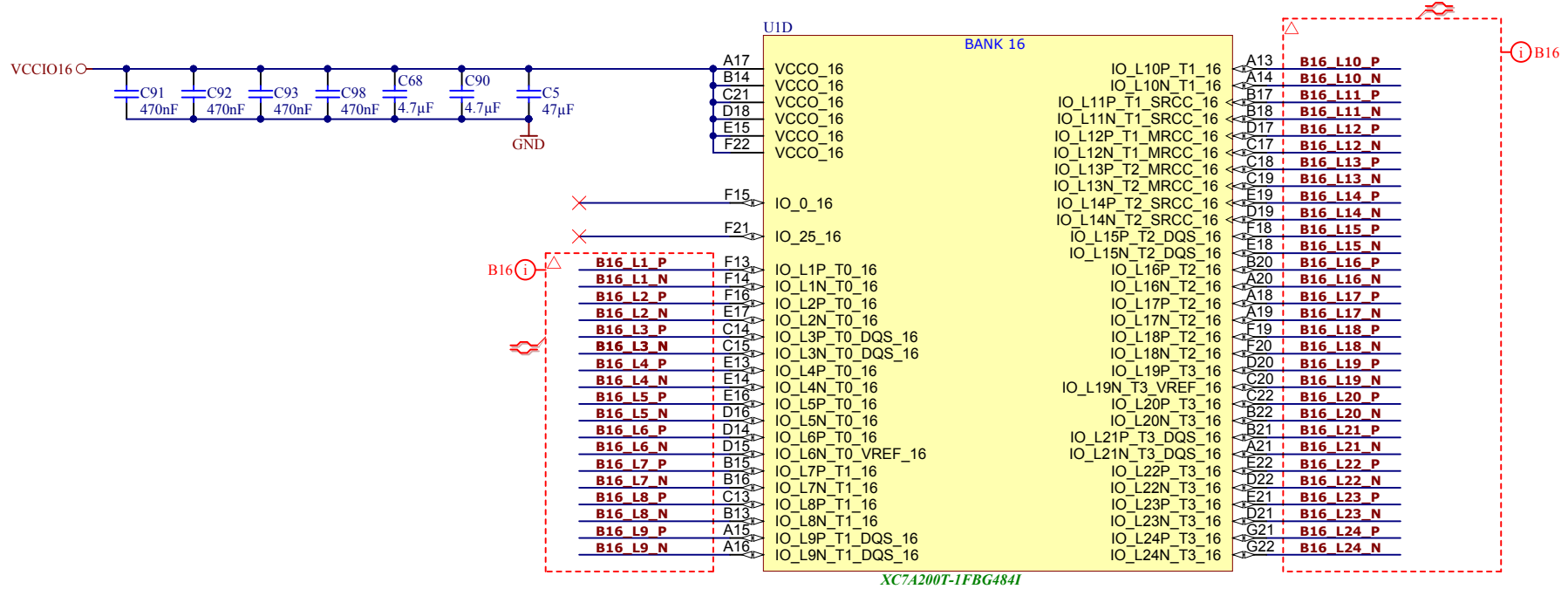
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Filename: B13.SchDoc		



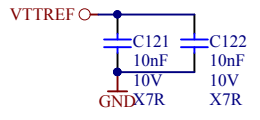
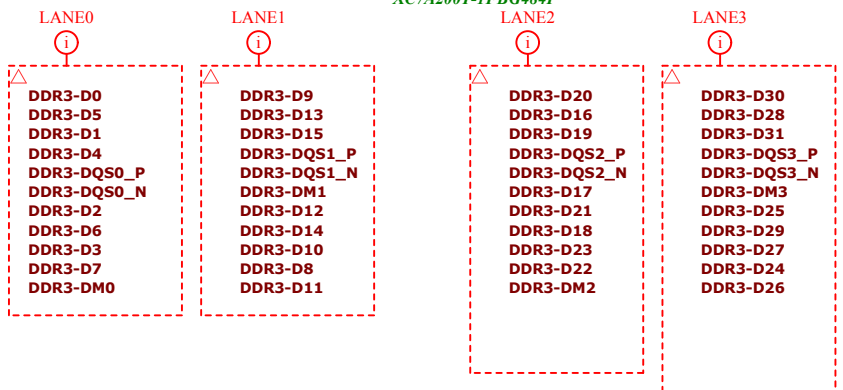
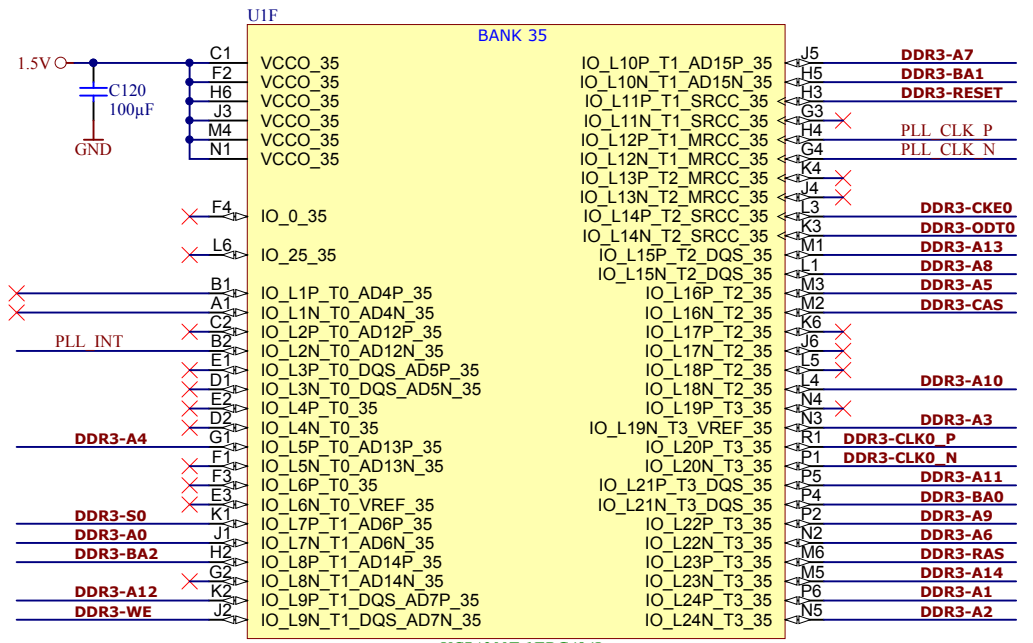
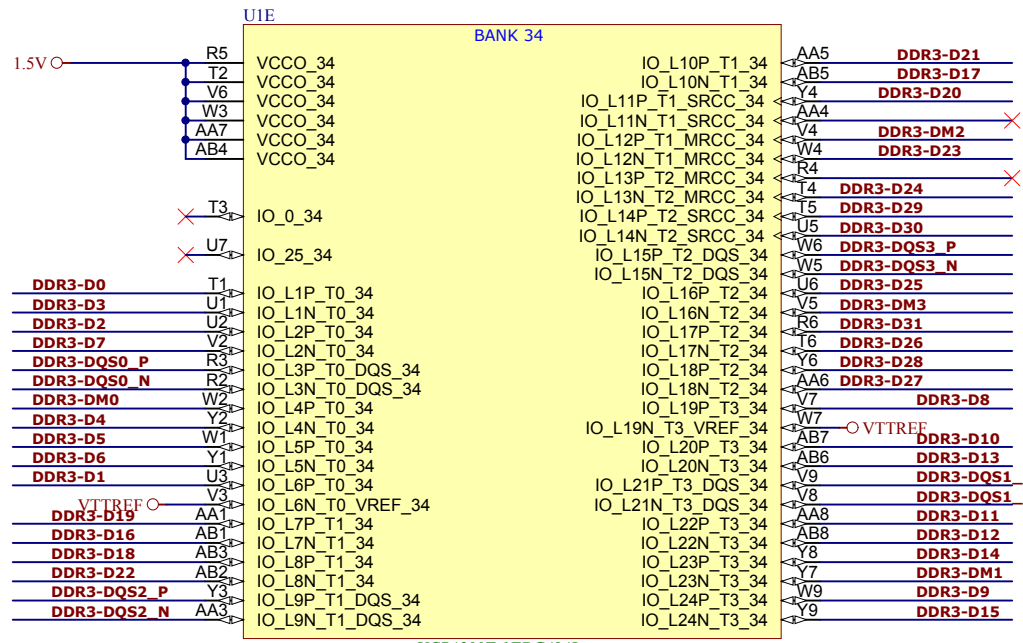
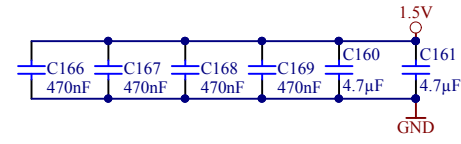
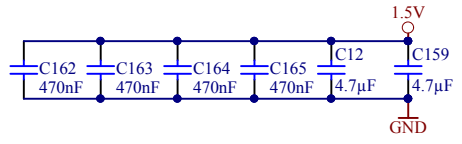
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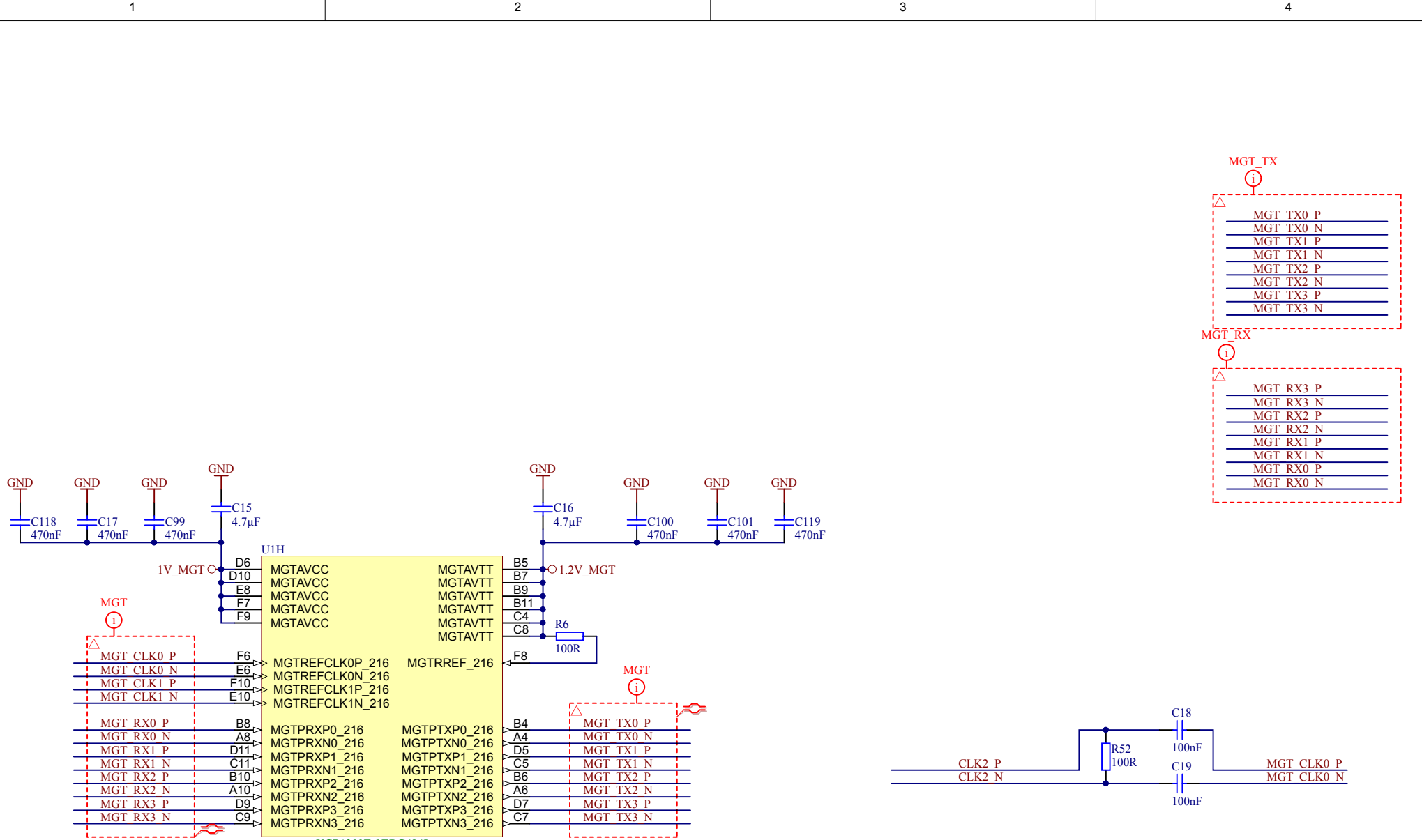
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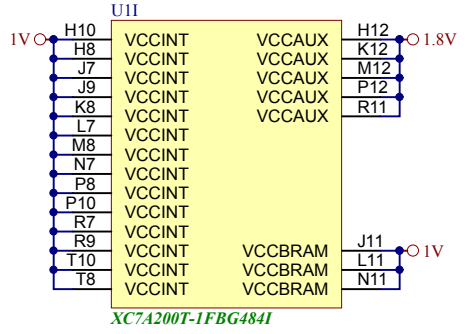
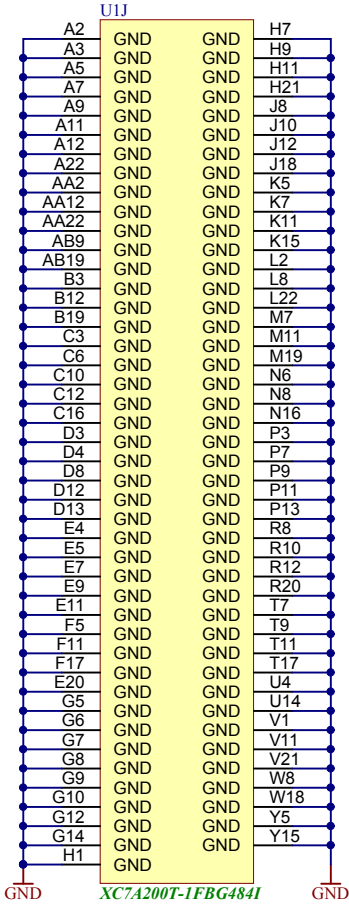
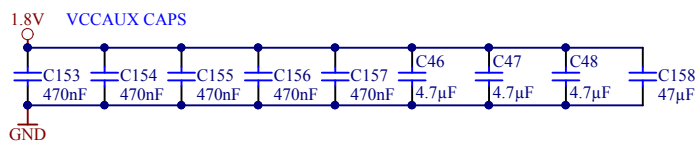
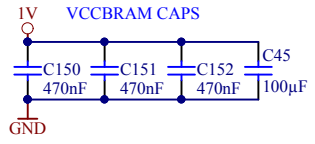
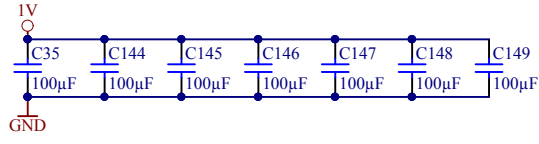
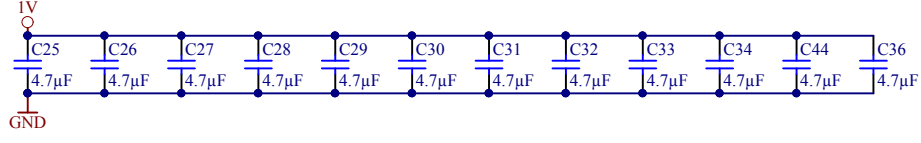
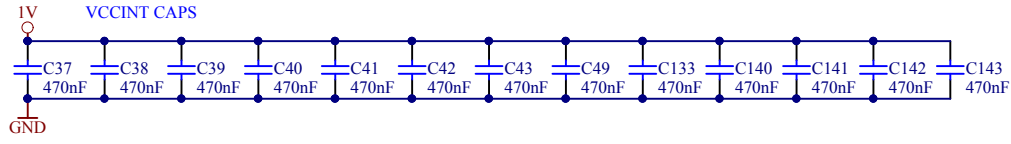
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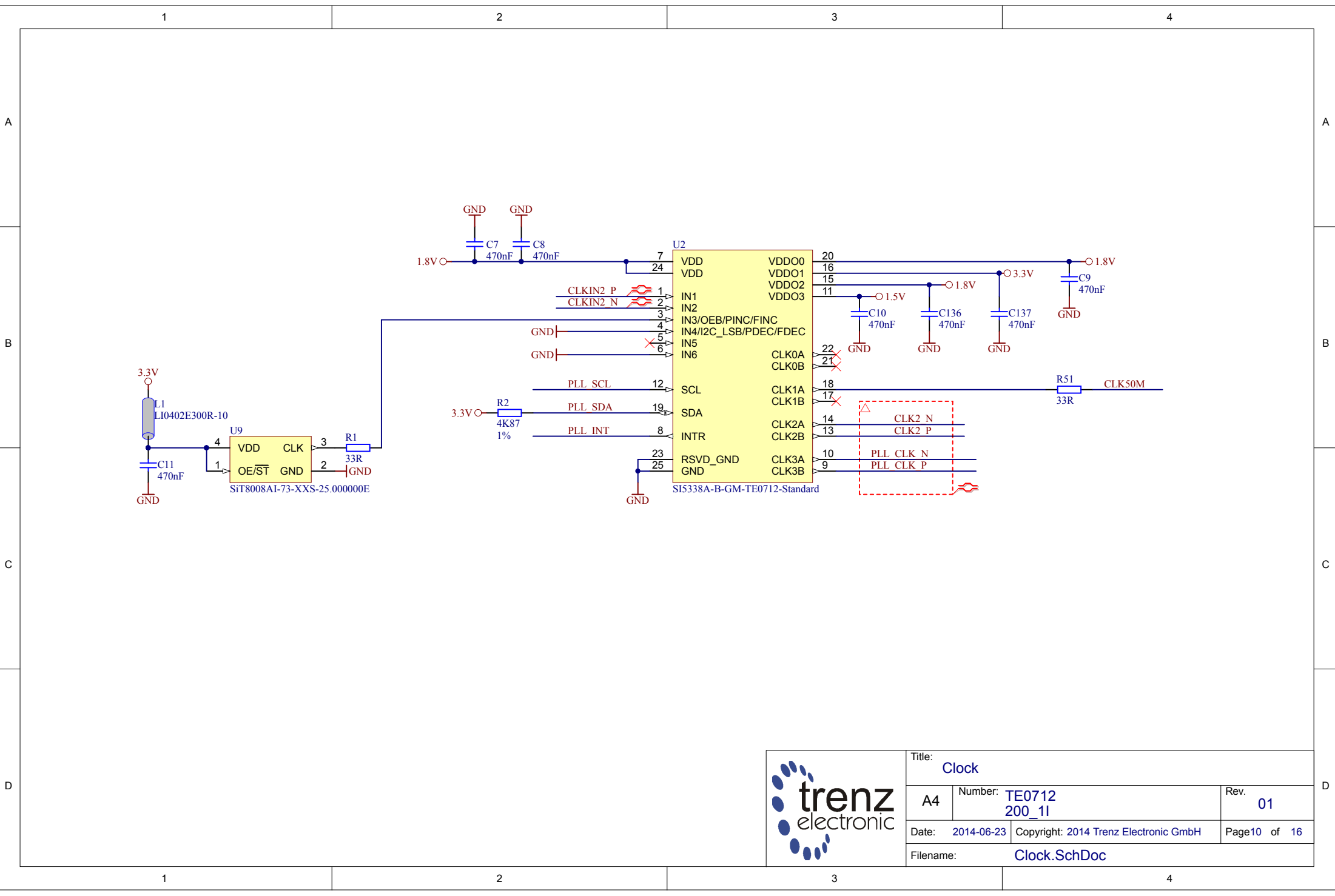
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			Title: Clock	
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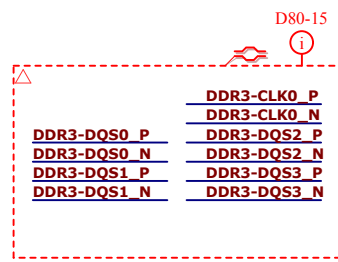
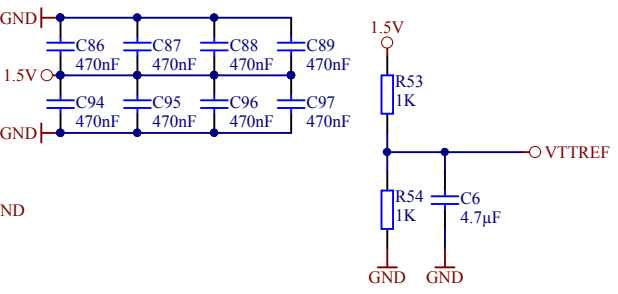
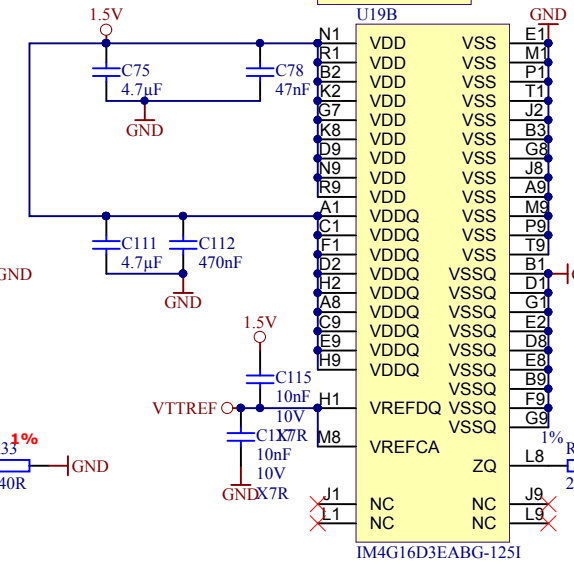
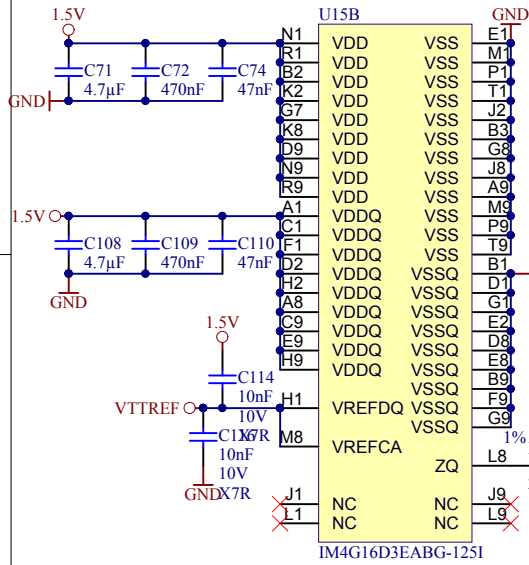
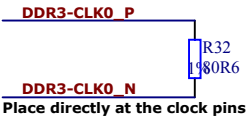
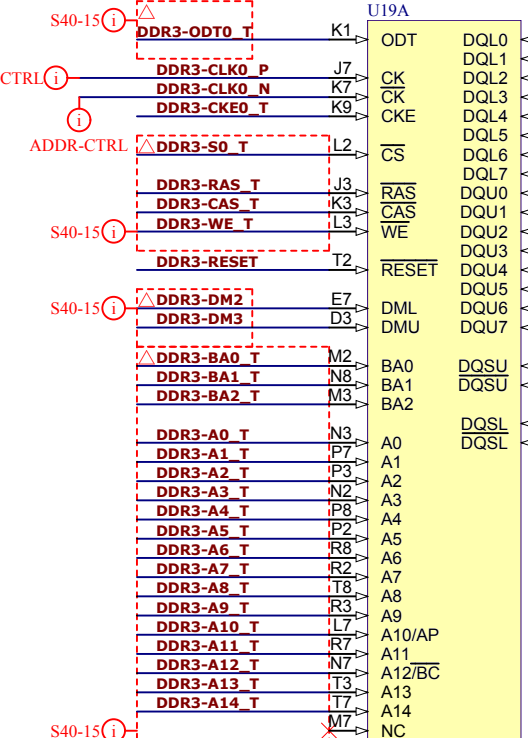
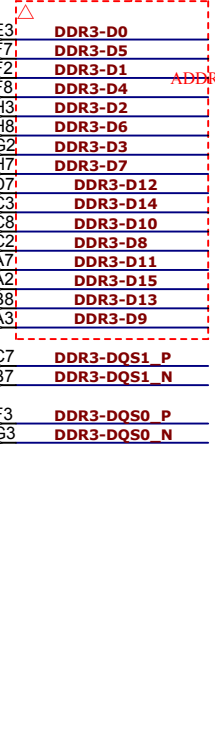
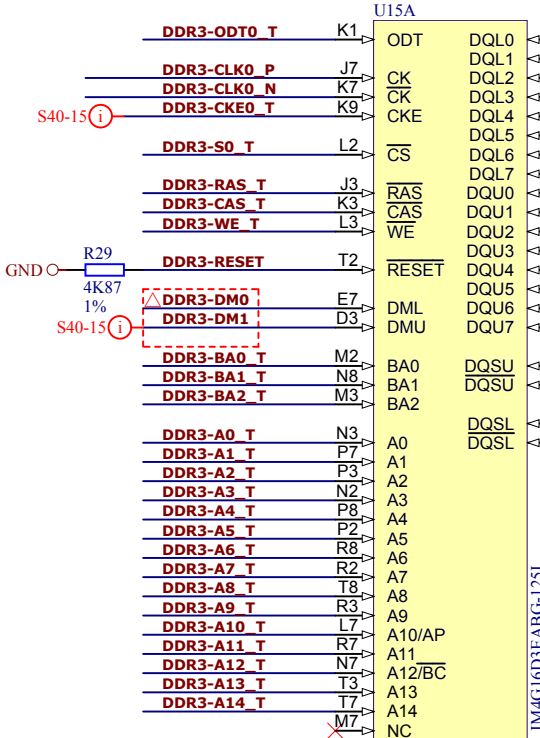
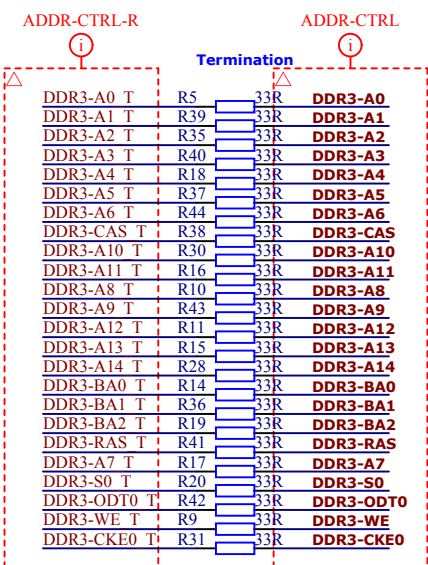
D

A

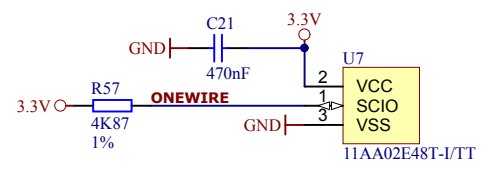
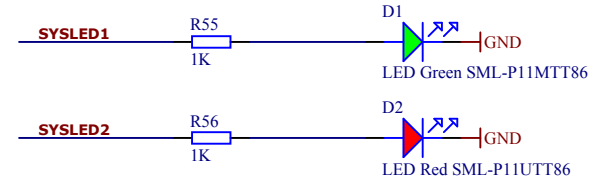
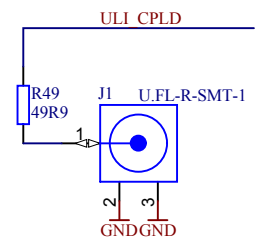
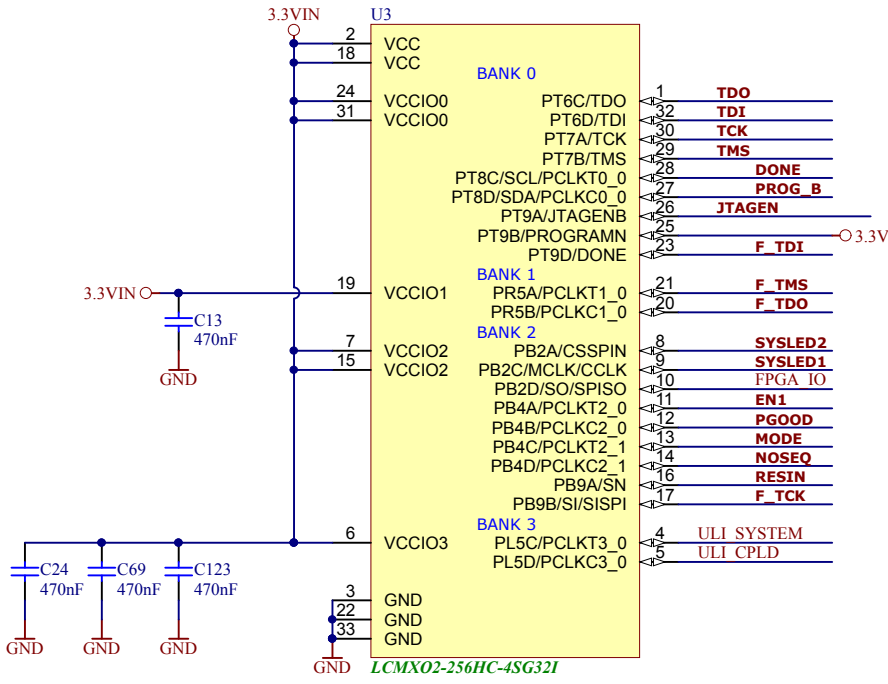
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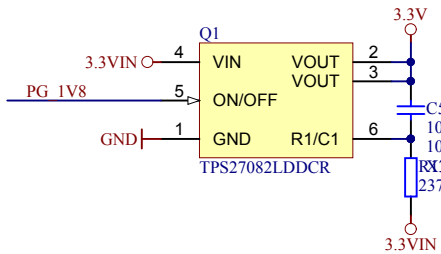
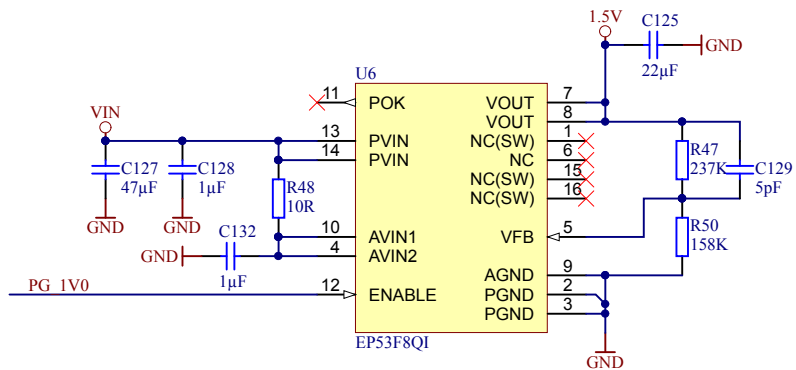
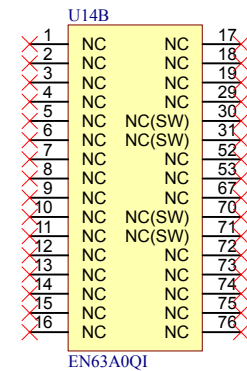
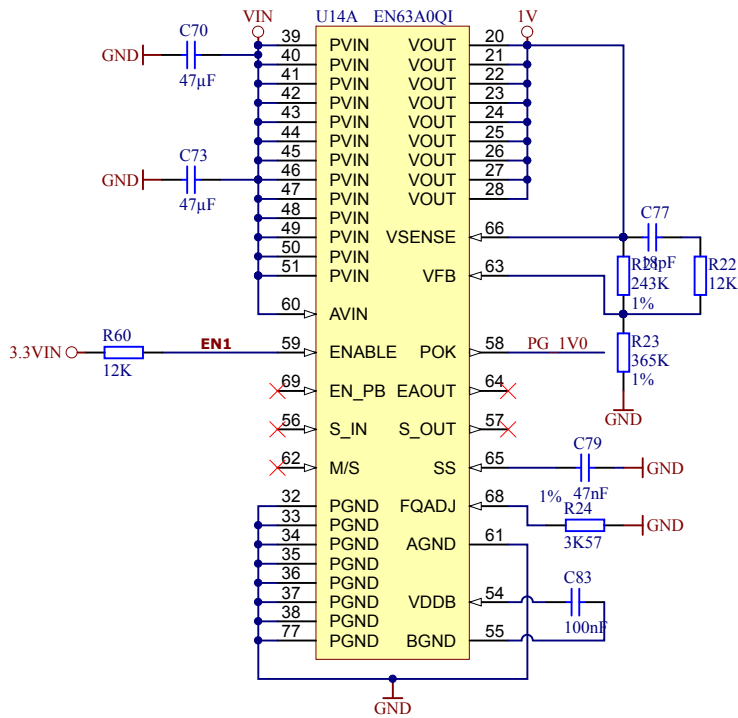
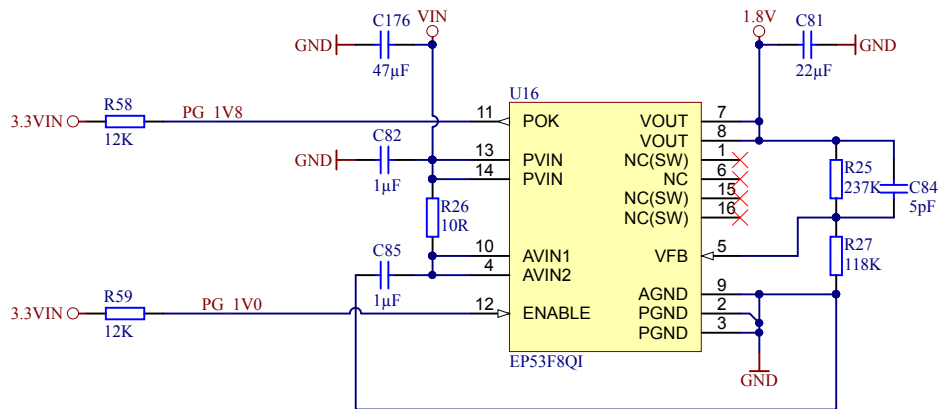
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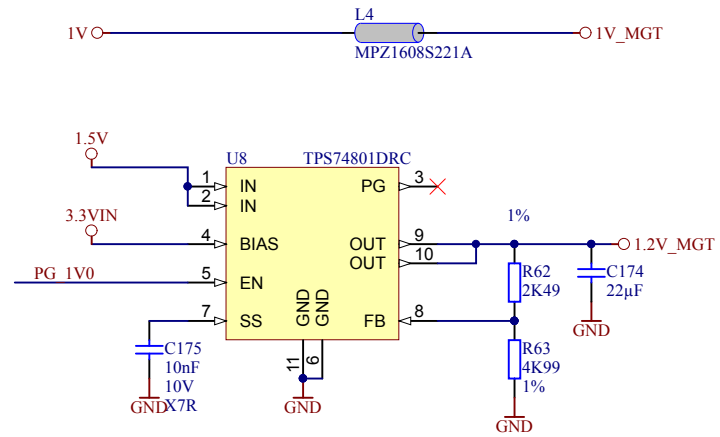
B

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Title: PWR		
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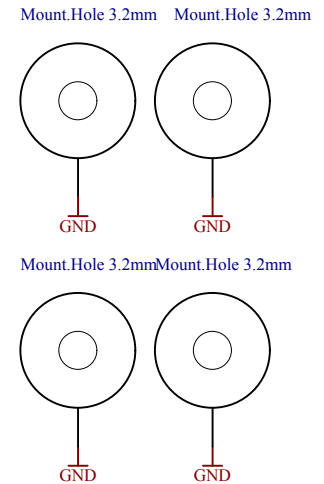
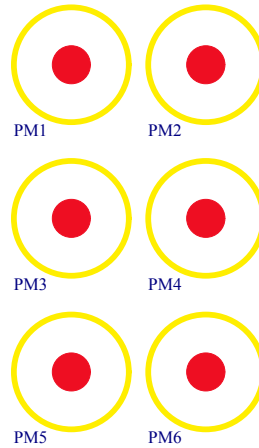
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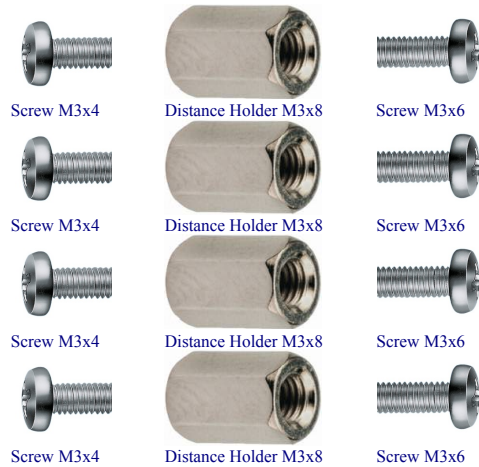
3


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U_B2B-Connectors
B2B-Connectors.SchDoc
U_B13
B13.SchDoc
U_B14
B14.SchDoc
U_B15
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U_B34
B34.SchDoc
U_FPGA-MGT
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U_FPGA-CFG
FPGA-CFG.SchDoc
U_FPGA-PWR
FPGA-PWR.SchDoc
U_Clock
ClOCK.SchDoc
U_DDR3-RAM
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Top of Board



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