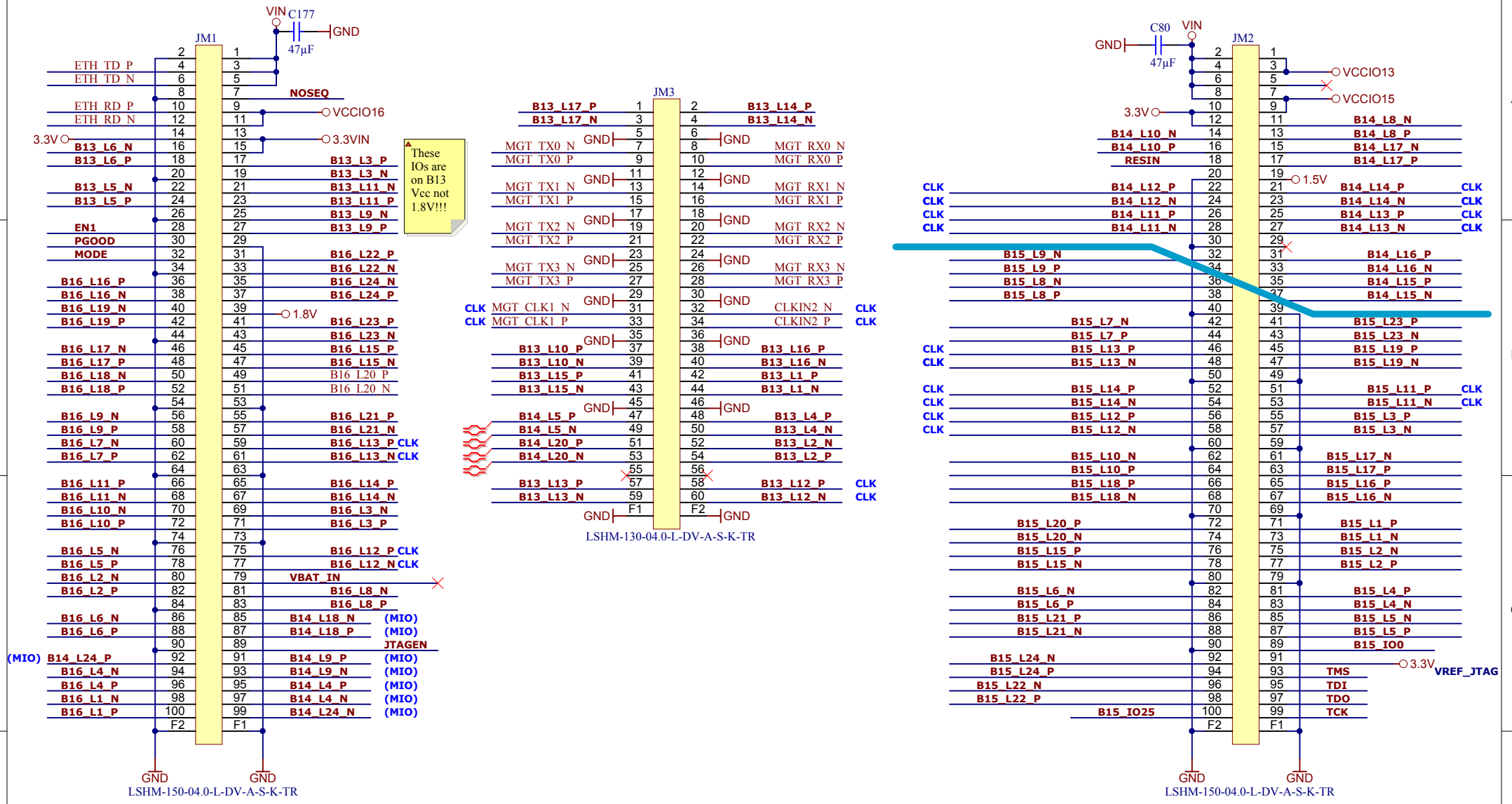
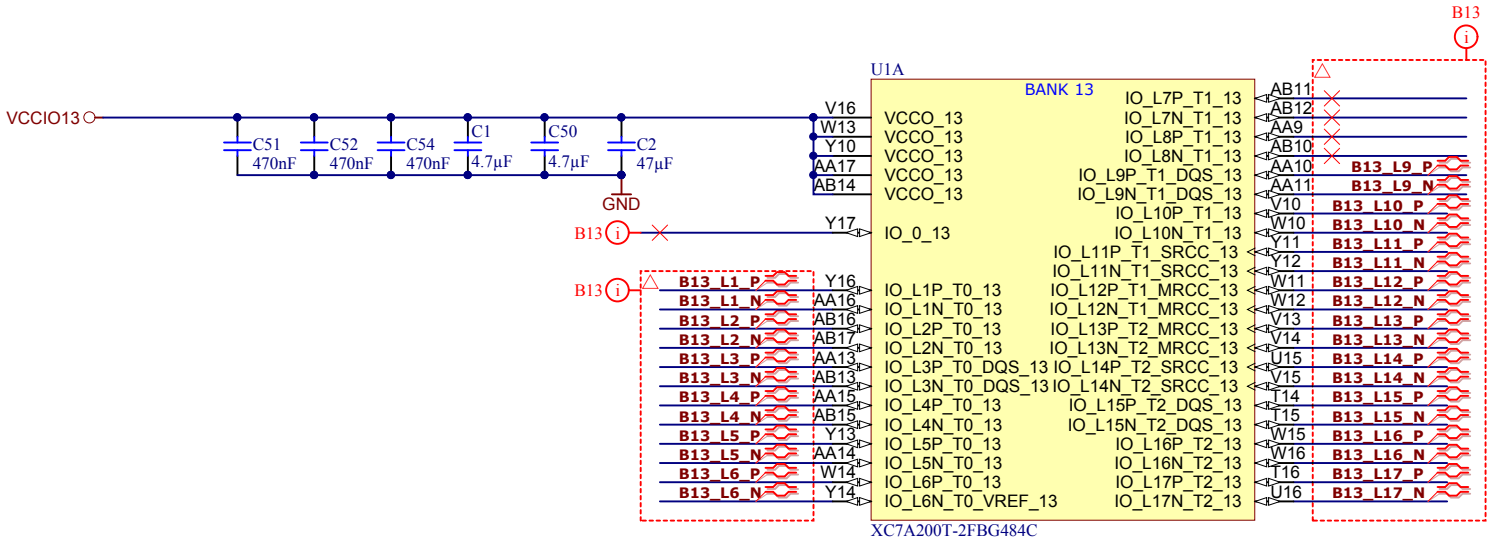
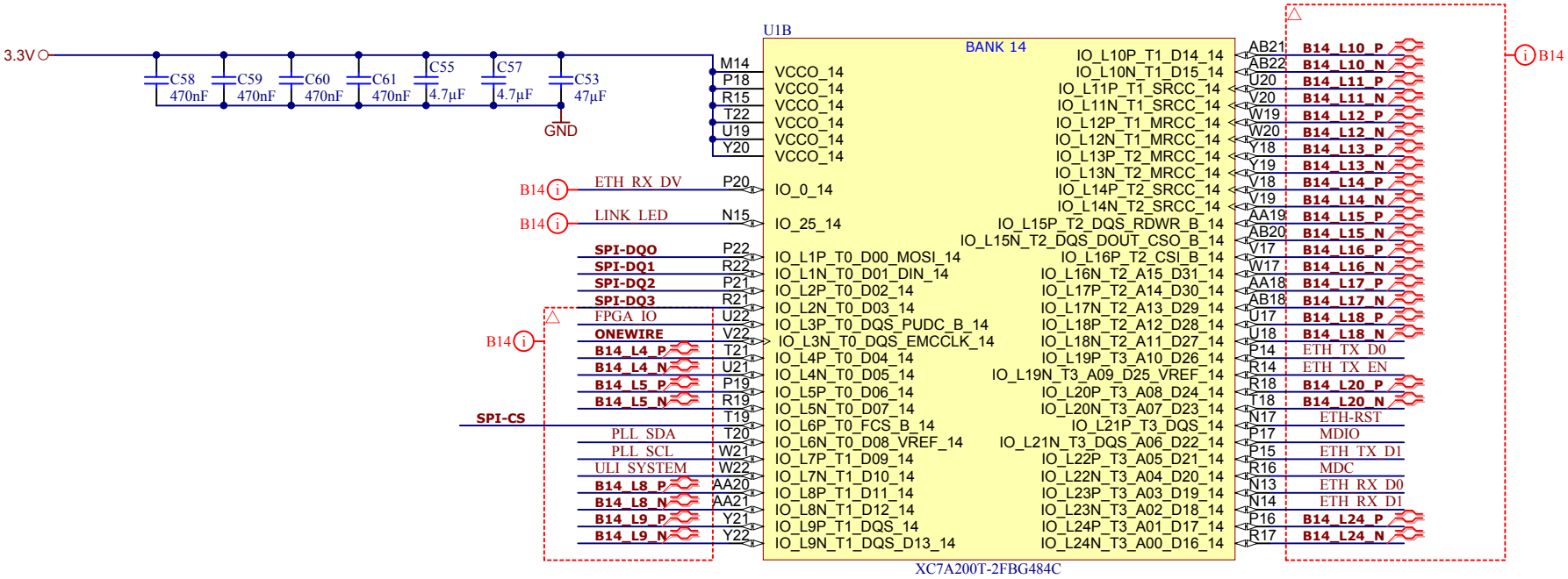


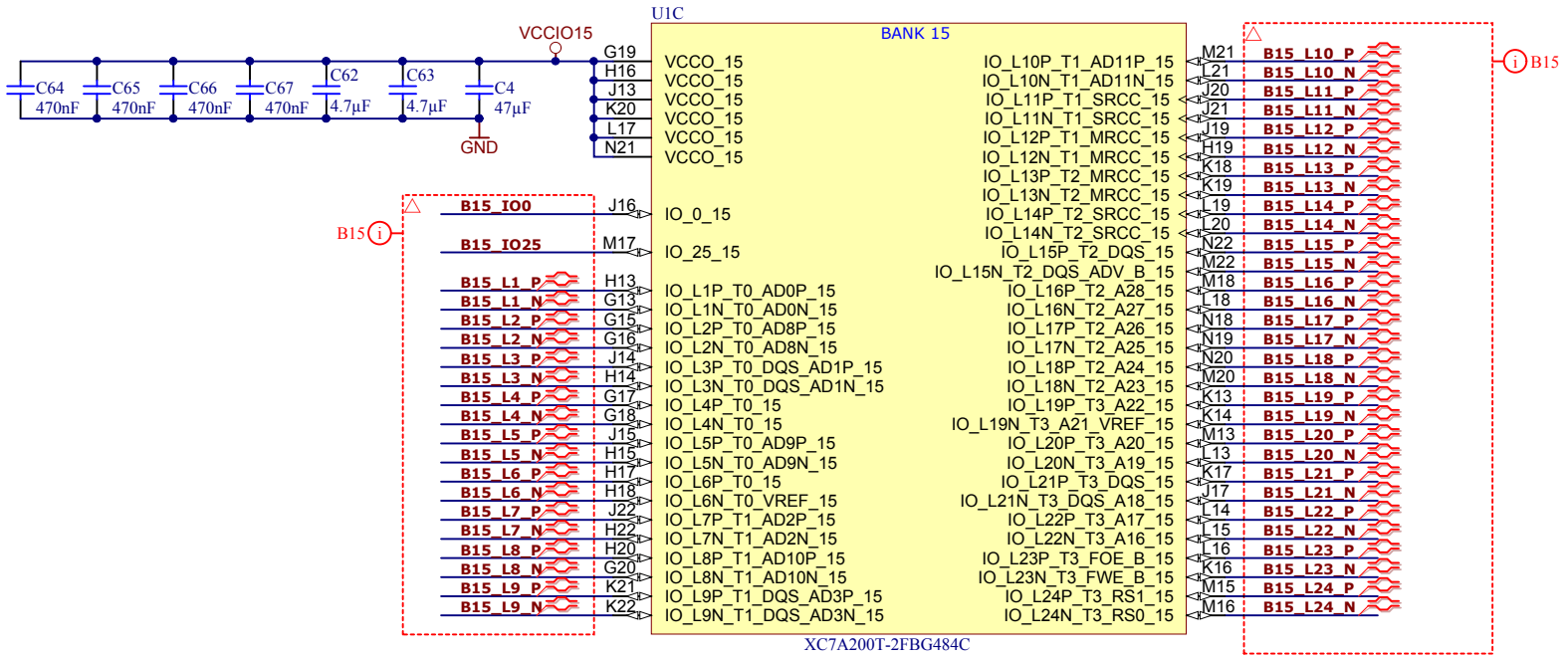
Title:	B2B	
A4	Number: TE0712 200-2C	Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page1 of 16
Filename:	B2B-Connectors.SchDoc	



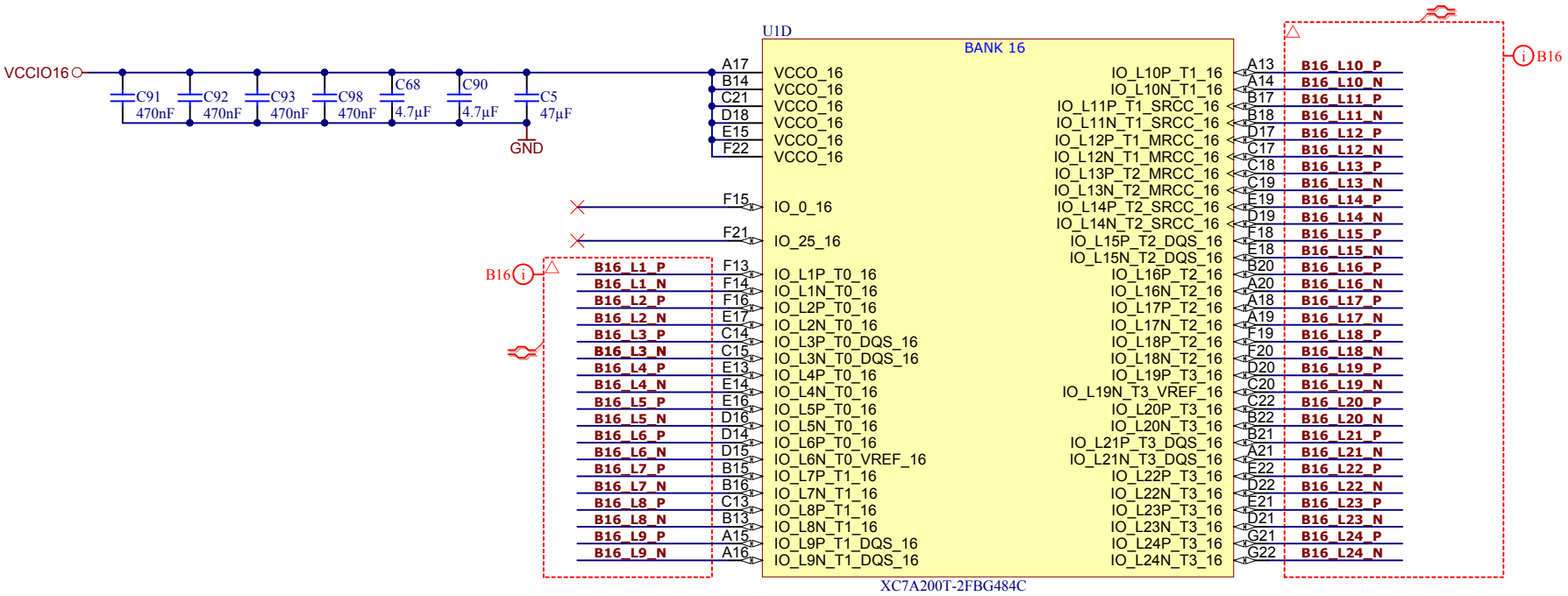
trenz electronic	Title: B13		
	A4	Number: TE0712 200-2C	Rev. 01
	Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page2 of 16
	Filename: B13.SchDoc		



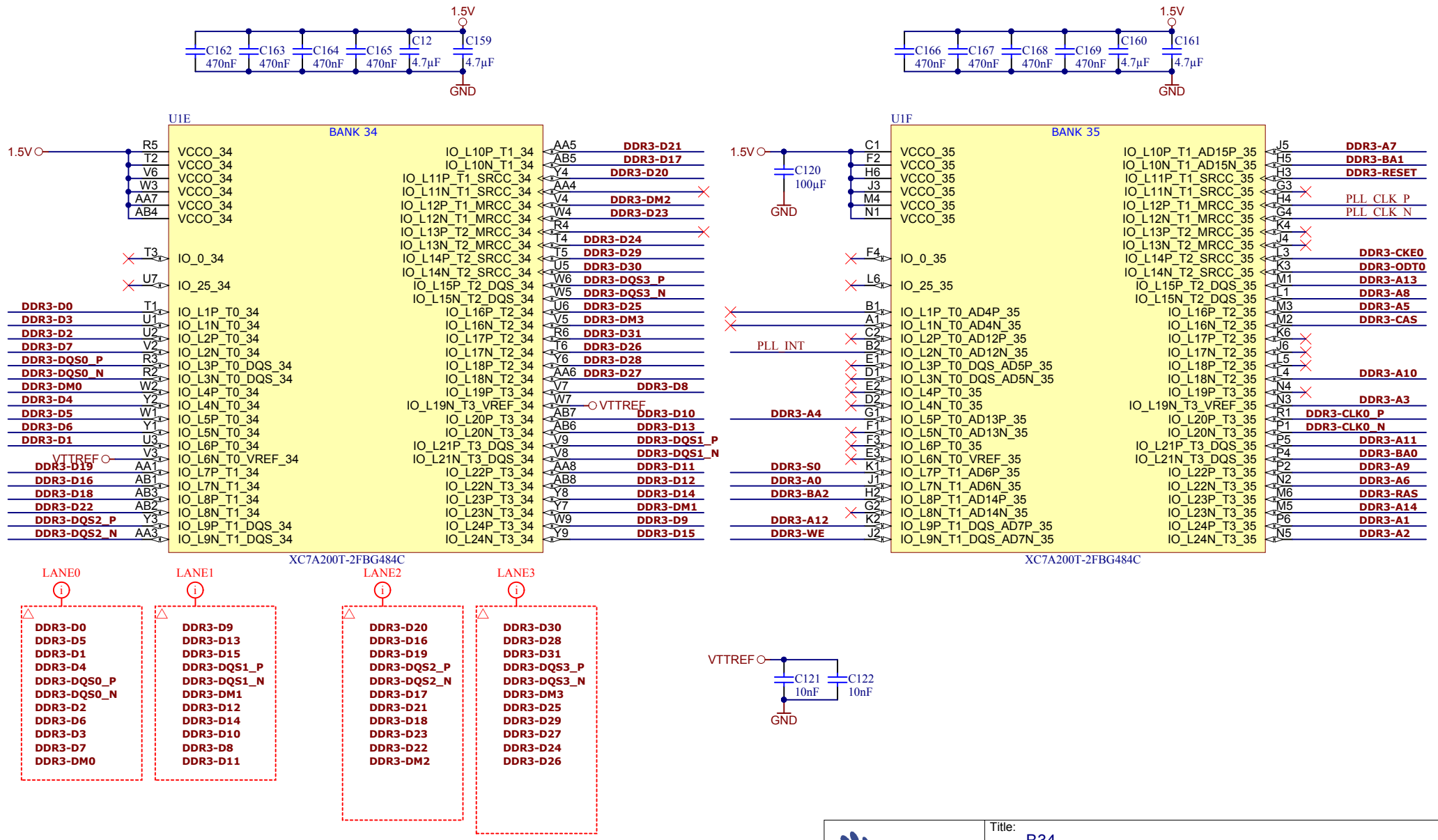
trenz electronic	Title: B14		
	A4	Number: TE0712 200-2C	Rev. 01
	Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page3 of 16
	Filename: B14.SchDoc		



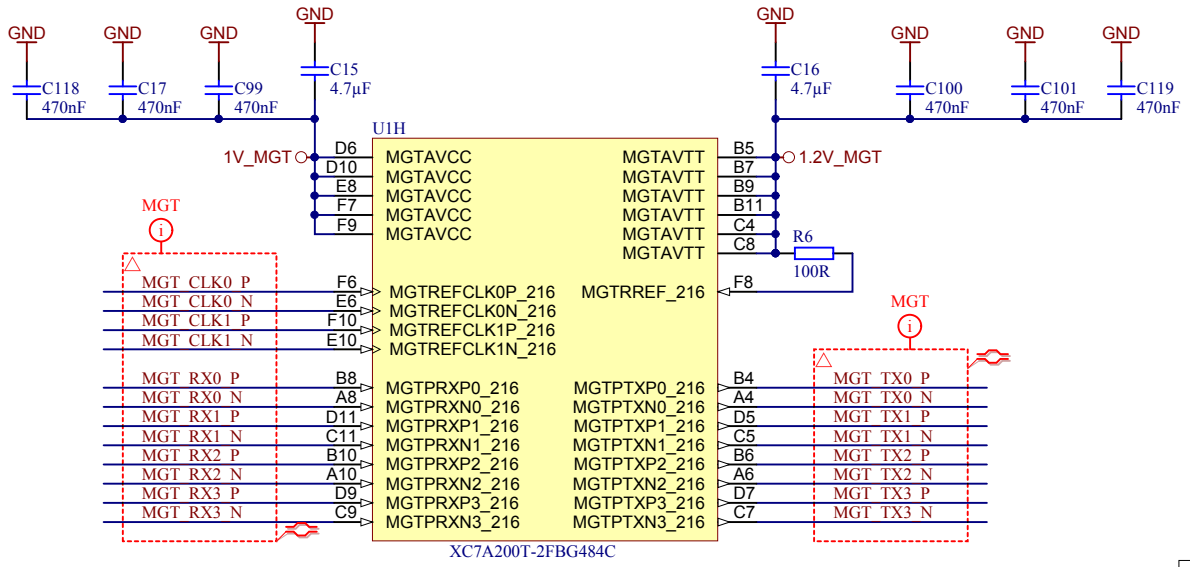
trenz electronic	Title: B15		
	A4	Number: TE0712 200-2C	Rev. 01
	Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page4 of 16
	Filename: B15.SchDoc		

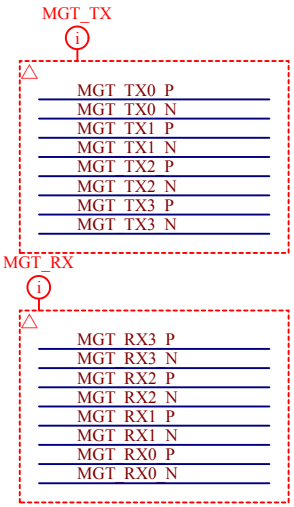


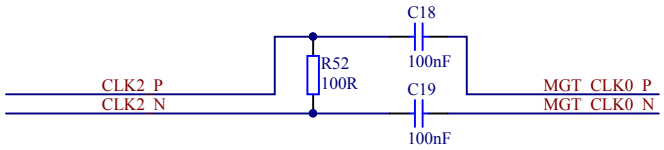
trenz electronic	Title: B16		
A4	Number: TE0712 200-2C		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page5 of 16
Filename: B16.SchDoc			



Title: B34			
A4	Number: TE0712 200-2C		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page6 of 16
Filename: B34.SchDoc			







Title: MGT			
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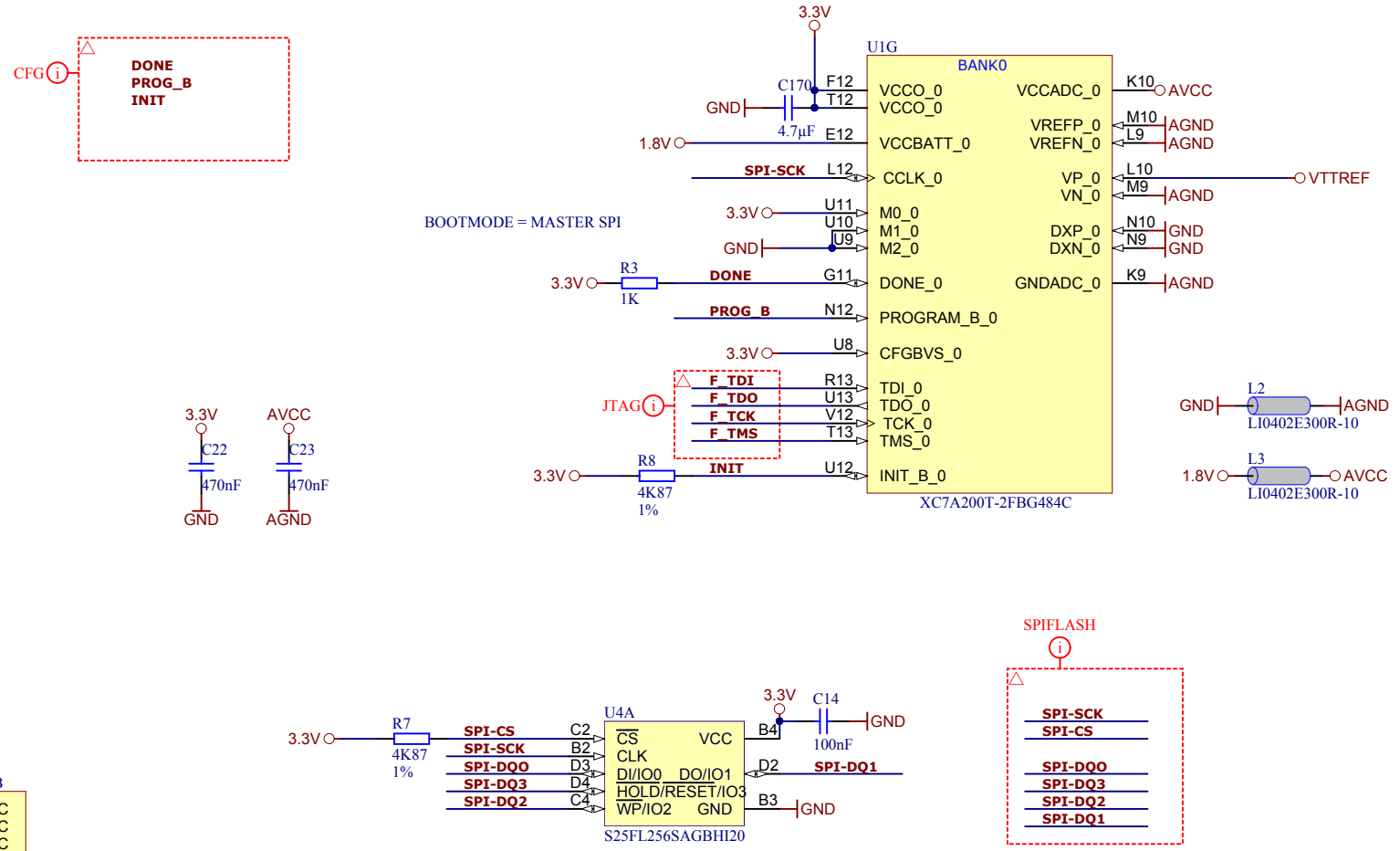
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page7 of 16
Filename: FPGA-MGT.SchDoc			


CFG
DONE
PROG_B
INIT
U1G
BANK0
3.3V
C170
4.7µF
GND
1.8V
F12
T12
E12
VCCO_0
VCCO_0
VCCBATT_0
VCCADC_0
K10
AVCC
VREFP_0
VREFN_0
M10
L9
AGND
SPI-SCK
L12
CCLK_0
VP_0
VN_0
L10
M9
VTTREF
BOOTMODE = MASTER SPI
U11
U10
U9
M0_0
M1_0
M2_0
DXP_0
DXN_0
N10
N9
R3
1K
DONE
G11
DONE_0
GNDADC_0
K9
PROG_B
N12
PROGRAM_B_0
U8
CFGBVS_0
JTAG
F_TDI
F_TDO
F_TCK
F_TMS
R13
U13
V12
T13
TDI_0
TDO_0
TCK_0
TMS_0
R8
4K87
1%
INIT
U12
INIT_B_0
XC7A200T-2FBG484C
L2
LI0402E300R-10
L3
LI0402E300R-10
C22
C23
470nF
AVCC
AGND
U4B
NC
S25FL256SAGBHI20
U4A
R7
4K87
1%
SPI-CS
SPI-SCK
SPI-DQ0
SPI-DQ3
SPI-DQ2
C2
B2
D3
D4
C4
CS
CLK
DI/IO0
DO/IO1
HOLD/RESET/IO3
WP/IO2
VCC
GND
B4
D2
B3
C14
100nF
SPI-DQ1
S25FL256SAGBHI20
SPIFLASH
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electronic
Title:
CFG
A4
Number:
TE0712
200-2C
Rev.
01
Date:
2014-06-23
Copyright: 2014 Trenz Electronic GmbH
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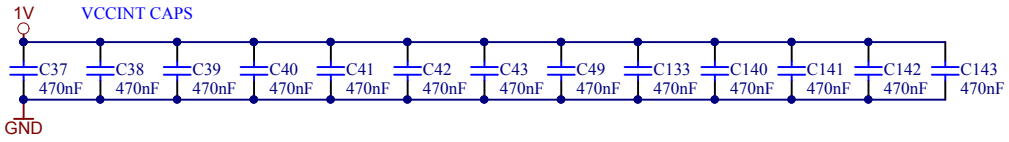
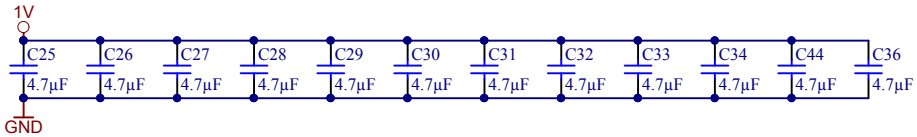
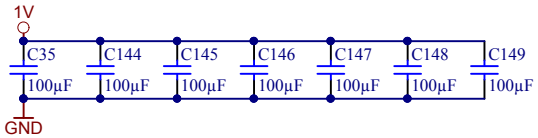
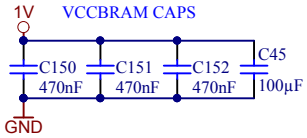
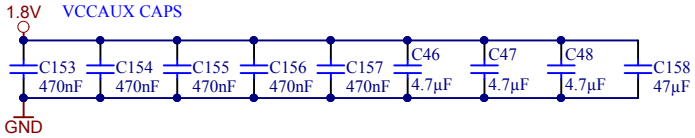
Filename:
FPGA-CFG.SchDoc

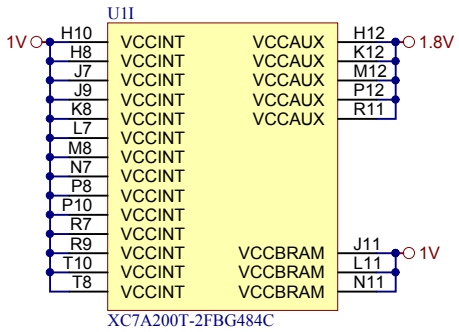


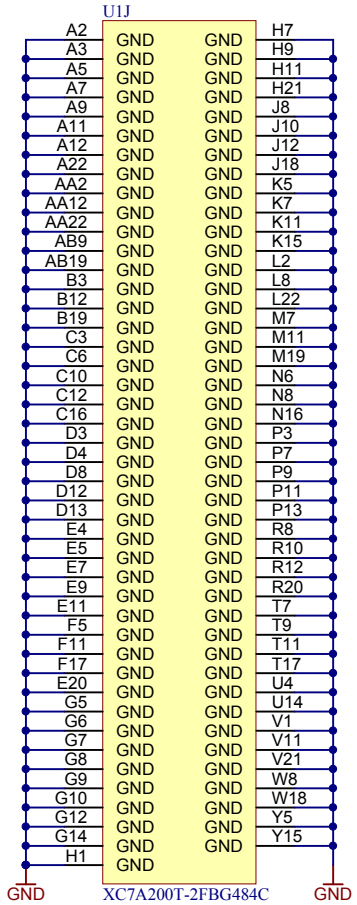












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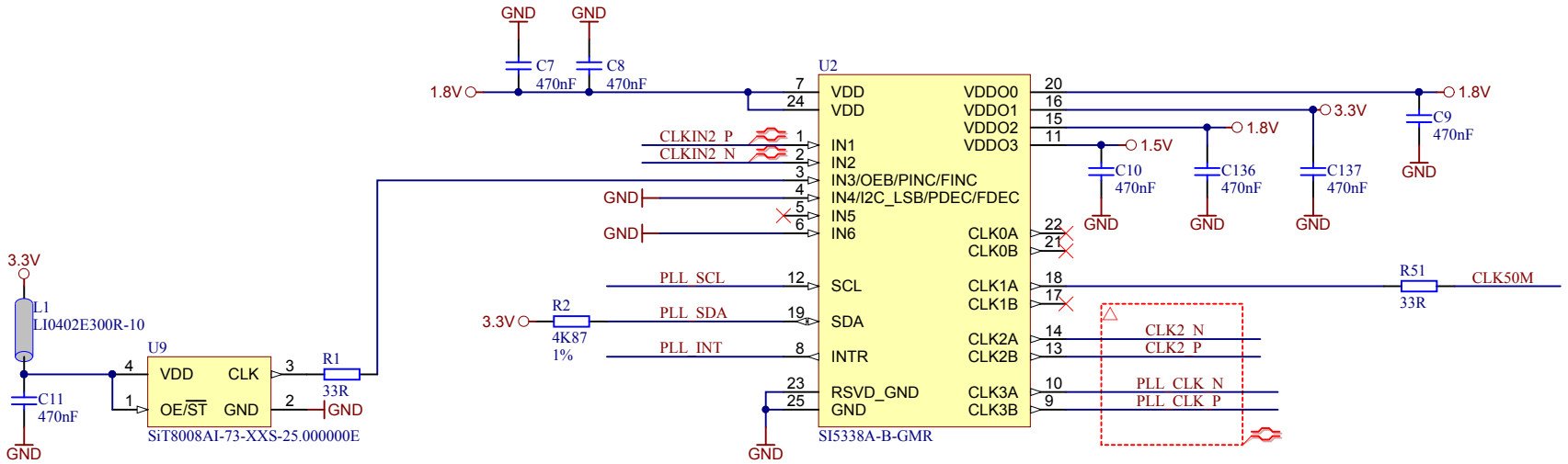
Title: PWR			
A4	Number: TE0712 200-2C		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page9 of 16
Filename: FPGA-PWR.SchDoc			



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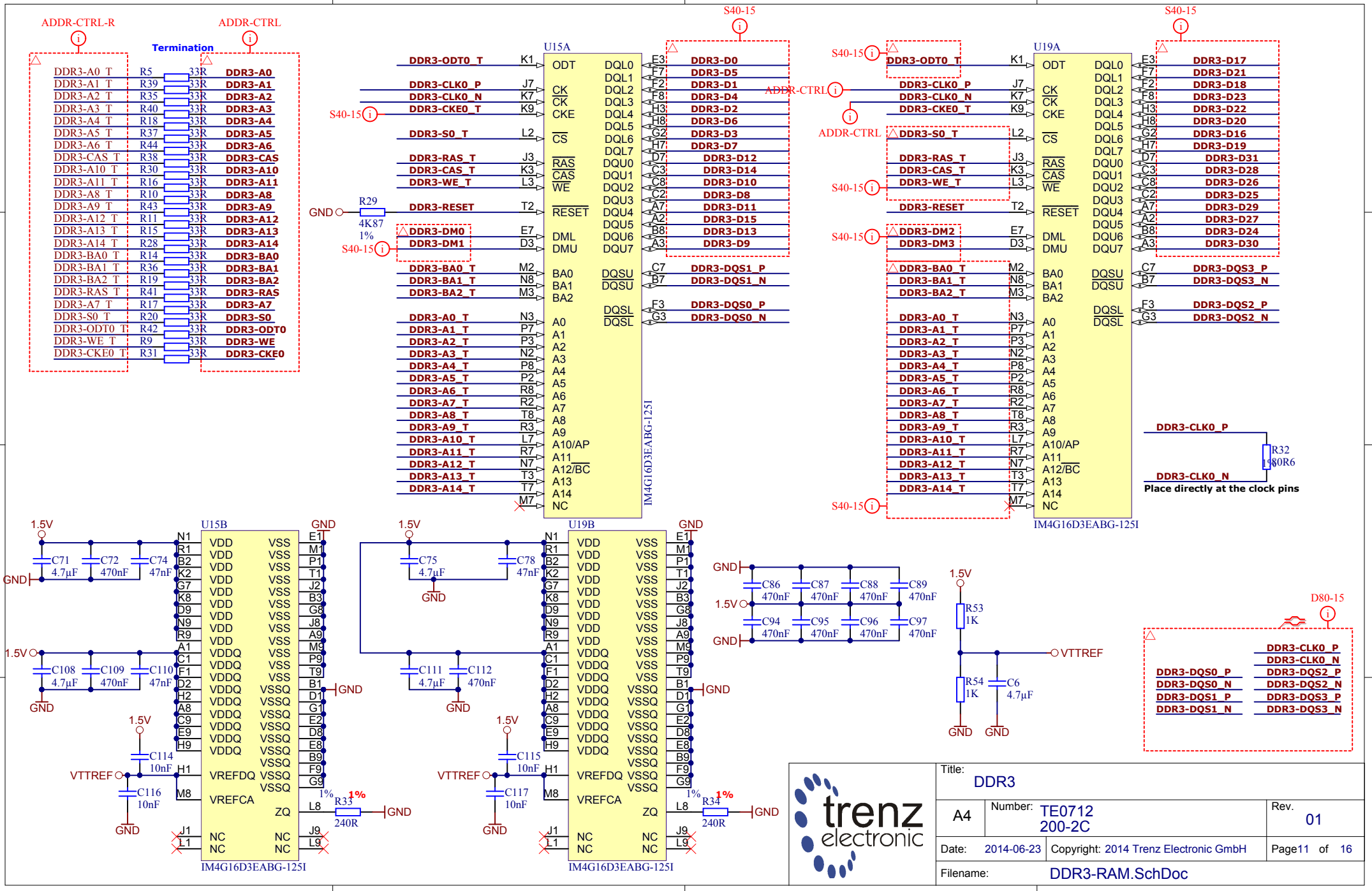
Title: Clock		
A4	Number: TE0712 200-2C	Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page10 of 16
Filename: Clock.SchDoc		


ADDR-CTRL-R
ADDR-CTRL
Termination
DDR3-A0_T R5 33R DDR3-A0
DDR3-A1_T R39 33R DDR3-A1
DDR3-A2_T R35 33R DDR3-A2
DDR3-A3_T R40 33R DDR3-A3
DDR3-A4_T R18 33R DDR3-A4
DDR3-A5_T R37 33R DDR3-A5
DDR3-A6_T R44 33R DDR3-A6
DDR3-CAS_T R38 33R DDR3-CAS
DDR3-A10_T R30 33R DDR3-A10
DDR3-A11_T R16 33R DDR3-A11
DDR3-A8_T R10 33R DDR3-A8
DDR3-A9_T R43 33R DDR3-A9
DDR3-A12_T R11 33R DDR3-A12
DDR3-A13_T R15 33R DDR3-A13
DDR3-A14_T R28 33R DDR3-A14
DDR3-BA0_T R14 33R DDR3-BA0
DDR3-BA1_T R36 33R DDR3-BA1
DDR3-BA2_T R19 33R DDR3-BA2
DDR3-RAS_T R41 33R DDR3-RAS
DDR3-A7_T R17 33R DDR3-A7
DDR3-S0_T R20 33R DDR3-S0
DDR3-ODT0_T R42 33R DDR3-ODT0
DDR3-WE_T R9 33R DDR3-WE
DDR3-CKE0_T R31 33R DDR3-CKE0
S40-15
U15A
U19A
ODT
CK
CKE
CS
RAS
CAS
WE
RESET
DML
DMU
BA0
BA1
BA2
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC
A13
A14
NC
DQSU
DQSL
DQU0
DQU1
DQU2
DQU3
DQU4
DQU5
DQU6
DQU7
DQL0
DQL1
DQL2
DQL3
DQL4
DQL5
DQL6
DQL7
R29
4K87
1%
GND
ADDR-CTRL
IM4G16D3EABG-125I
R32
180R6
DDR3-CLK0_P
DDR3-CLK0_N
Place directly at the clock pins
U15B
U19B
VDD
VSS
VDDQ
VSSQ
VREFDQ
VREFCA
ZQ
1.5V
VTTREF
C71 4.7µF
C72 470nF
C74 47nF
C108 4.7µF
C109 470nF
C110 47nF
C114 10nF
C116 10nF
C75 4.7µF
C78 47nF
C111 4.7µF
C112 470nF
C115 10nF
C117 10nF
C86 470nF
C87 470nF
C88 470nF
C89 470nF
C94 470nF
C95 470nF
C96 470nF
C97 470nF
R53 1K
R54 1K
C6 4.7µF
R33 240R
R34 240R
1%
D80-15
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-DQS2_P
DDR3-DQS2_N
DDR3-DQS3_P
DDR3-DQS3_N
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Title: DDR3
A4
Number: TE0712 200-2C
Rev. 01
Date: 2014-06-23
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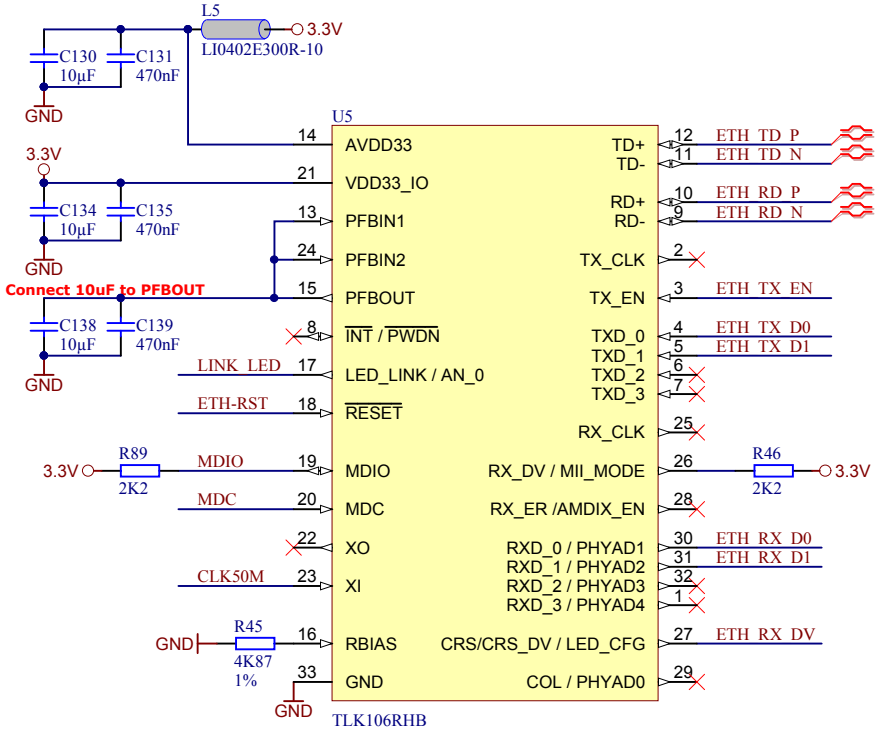
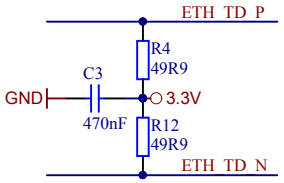
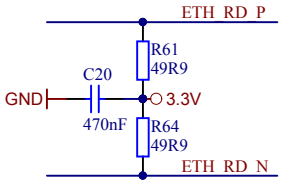
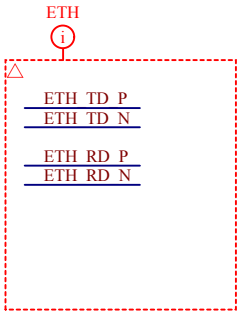
Filename: DDR3-RAM.SchDoc

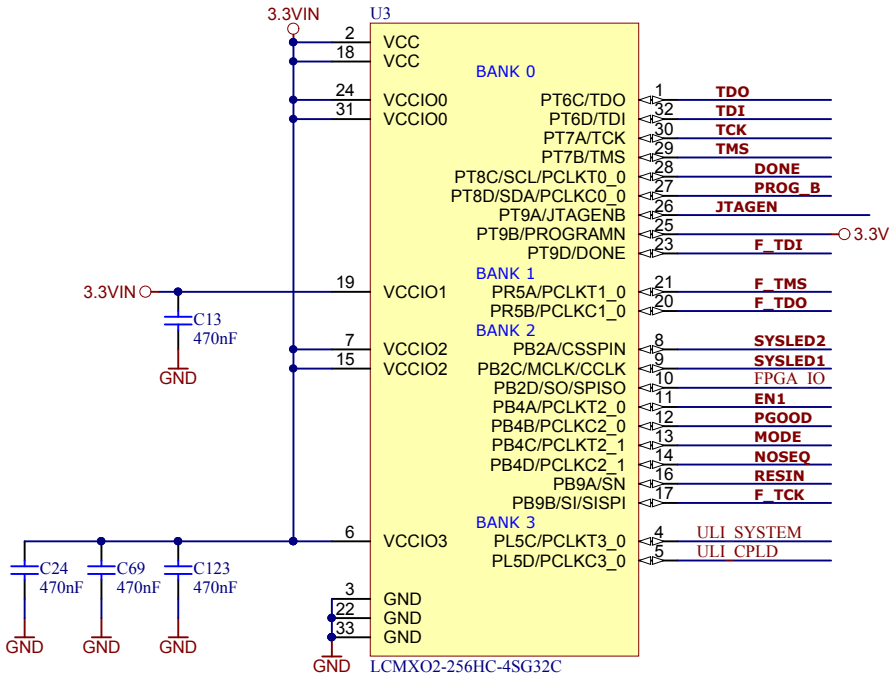


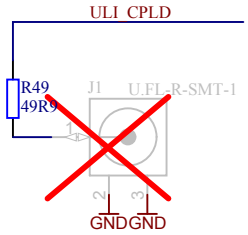


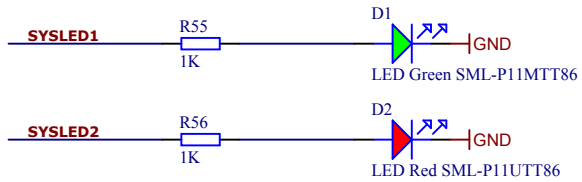


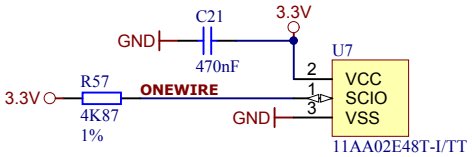


Title: ETH			
A4	Number: TE0712 200-2C		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page12 of 16
Filename: ETHERNET.SchDoc			









Title: CPLD			
A4	Number: TE0712 200-2C		Rev. 01
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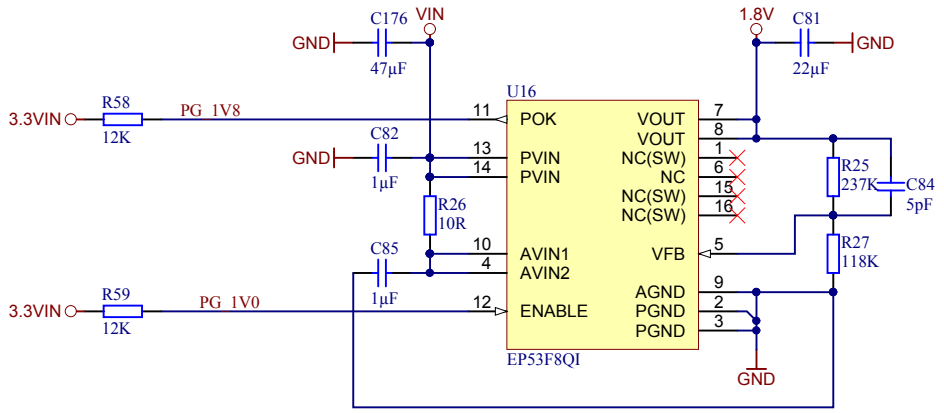
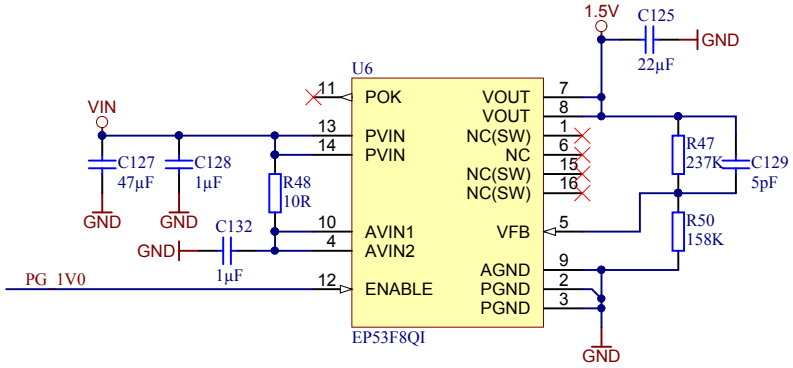
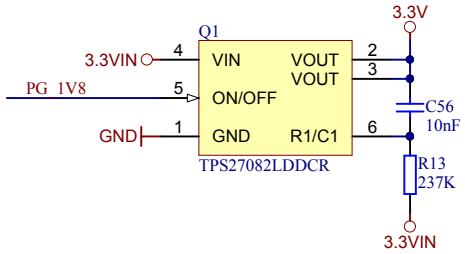
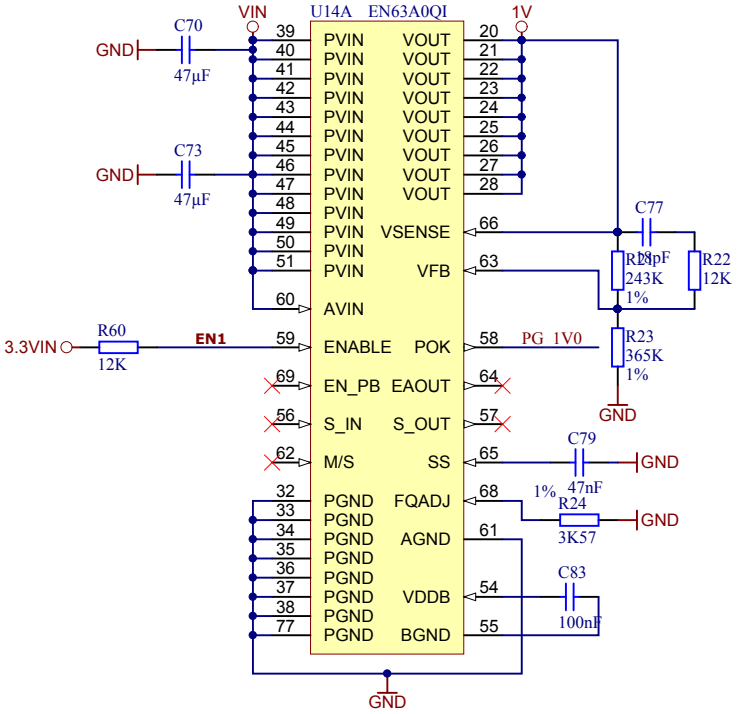
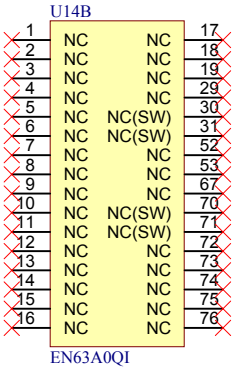
Filename: CPLD.SchDoc			



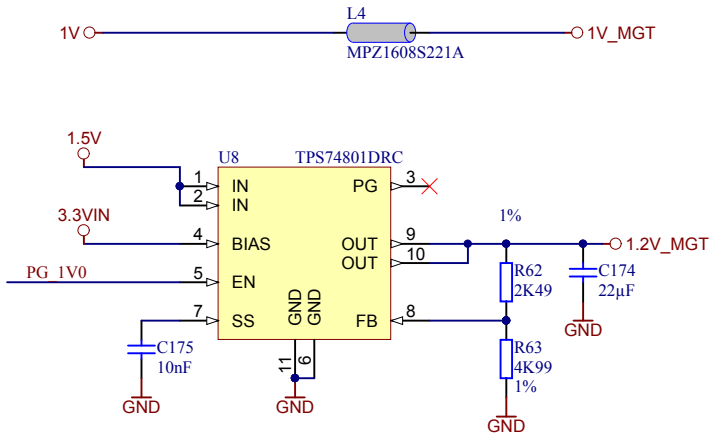








Title: PWR			
A4	Number: TE0712 200-2C		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page14 of 16
Filename: PWR1.SchDoc			



Title: PWR			
A4	Number: TE0712 200-2C		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page15 of 16
Filename: PWR2.SchDoc			

U_B2B-Connectors
B2B-Connectors.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_Clock
Clock.SchDoc

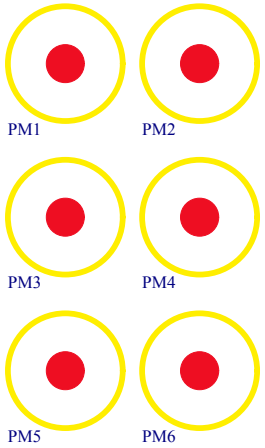
U_DDR3-RAM
DDR3-RAM.SchDoc

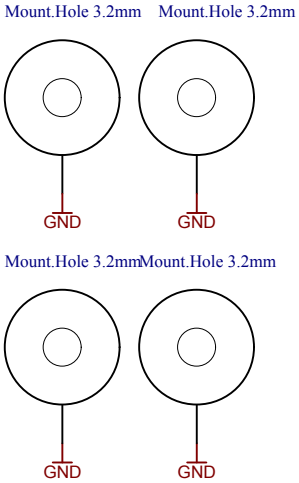
U_ETHERNET
ETHERNET.SchDoc

U_CPLD
CPLD.SchDoc

U_PWR1
PWR1.SchDoc

U_PWR2
PWR2.SchDoc





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Title: TE0712		
A4	Number: TE0712 200-2C	Rev. 01
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Filename: TE0712.SchDoc		